

Hipac

High performance passive and actives on chip

BGF106C

SIM Card Interface Filter and ESD Protection

BGF106C

Datasheet

Rev. 3.1, 2013-01-16
Final

Revision History Rev. 3.0, 2011-05-13

| Page or Item | Subjects (major changes since previous revision) |
|-----------------------------|--------------------------------------------------|
| Rev. 3.1, 2013-01-16 | |
| 4 | Features updated |
| | |
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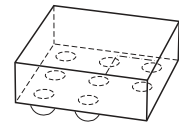
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Last Trademarks Update 2011-11-11

1 SIM Card Interface Filter and ESD Protection

1.1 Features

- ESD protection circuit and interface filter for SIM cards
- ESD protection according to IEC61000-4-2 for ± 15 kV contact discharge on external IOs
- Wafer level package with SnAgCu solder balls
- 400 μm solder ball pitch
- Pb-free (RoHS compliant) and halogen free package



WLP-8-11-N-3D



1.2 Description

BGF106C is an ESD protection circuit and filtering interface for SIM cards. All external IOs are protected against ESD pulses of ± 15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green lead-free and halogen-free package with a size of only 1.2 mm x 1.2 mm and a total height of 0.6 mm

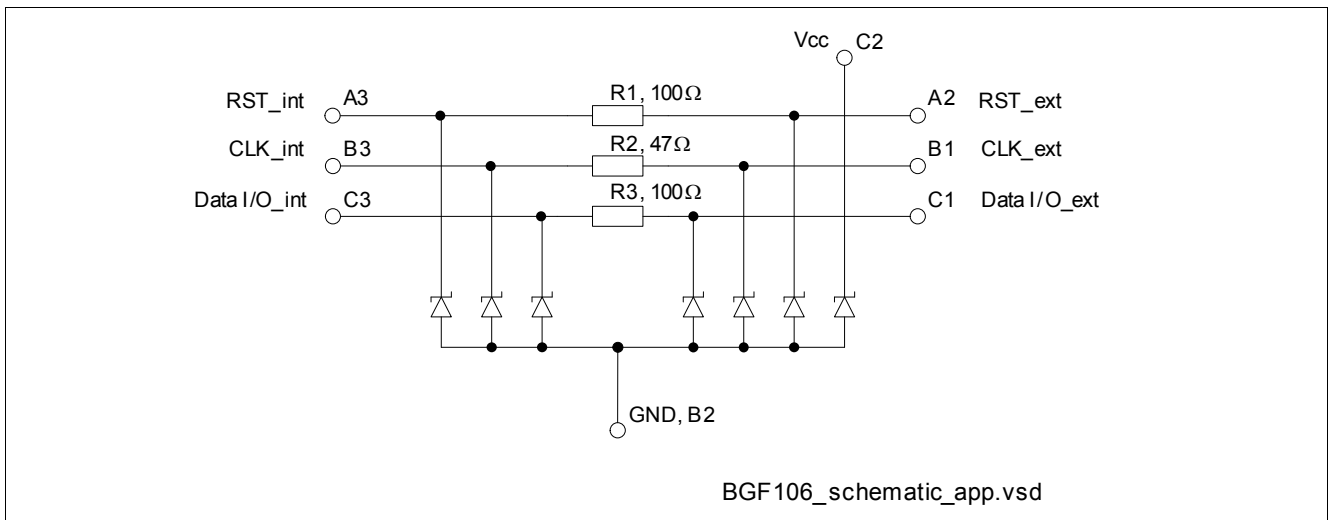


Figure 1-1 Schematic Diagram and Package Configuration

| Type | Package | Marking | Chip |
|---------|----------|---------|-------|
| BGF106C | WLP-8-11 | 6C | N0727 |

2 Characteristics

Table 2-1 Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------------------------------------|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Voltage at all pins to GND | V_P | 0 | – | 5.5 | V | – |
| Operating temperature range | T_{OP} | -40 | – | +85 | ° | – |
| Storage temperature range | T_{STG} | -65 | – | +150 | °C | – |
| Summed up input power for all pins | P_{in} | – | – | 60 | mW | $T_S < 70\text{ °C}$ |
| Electrostatic discharge according to IEC61000-4-2 | | | | | | |
| Contact discharge at internal pins A3, B3, C3 to any other pin | V_{ESD} | -2 | – | 2 | kV | – |
| Contact discharge at external pins A2, B1, C1, C2 to GND | V_{ESD} | -15 | – | 15 | kV | – |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics

Table 2-2 Electrical Characteristics¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------------------------------------|------------|--------|------|------|----------|--------------------------|
| | | Min. | Typ. | Max. | | |
| Resistors R_1, R_3 | $R_{1,3}$ | 80 | 100 | 120 | Ω | – |
| Resistor R_2 | R_2 | 37.6 | 47 | 56.4 | Ω | – |
| Reverse current of ESD protection diodes | I_R | – | 1 | 100 | nA | $V = 3\text{ V}$ |
| | | – | 2 | 1000 | nA | $V = 5\text{ V}$ |
| Breakdown voltage of ESD diodes | $V_{(BR)}$ | 6.5 | 7.8 | – | V | $I_{(BR)} = 1\text{ mA}$ |
| Line capacitance Capacitance of all lines to GND | C_T | – | 16.5 | 20 | pF | $V = 0\text{ V}$ |

1) at $T_A = 25\text{ °C}$

3 Typical Characteristics

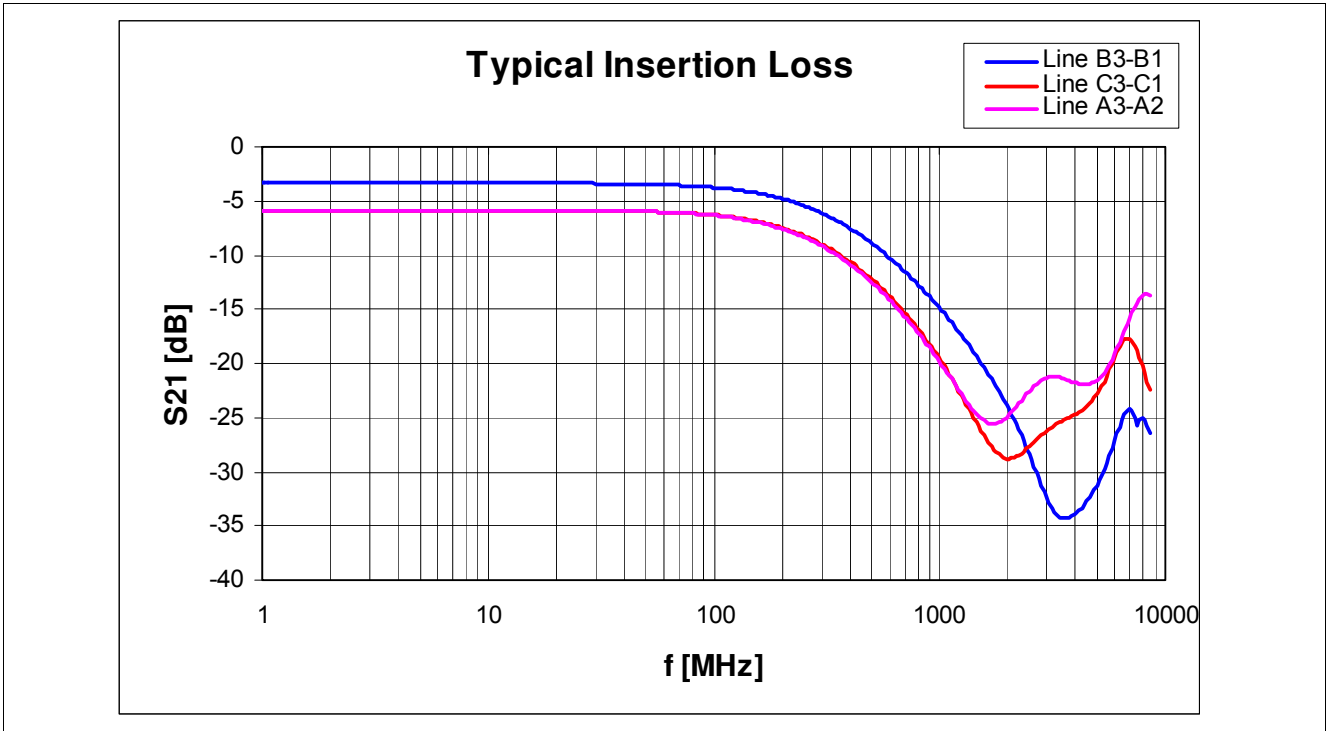


Figure 3-1 Insertion loss, $Z_S=Z_L=50 \Omega$

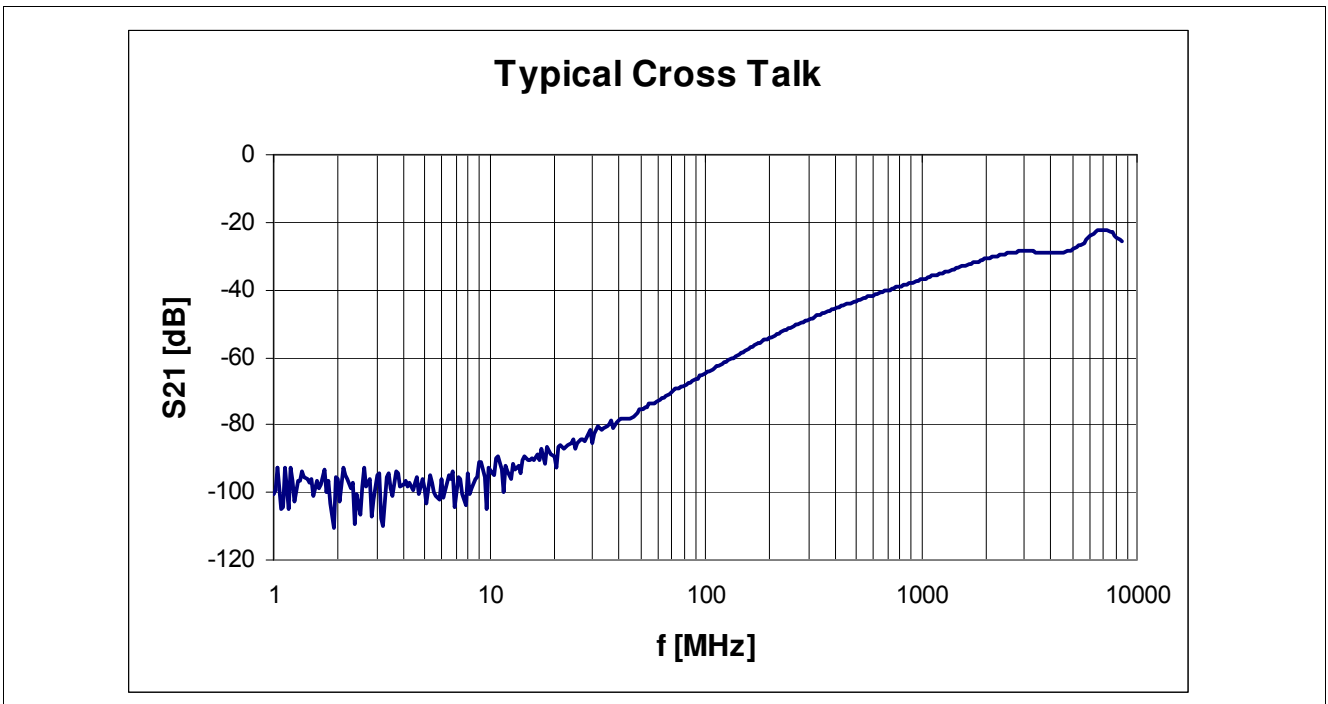


Figure 3-2 Cross talk, $Z_S=Z_L=50 \Omega$ (all unused input and output pins are terminated with 50Ω)

4 Package

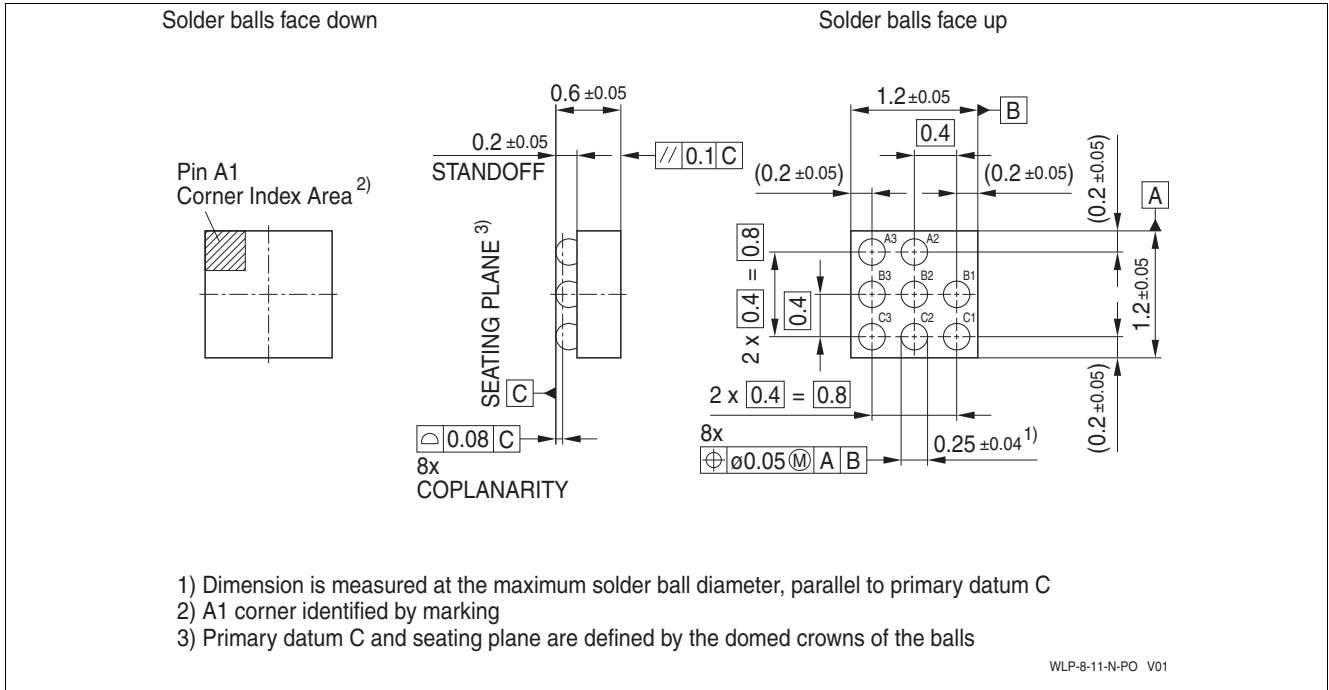


Figure 4-1 WLP-8-11 Package outline (dimension in mm)

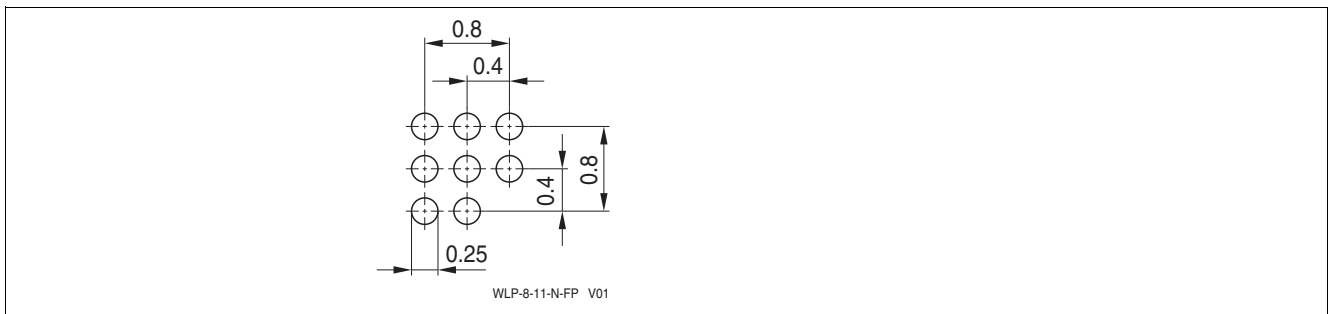


Figure 4-2 WLP-8-11 Footprint (dimension in mm)

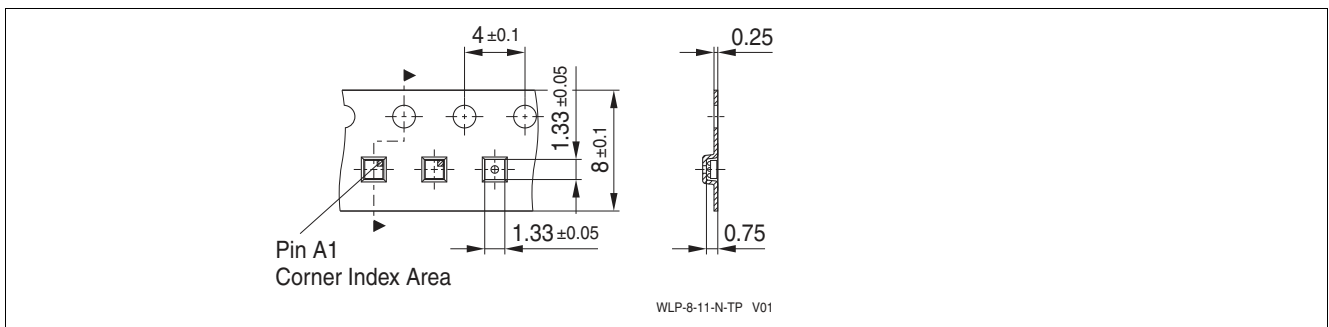


Figure 4-3 WLP-8-11 Packing (dimension in mm)

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