Never stop thinking

32-Bit

TC1766

32-Bit Single-Chip Microcontroller
Bare Die Delivery

Data Sheet
V1.10 2010-04

Microcontrollers

Edition 2010-04

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Never stop thinking

32-Bit

TC1766

32-Bit Single-Chip Microcontroller
Bare Die Delivery

Data Sheet

V1.10 2010-04

Microcontrollers

TC1766 Data Sheet

Revision History: V1.10, 2010-04

Previous Version: V1.8	
Page	Subjects (changes since V1.8)
24	Die placement on surf tape is updated, pad 1 of the die is located at the bottom of the surf tape.
3, 4, 19, 26, 27	Information for carrier tape packing are included at these sections - features, ordering information, storage conditions, die placement and dimension.

Trademarks

TriCore® is a trademark of Infineon Technologies AG.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Table of Contents

1 Summary of Features

- High-performance 32-bit super-scaler TriCore v1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 80 MHz operation at full temperature range
- Peripheral Control Processor with single cycle instruction (PCP2)
  - 8 KByte Parameter Memory (PRAM)
  - 12 KByte Code Memory (CMEM)
- Multiple on-chip memories
  - 56 KByte Local Data Memory (SRAM)
  - 8 KByte Overlay Memory
  - 16 KByte Scratch-Pad RAM (SPRAM)
  - 8 KByte Instruction Cache (ICACHE)
  - 1504 Kbyte Program Flash (for instruction code and constant data)
  - 32 Kbyte Data Flash (e.g. 4 Kbyte EEPROM emulation)
  - 16 KByte Boot ROM
- 8-channel DMA Controller
- Fast-response interrupt system with 2 x 255 hardware priority arbitration levels serviced by CPU or PCP2
- High-performance on-chip bus structure
  - 64-Bit Local Memory Bus (LMB) to Flash memory
  - System Peripheral Bus (SPB) for interconnections of functional units
- Versatile on-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASCs) with baudrate generator, parity, framing and overrun error detection
  - Two High Speed Synchronous Serial Channels (SSCs) with programmable data length and shift direction
  - One Micro Second Bus (MSC) interface for serial port expansion to external power devices
  - Two high-speed Micro Link Interfaces (MLIs) for serial inter-processor communication
  - One MultiCAN Module with two CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer

  - One General Purpose Timer Array Module (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One 16-channel Analog-to-Digital Converter unit (ADC) with selectable 8-bit, 10-bit, or 12-bit, supporting 32 input channels
  - One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 262.5ns
- 32 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1766ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5V
- I/O voltage of 3.3 V
- Die temperature under operating condition: -40° to +150°C
- Packaging: bare dies mounted on surf tape[1)]

1) Surf Tape packing will be replaced by Carrier Tape packing in the second quarter of 2010.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the TC1766 bare die, please refer to the “Product Catalog Microcontrollers” that summarizes all available microcontroller variants.

This document describes the derivatives of the device. **Table 1** enumerates the derivative.

Table 1 TC1766 Derivative Synopsis

Derivative	Package	Notes/Conditions
SAL-TC1766-192F80U	Bare die mounted on surf tape[1)]	T_D = -40°C to +150°C; f_{SYS} = 80 MHz; 8 Kbyte OVRAM

TC1766 Bare Die Data Sheet mainly covers bare die related parameters and specification issues. All other TC1766 characteristics and parameters are defined in the TC1766 package Data Sheet.

Note: All references of this document are based on V1.0 or higher of the TC1766 package Data Sheet.

2 General Device Information

2.1 Block Diagram

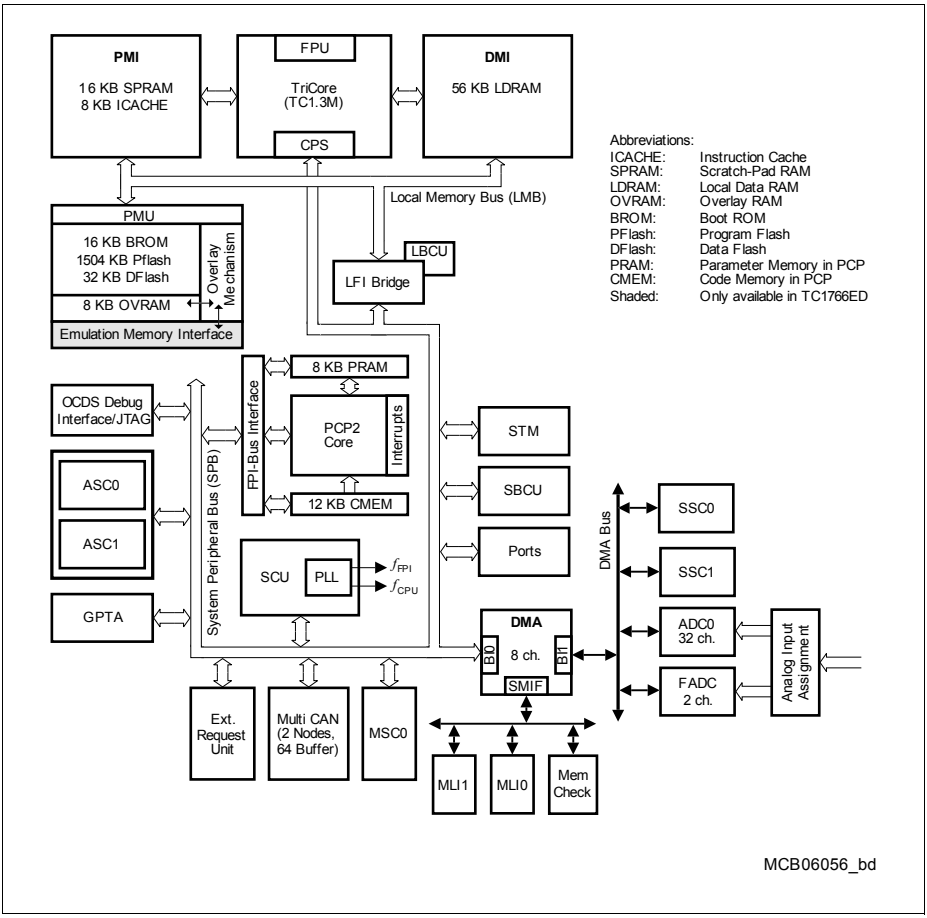

Figure 1 TC1766 Block Diagram

2.2 Pad Configuration

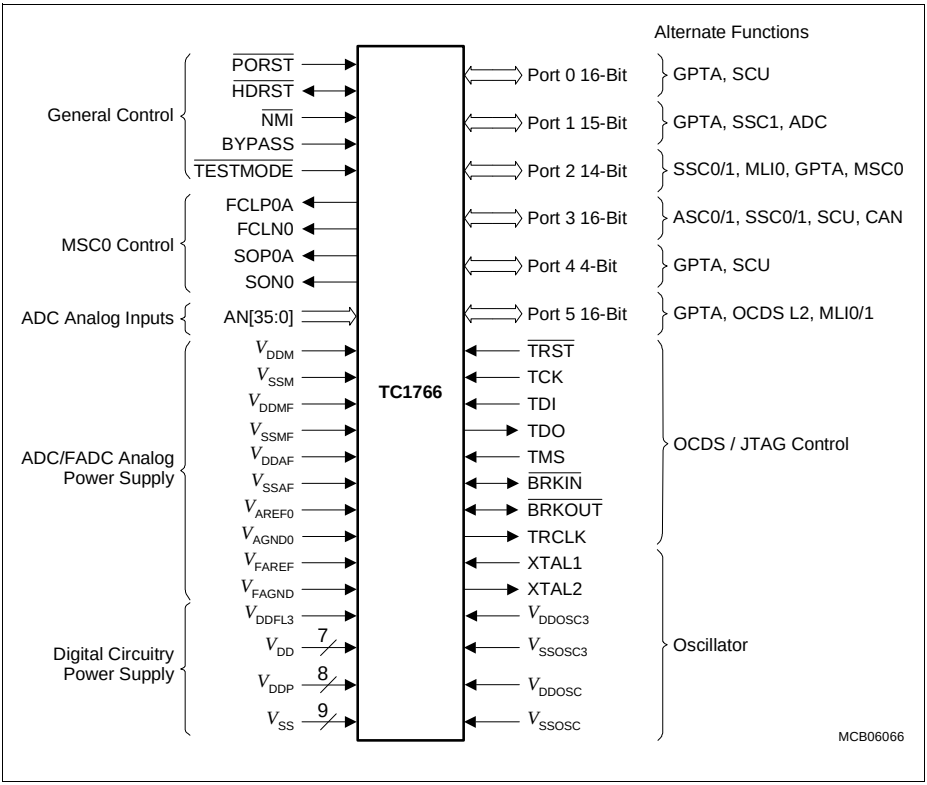

Figure 2 TC1766 Pad Configuration

2.3 Pad Configuration

*Note: There are four pad pairs which are converted to giant pads in BF-step, these are pad pairs numbered 25 and 26, 65 and 66, 169 and 170, 190 and 191. For more details, please refer to footnotes 2 to 5 in **Table 2**.*

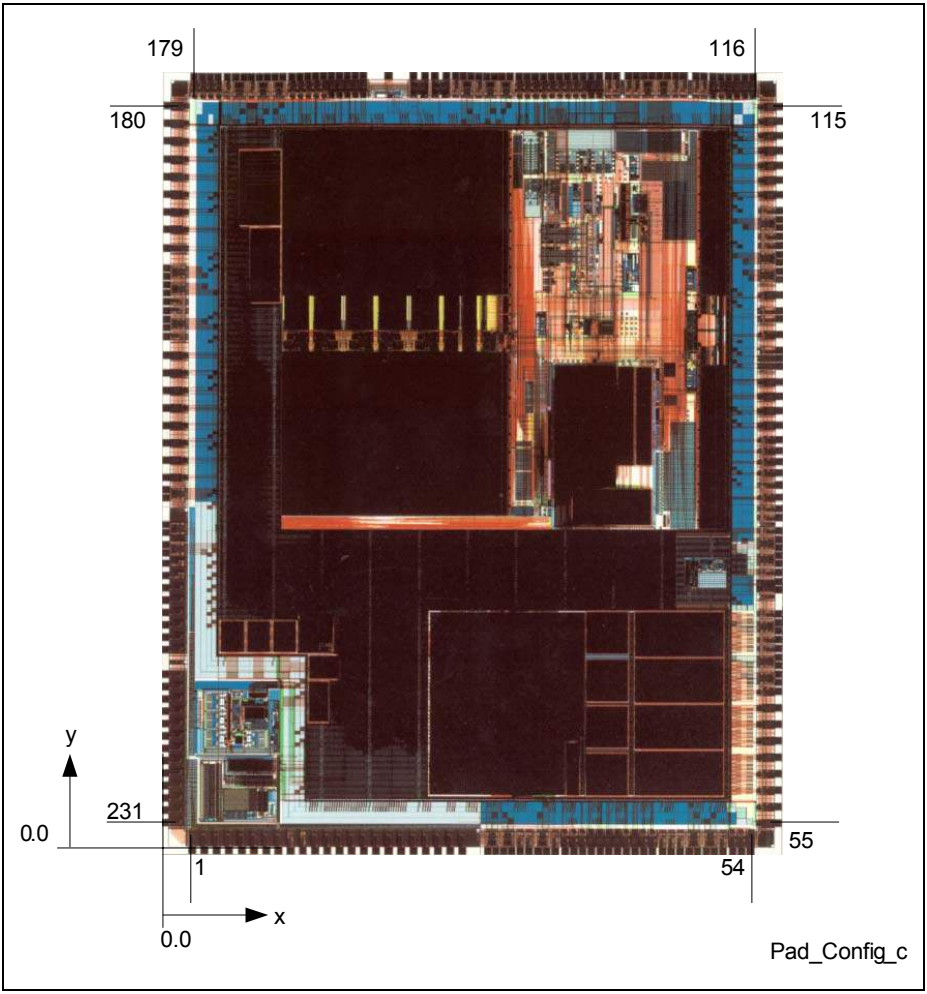

Figure 3 TC1766 Pad Configuration (top view)

2.4 Pad Definitions and Functions

Table 2 Pad Definitions and Functions

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
1	AN19	I	321	40	Analog input 19
2	AN18	I	446	40	Analog input 18
3	AN17	I	571	40	Analog input 17
4	AN16	I	696	40	Analog input 16
5	AN15	I	821	40	Analog input 15
6	AN14	I	946	40	Analog input 14
7	V_{AGND}	–	1071	40	ADC reference ground
8	V_{AREF}	–	1196	40	ADC reference voltage
9	V_{SSM}	–	1321	40	ADC analog part ground
10	V_{DDM}	–	1446	40	ADC analog part power supply (3.3 V)
11	AN13	I	1571	40	Analog input 13
12	AN12	I	1696	40	Analog input 12
13	AN11	I	1821	40	Analog input 11
14	AN10	I	1946	40	Analog input 10
15	AN9	I	2071	40	Analog input 9
16	AN8	I	2196	40	Analog input 8
17	AN6	I	2321	40	Analog input 6
18	AN5	I	2446	40	Analog input 5
19	AN4	I	2571	40	Analog input 4
20	AN3	I	2696	40	Analog input 3
21	AN2	I	2821	40	Analog input 2
22	AN1	I	2946	40	Analog input 1
23	AN0	I	3071	40	Analog input 0
24	V_{DD}	–	3335	40	Core and Logic and SRAM memory power supply (1.5V)
25	V_{SS} [1)2)]	–	3415	40	Ground
26	V_{SS} [1)2)]	–	3495	40	
27	V_{DD}	–	3575	40	Core and Logic and SRAM memory power supply (1.5V)

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
28	V_{DDP}	–	3665	40	IO power supply (3.3V)
29	V_{DDP}	–	3755	40	IO power supply (3.3V)
30	V_{SS}	–	3845	40	Ground
31	V_{DD} [1)]	–	3925	40	Core and Logic and SRAM memory power supply (1.5V)
32	V_{SS}	–	4015	40	Ground
33	P1.14	I/O	4117	40	Port 1 line 14
34	P1.13	I/O	4206	40	Port 1 line 13
35	P1.12	I/O	4296	40	Port 1 line 12
36	P2.0	I/O	4385	40	Port 2 line 0
37	P2.1	I/O	4474	40	Port 2 line 1
38	P2.2	I/O	4564	40	Port 2 line 2
39	P2.3	I/O	4653	40	Port 2 line 3
40	P2.4	I/O	4743	40	Port 2 line 4
41	P2.5	I/O	4832	40	Port 2 line 5
42	P2.6	I/O	4922	40	Port 2 line 6
43	P2.7	I/O	5011	40	Port 2 line 7
44	V_{SS}	–	5113	40	Ground
45	V_{SS}	–	5203	40	Ground
46	V_{DDP}	–	5293	40	IO power supply (3.3 V)
47	V_{DD}	–	5383	40	Core and Logic and SRAM memory power supply (1.5V)
48	V_{SS} [1)]	–	5463	40	Ground
49	V_{DD}	–	5553	40	Core and Logic and SRAM memory power supply (1.5V)
50	V_{SS}	–	5633	40	Ground
51	V_{SS}	–	5723	40	Ground
52	P4.0	I/O	5825	40	Port 4 line 0
53	P4.1	I/O	5914	40	Port 4 line 1
54	P4.2	I/O	6003	40	Port 4 line 2

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
55	P4.3	I/O	6286	325	Port 4 line 3
56	P1.0	I/O	6286	492	Port 1 line 0
57	P1.1	I/O	6286	658	Port 1 line 1
58	P1.2	I/O	6286	824	Port 1 line 2
59	P1.8	I/O	6286	991	Port 1 line 8
60	P1.9	I/O	6286	1157	Port 1 line 9
61	P1.10	I/O	6286	1324	Port 1 line 10
62	P1.11	I/O	6286	1490	Port 1 line 11
63	P1.3	I/O	6286	1656	Port 1 line 3
64	V_{DD}	–	6286	1750	Core and Logic and SRAM memory power supply (1.5 V)
65	V_{SS} [1)3)]	–	6286	1830	Ground
66	V_{SS} [1)3)]	–	6286	1920	
67	V_{DD}	–	6286	2000	Core and Logic and SRAM memory power supply (1.5V)
68	V_{DDP}	–	6286	2090	IO power supply (3.3 V)
69	V_{DDP}	–	6286	2180	IO power supply (3.3 V)
70	V_{SS}	–	6286	2270	Ground
71	V_{DD} [1)]	–	6286	2350	Core and Logic and SRAM memory power supply (1.5V)
72	V_{SS}	–	6286	2440	Ground
73	XTAL1	I	6286	2686	Oscillator/PLL/Clock generator input
74	XTAL2	O	6286	2766	Oscillator/PLL/Clock generator output
75	V_{SSOSC}	–	6286	2861	Main oscillator ground
76	V_{SSOSC}	–	6286	2951	Main oscillator ground
77	V_{DDOSC}	–	6286	3031	Main oscillator power supply (1.5 V)
78	V_{DD} [1)]	–	6286	3111	Core and Logic and SRAM memory power supply (1.5V)
79	V_{SS} [1)]	–	6286	3191	Ground
80	V_{DDOSC3}	–	6286	3281	Oscillator power supply (3.3 V)

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
81	V_{DDP}	–	6286	3416	IO power supply (3.3 V)
82	V_{SS} [1)]	–	6286	3506	Ground
83	P1.4	I/O	6286	3620	Port 1 line 4
84	V_{DDP} [1)]	–	6286	3743	IO power supply (3.3 V)
85	P1.5	I/O	6286	3867	Port 1 line 5
86	P1.6	I/O	6286	3979	Port 1 line 6
87	P1.7	I/O	6286	4090	Port 1 line 7
88	TDI	I	6286	4202	JTAG module serial data input
89	TMS	I	6286	4348	JTAG module state machine control input
90	TDO	O	6286	4494	JTAG module serial data output
91	$\overline{\text{TRST}}$	I	6286	4641	JTAG module reset/enable input
92	TCK	I	6286	4787	JTAG module clock input
93	$\overline{\text{BRKOUT}}$	O	6286	4946	OCDS break output
94	$\overline{\text{BRKIN}}$	I	6286	5026	OCDS break input
95	$\overline{\text{TESTMODE}}$	I	6286	5106	Test mode select input
96	BYPASS	I	6286	5265	PLL bypass control input
97	$\overline{\text{NMI}}$	I	6286	5424	Non-maskable interrupt input
98	$\overline{\text{PORST}}$	I	6286	5504	Power-on reset input
99	$\overline{\text{HDRST}}$	I/O	6286	5663	Hardware reset input / Reset indication output
100	V_{DD}	–	6286	5822	Core and Logic and SRAM memory power supply (1.5 V)
101	V_{SS} [1)]	–	6286	5902	Ground
102	V_{SS} [1)]	–	6286	5992	Ground
103	V_{DD}	–	6286	6072	Core and Logic and SRAM memory power supply (1.5V)
104	V_{DDP}	–	6286	6162	IO power supply (3.3 V)
105	V_{DDP}	–	6286	6252	IO power supply (3.3 V)
106	V_{SS}	–	6286	6342	Ground

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
107	V_{DD}[1)]	–	6286	6422	Core and Logic and SRAM memory power supply (1.5V)
108	V_{SS}	–	6286	6512	Ground
109	P3.5	I/O	6286	6670	Port 3 line 5
110	P3.6	I/O	6286	6817	Port 3 line 6
111	P3.8	I/O	6286	6963	Port 3 line 8
112	P3.2	I/O	6286	7110	Port 3 line 2
113	P3.3	I/O	6286	7256	Port 3 line 3
114	P3.7	I/O	6286	7402	Port 3 line 7
115	P3.4	I/O	6286	7549	Port 3 line 4
116	P3.15	I/O	6007	7852	Port 3 line 15
117	P3.14	I/O	5925	7852	Port 3 line 14
118	P3.1	I/O	5844	7852	Port 3 line 1
119	P3.0	I/O	5763	7852	Port 3 line 0
120	P3.10	I/O	5681	7852	Port 3 line 10
121	P3.9	I/O	5600	7852	Port 3 line 9
122	V_{SS}[1)]	–	5506	7852	Ground
123	V_{DDP}	–	5426	7852	IO power supply (3.3 V)
124	V_{DDP}	–	5302	7852	IO power supply (3.3 V)
125	V_{SS}	–	5222	7852	Ground
126	V_{DD}[1)]	–	5142	7852	Core and Logic and SRAM memory power supply (1.5V)
127	V_{SS}	–	5062	7852	Ground
128	V_{SS}[1)]	–	4982	7852	Ground
129	V_{DD}[1)]	–	4902	7852	Core and Logic and SRAM memory power supply (1.5V)
130	V_{DDP}	–	4822	7852	FLASH memory power supply (3.3 V)
131	V_{DDP}[1)]	–	4742	7852	FLASH memory power supply (3.3 V)
132	V_{SS}[1)]	–	4617	7852	Ground
133	V_{DDP}	–	4537	7852	IO power supply (3.3 V)

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
134	P3.13	I/O	4443	7852	Port 3 line 13
135	P3.12	I/O	4362	7852	Port 3 line 12
136	P3.11	I/O	4281	7852	Port 3 line 11
137	P0.0	I/O	4199	7852	Port 0 line 0
138	P0.1	I/O	4118	7852	Port 0 line 1
139	P0.2	I/O	4036	7852	Port 0 line 2
140	P0.3	I/O	3955	7852	Port 0 line 3
141	P0.8	I/O	3874	7852	Port 0 line 8
142	P0.9	I/O	3792	7852	Port 0 line 9
143	P0.10	I/O	3711	7852	Port 0 line 10
144	P0.11	I/O	3629	7852	Port 0 line 11
145	V_{DD}	–	3536	7852	Core and Logic and SRAM memory power supply (1.5V)
146	V_{SS} [1)]	–	3456	7852	Ground
147	V_{SS} [1)]	–	3376	7852	Ground
148	V_{DD}	–	3296	7852	Core and Logic and SRAM memory power supply (1.5V)
149	V_{DDP}	–	3216	7852	FLASH memory power supply (3.3 V)
150	V_{SS}	–	3136	7852	Ground
151	V_{DD} [1)]	–	3056	7852	Core and Logic and SRAM memory power supply (1.5V)
152	V_{SS}	–	2976	7852	Ground
153	FCLN0	O	2886	7852	MSC0 Differential Driver Clock Output Negative
154	FCLP0A	O	2766	7852	MSC0 Differential Driver Clock Output Positive A
155	SON0A	O	2666	7852	MSC0 Differential Driver Serial Data Output Negative A
156	SOP0A	O	2546	7852	MSC0 Differential Driver Serial Data Output Positive A
157	NC [1)]	–	2296	7852	LVDS Reference

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
158	P2.9	I/O	2042	7852	Port 2 line 9
159	P2.10	I/O	1960	7852	Port 2 line 10
160	P2.11	I/O	1879	7852	Port 2 line 11
161	P2.12	I/O	1797	7852	Port 2 line 12
162	P2.8	I/O	1716	7852	Port 2 line 8
163	P2.13	I/O	1635	7852	Port 2 line 13
164	P0.4	I/O	1553	7852	Port 0 line 4
165	P0.5	I/O	1472	7852	Port 0 line 5
166	P0.12	I/O	1390	7852	Port 0 line 12
167	P0.13	I/O	1309	7852	Port 0 line 13
168	V_{DD}	–	1215	7852	Core and Logic and SRAM memory power supply (1.5V)
169	V_{SS} [1)4)]	–	1135	7852	Ground
170	V_{SS} [1)4)]	–	1055	7852	
171	V_{DD}	–	975	7852	Core and Logic and SRAM memory power supply (1.5V)
172	V_{DDP}	–	895	7852	IO power supply (3.3 V)
173	V_{SS}	–	815	7852	Ground
174	V_{DD} [1)]	–	735	7852	Core and Logic and SRAM memory power supply (1.5V)
175	V_{SS}	–	655	7852	Ground
176	P0.6	I/O	561	7852	Port 0 line 6
177	P0.7	I/O	480	7852	Port 0 line 7
178	P0.14	I/O	398	7852	Port 0 line 14
179	P0.15	I/O	317	7852	Port 0 line 15
180	P5.0	I/O	40	7553	Port 5 line 0
181	P5.1	I/O	40	7376	Port 5 line 1
182	P5.2	I/O	40	7200	Port 5 line 2
183	P5.3	I/O	40	7023	Port 5 line 3
184	P5.4	I/O	40	6847	Port 5 line 4

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
185	P5.5	I/O	40	6671	Port 5 line 5
186	P5.6	I/O	40	6494	Port 5 line 6
187	P5.7	I/O	40	6318	Port 5 line 7
188	TRCLK	O	40	6129	OCDS L2 trace clock
189	V_{DD}	–	40	5928	Core and Logic and SRAM memory power supply (1.5 V)
190	V_{SS} [1)5)]	–	40	5848	Ground
191	V_{SS} [1)5)]	–	40	5758	
192	V_{DD}	–	40	5678	Core and Logic and SRAM memory power supply (1.5 V)
193	V_{DDP}	–	40	5588	IO power supply (3.3 V)
194	V_{DDP}	–	40	5498	IO power supply (3.3 V)
195	V_{SS}	–	40	5408	Ground
196	V_{DD} [1)]	–	40	5328	Core and Logic and SRAM memory power supply (1.5 V)
197	V_{SS}	–	40	5238	Ground
198	P5.8	I/O	40	5049	Port 5 line 8
199	P5.9	I/O	40	4872	Port 5 line 9
200	P5.10	I/O	40	4696	Port 5 line 10
201	P5.11	I/O	40	4520	Port 5 line 11
202	P5.12	I/O	40	4343	Port 5 line 12
203	P5.13	I/O	40	4167	Port 5 line 13
204	P5.14	I/O	40	3990	Port 5 line 14
205	P5.15	I/O	40	3814	Port 5 line 15
206	V_{DD} [1)]	–	40	3690	Core and Logic and SRAM memory power supply (1.5 V)
207	V_{SS} [1)]	–	40	3610	Ground
208	V_{SSAF}	–	40	3336	FADC Ground
209	V_{DDAF}	–	40	3256	FADC analog part logic power supply (1.5V)
210	NC	–	40	3131	Not Connected

Table 2 Pad Definitions and Functions (cont'd)

Pad Num	Pad Name (Symbol)	In / Out	Position [mm]		Function
			x	y	
211	V_{DDMF}	–	40	2946	FADC analog power supply (3.3V)
212	V_{SSMF}	–	40	2821	FADC Ground
213	V_{FAREF}	–	40	2696	ADC reference voltage
214	V_{FAGND}	–	40	2571	ADC reference ground
215	AN35	I	40	2446	FADC[1] negative analog input 35
216	AN34	I	40	2321	FADC[1] positive analog input 34
217	AN33	I	40	2196	FADC[0] negative analog input 33
218	AN32	I	40	2071	FADC[0] positive analog input 32
219	AN31	I	40	1821	Analog input 31
220	AN30	I	40	1696	Analog input 30
221	AN29	I	40	1571	Analog input 29
222	AN28	I	40	1446	Analog input 28
223	AN7	I	40	1321	Analog input 7
224	AN27	I	40	1196	Analog input 27
225	AN26	I	40	1071	Analog input 26
226	AN25	I	40	946	Analog input 25
227	AN24	I	40	821	Analog input 24
228	AN23	I	40	696	Analog input 23
229	AN22	I	40	571	Analog input 22
230	AN21	I	40	446	Analog input 21
231	AN20	I	40	321	Analog input 20

1) This pad is not bonded in TC1766 package devices
2) Giant pad 1 with the dimension of 162µm x 253.22µm
3) Giant pad 2 with the dimension of 162µm x 253.22µm
4) Giant pad 3 with the dimension of 152µm x 253.22µm
5) Giant pad 4 with the dimension of 152µm x 253.22µm

Note: Although not all pads are bonded in TC1766 package, it is recommended to bond as many supply pads as possible in system.

Note: All V_{SS} pads must be externally connected together. V_{DD} pads of the same type (e.g. all V_{DDP} lines) should be externally connected together.

Note: All dimensions refer to the corner of the die (0,0) within the chip sealing ring. Appropriate adjustment must be made to include sawing tolerances.

3 Electrical Parameters

3.1 General Parameters

3.1.1 Pad Driver and Pad Classes Summary

Please refer to the TC1766 package Data Sheet for the overview of the different pad driver classes and its basic characteristics, DC parameters and Absolute Maximum Ratings.

Table 3 shows the assignments of all digital I/O pads to pad classes and to V_{DD} power supply pads.

Table 3 Assignments of Digital Pads to Pad Classes and Power Supply Pads

Pads	Pad Classes	Power Supply	
Port 0, Port 1 [7:0], Port 1 [14:12], Port 2 line 4, Port 2 [7:6], Port 2 line 13, Port 3 [11:10], Port 4 [1:0], TDI, BYPASS	Class A1 (3.3 V)	V_{DDP}	V_{SS}
Port 1 [11:8], Port 2 [3:0], Port 2 line 5, Port 2 [12:8], Port 3 [9:0], Port 3 [15:12], Port 4 [3:2], Port 5, $\overline{\text{TRST}}$, TCK, TDO, TMS, NMI, $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$	Class A2 (3.3 V)	V_{DDP}	
$\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$	Class A3 (3.3 V)	V_{DDP}	
TRCLK	Class A4 (3.3 V)	V_{DDP}	
FCLP0A, FCLN0, SOP0A, SON0	Class C (nominal 3.3 V)	V_{DDP}	
AN31 to AN0 V_{AREF0}, V_{AGND0}	Class D (nominal 3.3 V)	V_{DDM}	V_{SSM}
AN35 to AN32 V_{FAREF}, V_{FAGND}	Class D (nominal 3.3 V)	V_{DDMF}, V_{DDAF}	V_{SSMF} V_{SSAF}
XTAL1, XTAL2	(nominal 3.3 V)	V_{DDOSC3} V_{DDOSC}	V_{SSOSC}
no functional pads assigned for Flash module	(nominal 3.3 V)	V_{DDFL3}	V_{SS}

3.1.2 Storage Conditions

TC1766 dies may be stored for a certain time under the conditions described below.

Table 4 Bare Die Storage Conditions and Duration

Storage Type	Ambient Atmosphere	Storage Condition		Storage Time
Bare dies mounted on surf tape[1] with Nitto film. Reels with Surf-Tape inclusive of desiccant sealed in Moisture Barrier Bag	Air	Atmosphere: Temperature: Humidity: Pressure:	>99% Nitrogen or inert gas 17°C – 25°C 7-25% RH slightly above ambient atmospheric pressure	max. 6 months
Bare dies mounted on carrier tape, protected with cover tape. Reels with Carrier-Tape inclusive of desiccant sealed in Moisture Barrier Bag				max. 12 months

1) Surf Tape packing will be replaced by Carrier Tape packing in the second quarter of 2010.

The dies shall be processed before end of maximum storage time is expired. Processing beyond expiring date is on user's risk. The storage time starts with the product date code.

3.1.3 Operating Conditions

Please refer to the TC1766 package Data Sheet for the details of the Operating Condition Parameters. This section documents the operating condition parameters that are not specified in the TC1766 package Data Sheet.

Table 5 Operating Condition Parameters

Parameter	Symbol		Limit Values		Unit	Notes Conditions
			Min.	Max.		
Digital supply voltage[1)]	V_{DDSRAM}	SR	1.42	1.58[2)]	V	–
Temperature of the bottom side of the die	T_D	SR	-40	+150	°C	–
Overload current	I_{OV}		–	0	mA	[3)]

1) Digital supply voltages applied to the TC1766 must be static regulated voltages which allow a typical voltage swing of ±5%.

2) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

3) An overload condition is not intended to be a normal operating condition.

3.2 DC Parameters

3.2.1 Input/Output Pins

Table 6 provides the characteristics of the input/output pins which are specific for the TC1766 Bare Die. Please refer to the TC1766 package Data Sheet for the common Input/Output DC Characteristics.

Table 6 Input/Output DC Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Notes Conditions
		Min.	Max.		
Class A Pads (3.3V-5% ≤ V_{DDP} ≤ 3.3V-3%)					
Output high voltage[1]	V_{OHA} CC	2.4	–	V	I_{OH} = -1.3 mA for medium driver mode, A1/A2 pads
		V_{DDP} - 0.6	–	V	I_{OH} = -1 mA for medium driver mode, A1/A2 pads I_{OH} = -280 µA for weak driver mode, A1/A2 pads
Class A Pads (3.3V-3% < V_{DDP} ≤ 3.3V+5%)					
Note: Please refer to TC1766 package Data Sheet.					

1) I_{OH} and V_{OHA} are based on T_D = 150°C.

3.3 Wafer Characteristics

Table 7 Wafer Characteristics

Item	Characteristic
Metallization layers	7
Metallization material	1st metallisation: Cu 2nd metallisation: Cu 3rd metallisation: Cu 4th metallisation: Cu 5th metallisation: Cu 6th metallisation: Cu 7th metallisation (BD-step): AlCu 7th metallisation (BF-step): AlCu, NiP, Pd, Au
Metallization thickness	Met1: 0.29 µm Met2: 0.32 µm Met3: 0.33 µm Met4: 0.32 µm Met5: 0.55 µm Met6: 0.55 µm Met7(BD-step): 1.2 µm Met7(BF-step): 4.53 µm
Topside passivation	Oxide/Nitride/Imide (subject to change) 0.45 / 0.4 / 5 µm
Backside metallization	none (silicon), must be connected to V_{SS}

4 Packaging

4.1 Chip Outline

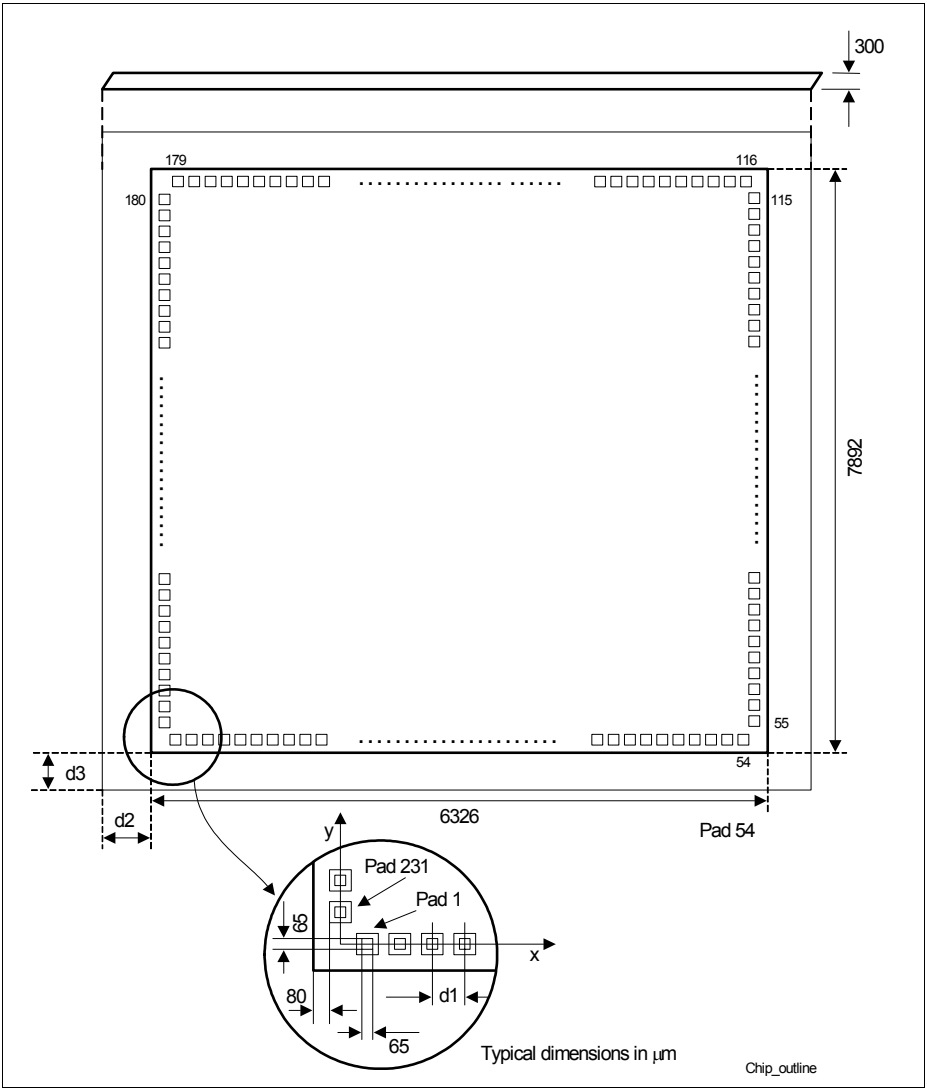

Figure 4 Chip Outline (top view)

Table 8 Dimensions of Pads Layout

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Distance between pads	*d1*	80	125	274	µm
Distance from border of die to border of chip, x-axis	*d2*	0	57	114	µm
Distance from border of die to border of chip, y-axis	*d3*	0	104	208	µm

4.2 Surf Tape Characteristics

Note: Surf Tape packing will be replaced by Carrier Tape packing in the second quarter of 2010.

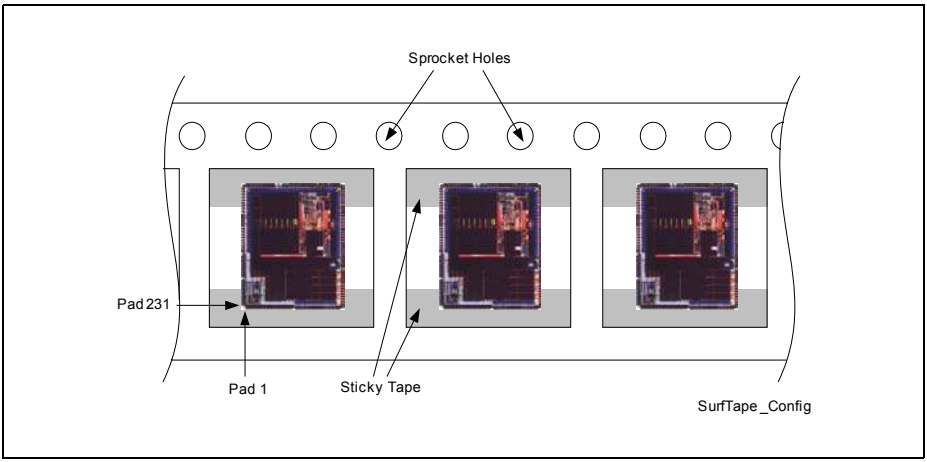

Figure 5 Die Placement on Surf Tape (top View)

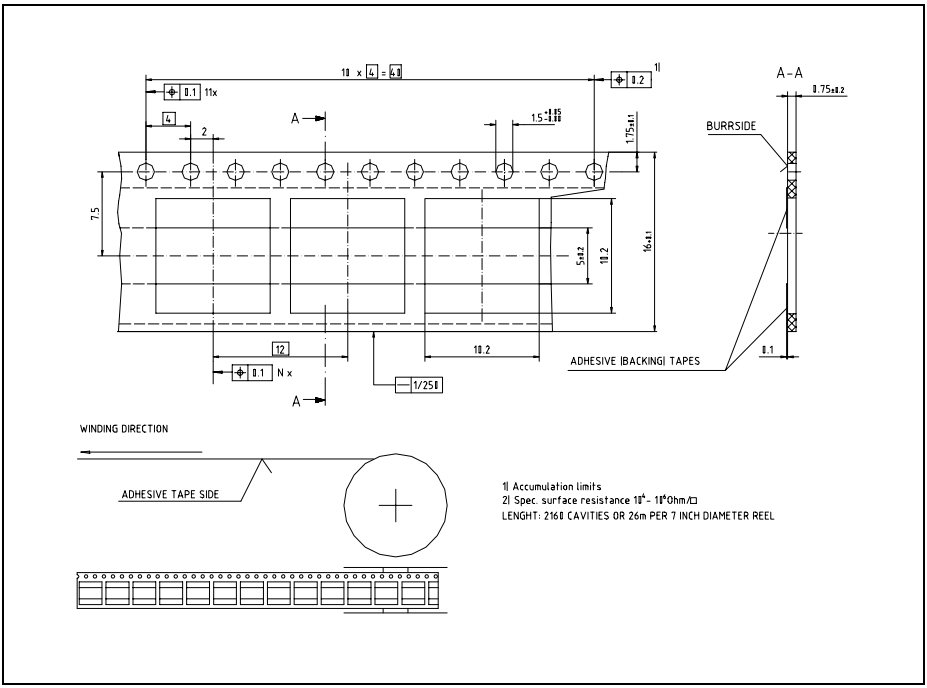

Figure 6 Surf Tape Dimensions

4.3 Carrier Tape Characteristics

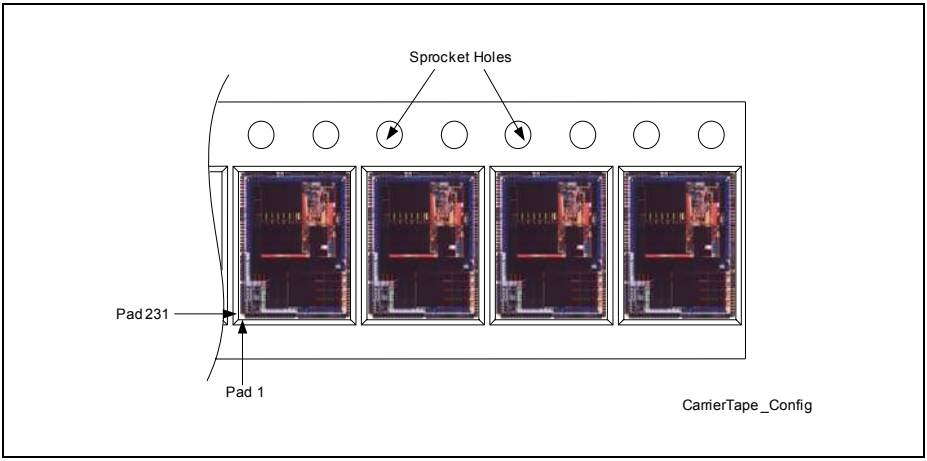

Figure 7 Die Placement on Carrier Tape (top View)

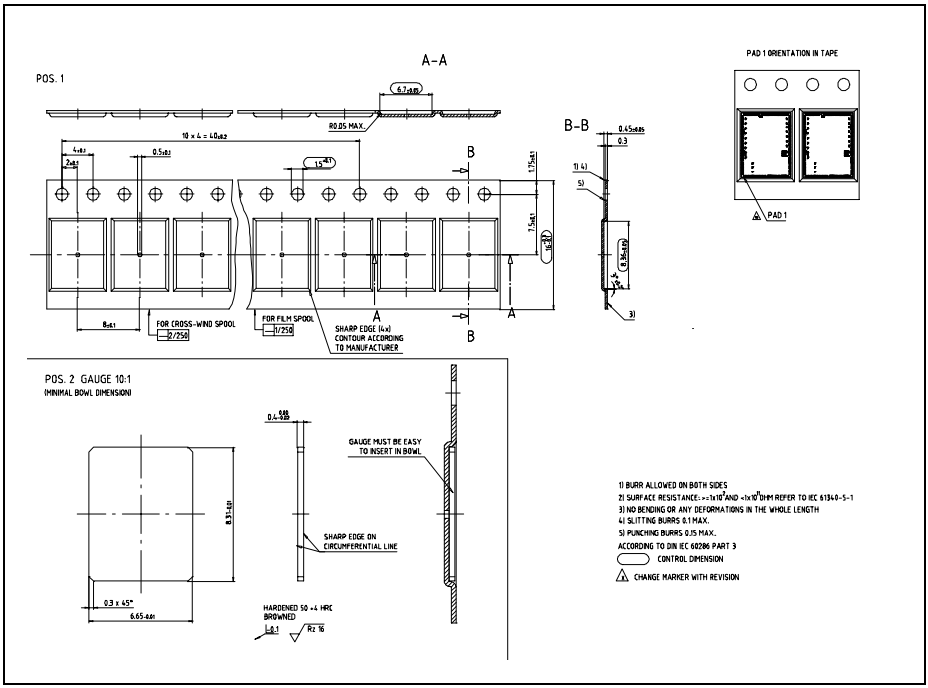

Figure 8 Carrier Tape Dimensions

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG