FAIRCHILD SEMICONDUCTOR™

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GTLP6C817
Low Drive GTLP/LVTTL 1:6 Clock Driver

General Description

The GTLP6C817 is a low drive clock driver that provides TTL to GTLP signal level translation (and vice versa). The device provides a high speed interface between cards operating at TTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

Features

- Interface between LVTTL and GTLP logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced CMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- 5V over voltage tolerance on LVTTL ports
- Open drain on GTLP to support wired-or connection
- A Port source/sink –12mA/+12mA
- B Port sink +40mA
- 1:6 fanout clock driver for TTL port
- 1:2 fanout clock driver for GTLP port

Ordering Code:

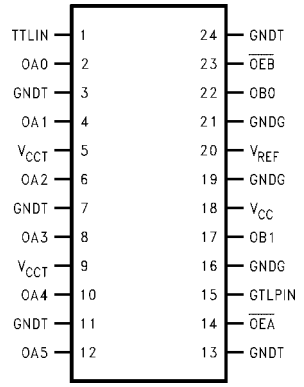
Order Number	Package Number	Package Description
GTLP6C817MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device is also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

Pin Names	Description
TTLIN, GTLPIN	Clock Inputs (TTL and GTLP respectively)
$\overline{OEB}$	Output Enable (Active LOW) GTLP Port (TTL Levels)
$\overline{OEA}$	Output Enable (Active LOW) TTL Port (TTL Levels)
V_{CCT}.GNDT	LVTTL Output Supplies (3V)
V_{CC}	Internal Circuitry V_{CC} (5V)
GNDG	OBn GTLP Output Grounds
V_{REF}	Voltage Reference Input
OA0–OA5	TTL Buffered Clock Outputs
OB0–OB1	GTLP Buffered Clock Outputs

Connection Diagram



Functional Description

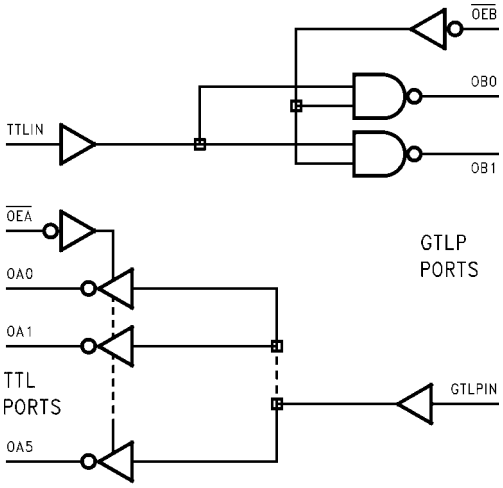
The GTLP6C817 is a low drive clock driver providing LVTTL-to-GTLP clock translation, and GTLP-to-LVTTL clock translation in the same package. The LVTTL-to-GTLP direction is a 1:2 clock driver path with a single Enable pin ($\overline{OEB}$). For the GTLP-to-LVTTL direction the clock receiver path is a 1:6 buffer with a single Enable control ($\overline{OEA}$). Data polarity is inverting for both directions.

Truth Tables

Inputs		Outputs
TTLIN	**$\overline{OEB}$**	**OBn**
H	L	L
L	L	H
X	H	High Z

Inputs		Outputs
GTLPIN	**$\overline{OEA}$**	**OAn**
H	L	L
L	L	H
X	H	High Z

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to +7.0V
DC Output Sink Current into	
OA Port I_{OL}	24 mA
DC Output Source Current	
from OA Port I_{OH}	−24 mA
DC Output Sink Current into	
OB Port in the LOW State I_{OL}	80 mA
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
ESD Rating	> 2000V
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Supply Voltage	
V_{CC}	4.75V to 5.25V
V_{CCT}	3.15V to 3.45V
Bus Termination Voltage (V_{TT})	
GTLP	1.47V to 1.53V
V_{REF}	0.98V to 1.02V
Input Voltage (V_I) on INA Port	
and Control Pins	0.0V to 5.5V
HIGH Level Output Current (I_{OH})	
OA Port	−12 mA
LOW Level Output Current (I_{OL})	
OA Port	+12 mA
OB Port	+40 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_o Absolute Maximum Rating must be observed.

Note 3: Unused input must be held HIGH or LOW.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 4)	Max	Units
V_{IH}	GTLPIN			V_{REF} + 0.05		V_{TT}	V
	Others			2.0			
V_{IL}	GTLPIN			0.0		V_{REF} − 0.05	V
	Others					0.8	
V_{REF}	GTLP				1.0		V
(Note 5)	GTL				0.8		
V_{TT}	GTLP				1.5		V
(Note 5)	GTL				1.2		
V_{IK}		V_{CC} = 4.75V V_{CCT} = 3.15V	I_I = −18 mA			−1.2	V
V_{OH}	OAn Port	V_{CC} = 4.75V V_{CCT} = 3.15V	I_{OH} = −100 µA	V_{CC}− 0.2			V
			I_{OH} = −6 mA	2.4			
			I_{OH} = −12 mA	2.2			
V_{OL}	OAn Port	V_{CC} = 4.75V V_{CCT} = 3.15V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 6 mA			0.4	
			I_{OL} = 12 mA			0.5	
V_{OL}	OBn Port	V_{CC} = 4.75V V_{CCT} = 3.15V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 40 mA			0.5	
I_I	TTLIN/ Control Pins	V_{CC} = 5.25V V_{CCT} = 3.45V	V_I = 5.25V V_I = 0V			5 −5	µA
	GTLPIN	V_{CC} = 5.25V V_{CCT} = 3.45V	$V_I = V_{TT}$ V_I = 0			5 −5	µA
I_{OFF}	TTLIN, OAn Port, Control Pins	V_{CC} = 0	V_I or V_O = 0V to 5.25V			30	µA
	GTLPIN, OBn Port	V_{CCT} = 0	V_I or V_O = 0 to V_{TT}			30	
I_{OZH}	OAn Port	V_{CC} = 5.25V	V_O = 5.25V			5	µA
	OBn Port	V_{CCT} = 3.45V	V_O = 1.5V			5	
I_{OZL}	OAn Port	V_{CC} = 5.25V	V_O = 0			−5	µA
	OBn Port	V_{CCT} = 3.45V	V_O = 0				

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 4)	Max	Units
$I_{PU/PD}$	All Ports	$V_{CC} = V_{CCT}$ = 0 to 1.5V	$\overline{OE}$ = Don't Care			30	µA
I_{CC} (5V)	OAn or OBn Ports	V_{CC} = 5.25V, V_{CCT} = 3.45V	Outputs HIGH			10	mA
			Outputs LOW			10	
			Outputs Disabled, $V_I = V_{CC}$ or GND			10	
I_{CC} (3V)	OAn or OBn Ports	V_{CC} = 5.25V, V_{CCT} = 3.45V	Outputs HIGH, LOW			45	µA
			Outputs Disabled, $V_I = V_{CC}$ or GND			45	
ΔI_{CC}	TTLIN	V_{CC} = 5.25V, V_{CCT} = 3.45V	$V_I = V_{CC}$–2.1			1	mA
C_{IN}	Control Pins/GTLPIN/TTLIN		$V_I = V_{CC}$ or 0		3	3.5	pF
C_{OUT}	OAn Port		$V_I = V_{CC}$ or 0		3	4.5	pF
	OBn Port		$V_I = V_{CC}$ or 0		4	5	

Note 4: All typical values are at V_{CC} = 5.0V V_{CCT} = 3.3V and T_A = 25°C.

Note 5: GTLP V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and R_{TERM} can be adjusted to accommodate backplane impedances other than 50Ω, within the boundaries of not exceeding the DC Absolute I_{OL} ratings. Similarly V_{REF} can be adjusted to compensate for changes in V_{TT}.

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air temperature. V_{REF} = 1.0V (unless otherwise noted).

C_L = 30 pF for OBn Port and C_L = 50 pF for OAn Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 6)	Max	Units
t_{PLH}	TTLIN	OBn	2.3		4.7	ns
t_{PHL}			1.5		4.6	
t_{PLH}	$\overline{OEB}$	OBn	2.4		4.8	ns
t_{PHL}			1.6		4.7	
t_{RISE}	Transition Time, OB Outputs (20% to 80%)			1.7		ns
t_{FALL}	Transition Time, OB outputs (20% to 80%)			2.1		ns
t_{RISE}	Transition Time, OA outputs (10% to 90%)			2.7		ns
t_{FALL}	Transition Time, OA outputs (10% to 90%)			2.2		ns
t_{PZH}, t_{PZL}	$\overline{OEA}$	OAn	2.4		6.5	ns
t_{PLZ}, t_{PHZ}			2.0		6.5	
t_{PLH}	GTLPIN	OAn	3.1		6.6	ns
t_{PHL}			2.8		6.0	

Note 6: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

Extended Electrical Characteristics

Over recommended ranges of supply voltage and operating free-air temperature V_{REF} = 1.0V (unless otherwise noted).

C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol		From (Input)	To (Output)	Min	Typ (Note 7)	Max	Unit
t_{OSLH}	(Note 8)	A	B		.05	.4	ns
t_{OSHL}	(Note 8)	A	B		.05	.4	
t_{PS}	(Note 9)	A	B		0.5	1.0	ns
$t_{PV(HL)}$	(Note 10) (Note 11)	A	B			.7	ns
t_{OSLH}	(Note 8)	B	A		.12	.5	ns
t_{OSHL}	(Note 8)	B	A		.12	.5	
t_{OST}	(Note 8)	B	A		.6	1.0	ns
t_{PS}	(Note 9)	B	A		0.5	1.0	ns
t_{PV}	(Note 10)	B	A			1.2	ns

Note 7: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

Note 8: t_{OSHL}/t_{OSLH} and t_{OST} - Output-to-Output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

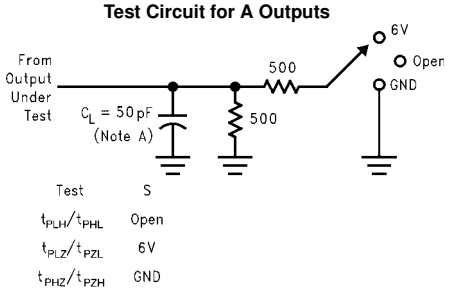
Note 9: t_{PS} - Pin or Transition skew is defined as the difference between the LOW-to-HIGH transition and the HIGH-to-LOW transition on the same pin. The parameter is measured across all the outputs of the same chip is specified for a specific worst case V_{CC} and temperature. This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 10: t_{PV} - Part-to-Part skew is defined as the absolute value of the difference between the actual propagation design for all outputs from device-to-device. The parameter is specified for a specific worst case V_{CC} and temperature. This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP output could vary on the backplane due to the loading and impedance seen by the device.

Note 11: Due to the open drain structure on GTLP outputs, t_{OST} and $t_{PV(LH)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_T values in the actual application.

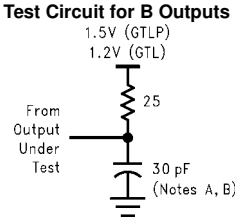
Test Circuit and Timing Waveforms

Test Circuit for A Outputs



Note A: C_L includes probes and jig capacitance.

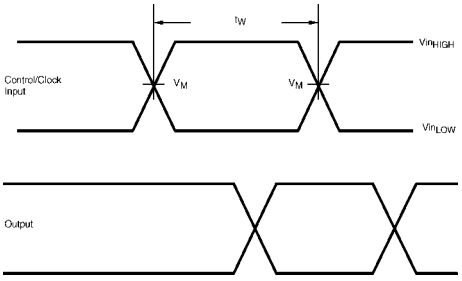
Test Circuit for B Outputs



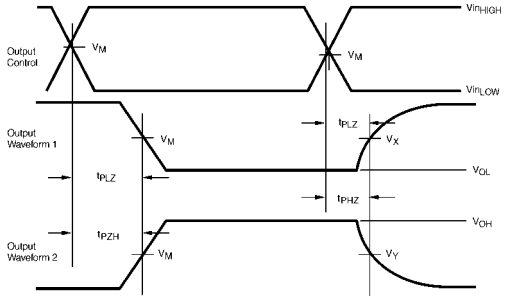
Note A: C_L includes probes and jig capacitance.

Note B: For B Port C_L = 30 pF is used for worst case.

Voltage Waveform - Propagation Delay Times



Voltage Waveform - Enable and Disable Times



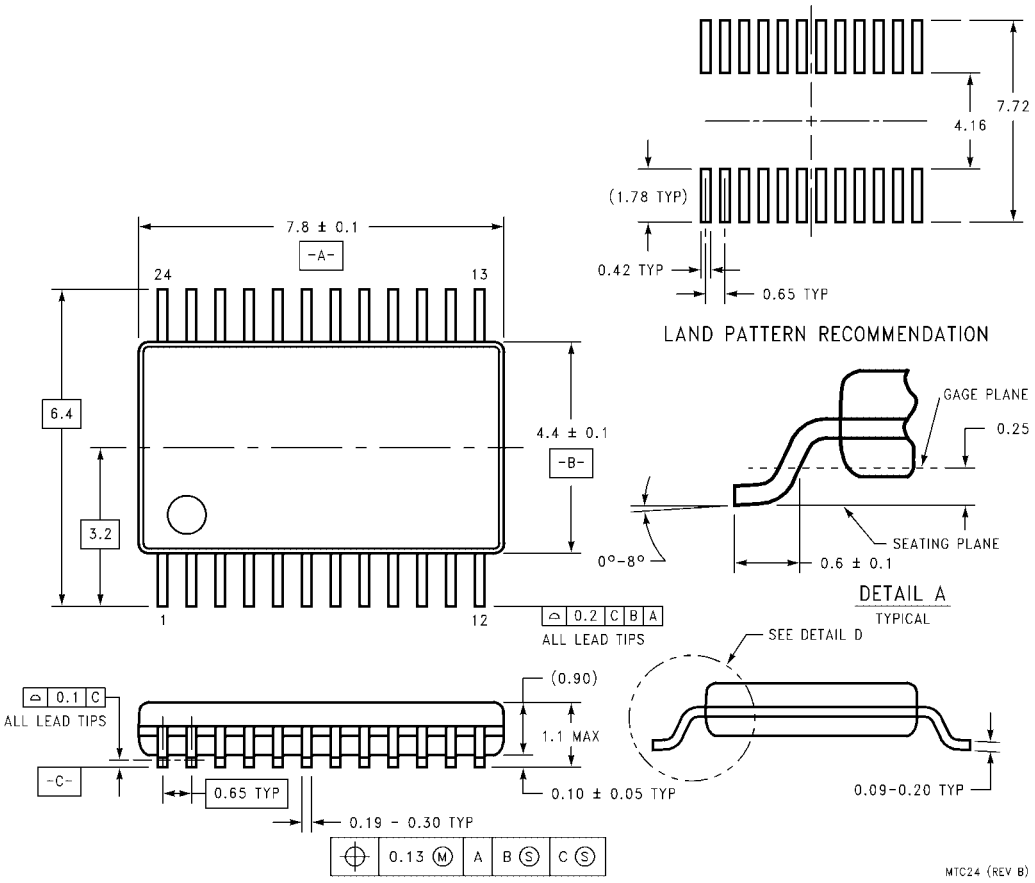
Output Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the control output
Output Waveforms 2 is for an output with internal conditions such that the output is HIGH except when disabled by the control output

Input and Measure Conditions

	A or LVTTL Pins	B or GTLP Pins
V_{inHIGH}	V_{CC}	1.5
V_{inLOW}	0.0	0.0
V_M	$V_{CC}/2$	1.0
V_X	V_{OL} + 0.3V	N/A
V_Y	V_{OH} + 0.3V	N/A

All input pulses have the following characteristics: Frequency = 10MHz, $t_{RISE} = t_{FALL}$ = 2 ns, Z_O = 50Ω.
The outputs are measured one at a time with one transition per measurement.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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