S t r u c t u r e　Silicon monolithic integrated circuit
Product Name　Audio music player for cellular phone
Product No.　**BU8903GU**
F e a t u r e s　The audio decoding HE-AAC, AAC-LC and MP3

○Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
Analog supply voltage	AVDD	-0.3 ～ 4.5	V	AVDD
Digital I/O supply voltage	VDDIO	-0.3 ～ 4.5	V	DVDDIO
Digital I/O2 supply voltage	VDDIO2	-0.3 ～ 4.5	V	DVDDIO2
CORE supply voltage	VDDCO	-0.3 ～ 2.16	V	DVDDCORE
Voltage applied to pins	VIN	DVSS-0.3 ～ VDDIO+0.3	V	
Power dissipation	Pd	1300	mW	(*1)
Storage temperature range	Tstg	-50 ～ 125	℃	
Operating temperature range	Topr	-30 ～ 85	℃	

(*1) Note:　Reduce to 13.0mW/℃ when Ta = 25℃ or above

○Recommended Operating Power Supply Voltage Range

Parameter	Symbol	rating			Unit	Remarks
		Min	Typ	Max		
Analog supply voltage	AVDD	2.7	2.8	3.3	V	AVDD
Digital I/O supply voltage	DVDDIO	DVDDCO	1.8	3.3	V	DVDDIO
Digital I/O2 supply voltage	VDDIO2	DVDDCO	3.0	3.3	V	DVDDIO2
Digital CORE supply voltage	VDDCO	1.40	1.5	1.65	V	DVDDCORE
MCLK1 input frequency	FMCLK1	32.768	-	26 000	KHz	32.768kHz or 2.688MHz~26MHz
MCLK2 input frequency	FMCLK2	2688	-	26 000	KHz	sine wave / square wave 2.688MHz~26MHz
MCLK duty	DMCLK	40	50	60	%	
Analog pin's load resistance	RL	10	-	-	kΩ	

This chip is not designed to protect itself against radioactive rays.

Status of this document

The English version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document,formal version takes priority.

○Electrical Characteristics

OVERALL electrical characteristics (Unless otherwise noted, Ta = 25℃)

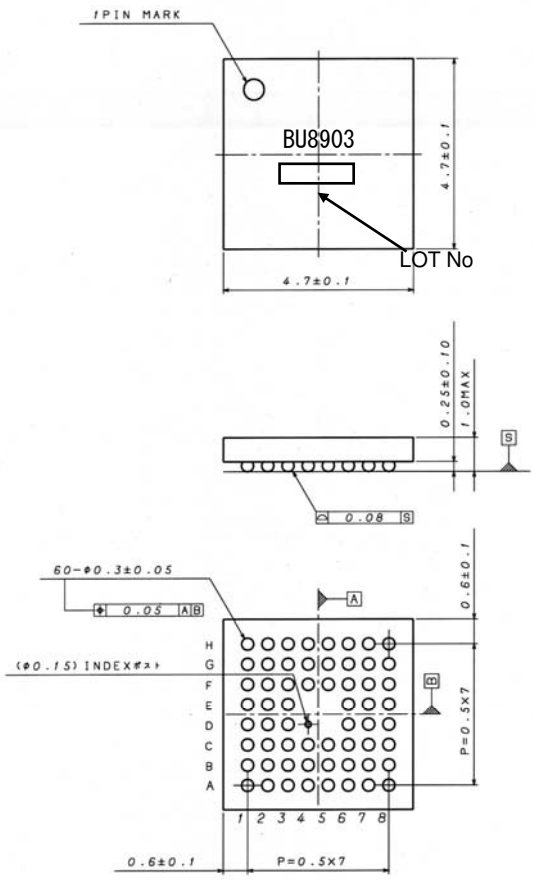
Parameter	Symbol	Rating			Unit	Conditions
		Min	Typ	Max		
Digital DC characteristics						
High-level input voltage	VIH	DVDDIO*0.7	-	-	V	
Low-level input voltage	VIL	-	-	DVDDIO *0.3	V	
High-level input current	IIH	-	-	1	uA	VIH=VDDIO
Low-level input current	IIL	-1	-	-	uA	VIL=DVSS
High-level output voltage	VOH	DVDDIO*0.8	-	-	V	IOH= -2mA (9)
Low-level output voltage	VOL	-	-	DVDDIO *0.2	V	IOL= 2mA (10)
Analog DC characteristics	DVDDCORE=1.5 [V], DVDDIO=3.0[V], AVDD=3.0[V], PLLVDD=3.0[V]					
VREF pin voltage	VAGND	1.30	1.45	1.60	V	IOUT=0A(no load)
Analog pin voltage	VOUT	1.30	1.45	1.60	V	IOUT=0A(no load) Not playing
General characteristics						
VREF pin rise time	TRVR	-	8	25	mS	When CVREF = 1uF, NRST=L→H
Analog pin characteristics	DVDDCORE=1.5[V], DVDDIO=3.0[V], AVDD=3.0[V], PLLVDD=3.0[V]					
Analog amplitude	VMAX	1.60	1.74	1.90	Vp-p	Theoretical value for dynamic range
Power consumption	DVDDCORE=1.5 [V], DVDDIO=3.0[V], AVDD=3.0[V], PLLVDD=3.0[V]					
Analog Idd1 (DA Converter)	AIDD1	-	3.6	5	mA	Playing
Analog Idd2 (PLLVDD)	AIDD2	-	0.6	1	mA	PLL related. Core clock dependent.
Digital Idd11 (DVDDCORE)	DIDD11	-	6.6	8	mA	Playing MP3
Digital Idd11 (DVDDCORE)	DIDD11	-	7.9	11	mA	Playing AAC-LC
Digital Idd11 (DVDDCORE)	DIDD11	-	14.7	17	mA	Playing HE-AAC
Digital Idd12 (DVDDIO+DVDDIO2)	DIDD12	-	0.4/0.5	1.0	mA	Playing
Analog Idd3	AIDD2	-	-	2	uA	Standby mode
Digital Idd20 (DVDDCORE)	DIDD20	-	20	150	uA	Standby mode (8)
Digital Idd21 (DVDDIO+DVDDIO2)	DIDD21	-	-	5	uA	Standby mode

DAC characteristics Typical value are at Ta=25[degree C] / AVDD=3.0[V]. Output load = no load .

Parameter	Symbol	Ratings			Unit	Note/conditions
		Min	Typ	Max		
Input Resolution			16		Bits	
Output range		1.45±0.80	1.45±0.87	1.45±0.95	V	A-weight Center level = 1.45V.
Total harmonic distortion +Noise	THD+N	70 (1)	85	-	dB	fs=44.1,48kHz, 20kHz LPF
Cross-talk	Xtalk	70 (1)	90	-	dB	1kHz ouput, 1kHz BPF
Signal to noise ratio	SNR	75 (1)	90(1)	-	dB	fs=44.1,48kHz, A-weight
Power Supply Rejection Ratio	PSRR	50 (2)	60	-	dB	A-weight,1kHz BPF

(1): Input frequency (f_in = 1kHz), 0 dBFs (FullScale).

○ External measure and View



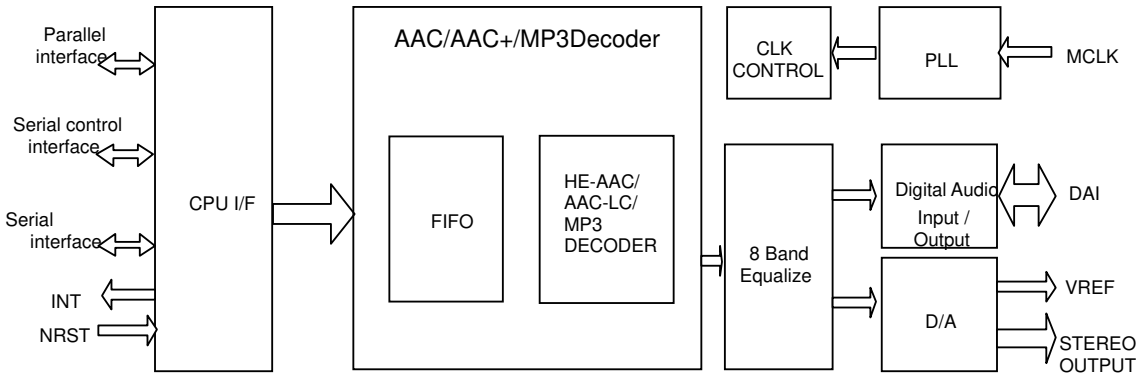
VCSP85H4（60Pin）　(Unit: mm)

○Pin layout diagram

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
A1	TM0	C5	IFSEL	F5	VREFSEL
A2	D11	C6	IICADDR	F6	VREF
A3	SPISDO(WR)	C7	COREDOWN	F7	LOUT
A4	DVDDCORE	C8	DIGLR	F8	MOUT
A5	DVSS	D1	DVSS	G1	D8
A6	MCLK1	D2	D4	G2	PLLVSS
A7	D13	D3	D5	G3	PLLVDD
A8	TM1	D6	DIGCK	G4	IICSDA
B1	D10	D7	DIGDOUT	G5	DVDDIO
B2	INT	D8	DIGDIN	G6	AVDD
B3	SPISDI(A0)	E1	DVDDCORE	G7	AVSS
B4	DVDDIO	E2	D3	G8	NC
B5	SPICLK(RD)	E3	D2	H1	TM2
B6	D12	E6	DVDDIO2	H2	D9
B7	D14	E7	DACMCK	H3	MCLK2
B8	D15	E8	DVSS	H4	DVSS
C1	D6	F1	D1	H5	DVDDCORE
C2	D7	F2	D0	H6	ROUT
C3	NRST	F3	PLLFILTER	H7	NC
C4	SPISEL(CS)	F4	IICSCL	H8	NC

Test pin setting　　TM0=L, TM1=L, TM2=L

○ Block diagram



○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents, we called ,Technical note, Functinal description, Application note.

Notes

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