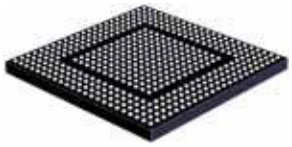
Freescale Semiconductor
Data Sheet: Advance Information

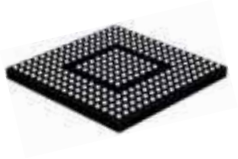
Document Number: PXS30
Rev. 1, 09/2011

PXS30

PXS30 Microcontroller Data Sheet



473 MAPBGA
(19 x 19 mm)



257 MAPBGA
(14 x 14 mm)

The PXS30 family represents a new generation of 32-bit microcontrollers based on the Power Architecture®. These devices provide a cost-effective, single chip display solution for the industrial market. An integrated TFT driver with digital video input ability from an external video source, significant on-chip memory, and low power design methodologies provide flexibility and reliability in meeting display demands in rugged environments. The advanced processor core offers high performance processing optimized for low power consumption, operating at speeds as high as 64 MHz. The family itself is fully scalable from 512 KB to 1 MB internal flash memory. The memory capacity can be further expanded via the on-chip QuadSPI serial flash controller module.

The PXS30 family platform has a single level of memory hierarchy supporting on-chip SRAM and flash memories. The 1 MB flash version features 160 KB of on-chip graphics SRAM to buffer cost effective color TFT displays driven via the on-chip Display Control Unit (DCU). See Table 1 for specific memory size and feature sets of the product family members.

The PXS30 family benefits from the extensive development infrastructure for Power Architecture devices, which is already well established. This includes full support from available software drivers, operating systems, and configuration code

to assist with users' implementations. See Section 3, Developer support, for more information.

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the PXS30 series of microcontroller units (MCUs). For functional characteristics, see the *PXS30 Microcontroller Reference Manual*.

1.2 Device comparison

Table 1. PXS30 Family Feature Set

Features		PXS3010	PXS3015	PXS3020
CPU	Type	2 × e200z7d (SoR[1]) in lock-step or decoupled operation		
	Architecture	Harvard		
	Execution speed	0–150 MHz (+2% FM)	0–180 MHz (+2% FM)	0–180 MHz (+2% FM)
	Nominal platform frequency (in 1:1, 1:2, and 1:3 modes)	0–75 MHz (+2% FM)	0–90 MHz (+2% FM)	0–90 MHz (+2% FM)
	MMU	64 entries (SoR)		
	Instruction set PPC	Yes		
	Instruction set VLE	Yes		
	Instruction cache	16 KB, 4-way with EDC (SoR)		
	Data cache	16 KB, 4-way with EDC (SoR)		
	MPU	Yes (SoR)		
Buses	Core bus	32-bit address, 64-bit data		
	Internal periphery bus	32-bit address, 32-bit data		
XBAR	Master × slave ports	Yes (SoR)		
Memory	Static RAM (SRAM)	256 KB (ECC)	384 KB (ECC)	512 KB (ECC)
	Code Flash memory	1 MB[2]	1.5 MB[2]	2 MB[2]
	Data Flash memory	64 KB[2]		

Table 1. PXS30 Family Feature Set (continued)

Features		PXS3010	PXS3015	PXS3020
Modules	Analog-to-Digital Converter (ADC)	257 pin pkg: 4 × 12 bit (22 external channels) 473 pin pkg: 4 × 12 bit (up to 34 external channels)		
	CRC unit	2 (3 contexts each)		
	Cross Triggering Unit (CTU)	2 modules		
	Serial Peripheral Interface (SPI)	2 modules (3 chip selects)	3 modules (3 chip selects)	
	Digital I/Os	≥ 16		
	DRAM Controller (DRAMC)	No	Yes[3]	
	Enhanced Direct Memory Access (eDMA)	2 modules, 32 channels each		
	eTimer	3 modules, 6 channels each		
	External Bus Interface (EBI)	1 module[3] 16-bit Data + Address or 32-bit Data with Address bus muxed[4]		
	Fast Ethernet Controller (FEC)	1 module		
	Fault Collection and Control Unit (FCCU)	1 module		
	CAN	4 modules (32 message buffers each)		
	PWM	3 modules (each 4 × 3 channels)		
	FlexRay	Optional		
	I^2C	2 modules	3 modules	
	Interrupt Controller (INTC)	Yes (SoR)		
	UART/LIN	3 modules	4 modules	
	Parallel Data Interface (PDI)	1 module[4]		
	Periodic Interrupt Timer (PIT)	1 module, 4 channels		
	Software Watchdog Timer (SWT)	Yes (SoR)		
	System Timer Module (STM)	Yes (SoR)		
	Temperature sensor	1 module		
	Wakeup Unit (WKPU)	Yes		
	Crossbar switch (XBAR)	3 modules, 2 are user-configurable		

Table 1. PXS30 Family Feature Set (continued)

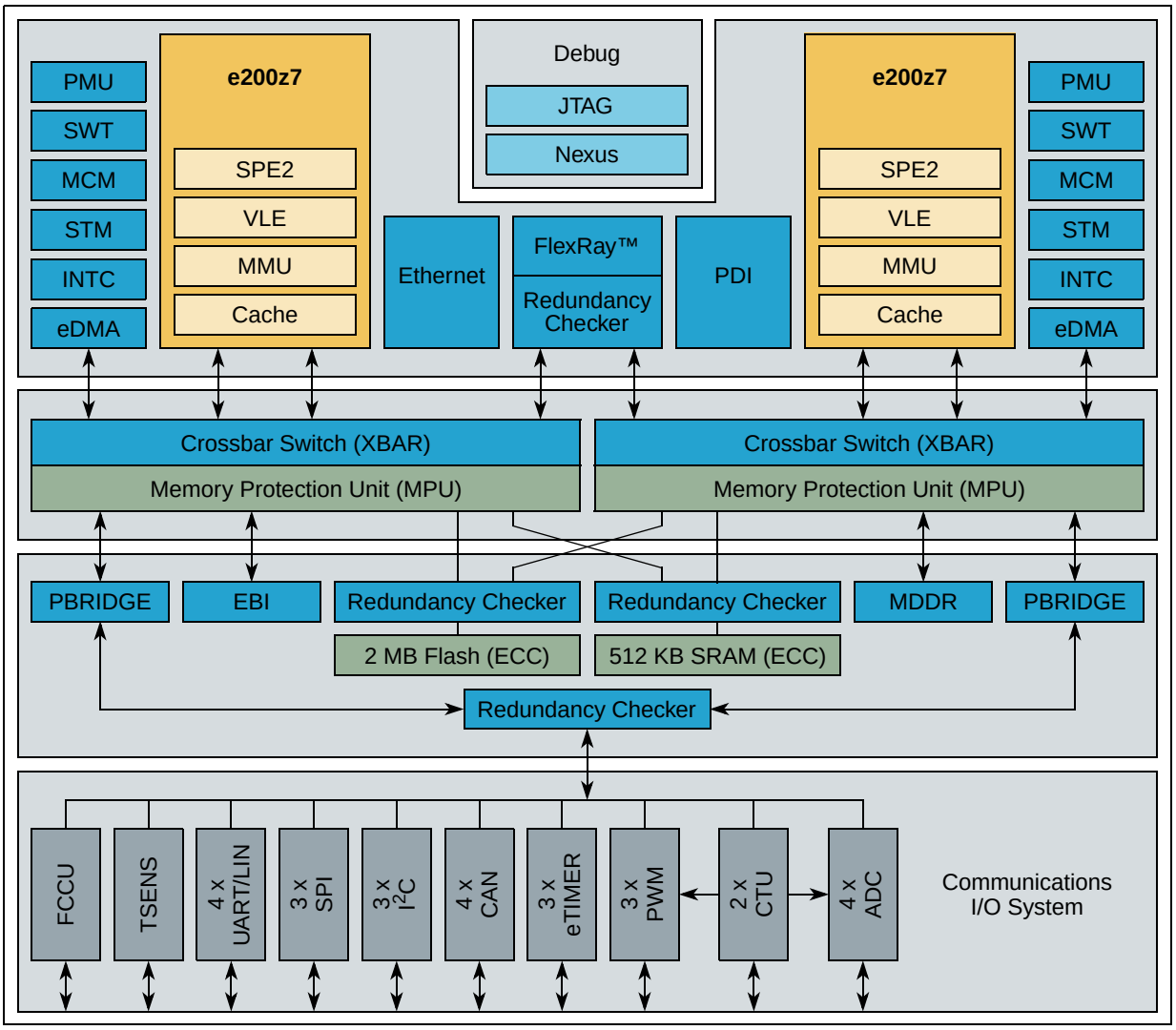
Features		PXS3010	PXS3015	PXS3020
Clocking	Clock monitor unit (CMU)	3 modules		
	Clock output	2 modules		
	Frequency-modulated phase-locked loop (FMPLL)	2 modules (system and auxiliary)		
	IRCOSC – 16 MHz	1		
	XOSC 4 MHz – 40 MHz	1		
Supply	Power management unit (PMU)	Yes		
	1.2 V low-voltage detector (LVD12)	1		
	1.2 V high-voltage detector (HVD12)	1		
	2.7 V low-voltage detector (LVD27)	4		
Debug	Nexus	Class 3+ (for cores and SRAM ports)		
Packages	MAPBGA	257 pins	473 pins	473 pins
Temperature	Ambient	See the T_A recommended operating condition in the device data sheet		

NOTES:
1 Sphere of Replication.
2 Does not include Test or Shadow Flash memory space.
3 Available only on 473-pin package.
4 DDR available only on 473 package. Other modules available as follows:
EBI or DDR on 473 package.
EBI + PDI on 473 package.
DDR + PDI on 473 package
PDI only on 257 package.

1.3 Block diagram

Figure 1 shows a top-level block diagram of the PXS30 device.

PXS30 Block Diagram



ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
CMU – Clock monitoring unit
CRC – Cyclic redundancy check unit
CTU – Cross triggering unit
EBI – External bus interface
ECC – Error correction code
ECSM – Error correction status module
eDMA – Enhanced direct memory access controller
FCCU – Fault collection and control unit
FEC – Fast Ethernet controller
FMPLL – Frequency-modulated phase-locked loop
I^2C – Inter-integrated circuit controller
IRCOSC – Internal RC oscillator
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
MC – Mode entry, clock, reset, & power modules
mDDR – Mobile double data rate dynamic RAM
PBRIDGE – Peripheral I/O bridge
PDI – Parallel data interface
PIT – Periodic interrupt timer
PMU – Power management unit
PWM – Pulse width modulator module
RC – Redundancy checker
RTC – Real time clock
SEMA4 – Semaphore unit
SIUL – System integration unit Lite
SPI – Serial peripheral interface controller
SSCM – System status and configuration module
STM – System timer module
SWT – Software watchdog timer
TSENS – Temperature sensor
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
XOSC – Crystal oscillator

Figure 1. PXS30 block diagram

1.4 Feature list

- High-performance e200z7d dual core
  - 32-bit Power Architecture® technology CPU
  - Up to 180 MHz core frequency
  - Dual-issue core
  - Variable length encoding (VLE)
  - Memory management unit (MMU) with 64 entries
  - 16 KB instruction cache and 16 KB data cache
- Memory available
  - Up to 2 MB Code flash memory with ECC
  - 64 KB Data flash memory with ECC
  - Up to 512 KB on-chip SRAM with ECC
- SIL3/ASILD innovative safety concept: LockStep mode and fail-safe protection
  - Sphere of replication (SoR) for key components
  - Redundancy checking units on outputs of the SoR connected to FCCU
  - Fault collection and control unit (FCCU)
  - Boot-time built-in self-test for memory (MBIST) and logic (LBIST) triggered by hardware
  - Boot-time built-in self-test for ADC and flash memory
  - Replicated safety-enhanced watchdog timer
  - Junction temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) units
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority interrupt controller
  - Replicated 32-channel eDMA controller
- GPIOs individually programmable as input, output, or special function
- 3 general-purpose eTimer units (6 channels each)
- 3 FlexPWM units with four 16-bit channels per module
- Communications interfaces
  - 4 LINFlex modules
  - 3 DSPI modules with automatic chip select generation
  - 4 FlexCAN interfaces (2.0B Active) with 32 message objects

  - FlexRay module (V2.1) with dual channel, up to 128 message objects and up to 10 Mbit/s
  - Fast Ethernet Controller (FEC)
  - 3 I^2C modules
- Four 12-bit analog-to-digital converters (ADCs)
  - 22 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADC conversion with timer and PWM
- External bus interface
- 16-bit external DDR memory controller
- Parallel digital interface (PDI)
- On-chip CAN/UART bootstrap loader
- Capable of operating on a single 3.3 V voltage supply
  - 3.3 V-only modules: I/O, oscillators, flash memory
  - 3.3 V or 5 V modules: ADCs, supply to internal VREG
  - 1.8–3.3 V supply range: DRAM/PDI
- Operating junction temperature range –40 to 150 °C

1.5 Feature details

1.5.1 High-performance e200z7d core processor

- Dual 32-bit Power Architecture® processor core
- Loose or tight core coupling
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 64-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 16 KB Instruction and 16 KB Data caches per core with line locking
  - Four way set associative
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data parity
- Vectored interrupt support
- Signal processing engine 2 (SPE2) auxiliary processing unit (APU) operating on 64-bit general purpose registers

- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single precision in hardware; double precision with software library
  - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions (except for guarded loads) do not increase interrupt latency in the PXS30
- To reduce latency, long cycle time instructions are aborted upon interrupt requests
- Extensive system development support through Nexus debug module

1.5.2 Crossbar switch (XBAR)

- 32-bit address bus, 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (DMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

1.5.4 Enhanced Direct Memory Access (eDMA) controller

- 32 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

1.5.5 Interrupt Controller (INTC)

- 208 peripheral interrupt requests
- 8 software settable sources
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

1.5.6 Frequency-Modulated Phase-Locked Loop (FMPLL)

Two FMPLLs are available on each device.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor and output clock divider ratio are software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 2 modes of operation
  - Normal PLL mode with crystal reference (default)
  - Normal PLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers as well as jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows running motor control periphery at different (precisely lower, equal, or higher ,as required) frequency than the system to ensure higher resolution

1.5.7 External Bus Interface (EBI)

- Available on 473-pin devices
- Data and address options:
  - 16-bit data and address (non-muxed)
  - 32-bit data and address (bus-muxed)
- MPC5561 324 BGA compatibility mode: 16-bit data bus, 24-bit address bus is default ADDR[8:31], but configurable to 26-bit address bus.
- Memory controller with support for various memory types
  - Non-burst and burst mode SDR flash and SRAM
  - Asynchronous/legacy flash and SRAM

- Configurable bus speed modes
- Support for 2 MB address space
- Chip select and write/byte enable options as presented in the pin-muxing table in Section 2, Package pinouts and signal descriptions
- Configurable wait states (via chip selects)
- Optional automatic CLKOUT gating to save power and reduce EMI

1.5.8 On-chip flash memory

- Up to 2 MB Code flash memory with ECC
- 64 KB Data flash memory with ECC
- Censorship protection scheme to prevent flash content visibility
- Multiple block sizes to support features such as boot block, operating system block, and EEPROM emulation
- Read-while-write with multiple partitions
- Parallel programming mode to support rapid end of line programming
- Hardware programming state machine

1.5.9 Cache memory

- Harvard architecture cache
- 16 KB instruction / 16 KB data
- Four-way set-associative Harvard (instruction and data) 256-bit long cache
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data parity

1.5.10 On-chip internal static RAM (SRAM)

- Up to 512 KB general-purpose SRAM
- ECC performs single-bit correction, double-bit error detection
  - Address included in ECC checkbase

1.5.11 DRAM controller

The DRAM controller (available only on 473-pin devices) is a multi-port controller that monitors incoming requests on the three AHB slave ports and decides (at each rising clock edge) what command needs to be sent to the external DRAM.

The DRAM controller on this device supports the following types of memories:

- Mobile DDR (mDDR)

- DDR 1
- DDR 2 (optional)
- SDR

The controller has the following features:

- Optimized timing for 32-byte bursts and single read accesses on the AHB interface
- Optimized timing for 8-byte and 16-byte bursts on the DRAMC interface
- Supports priority elevation on the slave ports for single accesses
- 16-bit wide DRAM interface
- One chip select (CS)
- mDDR memory controller
  - 16-bit external interface
  - Address range up to 8 MB

1.5.12 Boot Assist Module (BAM)

- Enables booting via serial mode (FlexCAN, LINFlex)
- Handles static mode in case of an erroneous boot procedure
- Implemented in 8 KB ROM
- Supports Lock Step Mode (LSM) and Decoupled Parallel Mode (DPM)

1.5.13 Parallel Data Interface (PDI)

- Support for external ADC and CMOS image sensors
- Parallel interface operation up to MCU system bus frequency
- Selectable data capture from rising or falling edge
- Receive FIFO with adjustable trigger thresholds
- Data width for 8, 10, 12, 14, and 16 bits
- Data Packing Unit to pack input data on 64-bit words — data packed on 8- or 16- bit boundary, depending on input data width
- Binary increasing channel select that allows as many as eight channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK

1.5.14 Deserial Serial Peripheral Interface (DSPI) modules

- Three Serial Peripheral Interfaces
  - Full duplex communication ports with interrupt and eDMA request support
  - Support for all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis

  - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Support for up to 60 Mbit/s in Slave Only Rx mode

1.5.15 Serial communication interface module (LINFlex)

The LINFlex on this device features the following:

- Supports LIN Master mode, LIN Slave mode, and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, or 16-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (parity, noise, and framing errors)
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- Support for DMA-enabled transfers

1.5.16 FlexCAN

- Thirty-two message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Programmable acceptance filters
- Individual Rx filtering per message buffer
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen-only mode capabilities
- Programmable clock source: system clock or oscillator clock
- Reception queue possible by setting more than one Rx message buffer with the same ID
- Backwards compatible with previous FlexCAN modules
- Safety CAN features on 1 CAN module as implemented on MPC5604P

1.5.17 Dual-channel FlexRay controller

- Full implementation of FlexRay Protocol Specification 2.1
- Sixty-four configurable message buffers can be handled
- Message buffers configurable as Tx, Rx, or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count, and message ID
- Programmable acceptance filters for RxFIFO message buffers
- Dual channel, each at up to 10 Mbit/s data rate

1.5.18 Periodic Interrupt Timer (PIT)

The PIT module implements the features below:

- Four general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for real time interrupt, clocked from main external oscillator
- Can be used for software tick or DMA trigger operation

1.5.19 System Timer Module (STM)

The STM implements the features below:

- Duplicated periphery to guarantee that safety targets (SIL3) are achieved
- Up-counter with four output compare registers
- OS task protection and hardware tick implementation as per current state-of-the-art AUTOSAR requirement

1.5.20 Motor control (MOTC) peripherals

The peripherals in this section can be used for general-purpose applications, but are specifically designed for motor control (MOTC) applications.

1.5.20.1 FlexPWM

The pulse width modulator module (FlexPWM) contains three PWM channels, each of which is configured to control a single half-bridge power stage. There may also be one or more fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), Permanent Magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency lower than or equal to platform frequency
- Clock source not modulated and independent from system clock (generated via auxiliary PLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM is supported
- Double-buffered PWM registers
  - — Integral reload rates from 1 to 16
  - — Half-cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - — External digital pin
  - — Internal timer channel

  - External ADC input, taking into account values set in ADC high and low limit registers
- DMA support

1.5.20.2 Cross Triggering Unit (CTU)

The CTU provides automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double-buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Maximum operating frequency lower than or equal to platform
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low-pass filter
- Double-buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double-buffered ADC command list pointers to minimize ADC-trigger unit update
- Double-buffered ADC conversion command list with as many as twenty-four ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows controlling ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.5.20.3 Analog-to-Digital Converter (ADC)

- Four independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V or 0–3.3 V
- Twenty-two single-ended input channels
- Supports eight FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal, or external triggers
- DMA and interrupt request support

1.5.20.4 eTimer module

Three 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Ability to operate up to platform frequency
- Individual channel capability
  - Input capture trigger
  - Output compare

  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

1.5.21 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Replicated IP to be used as checkers on the PBRIDGE output, flash controller output, SRAM Output, DMA Channel Mux inputs

1.5.22 Software Watchdog Timer (SWT)

This module implements the features below:

- Duplicated periphery to guarantee that safety targets (SIL3) are achieved
- Fault-tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows high level of safety (SIL3 monitor)

1.5.23 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device

- Collection of test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, NMI, reset, or safe mode)
  - External reaction (failure is reported to the outside world via configurable output pins)

1.5.24 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized pad control on per-pin basis
  - Pin function selection
  - Configurable weak pullup/pulldown
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.25 Cyclic Redundancy Checker (CRC) unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to an input register.

The CRC unit has the following features:

- Three sets of registers to allow three concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores the result in an internal register
- Implements the following standard CRC polynomials:
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads the core from cycle-consuming CRC and helps in checking the configuration signature for safe start-up or periodic procedures
- Connected as a peripheral on the internal peripheral bus
- Provides DMA support

1.5.26 Non-maskable interrupt (NMI)

The non-maskable interrupt with de-glitching filter is available to support high priority core exceptions.

1.5.27 System Status and Configuration Module (SSCM)

The SSCM on the PXS30 features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Classic PowerPC Book E code (default) or as Freescale VLE code out of flash
- Supports serial bootloading of either Classic PowerPC Book E code (default) or Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid

1.5.28 Nexus Development Interface (NDI)

- Per IEEE-ISTO 5001-2008
- Real-time development support for Power Architecture core through Nexus class 3 (some class 4 support)
- Nexus support to snoop system SRAM traffic
- Data trace of FlexRay accesses
- Read and write access
- Configured via the IEEE 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

1.5.29 IEEE 1149.1 JTAG controller (JTAGC)

- IEEE 1149.1-2001 Test Access Port (TAP) interface
- JCOMP input that provides the ability to share the TAP —selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
- 5-bit instruction register that supports additional public instructions
- Three test data registers:
  - — Bypass register
  - — Boundary scan register
  - — Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register, and associated circuitry

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the PXS30 in the 257 MAPBGA package. Figure 3 through Figure 6 show the PXS30 in the 473 MAPBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS_HV_IO	VSS_HV_IO	VDD_HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	VDD_HV_IO	fec RXD[2]	fec RX_CLK	fec RXD[0]	fec MDIO	fec TX_EN	fec TXD[3]	VSS_HV_IO	VSS_HV_IO	A
B	VSS_HV_IO	VSS_HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO [14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	VSS_HV_IO	fec RXD[3]	fec RX_ER	fec RXD[1]	fec TX_ER	fec TX_CLK	can0 TXD	VDD_HV_IO	VSS_HV_IO	B
C	VDD_HV_IO	nexus MDO [15]	VSS_HV_IO	FCCU_F[1]	flexray CB_RX	etimer0 ETC[0]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	JCOMP	fec CRS	fec TXD[0]	fec COL	can0 RXD	VSS_HV_PDI	pdi DATA [5]	pdi CLOCK	C
D	nexus MDO [2]	nexus MDO [3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[4]	VDD_HV_FLA	VSS_HV_FLA	fec TXD[2]	fec TXD[1]	fec RX_DV	fec MDC	VDD_HV_PDI	VSS_HV_IO	pdi DATA [0]	pdi DATA [1]	D
E	nexus MDO [0]	nexus MDO [1]	flexray CA_RX	NMI										pdi LINE_V	pdi DATA [2]	pdi DATA [3]	pdi DATA [4]	E
F	nexus MDO[6]	nexus MDO [11]	dspi1 SOUT	dspi1 SIN		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		mc_cgl clk_out	pdi DATA [6]	pdi DATA [7]	pdi DATA [8]	F
G	nexus MDO [4]	VDD_HV_IO	dspi0 SCK	dspi1 SCK		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [9]	pdi DATA [10]	pdi DATA [11]	pdi FRAME_V	G
H	nexus MDO [10]	VSS_HV_IO	dspi0 CS0	dspi1 CS0		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [12]	pdi DATA [13]	VDD_HV_PDI	flexpwm 0 X[0]	H
J	nexus MCKO	nexus MDO[8]	dspi2 CS0	dspi2 CS2		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [14]	pdi DATA [15]	VSS_HV_PDI	flexpwm 0 X[1]	J
K	nexus MSEO_B[0]	nexus MSEO_B[1]	nexus RDY_B	dspi0 SIN		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		flexpwm 0 X[2]	flexpwm 0 X[3]	flexpwm 0 A[1]	flexpwm 0 B[0]	K
L	nexus EVTO_B	nexus EVTI_B	dspi2 SCK	nexus MDO [13]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		VDD_HV_DRAM_VREF	TCK	flexpwm 0 B[1]	TDO	L
M	VDD_HV_OSC	VDD_HV_IO	dspi1 CS2	nexus MDO [12]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		flexpwm 0 B[2]	TDI	TMS	flexpwm 1 A[1]	M
N	XTALIN	VSS_HV_IO	dspi0 CS3	VSS_LV_PLL										flexpwm 0 B[3]	flexpwm 0 A[2]	flexpwm 1 A[0]	flexpwm 1 B[0]	N
P	VSS_HV_OSC	$\overline{\text{RESET}}$	dspi0 CS2	VDD_LV_PLL	etimer1 ETC[1]	etimer1 ETC[2]	adc0 AN[0]	etimer1 ETC[3]	VSS_HV_IO	VDD_HV_IO	adc0_adc1 AN[14]	etimer1 ETC[4]	etimer1 ETC[5]	VDD_HV_IO	flexpwm 0 A[3]	flexpwm 0 A[0]	flexpwm 1 B[1]	P
R	XTAL OUT	FCCU_F[0]	VSS_HV_IO	dspi1 CS3	adc2 AN[0]	adc2 AN[3]	VDD_HV_ADR_13	adc2_adc3 AN[14]	VDD_HV_ADR_02	adc0 AN[2]	adc0_adc1 AN[13]	adc1 AN[1]	VREG_CTRL	lin0 TXD	VSS_HV_IO	flexpwm 1 A[2]	flexpwm 1 B[2]	R
T	VSS_HV_IO	VDD_HV_IO	dspi2 SOUT	adc3 AN[0]	adc3 AN[3]	adc2 AN[2]	VSS_HV_ADR_13	adc2_adc3 AN[13]	VSS_HV_ADR_02	adc0 AN[1]	adc0_adc1 AN[12]	adc1 AN[0]	adc1 AN[2]	lin0 RXD	etimer1 ETC[0]	VDD_HV_IO	VSS_HV_IO	T
U	VSS_HV_IO	VSS_HV_IO	dspi2 SIN	adc3 AN[1]	adc3 AN[2]	adc2 AN[1]	adc2_adc3 AN[11]	adc2_adc3 AN[12]	VDD_HV_ADV	VSS_HV_ADV	adc0_adc1 AN[11]	VREG_INT_ENABLE	$\overline{\text{RESET}}$_SUP	VDD_HV_PMU	VSS_HV_PMU	VSS_HV_IO	VSS_HV_IO	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2. PXS30 257 MAPBGA pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_ HV_IO	VSS_ HV_IO	VDD_ HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	fec RX_DV	fec MDIO	fec TX_CLK	fec TX_EN
B	VSS_ HV_IO	VSS_ HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO[14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	fec RXD[3]	fec RX_ER	fec TXD[0]	fec RXD[0]
C	VDD_ HV_IO	nexus MDO[15]	VSS_ HV_IO	FCCU_ F[1]	flexray CB_RX	etimer0 ETC[4]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	fec TXD[2]	fec TXD[1]	fec CRS
D	nexus MDO[1]	nexus MDO[3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[0]	VDD_ HV_IO	VSS_ HV_IO	JCOMP	VSS_ HV_IO	VSS_ HV_FLA
E	nexus MDO[0]	nexus MDO[2]	flexray CA_RX	NMI								
F	nexus MDO[10]	nexus MDO[11]	nexus MDO[6]	nexus MDO[4]		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
G	nexus MCKO	VDD_ HV_IO	nexus MDO[8]	nexus MSEO_B[1]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
H	nexus EVTO_B	VSS_ HV_IO	nexus MSEO_B[0]	nexus EVTI_B		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
J	nexus RDY_B	nexus MDO[13]	nexus MDO[12]	dspi1 SIN		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
K	dspi0 SCK	dspi1 CS0	dspi1 SCK	dspi1 SOUT		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
L	dspi0 CS0	dspi2 CS2	dspi2 CS0	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
M	flexpwm0 X[0]	VDD_ HV_IO	dspi0 SIN	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR

Figure 3. PXS30 473 MAPBGA pinout (northwest, viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12
N	flexpwm0 A[0]	VSS_ HV_IO	flexpwm0 X[1]	flexpwm0 B[2]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
P	flexpwm0 B[0]	flexpwm0 B[1]	flexpwm0 A[2]	flexpwm0 A[3]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
R	flexpwm0 X[2]	flexpwm0 X[3]	flexpwm0 A[1]	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
T	flexpwm0 B[3]	flexpwm1 A[0]	flexpwm1 A[1]	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
U	flexpwm1 B[0]	flexpwm1 B[1]	flexpwm1 A[2]	dspi2 SCK		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
V	VDD_ HV_OSC	VDD_ HV_IO	flexpwm1 B[2]	dspi1 CS2		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
W	XTALIN	VSS_ HV_IO	dspi0 CS3	VSS_ LV_PLL								
Y	VSS_ HV_OSC	$\overline{\text{RESET}}$	dspi0 CS2	VDD_ LV_PLL	flexpwm1 X[0]	adc3 AN[0]	adc2_adc3 AN[11]	adc2_adc3 AN[14]	etimer1 ETC[1]	etimer1 ETC[2]	etimer1 ETC[3]	VSS_ HV_IO
AA	XTALOUT	FCCU_ F[0]	VSS_ HV_IO	dspi1 CS3	flexpwm1 X[1]	adc3 AN[1]	adc2_adc3 AN[12]	adc2 AN[0]	VDD_ HV_ADV	VSS_ HV_ADV	adc0 AN[2]	adc0 AN[5]
AB	VSS_ HV_IO	VDD_ HV_IO	dspi2 SOUT	flexpwm1 X[2]	flexpwm1 X[3]	adc3 AN[2]	adc2_adc3 AN[13]	adc2 AN[1]	adc2 AN[2]	adc0 AN[0]	adc0 AN[4]	adc0 AN[6]
AC	VSS_ HV_IO	VSS_ HV_IO	dspi2 SIN	flexpwm1 A[3]	flexpwm1 B[3]	adc3 AN[3]	VDD_HV_ ADR_23	VSS_HV_ ADR_23	adc2 AN[3]	adc0 AN[1]	adc0 AN[3]	VDD_ HV_ADR_0
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 4. PXS30 473 MAPBGA pinout (southwest, viewed from above)

13	14	15	16	17	18	19	20	21	22	23	
fec TXD[3]	VDD_ HV_IO	pdi DATA[3]	pdi DATA[1]	pdi CLOCK	pdi DATA[7]	pdi DATA[10]	pdi DATA[13]	pdi DATA[15]	VSS_ HV_IO	VSS_ HV_IO	A
fec TX_ER	VSS_ HV_IO	pdi DATA[6]	pdi DATA[4]	pdi DATA[0]	pdi LINE_V	pdi DATA[9]	pdi DATA[14]	can0 TXD	VDD_ HV_IO	VSS_ HV_IO	B
fec RX_CLK	fec RXD[1]	fec COL	pdi DATA[5]	pdi DATA[2]	pdi DATA[8]	pdi DATA[12]	can0 RXD	VSS_ HV_PDI	siul GPIO[197]	dramc CAS	C
VDD_ HV_FLA	fec RXD[2]	fec MDC	VDD_ HV_PDI	VSS_ HV_PDI	pdi DATA[11]	pdi FRAME_V	VDD_ HV_PDI	dramc BA[1]	siul GPIO[195]	dramc BA[0]	D
							mc_cgl clk_out	siul GPIO[149]	dramc CS0	dramc BA[2]	E
VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR		dramc RAS	siul GPIO[194]	siul GPIO[148]	dramc D[5]	F
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		siul GPIO[196]	dramc DQS[0]	dramc DM[0]	dramc D[7]	G
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[2]	VDD_HV_ DRAM_VTT	VDD_HV_ DRAM	VSS_HV_ DRAM	H
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[0]	dramc D[1]	dramc D[3]	dramc D[6]	J
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VSS_ HV_IO	dramc D[4]	dramc D[8]	dramc D[9]	K
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VDD_ HV_IO	VDD_HV_ DRAM_VTT	VSS_HV_ DRAM	VDD_HV_ DRAM	L
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ODT	dramc WEB	dramc D[11]	dramc D[10]	M

Figure 5. PXS30 473 MAPBGA pinout (northeast, viewed from above)

VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc DQS[1]	dramc DM[1]	dramc D[13]	dramc D[12]	N
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[14]	dramc D[15]	VSS_HV_ DRAM	VDD_HV_ DRAM	P
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VDD_HV_ DRAM_VREF	dramc ADD[3]	dramc CKE	dramc CLKB	R
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ADD[8]	dramc ADD[9]	dramc ADD[1]	dramc CLK	T
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ADD[6]	dramc ADD[12]	VDD_HV_ DRAM	dramc ADD[0]	U
VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR		lin0 TXD	dramc ADD[13]	VSS_HV_ DRAM	dramc ADD[2]	V
							lin0 RXD	dramc ADD[14]	dramc ADD[7]	dramc ADD[4]	W
VDD_ HV_IO	adc0_adc1 AN[11]	etimer1 ETC[5]	etimer1 ETC[4]	adc1 AN[8]	adc1 AN[6]	TCK	VDD_HV_IO	dramc ADD[15]	dramc ADD[11]	dramc ADD[5]	Y
adc0 AN[8]	adc0_adc1 AN[12]	adc1 AN[0]	adc1 AN[2]	adc1 AN[5]	adc1 AN[7]	TDI	etimer1 ETC[0]	VSS_HV_IO	lin1 TXD	dramc ADD[10]	AA
adc0 AN[7]	adc0_adc1 AN[13]	adc1 AN[1]	adc1 AN[3]	adc1 AN[4]	TDO	TMS	RESERVED	lin1 RXD	VDD_ HV_IO	VSS_ HV_IO	AB
VSS_ HV_ADR_0	adc0_adc1 AN[14]	VDD_ HV_ADR_1	VSS_ HV_ADR_1	VDD_ HV_PMU	VREG_CTRL	VSS_ HV_PMU	$\overline{\text{RESET}}$_ $\overline{\text{SUP}}$	VREG_INT_ ENABLE	VSS_ HV_IO	VSS_ HV_IO	AC
13	14	15	16	17	18	19	20	21	22	23	

Figure 6. PXS30 473 MAPBGA pinout (southeast, viewed from above)

2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration for this device.

2.2.1 Pad types

Table 2 lists the pad types used on the PXS30.

Table 2. Pad types

Pad Type	Description
GP Slow	Slow buffer with CMOS Schmitt trigger and pullup/pulldown.
GP Slow/Fast	Programmable slow/fast buffer with CMOS Schmitt trigger, pullup/pulldown.
GP Slow/Medium	Programmable slow/medium buffer with CMOS Schmitt trigger, pullup/pulldown. Programmable slow/medium buffer with CMOS Schmitt trigger, pullup/pulldown and Injection proof analog switch.
GP Slow/Symmetric	Programmable slow/symmetric buffer with CMOS Schmitt trigger, pullup/pulldown.
PDI Medium	Medium slew-rate output with four selectable slew rates. Contains an input buffer and weak pullup/pulldown.
PDI Fast	Fast slew-rate output with four selectable slew rates. Contains an input buffer and weak pullup/pulldown.
DRAM ACC	Bidirectional DDR pad. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM CLK	Differential clock driver
DRAM DQ	Bidirectional DDR pad with integrated ODT. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM ODT CTL	Enable On Die Termination control
Analog	CMOS Schmitt trigger cell with injection proof analog switch.
Analog Shared	CMOS Schmitt trigger cell with two injection-proof analog switches.

2.2.2 Power supply and reference voltage pins

Table 3 shows the supply pins for the PXS30 in the 257 MAPBGA package. Table 5 shows the supply pins for the PXS30 in the 473 MAPBGA package.

Table 4 and Table 6 show the pins not populated on the PXS30 257 MAPBGA and 473 MAPBGA packages, respectively.

Table 3. 257 MAPBGA supply pins

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F9	VDD_LV_COR	VDD_LV
A9	VDD_HV_IO	VDD_HV	F10	VDD_LV_COR	VDD_LV
B16	VDD_HV_IO	VDD_HV	F11	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F12	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	G12	VDD_LV_COR	VDD_LV
P10	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
P14	VDD_HV_IO	VDD_HV	H12	VDD_LV_COR	VDD_LV
T2	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T16	VDD_HV_IO	VDD_HV	J12	VDD_LV_COR	VDD_LV
L14	VDD_HV_DRAM_VREF	VDD_HV	K6	VDD_LV_COR	VDD_LV
D8	VDD_HV_FLA	VDD_HV	K12	VDD_LV_COR	VDD_LV
M1	VDD_HV_OSC	VDD_HV	L6	VDD_LV_COR	VDD_LV
D14	VDD_HV_PDI	VDD_HV	L12	VDD_LV_COR	VDD_LV
H16	VDD_HV_PDI	VDD_HV	M6	VDD_LV_COR	VDD_LV
U14	VDD_HV_PMU	VDD_HV	M7	VDD_LV_COR	VDD_LV
R7	VDD_HV_ADR_13	VDD_HV_A	M8	VDD_LV_COR	VDD_LV
R9	VDD_HV_ADR_02	VDD_HV_A	M9	VDD_LV_COR	VDD_LV
U9	VDD_HV_ADV	VDD_HV_A	M10	VDD_LV_COR	VDD_LV
F6	VDD_LV_COR	VDD_LV	M11	VDD_LV_COR	VDD_LV
F7	VDD_LV_COR	VDD_LV	M12	VDD_LV_COR	VDD_LV
F8	VDD_LV_COR	VDD_LV	P4	VDD_LV_PLL	VDD_LV
V_{SS}					
A1	VSS_HV_IO	VSS_HV	G7	VSS_LV_COR	VSS_LV
A2	VSS_HV_IO	VSS_HV	G8	VSS_LV_COR	VSS_LV
A16	VSS_HV_IO	VSS_HV	G9	VSS_LV_COR	VSS_LV
A17	VSS_HV_IO	VSS_HV	G10	VSS_LV_COR	VSS_LV
B1	VSS_HV_IO	VSS_HV	G11	VSS_LV_COR	VSS_LV
B2	VSS_HV_IO	VSS_HV	H7	VSS_LV_COR	VSS_LV
B9	VSS_HV_IO	VSS_HV	H8	VSS_LV_COR	VSS_LV
B17	VSS_HV_IO	VSS_HV	H9	VSS_LV_COR	VSS_LV
C3	VSS_HV_IO	VSS_HV	H10	VSS_LV_COR	VSS_LV

Table 3. 257 MAPBGA supply pins (continued)

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
D15	VSS_HV_IO	VSS_HV	H11	VSS_LV_COR	VSS_LV
H2	VSS_HV_IO	VSS_HV	J7	VSS_LV_COR	VSS_LV
N2	VSS_HV_IO	VSS_HV	J8	VSS_LV_COR	VSS_LV
P9	VSS_HV_IO	VSS_HV	J9	VSS_LV_COR	VSS_LV
R3	VSS_HV_IO	VSS_HV	J10	VSS_LV_COR	VSS_LV
R15	VSS_HV_IO	VSS_HV	J11	VSS_LV_COR	VSS_LV
T1	VSS_HV_IO	VSS_HV	K7	VSS_LV_COR	VSS_LV
T17	VSS_HV_IO	VSS_HV	K8	VSS_LV_COR	VSS_LV
U1	VSS_HV_IO	VSS_HV	K9	VSS_LV_COR	VSS_LV
U2	VSS_HV_IO	VSS_HV	K10	VSS_LV_COR	VSS_LV
U16	VSS_HV_IO	VSS_HV	K11	VSS_LV_COR	VSS_LV
U17	VSS_HV_IO	VSS_HV	L7	VSS_LV_COR	VSS_LV
D9	VSS_HV_FLA	VSS_HV	L8	VSS_LV_COR	VSS_LV
P1	VSS_HV_OSC	VSS_HV	L9	VSS_LV_COR	VSS_LV
C15	VSS_HV_PDI	VSS_HV	L10	VSS_LV_COR	VSS_LV
J16	VSS_HV_PDI	VSS_HV	L11	VSS_LV_COR	VSS_LV
T9	VSS_HV_ADR_02	VSS_HV_A	N4	VSS_LV_PLL	VSS_LV
T7	VSS_HV_ADR_13	VSS_HV_A	U15	VSS_HV_PMU	VSS_LV
U10	VSS_HV_ADV	VSS_HV_A			

Table 4. 257 MAPBGA Balls not populated on package

E5	E6	E7	E8	E9	E10	E11	E12
E13	F5	F13	G5	G13	H5	H13	J5
J13	K5	K13	L5	L13	M5	M13	N5
N6	N7	N8	N9	N10	N11	N12	N13

Table 5. 473 MAPBGA supply pins

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F15	VDD_LV_COR	VDD_LV
A14	VDD_HV_IO	VDD_HV	F16	VDD_LV_COR	VDD_LV
B22	VDD_HV_IO	VDD_HV	F17	VDD_LV_COR	VDD_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
C1	VDD_HV_IO	VDD_HV	F18	VDD_LV_COR	VDD_LV
D8	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G18	VDD_LV_COR	VDD_LV
L20	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	H18	VDD_LV_COR	VDD_LV
M4	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T4	VDD_HV_IO	VDD_HV	J18	VDD_LV_COR	VDD_LV
V2	VDD_HV_IO	VDD_HV	K6	VDD_LV_COR	VDD_LV
Y13	VDD_HV_IO	VDD_HV	K18	VDD_LV_COR	VDD_LV
Y20	VDD_HV_IO	VDD_HV	L6	VDD_LV_COR	VDD_LV
AB2	VDD_HV_IO	VDD_HV	L18	VDD_LV_COR	VDD_LV
AB22	VDD_HV_IO	VDD_HV	M6	VDD_LV_COR	VDD_LV
AC12	VDD_HV_ADR_0	VDD_HV_A	M18	VDD_LV_COR	VDD_LV
AC15	VDD_HV_ADR_1	VDD_HV_A	N6	VDD_LV_COR	VDD_LV
AC7	VDD_HV_ADR_23	VDD_HV_A	N18	VDD_LV_COR	VDD_LV
AA9	VDD_HV_ADV	VDD_HV_A	P6	VDD_LV_COR	VDD_LV
H22	VDD_HV_DRAM	VDD_HV	P18	VDD_LV_COR	VDD_LV
L23	VDD_HV_DRAM	VDD_HV	R6	VDD_LV_COR	VDD_LV
P23	VDD_HV_DRAM	VDD_HV	R18	VDD_LV_COR	VDD_LV
U22	VDD_HV_DRAM	VDD_HV	T6	VDD_LV_COR	VDD_LV
R20	VDD_HV_DRAM_VREF	VDD_HV	T18	VDD_LV_COR	VDD_LV
H21	VDD_HV_DRAM_VTT	VDD_HV	U6	VDD_LV_COR	VDD_LV
L21	VDD_HV_DRAM_VTT	VDD_HV	U18	VDD_LV_COR	VDD_LV
D13	VDD_HV_FLA	VDD_HV	V6	VDD_LV_COR	VDD_LV
V1	VDD_HV_OSC	VDD_HV	V7	VDD_LV_COR	VDD_LV
D16	VDD_HV_PDI	VDD_HV	V8	VDD_LV_COR	VDD_LV
D20	VDD_HV_PDI	VDD_HV	V9	VDD_LV_COR	VDD_LV
AC17	VDD_HV_PMU	VDD_HV	V10	VDD_LV_COR	VDD_LV
F6	VDD_LV_COR	VDD_LV	V11	VDD_LV_COR	VDD_LV
F7	VDD_LV_COR	VDD_LV	V12	VDD_LV_COR	VDD_LV
F8	VDD_LV_COR	VDD_LV	V13	VDD_LV_COR	VDD_LV
F9	VDD_LV_COR	VDD_LV	V14	VDD_LV_COR	VDD_LV
F10	VDD_LV_COR	VDD_LV	V15	VDD_LV_COR	VDD_LV
F11	VDD_LV_COR	VDD_LV	V16	VDD_LV_COR	VDD_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
F12	VDD_LV_COR	VDD_LV	V17	VDD_LV_COR	VDD_LV
F13	VDD_LV_COR	VDD_LV	V18	VDD_LV_COR	VDD_LV
F14	VDD_LV_COR	VDD_LV	Y4	VDD_LV_PLL	VDD_LV
V_{SS}					
A2	VSS_HV_IO	VSS_HV	L7	VSS_LV_COR	VSS_LV
A22	VSS_HV_IO	VSS_HV	L8	VSS_LV_COR	VSS_LV
A23	VSS_HV_IO	VSS_HV	L9	VSS_LV_COR	VSS_LV
B1	VSS_HV_IO	VSS_HV	L10	VSS_LV_COR	VSS_LV
B2	VSS_HV_IO	VSS_HV	L11	VSS_LV_COR	VSS_LV
B14	VSS_HV_IO	VSS_HV	L12	VSS_LV_COR	VSS_LV
B23	VSS_HV_IO	VSS_HV	L13	VSS_LV_COR	VSS_LV
C3	VSS_HV_IO	VSS_HV	L14	VSS_LV_COR	VSS_LV
D9	VSS_HV_IO	VSS_HV	L15	VSS_LV_COR	VSS_LV
D11	VSS_HV_IO	VSS_HV	L16	VSS_LV_COR	VSS_LV
H2	VSS_HV_IO	VSS_HV	L17	VSS_LV_COR	VSS_LV
K20	VSS_HV_IO	VSS_HV	M7	VSS_LV_COR	VSS_LV
L4	VSS_HV_IO	VSS_HV	M8	VSS_LV_COR	VSS_LV
N2	VSS_HV_IO	VSS_HV	M9	VSS_LV_COR	VSS_LV
A1	VSS_HV_IO	VSS_HV	M10	VSS_LV_COR	VSS_LV
R4	VSS_HV_IO	VSS_HV	M11	VSS_LV_COR	VSS_LV
W2	VSS_HV_IO	VSS_HV	M12	VSS_LV_COR	VSS_LV
Y12	VSS_HV_IO	VSS_HV	M13	VSS_LV_COR	VSS_LV
AA3	VSS_HV_IO	VSS_HV	M14	VSS_LV_COR	VSS_LV
AA21	VSS_HV_IO	VSS_HV	M15	VSS_LV_COR	VSS_LV
AB1	VSS_HV_IO	VSS_HV	M16	VSS_LV_COR	VSS_LV
AB23	VSS_HV_IO	VSS_HV	M17	VSS_LV_COR	VSS_LV
AC1	VSS_HV_IO	VSS_HV	N7	VSS_LV_COR	VSS_LV
AC2	VSS_HV_IO	VSS_HV	N8	VSS_LV_COR	VSS_LV
AC22	VSS_HV_IO	VSS_HV	N9	VSS_LV_COR	VSS_LV
AC23	VSS_HV_IO	VSS_HV	N10	VSS_LV_COR	VSS_LV
AC13	VSS_HV_ADR_0	VSS_HV_A	N11	VSS_LV_COR	VSS_LV
AC16	VSS_HV_ADR_1	VSS_HV_A	N12	VSS_LV_COR	VSS_LV
AC8	VSS_HV_ADR_23	VSS_HV_A	N13	VSS_LV_COR	VSS_LV
AA10	VSS_HV_ADV	VSS_HV_A	N14	VSS_LV_COR	VSS_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
H23	VSS_HV_DRAM	VSS_HV	N15	VSS_LV_COR	VSS_LV
L22	VSS_HV_DRAM	VSS_HV	N16	VSS_LV_COR	VSS_LV
P22	VSS_HV_DRAM	VSS_HV	N17	VSS_LV_COR	VSS_LV
V22	VSS_HV_DRAM	VSS_HV	P7	VSS_LV_COR	VSS_LV
D12	VSS_HV_FLA	VSS_HV	P8	VSS_LV_COR	VSS_LV
Y1	VSS_HV_OSC	VSS_HV	P9	VSS_LV_COR	VSS_LV
C21	VSS_HV_PDI	VSS_HV	P10	VSS_LV_COR	VSS_LV
D17	VSS_HV_PDI	VSS_HV	P11	VSS_LV_COR	VSS_LV
G7	VSS_LV_COR	VSS_LV	P12	VSS_LV_COR	VSS_LV
G8	VSS_LV_COR	VSS_LV	P13	VSS_LV_COR	VSS_LV
G9	VSS_LV_COR	VSS_LV	P14	VSS_LV_COR	VSS_LV
G10	VSS_LV_COR	VSS_LV	P15	VSS_LV_COR	VSS_LV
G11	VSS_LV_COR	VSS_LV	P16	VSS_LV_COR	VSS_LV
G12	VSS_LV_COR	VSS_LV	P17	VSS_LV_COR	VSS_LV
G13	VSS_LV_COR	VSS_LV	R7	VSS_LV_COR	VSS_LV
G14	VSS_LV_COR	VSS_LV	R8	VSS_LV_COR	VSS_LV
G15	VSS_LV_COR	VSS_LV	R9	VSS_LV_COR	VSS_LV
G16	VSS_LV_COR	VSS_LV	R10	VSS_LV_COR	VSS_LV
G17	VSS_LV_COR	VSS_LV	R11	VSS_LV_COR	VSS_LV
H7	VSS_LV_COR	VSS_LV	R12	VSS_LV_COR	VSS_LV
H8	VSS_LV_COR	VSS_LV	R13	VSS_LV_COR	VSS_LV
H9	VSS_LV_COR	VSS_LV	R14	VSS_LV_COR	VSS_LV
H10	VSS_LV_COR	VSS_LV	R15	VSS_LV_COR	VSS_LV
H11	VSS_LV_COR	VSS_LV	R16	VSS_LV_COR	VSS_LV
H12	VSS_LV_COR	VSS_LV	R17	VSS_LV_COR	VSS_LV
H13	VSS_LV_COR	VSS_LV	T7	VSS_LV_COR	VSS_LV
H14	VSS_LV_COR	VSS_LV	T8	VSS_LV_COR	VSS_LV
H15	VSS_LV_COR	VSS_LV	T9	VSS_LV_COR	VSS_LV
H16	VSS_LV_COR	VSS_LV	T10	VSS_LV_COR	VSS_LV
H17	VSS_LV_COR	VSS_LV	T11	VSS_LV_COR	VSS_LV
J7	VSS_LV_COR	VSS_LV	T12	VSS_LV_COR	VSS_LV
J8	VSS_LV_COR	VSS_LV	T13	VSS_LV_COR	VSS_LV
J9	VSS_LV_COR	VSS_LV	T14	VSS_LV_COR	VSS_LV
J10	VSS_LV_COR	VSS_LV	T15	VSS_LV_COR	VSS_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball Number	Ball Name	Pad Type	Ball Number	Ball Name	Pad Type
J11	VSS_LV_COR	VSS_LV	T16	VSS_LV_COR	VSS_LV
J12	VSS_LV_COR	VSS_LV	T17	VSS_LV_COR	VSS_LV
J13	VSS_LV_COR	VSS_LV	U7	VSS_LV_COR	VSS_LV
J14	VSS_LV_COR	VSS_LV	U8	VSS_LV_COR	VSS_LV
J15	VSS_LV_COR	VSS_LV	U9	VSS_LV_COR	VSS_LV
J16	VSS_LV_COR	VSS_LV	U10	VSS_LV_COR	VSS_LV
J17	VSS_LV_COR	VSS_LV	U11	VSS_LV_COR	VSS_LV
K7	VSS_LV_COR	VSS_LV	U12	VSS_LV_COR	VSS_LV
K8	VSS_LV_COR	VSS_LV	U13	VSS_LV_COR	VSS_LV
K9	VSS_LV_COR	VSS_LV	U14	VSS_LV_COR	VSS_LV
K10	VSS_LV_COR	VSS_LV	U15	VSS_LV_COR	VSS_LV
K11	VSS_LV_COR	VSS_LV	U16	VSS_LV_COR	VSS_LV
K12	VSS_LV_COR	VSS_LV	U17	VSS_LV_COR	VSS_LV
K13	VSS_LV_COR	VSS_LV	W4	VSS_LV_PLL	VSS_LV
K14	VSS_LV_COR	VSS_LV	AC19	VSS_HV_PMU	VSS_LV
K15	VSS_LV_COR	VSS_LV	D5	RESERVED	VSS_HV
K16	VSS_LV_COR	VSS_LV	AB20	RESERVED	VSS_HV
K17	VSS_LV_COR	VSS_LV			

Table 6. 473 MAPBGA Balls not populated on package

E5	E6	E7	E8	E9	E10	E11	E12
E13	E14	E15	E16	E17	E18	E19	F5
F19	G5	G19	H5	H19	J5	J19	K5
K19	L5	L19	M5	M19	N5	N19	P5
P19	R5	R19	T5	T19	U5	U19	V5
V19	W5	W6	W7	W8	W9	W10	W11
W12	W13	W14	W15	W16	W17	W18	W19

2.2.3 System pins

Table 7 shows the system pins for the PXS30 in the 257 MAPBGA package. Table 8 shows the system pins for the PXS30 in the 473 MAPBGA package.

Table 7. 257 MAPBGA system pins

Ball Number	Ball Name	Weak pull during reset	Safe Mode default condition	Pad Type	Power Domain
C4	FCCU_F[1]	disabled	not available	GP Slow/Medium	VDD_HV_IO
C10	JCOMP	pull down	not available	GP Slow	VDD_HV_IO
E1	Nexus MDO[0][1]	—	not available	GP Slow/Fast	VDD_HV_IO
E4	NMI	pull up	not available	GP Slow	VDD_HV_IO
L15	TCK	pull up	not available	GP Slow	VDD_HV_IO
M16	TMS	pull up	not available	GP Slow	VDD_HV_IO
N1	XTALIN	—	not available	Analog Feedthrough	VDD_HV_IO
P2	$\overline{\text{RESET}}$	pull down	not available	Reset	VDD_HV_IO
R1	XTALOUT	—	not available	Analog Feedthrough	VDD_HV_IO
R2	FCCU_F[0]	disabled	not available	GP Slow/Medium	VDD_HV_IO
R13	VREG_CTRL	—	—	Analog Feedthrough	VDD_REG
U12	VREG_INT_ENABLE	—	—	Analog Feedthrough	VDD_HV_IO
U13	$\overline{\text{RESET\_SUP}}$	pull down	—	Analog Feedthrough	VDD_HV_IO

NOTES:
1 Do not connect pin directly to a power supply or ground.

Table 8. 473 MAPBGA system pins

Ball Number	Ball Name	Weak pull during reset	Safe Mode default condition	Pad Type	Power Domain
C4	FCCU_F[1]	disabled	not available	GP Slow/Medium	VDD_HV_IO
D10	JCOMP	pull down	not available	GP Slow	VDD_HV_IO
E1	Nexus MDO[0][1]	—	not available	GP Slow/Fast	VDD_HV_IO
E4	NMI	pull up	not available	GP Slow	VDD_HV_IO
R23	dramc CLKB	—	—	DRAM CLK	VDD_HV_DRAM
T23	dramc CLK	disabled	—	DRAM CLK	VDD_HV_DRAM
W1	XTALIN	—	not available	Analog Feedthrough	VDD_HV_IO
Y2	$\overline{\text{RESET}}$	pull down	not available	Reset	VDD_HV_IO
Y19	TCK	pull up	not available	GP Slow	VDD_HV_IO
AA1	XTALOUT	—	not available	Analog Feedthrough	VDD_HV_IO
AA2	FCCU_F[0]	disabled	not available	GP Slow/Medium	VDD_HV_IO
AB19	TMS	pull up	not available	GP Slow	VDD_HV_IO
AC18	VREG_CTRL	—	—	Analog Feedthrough	VDD_REG
AC20	$\overline{\text{RESET\_SUP}}$	pull down	—	Analog Feedthrough	VDD_HV_IO
AC21	VREG_INT_ENABLE	—	—	Analog Feedthrough	VDD_HV_IO

NOTES:
1 Do not connect pin directly to a power supply or ground.

2.2.4 Multiplexed pins

Table 9 shows the pin multiplexing for the PXS30 in the 257 MAPBGA package. Table 10 shows the pin multiplexing for the PXS30 in the 473 MAPBGA package.

Table 9. 257 MAPBGA pin multiplexing

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
A4	GPIO	nexus MDO[5][1]	A0: siul_GPIO[114] A1: _ A2: npc_wrapper_MDO[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A5	GPIO	nexus MDO[7][1]	A0: siul_GPIO[112] A1: _ A2: npc_wrapper_MDO[7] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A6	GPIO	nexus MDO[9][1]	A0: siul_GPIO[110] A1: _ A2: npc_wrapper_MDO[9] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A7	GPIO	flexray CB_TX	A0: siul_GPIO[51] A1: flexray_CB_TX A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A8	GPIO	flexray CA_TR_EN	A0: siul_GPIO[47] A1: flexray_CA_TR_EN A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A10	GPIO	fec RXD[2]	A0: siul_GPIO[213] A1: _ A2: _ A3: dspi2_SOUT	I: fec_RXD[2] I: _ I: siul_EIRQ[21]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A11	GPIO	fec RX_CLK	A0: siul_GPIO[209] A1: flexray_DBG2 A2: etimer2_ETC[2] A3: dspi0_CS6	I: fec_RX_CLK I: _ I: siul_EIRQ[25]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
A12	GPIO	fec RXD[0]	A0: siul_GPIO[211] A1: i2c1_clock A2: _ A3: _	I: fec_RXD[0] I: _ I: siul_EIRQ[27]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A13	GPIO	fec MDIO	A0: siul_GPIO[198] A1: fec_MDIO A2: _ A3: dspi2_CS0	I: _ I: _ I: siul_EIRQ[28]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A14	GPIO	fec TX_EN	A0: siul_GPIO[200] A1: fec_TX_EN A2: _ A3: lin0_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO
B4	GPIO	can1 TXD	A0: siul_GPIO[14] A1: can1_TXD A2: _ A3: _	I: _ I: _ I: siul_EIRQ[13]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B5	GPIO	nexus MDO[14][1]	A0: siul_GPIO[219] A1: _ A2: npc_wrapper_MDO[14] A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
B6	GPIO	dspi2 CS1	A0: siul_GPIO[9] A1: dspi2_CS1 A2: _ A3: _	I: flexpwm0_FAULT[0] I: lin3_RXD I: can2_RXD	—	disabled	GP Slow/ Medium	VDD_HV_IO
B7	GPIO	flexray CB_TR_EN	A0: siul_GPIO[52] A1: flexray_CB_TR_EN A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
B8	GPIO	flexray CA_TX	A0: siul_GPIO[48] A1: flexray_CA_TX A2: _ A3: _	I: ctu1_EXT_IN I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B10	GPIO	fec RXD[3]	A0: siul_GPIO[214] A1: i2c1_data A2: _ A3: _	I: fec_RXD[3] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B11	GPIO	fec RX_ER	A0: siul_GPIO[215] A1: _ A2: _ A3: dspi0_CS1	I: fec_RX_ER I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B12	GPIO	fec RXD[1]	A0: siul_GPIO[212] A1: dspi1_CS1 A2: etimer2_ETC[5] A3: _	I: fec_RXD[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B13	GPIO	fec TX_ER	A0: siul_GPIO[205] A1: fec_TX_ER A2: dspi2_CS3 A3: _	I: flexpwm1_FAULT[3] I: lin0_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B14	GPIO	fec TX_CLK	A0: siul_GPIO[207] A1: flexray_DBG0 A2: etimer2_ETC[4] A3: dspi0_CS4	I: fec_TX_CLK I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B15	GPIO	can0 TXD	A0: siul_GPIO[16] A1: can0_TXD A2: _ A3: sscm_DEBUG[0]	I: _ I: _ I: siul_EIRQ[15]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C2	GPIO	nexus MDO[15][1]	A0: siul_GPIO[220] A1: _ A2: npc_wrapper_MDO[15] A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
C5	GPIO	flexray CB_RX	A0: siul_GPIO[50] A1: _ A2: ctu1_EXT_TGR A3: _	I: flexray_CB_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
C6	GPIO	etimer0 ETC[0]	A0: siul_GPIO[0] A1: etimer0_ETC[0] A2: _ A3: _	I: dspi2_SIN I: _ I: siul_EIRQ[0]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C7	GPIO	etimer0 ETC[1]	A0: siul_GPIO[1] A1: etimer0_ETC[1] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[1]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C8	GPIO	etimer0 ETC[2]	A0: siul_GPIO[2] A1: etimer0_ETC[2] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[2]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C9	GPIO	etimer0 ETC[3]	A0: siul_GPIO[3] A1: etimer0_ETC[3] A2: _ A3: _	I: _ I: mc_rgm_ABS[2] I: siul_EIRQ[3]	—	pull down	GP Slow/ Medium	VDD_HV_IO
C11	GPIO	fec CRS	A0: siul_GPIO[208] A1: flexray_DBG1 A2: etimer2_ETC[3] A3: dspi0_CS5	I: fec_CRS I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C12	GPIO	fec TXD[0]	A0: siul_GPIO[201] A1: fec_TXD[0] A2: etimer2_ETC[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C13	GPIO	fec COL	A0: siul_GPIO[206] A1: fec_COL A2: _ A3: lin1_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C14	GPIO	can0 RXD	A0: siul_GPIO[17] A1: _ A2: _ A3: sscm_DEBUG[1]	I: can0_RXD I: can1_RXD I: siul_EIRQ[16]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C16	GPIO	pdi DATA[5]	A0: siul_GPIO[136] A1: flexpwm2_A[0] A2: _ A3: etimer1_ETC[0]	I: pdi_DATA[5] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
C17	GPIO	pdi CLOCK	A0: siul_GPIO[128] A1: flexpwm2_B[1] A2: _ A3: etimer1_ETC[3]	I: pdi_CLOCK I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
D1	GPIO	nexus MDO[2][1]	A0: siul_GPIO[85] A1: _ A2: npc_wrapper_MDO[2] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D2	GPIO	nexus MDO[3][1]	A0: siul_GPIO[84] A1: _ A2: npc_wrapper_MDO[3] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D3	GPIO	can1 RXD	A0: siul_GPIO[15] A1: _ A2: _ A3: _	I: can1_RXD I: can0_RXD I: siul_EIRQ[14]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D4	GPIO	dspi0 SOUT	A0: siul_GPIO[38] A1: dspi0_SOUT A2: _ A3: sscm_DEBUG[6]	I: _ I: _ I: siul_EIRQ[24]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D6	GPIO	etimer0 ETC[5]	A0: siul_GPIO[44] A1: etimer0_ETC[5] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D7	GPIO	etimer0 ETC[4]	A0: siul_GPIO[43] A1: etimer0_ETC[4] A2: _ A3: _	I: _ I: mc_rgm_ABS[0] I: _	—	pull down	GP Slow/ Medium	VDD_HV_IO
D10	GPIO	fec TXD[2]	A0: siul_GPIO[203] A1: fec_TXD[2] A2: _ A3: _	I: flexpwm1_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D11	GPIO	fec TXD[1]	A0: siul_GPIO[202] A1: fec_TXD[1] A2: _ A3: dspi2_SCK	I: flexpwm1_FAULT[0] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
D12	GPIO	fec RX_DV	A0: siul_GPIO[210] A1: flexray_DBG3 A2: etimer2_ETC[0] A3: dspi0_CS7	I: fec_RX_DV I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D13	GPIO	fec MDC	A0: siul_GPIO[199] A1: fec_MDC A2: _ A3: _	I: _ I: lin1_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D16	GPIO	pdi DATA[0]	A0: siul_GPIO[131] A1: _ A2: lin3_TXD A3: _	I: pdi_DATA[0] I: _ I: flexpwm2_FAULT[2]	—	disabled	PDI Medium	VDD_HV_PDI
D17	GPIO	pdi DATA[1]	A0: siul_GPIO[132] A1: flexpwm2_B[3] A2: _ A3: _	I: pdi_DATA[1] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
E2	GPIO	nexus MDO[1][1]	A0: siul_GPIO[86] A1: _ A2: npc_wrapper_MDO[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
E3	GPIO	flexray CA_RX	A0: siul_GPIO[49] A1: _ A2: ctu0_EXT_TGR A3: _	I: flexray_CA_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
E14	GPIO	pdi LINE_V	A0: siul_GPIO[129] A1: _ A2: lin2_TXD A3: _	I: pdi_LINE_V I: _ I: flexpwm2_FAULT[0]	—	disabled	PDI Medium	VDD_HV_PDI
E15	GPIO	pdi DATA[2]	A0: siul_GPIO[133] A1: flexpwm2_A[1] A2: _ A3: etimer1_ETC[2]	I: pdi_DATA[2] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
E16	GPIO	pdi DATA[3]	A0: siul_GPIO[134] A1: flexpwm2_X[1] A2: _ A3: _	I: pdi_DATA[3] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
E17	GPIO	pdi DATA[4]	A0: siul_GPIO[135] A1: flexpwm2_A[2] A2: _ A3: etimer1_ETC[4]	I: pdi_DATA[4] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G3	GPIO	dspi0 SCK	A0: siul_GPIO[37] A1: dspi0_SCK A2: _ A3: sscm_DEBUG[5]	I: flexpwm0_FAULT[3] I: _ I: siul_EIRQ[23]	—	disabled	GP Slow/ Medium	VDD_HV_IO
G4	GPIO	dspi1 SCK	A0: siul_GPIO[6] A1: dspi1_SCK A2: _ A3: _	I: _ I: _ I: siul_EIRQ[6]	—	disabled	GP Slow/ Medium	VDD_HV_IO
G14	GPIO	pdi DATA[9]	A0: siul_GPIO[140] A1: flexpwm2_X[2] A2: _ A3: _	I: pdi_DATA[9] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G15	GPIO	pdi DATA[10]	A0: siul_GPIO[141] A1: flexpwm2_X[3] A2: _ A3: _	I: pdi_DATA[10] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G16	GPIO	pdi DATA[11]	A0: siul_GPIO[142] A1: flexpwm2_X[0] A2: _ A3: _	I: pdi_DATA[11] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G17	GPIO	pdi FRAME_V	A0: siul_GPIO[130] A1: _ A2: _ A3: _	I: pdi_FRAME_V I: lin2_RXD I: flexpwm2_FAULT[1]	—	disabled	PDI Medium	VDD_HV_PDI
H1	GPIO	nexus MDO[10][1]	A0: siul_GPIO[109] A1: _ A2: npc_wrapper_MDO[10] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
H3	GPIO	dspi0 CS0	A0: siul_GPIO[36] A1: dspi0_CS0 A2: _ A3: sscm_DEBUG[4]	I: _ I: _ I: siul_EIRQ[22]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
H4	GPIO	dspi1 CS0	A0: siul_GPIO[5] A1: dspi1_CS0 A2: _ A3: dspi0_CS7	I: _ I: _ I: siul_EIRQ[5]	—	disabled	GP Slow/ Medium	VDD_HV_IO
H14	GPIO	pdi DATA[12]	A0: siul_GPIO[143] A1: _ A2: _ A3: _	I: pdi_DATA[12] I: lin3_RXD I: flexpwm2_FAULT[3]	—	disabled	PDI Medium	VDD_HV_PDI
H15	GPIO	pdi DATA[13]	A0: siul_GPIO[144] A1: pdi_SENS_SEL[2] A2: ctu1_EXT_TGR A3: _	I: pdi_DATA[13] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
H17	GPIO	flexpwm0 X[0]	A0: siul_GPIO[194] A1: flexpwm0_X[0] A2: ebi_D28 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
J1	GPIO	nexus MCKO	A0: siul_GPIO[87] A1: _ A2: npc_wrapper_MCKO A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J2	GPIO	nexus MDO[8][1]	A0: siul_GPIO[111] A1: _ A2: npc_wrapper_MDO[8] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J3	GPIO	dspi2 CS0	A0: siul_GPIO[10] A1: dspi2_CS0 A2: _ A3: can3_TXD	I: _ I: _ I: siul_EIRQ[9]	—	disabled	GP Slow/ Medium	VDD_HV_IO
J4	GPIO	dspi2 CS2	A0: siul_GPIO[42] A1: dspi2_CS2 A2: lin3_TXD A3: can2_TXD	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
J14	GPIO	pdi DATA[14]	A0: siul_GPIO[145] A1: pdi_SENS_SEL[1] A2: i2c2_clock A3: _	I: pdi_DATA[14] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
J15	GPIO	pdi DATA[15]	A0: siul_GPIO[146] A1: pdi_SENS_SEL[0] A2: i2c2_data A3: _	I: pdi_DATA[15] I: ctu1_EXT_IN I: _	—	disabled	PDI Medium	VDD_HV_PDI
J17	GPIO	flexpwm0 X[1]	A0: siul_GPIO[195] A1: flexpwm0_X[1] A2: ebi_D29 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K1	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K2	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K3	GPIO	nexus RDY_B	A0: siul_GPIO[216] A1: _ A2: nexus_RDY_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K4	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
K14	GPIO	flexpwm0 X[2]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_D30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K15	GPIO	flexpwm0 X[3]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_D31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K16	GPIO	flexpwm0 A[1]	A0: siul_GPIO[149] A1: _ A2: ebi_RD_WR A3: flexpwm0_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
K17	GPIO	flexpwm0 B[0]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
L1	GPIO	nexus EVTO_B	A0: siul_GPIO[90] A1: _ A2: npc_wrapper_EVTO_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
L2	GPIO	nexus EVTI_B	A0: siul_GPIO[91] A1: _ A2: leo_sor_proxy_EVTI_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
L3	GPIO	dspi2 SCK	A0: siul_GPIO[11] A1: dspi2_SCK A2: _ A3: _	I: can3_RXD I: _ I: siul_EIRQ[10]	—	disabled	GP Slow/ Medium	VDD_HV_IO
L4	GPIO	nexus MDO[13][1]	A0: siul_GPIO[218] A1: _ A2: npc_wrapper_MDO[13] A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
L16	GPIO	flexpwm0 B[1]	A0: siul_GPIO[150] A1: dramc_CS0 A2: ebi_TS A3: flexpwm0_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
L17	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
M3	GPIO	dspi1 CS2	A0: siul_GPIO[56] A1: dspi1_CS2 A2: _ A3: dspi0_CS5	I: flexpwm0_FAULT[3] I: lin2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M4	GPIO	nexus MDO[12][1]	A0: siul_GPIO[217] A1: _ A2: npc_wrapper_MDO[12] A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
M14	GPIO	flexpwm0 B[2]	A0: siul_GPIO[152] A1: dramc_CAS A2: ebi_WE_BE_1 A3: flexpwm0_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
M15	GPIO	TDI	A0: siul_GPIO[21] A1: _ A2: _ A3: _	I: jtagc_TDI I: _ I: _	—	pull up	GP Slow/ Medium	VDD_HV_IO
M17	GPIO	flexpwm1 A[1]	A0: siul_GPIO[157] A1: dramc_ODT A2: ebi_CS1 A3: flexpwm1_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N14	GPIO	flexpwm0 B[3]	A0: siul_GPIO[154] A1: dramc_BA[0] A2: ebi_WE_BE_3 A3: flexpwm0_B[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N15	GPIO	flexpwm0 A[2]	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N16	GPIO	flexpwm1 A[0]	A0: siul_GPIO[155] A1: dramc_BA[1] A2: ebi_BDIP A3: flexpwm1_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N17	GPIO	flexpwm1 B[0]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P3	GPIO	dspi0 CS2	A0: siul_GPIO[54] A1: dspi0_CS2 A2: i2c2_data A3: _	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
P5	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO
P6	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P7	ANA	adc0 AN[0]	—	siul_GPI[23] lin0_RXD	AN: adc0_AN[0]		Analog	VDD_HV_ADR02
P8	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pull down	GP Slow/ Medium	VDD_HV_IO
P11	ANA	adc0_adc1 AN[14]	—	siul_GPI[28]	AN: adc0_adc1_AN[14]		Analog Shared	VDD_HV_ADR02
P12	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
P13	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
P15	GPIO	flexpwm0 A[3]	A0: siul_GPIO[153] A1: dramc_WEB A2: ebi_WE_BE_2 A3: flexpwm0_A[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P16	GPIO	flexpwm0 A[0]	A0: siul_GPIO[147] A1: dramc_CKE A2: ebi_OE A3: flexpwm0_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
P17	GPIO	flexpwm1 B[1]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
R4	GPIO	dspi1 CS3	A0: siul_GPIO[55] A1: dspi1_CS3 A2: lin2_TXD A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R5	ANA	adc2 AN[0]	—	siul_GPI[221]	AN: adc2_AN[0]	—	Analog	VDD_HV_ADR02
R6	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR02
R8	ANA	adc2_adc3 AN[14]	—	siul_GPI[228]	AN: adc2_adc3_AN[14]	—	Analog Shared	VDD_HV_ADR13
R10	ANA	adc0 AN[2]	—	siul_GPI[33]	AN: adc0_AN[2]	—	Analog	VDD_HV_ADR02
R11	ANA	adc0_adc1 AN[13]	—	siul_GPI[27]	AN: adc0_adc1_AN[13]	—	Analog Shared	VDD_HV_ADR02
R12	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR13
R14	GPIO	lin0 TXD	A0: siul_GPIO[18] A1: lin0_TXD A2: i2c0_clock A3: sscm_DEBUG[2]	I: _ I: _ I: siul_EIRQ[17]	—	disabled	GP Slow/ Medium	VDD_HV_IO
R16	GPIO	flexpwm1 A[2]	A0: siul_GPIO[164] A1: dramc_ADD[6] A2: ebi_ADD14 A3: flexpwm1_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
R17	GPIO	flexpwm1 B[2]	A0: siul_GPIO[165] A1: dramc_ADD[7] A2: ebi_ADD15 A3: flexpwm1_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
T3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO
T4	ANA	adc3 AN[0]	—	siul_GPI[229]	AN: adc3_AN[0]	—	Analog	VDD_HV_ADR13
T5	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	Analog	VDD_HV_ADR13
T6	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR02
T8	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR02
T10	ANA	adc0 AN[1]	—	siul_GPI[24] etimer0_ETC[5]	AN: adc0_AN[1]	—	Analog	VDD_HV_ADR02
T11	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR02
T12	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR13
T13	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR13

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
T14	GPIO	lin0 RXD	A0: siul_GPIO[19] A1: _ A2: i2c0_data A3: sscm_DEBUG[3]	I: lin0_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T15	GPIO	etimer1 ETC[0]	A0: siul_GPIO[4] A1: etimer1_ETC[0] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[4]	—	disabled	GP Slow/ Medium	VDD_HV_IO
U3	GPIO	dspi2 SIN	A0: siul_GPIO[13] A1: _ A2: _ A3: _	I: dspi2_SIN I: flexpwm0_FAULT[0] I: siul_EIRQ[12]	—	disabled	GP Slow/ Medium	VDD_HV_IO
U4	ANA	adc3 AN[1]	—	siul_GPI[230]	AN: adc3_AN[1]	—	Analog	VDD_HV_ADR13
U5	ANA	adc3 AN[2]	—	siul_GPI[231]	AN: adc3_AN[2]	—	Analog	VDD_HV_ADR13
U6	ANA	adc2 AN[1]	—	siul_GPI[222]	AN: adc2_AN[1]	—	Analog	VDD_HV_ADR02
U7	ANA	adc2_adc3 AN[11]	—	siul_GPI[225]	AN: adc2_adc3_AN[11]	—	Analog Shared	VDD_HV_ADR13
U8	ANA	adc2_adc3 AN[12]	—	siul_GPI[226]	AN: adc2_adc3_AN[12]	—	Analog Shared	VDD_HV_ADR13
U11	ANA	adc0_adc1 AN[11]	—	siul_GPI[25]	AN: adc0_adc1_AN[11]	—	Analog Shared	VDD_HV_ADR02
END OF 257 MAPBGA PIN MULTIPLEXING TABLE								

NOTES:
1 Do not connect pin directly to a power supply or ground.

Table 10. 473 MAPBGA pin multiplexing

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
A4	GPIO	nexus MDO[5][1]	A0: siul_GPIO[114] A1: _ A2: npc_wrapper_MDO[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A5	GPIO	nexus MDO[7][1]	A0: siul_GPIO[112] A1: _ A2: npc_wrapper_MDO[7] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A6	GPIO	nexus MDO[9][1]	A0: siul_GPIO[110] A1: _ A2: npc_wrapper_MDO[9] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A7	GPIO	flexray CB_TX	A0: siul_GPIO[51] A1: flexray_CB_TX A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A8	GPIO	flexray CA_TR_EN	A0: siul_GPIO[47] A1: flexray_CA_TR_EN A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A9	GPIO	fec RX_DV	A0: siul_GPIO[210] A1: flexray_DBG3 A2: etimer2_ETC[0] A3: dspi0_CS7	I: fec_RX_DV I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A10	GPIO	fec MDIO	A0: siul_GPIO[198] A1: fec_MDIO A2: _ A3: dspi2_CS0	I: _ I: _ I: siul_EIRQ[28]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A11	GPIO	fec TX_CLK	A0: siul_GPIO[207] A1: flexray_DBG0 A2: etimer2_ETC[4] A3: dspi0_CS4	I: fec_TX_CLK I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A12	GPIO	fec TX_EN	A0: siul_GPIO[200] A1: fec_TX_EN A2: _ A3: lin0_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
A13	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	pdi DATA[3]	A0: siul_GPIO[134] A1: flexpwm2_X[1] A2: _ A3: _	I: pdi_DATA[3] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A16	GPIO	pdi DATA[1]	A0: siul_GPIO[132] A1: flexpwm2_B[3] A2: _ A3: _	I: pdi_DATA[1] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A17	GPIO	pdi CLOCK	A0: siul_GPIO[128] A1: flexpwm2_B[1] A2: _ A3: etimer1_ETC[3]	I: pdi_CLOCK I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A18	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A19	GPIO	pdi DATA[10]	A0: siul_GPIO[141] A1: flexpwm2_X[3] A2: _ A3: _	I: pdi_DATA[10] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A20	GPIO	pdi DATA[13]	A0: siul_GPIO[144] A1: pdi_SENS_SEL[2] A2: ctu1_EXT_TGR A3: _	I: pdi_DATA[13] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A21	GPIO	pdi DATA[15]	A0: siul_GPIO[146] A1: pdi_SENS_SEL[0] A2: i2c2_data A3: _	I: pdi_DATA[15] I: ctu1_EXT_IN I: _	—	disabled	PDI Medium	VDD_HV_PDI
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
B4	GPIO	can1 TXD	A0: siul_GPIO[14] A1: can1_TXD A2: _ A3: _	I: _ I: _ I: siul_EIRQ[13]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B5	GPIO	nexus MDO[14][1]	A0: siul_GPIO[219] A1: _ A2: npc_wrapper_MDO[14] A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
B6	GPIO	dspi2 CS1	A0: siul_GPIO[9] A1: dspi2_CS1 A2: _ A3: _	I: flexpwm0_FAULT[0] I: lin3_RXD I: can2_RXD	—	disabled	GP Slow/ Medium	VDD_HV_IO
B7	GPIO	flexray CB_TR_EN	A0: siul_GPIO[52] A1: flexray_CB_TR_EN A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B8	GPIO	flexray CA_TX	A0: siul_GPIO[48] A1: flexray_CA_TX A2: _ A3: _	I: ctu1_EXT_IN I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B9	GPIO	fec RXD[3]	A0: siul_GPIO[214] A1: i2c1_data A2: _ A3: _	I: fec_RXD[3] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B10	GPIO	fec RX_ER	A0: siul_GPIO[215] A1: _ A2: _ A3: dspi0_CS1	I: fec_RX_ER I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B11	GPIO	fec TXD[0]	A0: siul_GPIO[201] A1: fec_TXD[0] A2: etimer2_ETC[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B12	GPIO	fec RXD[0]	A0: siul_GPIO[211] A1: i2c1_clock A2: _ A3: _	I: fec_RXD[0] I: _ I: siul_EIRQ[27]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
B13	GPIO	fec TX_ER	A0: siul_GPIO[205] A1: fec_TX_ER A2: dspi2_CS3 A3: _	I: flexpwm1_FAULT[3] I: lin0_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B16	GPIO	pdi DATA[4]	A0: siul_GPIO[135] A1: flexpwm2_A[2] A2: _ A3: etimer1_ETC[4]	I: pdi_DATA[4] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B17	GPIO	pdi DATA[0]	A0: siul_GPIO[131] A1: _ A2: lin3_TXD A3: _	I: pdi_DATA[0] I: _ I: flexpwm2_FAULT[2]	—	disabled	PDI Medium	VDD_HV_PDI
B18	GPIO	pdi LINE_V	A0: siul_GPIO[129] A1: _ A2: lin2_TXD A3: _	I: pdi_LINE_V I: _ I: flexpwm2_FAULT[0]	—	disabled	PDI Medium	VDD_HV_PDI
B19	GPIO	pdi DATA[9]	A0: siul_GPIO[140] A1: flexpwm2_X[2] A2: _ A3: _	I: pdi_DATA[9] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B20	GPIO	pdi DATA[14]	A0: siul_GPIO[145] A1: pdi_SENS_SEL[1] A2: i2c2_clock A3: _	I: pdi_DATA[14] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B21	GPIO	can0 TXD	A0: siul_GPIO[16] A1: can0_TXD A2: _ A3: sscm_DEBUG[0]	I: _ I: _ I: siul_EIRQ[15]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C2	GPIO	nexus MDO[15][1]	A0: siul_GPIO[220] A1: _ A2: npc_wrapper_MDO[15] A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
C5	GPIO	flexray CB_RX	A0: siul_GPIO[50] A1: _ A2: ctu1_EXT_TGR A3: _	I: flexray_CB_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C6	GPIO	etimer0 ETC[4]	A0: siul_GPIO[43] A1: etimer0_ETC[4] A2: _ A3: _	I: _ I: mc_rgm_ABS[0] I: _	—	pull down	GP Slow/ Medium	VDD_HV_IO
C7	GPIO	etimer0 ETC[1]	A0: siul_GPIO[1] A1: etimer0_ETC[1] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[1]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C8	GPIO	etimer0 ETC[2]	A0: siul_GPIO[2] A1: etimer0_ETC[2] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[2]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C9	GPIO	etimer0 ETC[3]	A0: siul_GPIO[3] A1: etimer0_ETC[3] A2: _ A3: _	I: _ I: mc_rgm_ABS[2] I: siul_EIRQ[3]	—	pull down	GP Slow/ Medium	VDD_HV_IO
C10	GPIO	fec TXD[2]	A0: siul_GPIO[203] A1: fec_TXD[2] A2: _ A3: _	I: flexpwm1_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C11	GPIO	fec TXD[1]	A0: siul_GPIO[202] A1: fec_TXD[1] A2: _ A3: dspi2_SCK	I: flexpwm1_FAULT[0] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C12	GPIO	fec CRS	A0: siul_GPIO[208] A1: flexray_DBG1 A2: etimer2_ETC[3] A3: dspi0_CS5	I: fec_CRS I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C13	GPIO	fec RX_CLK	A0: siul_GPIO[209] A1: flexray_DBG2 A2: etimer2_ETC[2] A3: dspi0_CS6	I: fec_RX_CLK I: _ I: siul_EIRQ[25]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
C14	GPIO	fec RXD[1]	A0: siul_GPIO[212] A1: dspi1_CS1 A2: etimer2_ETC[5] A3: _	I: fec_RXD[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C15	GPIO	fec COL	A0: siul_GPIO[206] A1: fec_COL A2: _ A3: lin1_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C16	GPIO	pdi DATA[5]	A0: siul_GPIO[136] A1: flexpwm2_A[0] A2: _ A3: etimer1_ETC[0]	I: pdi_DATA[5] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C17	GPIO	pdi DATA[2]	A0: siul_GPIO[133] A1: flexpwm2_A[1] A2: _ A3: etimer1_ETC[2]	I: pdi_DATA[2] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C18	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C19	GPIO	pdi DATA[12]	A0: siul_GPIO[143] A1: _ A2: _ A3: _	I: pdi_DATA[12] I: lin3_RXD I: flexpwm2_FAULT[3]	—	disabled	PDI Medium	VDD_HV_PDI
C20	GPIO	can0 RXD	A0: siul_GPIO[17] A1: _ A2: _ A3: sscm_DEBUG[1]	I: can0_RXD I: can1_RXD I: siul_EIRQ[16]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C22	GPIO	siul GPIO[197]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_D31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
C23	GPIO	dramc CAS	A0: siul_GPIO[152] A1: dramc_CAS A2: ebi_WE_BE_1 A3: flexpwm0_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
D1	GPIO	nexus MDO[1][1]	A0: siul_GPIO[86] A1: _ A2: npc_wrapper_MDO[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D2	GPIO	nexus MDO[3][1]	A0: siul_GPIO[84] A1: _ A2: npc_wrapper_MDO[3] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D3	GPIO	can1 RXD	A0: siul_GPIO[15] A1: _ A2: _ A3: _	I: can1_RXD I: can0_RXD I: siul_EIRQ[14]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D4	GPIO	dspi0 SOUT	A0: siul_GPIO[38] A1: dspi0_SOUT A2: _ A3: sscm_DEBUG[6]	I: _ I: _ I: siul_EIRQ[24]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D6	GPIO	etimer0 ETC[5]	A0: siul_GPIO[44] A1: etimer0_ETC[5] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D7	GPIO	etimer0 ETC[0]	A0: siul_GPIO[0] A1: etimer0_ETC[0] A2: _ A3: _	I: dspi2_SIN I: _ I: siul_EIRQ[0]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D14	GPIO	fec RXD[2]	A0: siul_GPIO[213] A1: _ A2: _ A3: dspi2_SOUT	I: fec_RXD[2] I: _ I: siul_EIRQ[21]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D15	GPIO	fec MDC	A0: siul_GPIO[199] A1: fec_MDC A2: _ A3: _	I: _ I: lin1_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D18	GPIO	pdi DATA[11]	A0: siul_GPIO[142] A1: flexpwm2_X[0] A2: _ A3: _	I: pdi_DATA[11] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
D19	GPIO	pdi FRAME_V	A0: siul_GPIO[130] A1: _ A2: _ A3: _	I: pdi_FRAME_V I: lin2_RXD I: flexpwm2_FAULT[1]	—	disabled	PDI Medium	VDD_HV_PDI
D21	GPIO	dramc BA[1]	A0: siul_GPIO[155] A1: dramc_BA[1] A2: ebi_BDIP A3: flexpwm1_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
D22	GPIO	siul GPIO[195]	A0: siul_GPIO[195] A1: flexpwm0_X[1] A2: ebi_D29 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
D23	GPIO	dramc BA[0]	A0: siul_GPIO[154] A1: dramc_BA[0] A2: ebi_WE_BE_3 A3: flexpwm0_B[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
E2	GPIO	nexus MDO[2][1]	A0: siul_GPIO[85] A1: _ A2: npc_wrapper_MDO[2] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
E3	GPIO	flexray CA_RX	A0: siul_GPIO[49] A1: _ A2: ctu0_EXT_TGR A3: _	I: flexray_CA_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
E20	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
E21	GPIO	siul GPIO[149]	A0: siul_GPIO[149] A1: _ A2: ebi_RD_WR A3: flexpwm0_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
E22	GPIO	dramc CS0	A0: siul_GPIO[150] A1: dramc_CS0 A2: ebi_TS A3: flexpwm0_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
E23	GPIO	dramc BA[2]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F1	GPIO	nexus MDO[10][1]	A0: siul_GPIO[109] A1: _ A2: npc_wrapper_MDO[10] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F4	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F20	GPIO	dramc RAS	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F21	GPIO	siul GPIO[194]	A0: siul_GPIO[194] A1: flexpwm0_X[0] A2: ebi_D28 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F22	GPIO	siul GPIO[148]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F23	GPIO	dramc D[5]	A0: siul_GPIO[179] A1: dramc_D[5] A2: ebi_D13 A3: ebi_ADD29	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
G1	GPIO	nexus MCKO	A0: siul_GPIO[87] A1: _ A2: npc_wrapper_MCKO A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G3	GPIO	nexus MDO[8][1]	A0: siul_GPIO[111] A1: _ A2: npc_wrapper_MDO[8] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G4	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G20	GPIO	siul GPIO[196]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_D30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
G21	GPIO	dramc DQS[0]	A0: siul_GPIO[190] A1: dramc_DQS[0] A2: ebi_D24 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G22	GPIO	dramc DM[0]	A0: siul_GPIO[192] A1: dramc_DM[0] A2: ebi_D26 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G23	GPIO	dramc D[7]	A0: siul_GPIO[181] A1: dramc_D[7] A2: ebi_D15 A3: ebi_ADD31	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
H1	GPIO	nexus EVTO_B	A0: siul_GPIO[90] A1: _ A2: npc_wrapper_EVTO_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
H3	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
H4	GPIO	nexus EVTI_B	A0: siul_GPIO[91] A1: _ A2: leo_sor_proxy_EVTI_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
H20	GPIO	dramc D[2]	A0: siul_GPIO[176] A1: dramc_D[2] A2: ebi_D10 A3: ebi_ADD26	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
J1	GPIO	nexus RDY_B	A0: siul_GPIO[216] A1: _ A2: nexus_RDY_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J2	GPIO	nexus MDO[13][1]	A0: siul_GPIO[218] A1: _ A2: npc_wrapper_MDO[13] A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J3	GPIO	nexus MDO[12][1]	A0: siul_GPIO[217] A1: _ A2: npc_wrapper_MDO[12] A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
J20	GPIO	dramc D[0]	A0: siul_GPIO[174] A1: dramc_D[0] A2: ebi_D8 A3: ebi_ADD24	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
J21	GPIO	dramc D[1]	A0: siul_GPIO[175] A1: dramc_D[1] A2: ebi_D9 A3: ebi_ADD25	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
J22	GPIO	dramc D[3]	A0: siul_GPIO[177] A1: dramc_D[3] A2: ebi_D11 A3: ebi_ADD27	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
J23	GPIO	dramc D[6]	A0: siul_GPIO[180] A1: dramc_D[6] A2: ebi_D14 A3: ebi_ADD30	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K1	GPIO	dspi0 SCK	A0: siul_GPIO[37] A1: dspi0_SCK A2: _ A3: sscm_DEBUG[5]	I: flexpwm0_FAULT[3] I: _ I: siul_EIRQ[23]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K2	GPIO	dspi1 CS0	A0: siul_GPIO[5] A1: dspi1_CS0 A2: _ A3: dspi0_CS7	I: _ I: _ I: siul_EIRQ[5]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K3	GPIO	dspi1 SCK	A0: siul_GPIO[6] A1: dspi1_SCK A2: _ A3: _	I: _ I: _ I: siul_EIRQ[6]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K4	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K21	GPIO	dramc D[4]	A0: siul_GPIO[178] A1: dramc_D[4] A2: ebi_D12 A3: ebi_ADD28	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K22	GPIO	dramc D[8]	A0: siul_GPIO[182] A1: dramc_D[8] A2: ebi_D16 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K23	GPIO	dramc D[9]	A0: siul_GPIO[183] A1: dramc_D[9] A2: ebi_D17 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
L1	GPIO	dspi0 CS0	A0: siul_GPIO[36] A1: dspi0_CS0 A2: _ A3: sscm_DEBUG[4]	I: _ I: _ I: siul_EIRQ[22]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
L2	GPIO	dspi2 CS2	A0: siul_GPIO[42] A1: dspi2_CS2 A2: lin3_TXD A3: can2_TXD	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
L3	GPIO	dspi2 CS0	A0: siul_GPIO[10] A1: dspi2_CS0 A2: _ A3: can3_TXD	I: _ I: _ I: siul_EIRQ[9]	—	disabled	GP Slow/ Medium	VDD_HV_IO
M1	GPIO	flexpwm0 X[0]	A0: siul_GPIO[57] A1: flexpwm0_X[0] A2: lin2_TXD A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M3	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M20	GPIO	dramc ODT	A0: siul_GPIO[157] A1: dramc_ODT A2: ebi_CS1 A3: flexpwm1_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
M21	GPIO	dramc WEB	A0: siul_GPIO[153] A1: dramc_WEB A2: ebi_WE_BE_2 A3: flexpwm0_A[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
M22	GPIO	dramc D[11]	A0: siul_GPIO[185] A1: dramc_D[11] A2: ebi_D19 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
M23	GPIO	dramc D[10]	A0: siul_GPIO[184] A1: dramc_D[10] A2: ebi_D18 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N1	GPIO	flexpwm0 A[0]	A0: siul_GPIO[58] A1: flexpwm0_A[0] A2: _ A3: _	I: _ I: etimer0_ETC[0] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
N3	GPIO	flexpwm0 X[1]	A0: siul_GPIO[60] A1: flexpwm0_X[1] A2: _ A3: _	I: lin2_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N4	GPIO	flexpwm0 B[2]	A0: siul_GPIO[100] A1: flexpwm0_B[2] A2: _ A3: _	I: _ I: etimer0_ETC[5] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N20	GPIO	dramc DQS[1]	A0: siul_GPIO[191] A1: dramc_DQS[1] A2: ebi_D25 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N21	GPIO	dramc DM[1]	A0: siul_GPIO[193] A1: dramc_DM[1] A2: ebi_D27 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N22	GPIO	dramc D[13]	A0: siul_GPIO[187] A1: dramc_D[13] A2: ebi_D21 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N23	GPIO	dramc D[12]	A0: siul_GPIO[186] A1: dramc_D[12] A2: ebi_D20 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
P1	GPIO	flexpwm0 B[0]	A0: siul_GPIO[59] A1: flexpwm0_B[0] A2: _ A3: _	I: _ I: etimer0_ETC[1] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P2	GPIO	flexpwm0 B[1]	A0: siul_GPIO[62] A1: flexpwm0_B[1] A2: _ A3: _	I: _ I: etimer0_ETC[3] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P3	GPIO	flexpwm0 A[2]	A0: siul_GPIO[99] A1: flexpwm0_A[2] A2: _ A3: _	I: _ I: etimer0_ETC[4] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
P4	GPIO	flexpwm0 A[3]	A0: siul_GPIO[102] A1: flexpwm0_A[3] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P20	GPIO	dramc D[14]	A0: siul_GPIO[188] A1: dramc_D[14] A2: ebi_D22 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
P21	GPIO	dramc D[15]	A0: siul_GPIO[189] A1: dramc_D[15] A2: ebi_D23 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
R1	GPIO	flexpwm0 X[2]	A0: siul_GPIO[98] A1: flexpwm0_X[2] A2: lin3_TXD A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R2	GPIO	flexpwm0 X[3]	A0: siul_GPIO[101] A1: flexpwm0_X[3] A2: _ A3: _	I: lin3_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R3	GPIO	flexpwm0 A[1]	A0: siul_GPIO[80] A1: flexpwm0_A[1] A2: _ A3: _	I: _ I: etimer0_ETC[2] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R21	GPIO	dramc ADD[3]	A0: siul_GPIO[161] A1: dramc_ADD[3] A2: ebi_ADD11 A3: ebi_TEA	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
R22	GPIO	dramc CKE	A0: siul_GPIO[147] A1: dramc_CKE A2: ebi_OE A3: flexpwm0_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T1	GPIO	flexpwm0 B[3]	A0: siul_GPIO[103] A1: flexpwm0_B[3] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
T2	GPIO	flexpwm1 A[0]	A0: siul_GPIO[117] A1: flexpwm1_A[0] A2: _ A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T3	GPIO	flexpwm1 A[1]	A0: siul_GPIO[120] A1: flexpwm1_A[1] A2: _ A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T20	GPIO	dramc ADD[8]	A0: siul_GPIO[166] A1: dramc_ADD[8] A2: ebi_D0 A3: ebi_ADD16	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T21	GPIO	dramc ADD[9]	A0: siul_GPIO[167] A1: dramc_ADD[9] A2: ebi_D1 A3: ebi_ADD17	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T22	GPIO	dramc ADD[1]	A0: siul_GPIO[159] A1: dramc_ADD[1] A2: ebi_ADD9 A3: ebi_CS3	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U1	GPIO	flexpwm1 B[0]	A0: siul_GPIO[118] A1: flexpwm1_B[0] A2: _ A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U2	GPIO	flexpwm1 B[1]	A0: siul_GPIO[121] A1: flexpwm1_B[1] A2: _ A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U3	GPIO	flexpwm1 A[2]	A0: siul_GPIO[123] A1: flexpwm1_A[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U4	GPIO	dspi2 SCK	A0: siul_GPIO[11] A1: dspi2_SCK A2: _ A3: _	I: can3_RXD I: _ I: siul_EIRQ[10]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
U20	GPIO	dramc ADD[6]	A0: siul_GPIO[164] A1: dramc_ADD[6] A2: ebi_ADD14 A3: flexpwm1_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U21	GPIO	dramc ADD[12]	A0: siul_GPIO[170] A1: dramc_ADD[12] A2: ebi_D4 A3: ebi_ADD20	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U23	GPIO	dramc ADD[0]	A0: siul_GPIO[158] A1: dramc_ADD[0] A2: ebi_ADD8 A3: ebi_CS2	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V3	GPIO	flexpwm1 B[2]	A0: siul_GPIO[124] A1: flexpwm1_B[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V4	GPIO	dspi1 CS2	A0: siul_GPIO[56] A1: dspi1_CS2 A2: _ A3: dspi0_CS5	I: flexpwm0_FAULT[3] I: lin2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V20	GPIO	lin0 TXD	A0: siul_GPIO[18] A1: lin0_TXD A2: i2c0_clock A3: sscm_DEBUG[2]	I: _ I: _ I: siul_EIRQ[17]	—	disabled	GP Slow/ Medium	VDD_HV_IO
V21	GPIO	dramc ADD[13]	A0: siul_GPIO[171] A1: dramc_ADD[13] A2: ebi_D5 A3: ebi_ADD21	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V23	GPIO	dramc ADD[2]	A0: siul_GPIO[160] A1: dramc_ADD[2] A2: ebi_ADD10 A3: ebi_TA	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
W3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
W20	GPIO	lin0 RXD	A0: siul_GPIO[19] A1: _ A2: i2c0_data A3: sscm_DEBUG[3]	I: lin0_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
W21	GPIO	dramc ADD[14]	A0: siul_GPIO[172] A1: dramc_ADD[14] A2: ebi_D6 A3: ebi_ADD22	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
W22	GPIO	dramc ADD[7]	A0: siul_GPIO[165] A1: dramc_ADD[7] A2: ebi_ADD15 A3: flexpwm1_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
W23	GPIO	dramc ADD[4]	A0: siul_GPIO[162] A1: dramc_ADD[4] A2: ebi_ADD12 A3: ebi_ALE	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
Y3	GPIO	dspi0 CS2	A0: siul_GPIO[54] A1: dspi0_CS2 A2: i2c2_data A3: _	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y5	GPIO	flexpwm1 X[0]	A0: siul_GPIO[116] A1: flexpwm1_X[0] A2: etimer2_ETC[0] A3: dspi0_CS1	I: ctu0_EXT_IN I: ctu1_EXT_IN I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y6	ANA	adc3 AN[0]	—	siul_GPI[229]	AN: adc3_AN[0]	—	Analog	VDD_HV_ADR23
Y7	ANA	adc2_adc3 AN[11]	—	siul_GPI[225]	AN: adc2_adc3_AN[11]	—	Analog Shared	VDD_HV_ADR23
Y8	ANA	adc2_adc3 AN[14]	—	siul_GPI[228]	AN: adc2_adc3_AN[14]	—	Analog Shared	VDD_HV_ADR23

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
Y9	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y10	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y11	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pull down	GP Slow/ Medium	VDD_HV_IO
Y14	ANA	adc0_adc1 AN[11]	—	siul_GPI[25]	AN: adc0_adc1_AN[11]	—	Analog Shared	VDD_HV_ADR0
Y15	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y16	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y17	ANA	adc1 AN[8]	—	siul_GPI[74]	AN: adc1_AN[8]	—	Analog	VDD_HV_ADR1
Y18	ANA	adc1 AN[6]	—	siul_GPI[76]	AN: adc1_AN[6]	—	Analog	VDD_HV_ADR1
Y21	GPIO	dramc ADD[15]	A0: siul_GPIO[173] A1: dramc_ADD[15] A2: ebi_D7 A3: ebi_ADD23	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
Y22	GPIO	dramc ADD[11]	A0: siul_GPIO[169] A1: dramc_ADD[11] A2: ebi_D3 A3: ebi_ADD19	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
Y23	GPIO	dramc ADD[5]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AA4	GPIO	dspi1 CS3	A0: siul_GPIO[55] A1: dspi1_CS3 A2: lin2_TXD A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA5	GPIO	flexpwm1 X[1]	A0: siul_GPIO[119] A1: flexpwm1_X[1] A2: etimer2_ETC[1] A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA6	ANA	adc3 AN[1]	—	siul_GPI[230]	AN: adc3_AN[1]	—	Analog	VDD_HV_ADR23
AA7	ANA	adc2_adc3 AN[12]	—	siul_GPI[226]	AN: adc2_adc3_AN[12]	—	Analog Shared	VDD_HV_ADR23
AA8	ANA	adc2 AN[0]	—	siul_GPI[221]	AN: adc2_AN[0]	—	Analog	VDD_HV_ADR23
AA11	ANA	adc0 AN[2]	—	siul_GPI[33]	AN: adc0_AN[2]	—	Analog	VDD_HV_ADR0
AA12	ANA	adc0 AN[5]	—	siul_GPI[66]	AN: adc0_AN[5]	—	Analog	VDD_HV_ADR0
AA13	ANA	adc0 AN[8]	—	siul_GPI[69]	AN: adc0_AN[8]	—	Analog	VDD_HV_ADR0

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
AA14	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR0
AA15	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR1
AA16	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR1
AA17	ANA	adc1 AN[5]	—	siul_GPI[64]	AN: adc1_AN[5]	—	Analog	VDD_HV_ADR1
AA18	ANA	adc1 AN[7]	—	siul_GPI[73]	AN: adc1_AN[7]	—	Analog	VDD_HV_ADR1
AA19	GPIO	TDI	A0: siul_GPIO[21] A1: _ A2: _ A3: _	I: jtagc_TDI I: _ I: _	—	pull up	GP Slow/ Medium	VDD_HV_IO
AA20	GPIO	etimer1 ETC[0]	A0: siul_GPIO[4] A1: etimer1_ETC[0] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[4]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA22	GPIO	lin1 TXD	A0: siul_GPIO[94] A1: lin1_TXD A2: i2c1_clock A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA23	GPIO	dramc ADD[10]	A0: siul_GPIO[168] A1: dramc_ADD[10] A2: ebi_D2 A3: ebi_ADD18	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AB3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
AB4	GPIO	flexpwm1 X[2]	A0: siul_GPIO[122] A1: flexpwm1_X[2] A2: etimer2_ETC[2] A3: dspi0_CS5	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AB5	GPIO	flexpwm1 X[3]	A0: siul_GPIO[125] A1: flexpwm1_X[3] A2: etimer2_ETC[3] A3: dspi0_CS6	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AB6	ANA	adc3 AN[2]	—	siul_GPI[231]	AN: adc3_AN[2]	—	Analog	VDD_HV_ADR23
AB7	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR23
AB8	ANA	adc2 AN[1]	—	siul_GPI[222]	AN: adc2_AN[1]	—	Analog	VDD_HV_ADR23
AB9	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR23
AB10	ANA	adc0 AN[0]	—	siul_GPI[23] lin0_RXD	AN: adc0_AN[0]	—	Analog	VDD_HV_ADR0
AB11	ANA	adc0 AN[4]	—	siul_GPI[70]	AN: adc0_AN[4]	—	Analog	VDD_HV_ADR0
AB12	ANA	adc0 AN[6]	—	siul_GPI[71]	AN: adc0_AN[6]	—	Analog	VDD_HV_ADR0
AB13	ANA	adc0 AN[7]	—	siul_GPI[68]	AN: adc0_AN[7]	—	Analog	VDD_HV_ADR0
AB14	ANA	adc0_adc1 AN[13]	—	siul_GPI[27]	AN: adc0_adc1_AN[13]	—	Analog Shared	VDD_HV_ADR0

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
AB15	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR1
AB16	ANA	adc1 AN[3]	—	siul_GPI[32]	AN: adc1_AN[3]	—	Analog	VDD_HV_ADR1
AB17	ANA	adc1 AN[4]	—	siul_GPI[75]	AN: adc1_AN[4]	—	Analog	VDD_HV_ADR1
AB18	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
AB21	GPIO	lin1 RXD	A0: siul_GPIO[95] A1: _ A2: i2c1_data A3: _	I: lin1_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC3	GPIO	dspi2 SIN	A0: siul_GPIO[13] A1: _ A2: _ A3: _	I: dspi2_SIN I: flexpwm0_FAULT[0] I: siul_EIRQ[12]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC4	GPIO	flexpwm1 A[3]	A0: siul_GPIO[126] A1: flexpwm1_A[3] A2: etimer2_ETC[4] A3: dspi0_CS7	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC5	GPIO	flexpwm1 B[3]	A0: siul_GPIO[127] A1: flexpwm1_B[3] A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC6	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	GP Slow/ Medium	VDD_HV_ADR23
AC9	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR23

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball Number	Ball Type	Ball Name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad Type	Power Domain
AC10	ANA	adc0 AN[1]	—	siul_GPI[24] etimer0_ETC[5]	AN: adc0_AN[1]	—	Analog	VDD_HV_ADR0
AC11	ANA	adc0 AN[3]	—	siul_GPI[34]	AN: adc0_AN[3]	—	Analog	VDD_HV_ADR0
AC14	ANA	adc0_adc1 AN[14]	—	siul_GPI[28]	AN: adc0_adc1_AN[14]	—	Analog Shared	VDD_HV_ADR0
END OF 473 MAPBGA PIN MULTIPLEXING TABLE								

NOTES:
1 Do not connect pin directly to a power supply or ground.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

The “Symbol” column of the electrical parameter and timings tables may contain an additional column containing “SR”, “CC”, “P”, “C”, “T” or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the *input* voltage of a voltage regulator.
- “CC” identifies specifications that define normal device operation. Where available, the letters “P”, “C”, “T” or “D” replace the letter “CC” and apply to these controller characteristics. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 11. Absolute maximum ratings[1]

No.	Symbol		Parameter	Conditions	Min	Max[2]	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	–0.3	5.5[3]	V
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	–0.1	0.1	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	–0.3	3.6[4,5]	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	–0.1	0.1	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	–0.3	3.6[4,5]	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	–0.1	0.1	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	–0.3	3.6[4,5]	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	–0.1	0.1	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	–0.3	3.6[4,5]	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	–0.1	0.1	V
11	$V_{DD\_HV\_DRAM}$	SR	DRAM interface supply voltage	—	–0.3	3.6[4,5]	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	–0.1	0.1	V
13	$V_{DD\_HV\_ADRx}$[6]	SR	ADC*x* high reference voltage	—	–0.3	6.0	V
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	–0.1	0.1	V

Table 11. Absolute maximum ratings[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Max[2]	Unit
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	–0.3	3.6[4,5]	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	–0.1	0.1	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic	—	–0.3	1.32[7]	V
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	–0.1	0.1	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage	—	–0.3	1.4	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	–0.1	0.1	V
21	TV_{DD}	SR	Slope characteristics on all V_{DD} during power up	—	—	25	mV/µs
22	V_{IN}	SR	Voltage on any pin with respect to its supply rail $V_{DD\_HV\_xxx}$	Relative to $V_{DD\_HV\_xxx}$	–0.3	$V_{DD\_HV\_xxx}$ + 0.3[8]	V
23	I_{INJPAD}	SR	Injected input current on any pin during overload condition (incl. analog pins TBD)	—	–10	10	mA
24	$I_{INJPADA}$	SR	Injected input current on any analog pin during overload condition	—	–3	3	mA
25	I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
26	T_{STG}	SR	Storage temperature	—	–55	150	°C
27	T_{SDR}	SR	Maximum Solder Temperature[9] Pb-free package SnPb package	—	 — —	 260 245	°C
28	MSL	SR	Moisture Sensitivity Level[10]	—	—	3	—

NOTES:
1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. TBD V for 10 hours cumulative time, 5.0 V + 10% for time remaining.
4. 5.3 V for 10 hours cumulative over lifetime of device, 3.63 V for time remaining.
5. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
6. All $V_{DD\_HV\_ADRx}$ rails must be operated at the same supply voltage.
7. 2.0 V for 10 hours cumulative time, 1.2 V + 10% for time remaining.
8. Only when $V_{DD\_HV\_xxx} < 5.2$ V.
9. Solder profile per CDF-AEC-Q100.
10. Moisture sensitivity per JEDEC test method A112.

3.3 Recommended operating conditions

Table 12. Recommended operating conditions[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	3.0	5.5	V

Table 12. Recommended operating conditions[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	0	0	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	3.0	3.6	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	0	0	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	3.0	3.6	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	0	0	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	3.0	3.6	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	0	0	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	1.62	3.6	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	0	0	V
11	$V_{DD\_HV\_DRAM}$	SR	DRAM interface supply voltage	—	1.62	3.6	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	0	0	V
13	$V_{DD\_HV\_ADRx}$	SR	ADC*x* high reference voltage	—	3.0	3.6	V
				Alternate input voltage	4.5	5.5	
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	0	0	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	3.0	3.6	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	0	0	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic[2]	External VREG mode	1.14	1.32	V
17a		CC		Internal VREG Mode	1.14	1.32	V
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	0	0	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage[2]	External VREG mode	1.14	1.32	V
19a		CC		Internal VREG Mode	1.14	1.32	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	0	0	V
21	T_A	SR	Ambient temperature under bias[3]	257 MAPBGA	–40	105[4]	°C
				473 MAPBGA	–40	125	°C
22	T_J	SR	Junction temperature under bias	257 MAPBGA	–40	150	°C
				473 MAPBGA	–40	150	

NOTES:
1 These specifications are design targets and are subject to change per device characterization.
2 The jitter specifications for both PLLs holds true only up to 50 mV noise (peak to peak) on $V_{DD\_LV\_COR}$ and $V_{DD\_LV\_PLL}$.
3 See Table 1 for available frequency and package options.
4 Preliminary data.

3.4 Thermal characteristics

Table 13. Thermal characteristics for package options[1]

No.	Symbol		Parameter	Conditions	Value		Unit
					BGA 257	BGA 473	
1	$R_{\theta JA}$	CC	Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	≤ 40	≤ 34	°C/W
2	$R_{\theta JA}$	CC	Thermal resistance junction-to-ambient natural convection[2]	Four layer board – 2s2p	≤ 22	≤ 20	°C/W
3	$R_{\theta JMA}$	CC	Thermal resistance junction-to-moving-air ambient[2]	@ 200 ft./min., single layer board – 1s	≤ 32	≤ 26	°C/W
4	$R_{\theta JMA}$	CC	Thermal resistance junction-to-moving-air ambient[2]	@ 200 ft./min., four layer board – 2s2p	≤ 18	≤ 17	°C/W
5	$R_{\theta JB}$	CC	Thermal resistance junction-to-board[3]	—	≤ 10	≤ 10	°C/W
6	$R_{\theta JC}$	CC	Thermal resistance junction-to-case[4]	—	≤ 6	≤ 6	°C/W
7	Ψ_{JT}	CC	Junction-to-package-top natural convection[5]	—	≤ 2	≤ 2	°C/W

NOTES:
1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer

board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

See [6] to [10] in Section 6, Reference documents, for more information.

3.5 Electromagnetic interference (EMI) characteristics

3.5.1 Test Setup

Electromagnetic emission tests are performed by TEM cell [2] and via direct coupling [3] (150 Ohm) measurements.

Electromagnetic immunity are measured by DPI [4].

See Section 6, Reference documents, for more information.

3.5.2 Test parameters

The following test parameters shall be used:

Table 14. EMC test parameters

Method	Frequency Range	Receiver	
		BW	Step Size
150 Ohm	1 MHz to 1000 MHz	1 MHz	500 kHz
TEM			

In case of only narrow band disturbances the maximum of the results will not change. In case of broadband signals the emission has to be below the limits.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	750 (corners)	V
						500	

NOTES:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Power Management Controller (PMC) electrical characteristics

3.8.1 PMC electrical specifications

This section contains electrical characteristics for the PMC.

Table 17. PMC electrical specifications

No.	Symbol		Parameter	Min	Typ	Max	Unit
2	$V_{DD\_LV\_COR}$	CC	Nominal V_{RC} regulated 1.2 V output $V_{DD\_HV\_PMU}$	—	1.28	—	V
3	PorC	CC	POR rising V_{DD} 1.2 V • POR V_{DD} variation • POR 1.2 V hysteresis	— PorC – 30% —	0.7 PorC 75	— PorC + 30% —	V V mV
4	LvdC	CC	Nominal LVD 1.2 V • LVD 1.2 V at reset (LVDCR) • LVD 1.2 V variation at reset • LVD 1.2 V variation after reset • LVD 1.2 V hysteresis	— — LvdC – 3.5% LvdC – 3% 10	1.175[1] 1.215[1] LvdC[1] LvdC[1] 15	— — LvdC + 3.5% LvdC + 3% 20	V V V V mV
5	HvdC	CC	Nominal HVD 1.2 V • HVD 1.2 V at reset (HVDCR) • HVD 1.2 V variation at reset • HVD 1.2 V variation after reset • HVD 1.2 V hysteresis	— — HvdC – 3.5% HvdC – 3% 10	1.32[1] 1.44[1] HvdC[1] HvdC[1] 15	— — HvdC + 3.5% HvdC + 3% 20	 V V V mV
6	VddStepC	CC	Trimming step LVD 1.2 V, HVD 1.2 V, VRC 1.2 V	—	5	—	mV
7	PorReg	CC	POR rising on V_{DDREG} • POR V_{DDREG} variation • POR V_{DDREG} hysteresis	— PorReg – 30% —	2.00 PorReg 250	— PorReg + 30% —	V V mV
8	LvdReg	CC	Nominal rising LVD 3.3 V on V_{DDREG}, V_{DDIO}, $V_{DDFLASH}$, and V_{DDADC} • LVD 3.3 V variation at reset • LVD 3.3 V variation after reset • LVD 3.3 V hysteresis • Minimum slew rate • Maximum slew rate	— LvdReg – 3.5% LvdReg – 3% — — —	2.865 LvdReg[1] LvdReg[1] 30 50 25	— LvdReg + 3.5% LvdReg + 3% — — —	 V V mV mV/ms mV/µs
9	LvdStepReg	CC	Trimming step LVD 3.3 V	—	30	—	mV

NOTES:
1 Rising V_{DD}.

3.8.2 PMC board schematic and components

Figure 7 shows a sample application for the PMC.

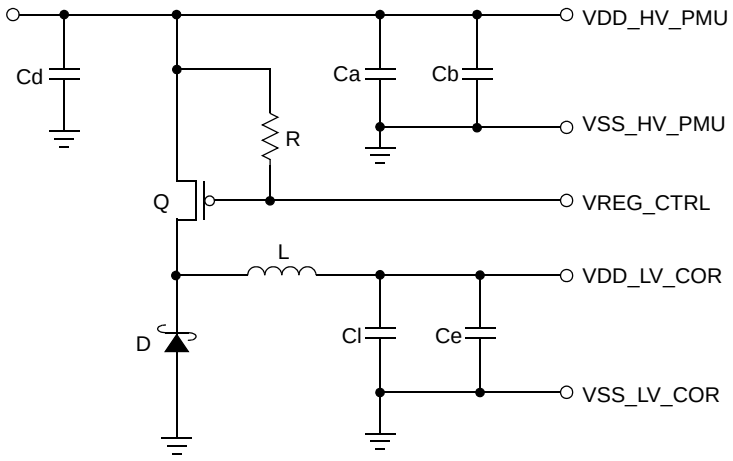


Figure 7. PMU mandatory external components

Table 18. VRC SMPS recommended external devices

Reference Designator	Part Description	Part Type	Nominal	Description
Ca	—	capacitor	20 µF, 20 V	Filter capacitor
Cb	—	capacitor	0.1 µF, 20 V	Filter capacitor
Cd	—	capacitor	20 µF, 20 V	Supply decoupling cap, ESR < 50 mΩ, as close to p-MOS source as possible
Ce	—	capacitor	0.1 µF, 16 V	Ceramic
Cl	—	capacitor	20 µF, 16 V	Buck capacitor, total ESR < 100 mΩ, as close to the coil as possible
D	SS8P3L	Schottky	—	Vishay low Vf Schottky diode
L	—	inductor	4 µH, 1.5 A	Buck shielded coil low ESR
Q	SUD50P04/SQD50P04	pMOS	2 A, 40 V	Vishay low threshold p-MOS, V_{th} < 2.5 V, Rdson@4.5 V < 20 mΩ, Cg < 5 nF
R	—	resistor	50–100 kΩ	Pull up for power p-MOS gate

3.9 Supply current characteristics

Table 19. Current consumption characteristics[1]

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	I_{DD_LV}	CC	Maximum run I_{DD} (incl. digital core logic and analog block of the LV rail)	V_{DD_LV} = 1.36 V, f_{Core} = 180 MHz, 1:2 Mode, DPM, both cores executing EMC test code, internal VREG mode, all caches enabled, code execution of core 0 from code flash 0, code execution of core 1 from code flash 1, FMPLL_1 active at 120 MHz.	—	600	900	mA
2	$I_{DD\_LV\_PLL}$	CC	Maximum run I_{DD} for each PLL[2]	$V_{DD\_LV\_PLL}$ = 1.36 V, f_{VCO} running at maximum frequency.	—	1.5	2	mA
3	$I_{DD\_HV\_FLA}$	CC	Maximum run I_{DD} Flash	$V_{DD\_HV\_FLA}$ = 3.6 V, DPM, both cores executing EMC test code, code execution of core 0 from code flash 0, code execution of core 1 from code flash 1.	—	20	30	mA
4	$I_{DD\_HV\_OSC}$	CC	Maximum run I_{DD} OSC	f_{OSC} 4 MHz to 40 MHz, $V_{DD\_HV\_OSC}$ 3.6 V	—	1	3	mA
5	$I_{DD\_HV\_ADV}$	CC	Maximum run I_{DD} for each ADC[3]	$V_{DD\_HV\_ADV}$ = 3.6 V	—	2	4	mA
6	$I_{DD\_HV\_ADR02}$[4]	CC	Maximum reference I_{DD}[5]	ADC0 powered on[6]	—	—	2	mA
				ADC2 powered on	—	—	1.2	mA
7	$I_{DD\_HV\_ADR13}$[4]	CC	Maximum reference I_{DD}[5]	ADC1 powered on	—	—	1.2	mA
				ADC3 powered on	—	—	1.2	mA
8	$I_{DD\_HV\_ADR0}$[7]	CC	Maximum reference I_{DD}	ADC0 powered on[6]	—	—	2	mA
9	$I_{DD\_HV\_ADR1}$[7]	CC	Maximum reference I_{DD}	ADC1 powered on	—	—	1.2	mA
10	$I_{DD\_HV\_ADR23}$[7]	CC	Maximum reference I_{DD}[5]	ADC2 powered on	—	—	1.2	mA
				ADC3 powered on	—	—	1.2	mA

NOTES:
1. Applies to T_J = –40 °C to 150 °C.
2. Total current on $I_{DD\_LV\_PLL}$ needs to be multiplied with the number of active PLLs.
3. Total current on $I_{DD\_HV\_ADV}$ needs to be multiplied with the number of active ADCs.
4. 257 MAPBGA only.
5. Total current on $I_{DD\_HV\_ADRxx}$ is the sum of both references if both ADCs are powered on.
6. ADC0 includes 0.7 mA dissipation for the temperature sensor (TSENS).
7. 473 MAPBGA only.

3.10 Temperature sensor electrical characteristics

Table 20. Temperature sensor electrical characteristics

Symbol			Parameter	Conditions	Min	Max	Unit
1	—	P	Accuracy	T_J = –40 °C to T_A = 125 °C	–10	10	°C

Table 20. Temperature sensor electrical characteristics (continued)

Symbol			Parameter	Conditions	Min	Max	Unit
2	T_S	D	Minimum sampling period	—	4	—	µs

3.11 Main oscillator electrical characteristics

The PXS30 provides an oscillator/resonator driver.

Table 21. Main oscillator electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
1	F_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
2	$T_{XOSCHSSU}$	CC	Oscillator start-up time	f_{OSC} = 4 MHz to 40 MHz	—	TBD	TBD	µs
3	V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
4	V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

NOTES:
1 V_{DD} = 3.0 V to 3.6 V, T_J = –40 to 150 °C, unless otherwise specified.

3.12 FMPLL electrical characteristics

Table 22. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range[1]	Crystal reference	TBD	—	TBD	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	TBD	—	TBD	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	See Chapter 30, "Frequency-Modulated Phase-Locked Loop (FMPLL)," in the *PXS30 Reference Manual (PXS30RM)* for more details on PLL configuration.	16	—	256	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	TBD	—	TBD	MHz
f_{sys}	D	On-chip FMPLL frequency[2]	—	TBD	—	TBD	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window[2]	Lower limit	TBD	—	TBD	MHz
			Upper limit	TBD	—	TBD	
f_{SCM}	D	Self-clocked mode frequency[3,4]	—	TBD	—	TBD	MHz

Table 22. FMPLL electrical characteristics (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
t_{lpll}	D	FMPLL lock time [5, 6]	—	—	—	TBD	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter[7,8,9,10]	Peak-to-peak (clock edge to clock edge), f_{SYS} maximum	TBD	—	TBD	ps
			Long-term jitter (avg. over 2 ms interval), f_{SYS} maximum	TBD	—	TBD	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±500	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	TBD	—	TBD	% f_{sys}
f_{UL}	D	Frequency un-LOCK range	—	TBD	—	TBD	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth	Center spread	TBD	—	TBD	% f_{sys}
			Down Spread	TBD	—	TBD	
f_{MOD}	D	Modulation frequency[11]	—	TBD	—	TBD	kHz

NOTES:
1 Considering operation with FMPLL not bypassed.

2 "Loss of Reference Frequency" window is the reference frequency range outside of which the FMPLL is in self clocked mode.

3 Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the f_{LOR} window.

4 f_{VCO} is the frequency at the output of the VCO; its range is 256–512 MHz.
f_{SCM} is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
$f_{SYS} = f_{VCO} \div ODF$

5 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.

6 This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

7 This value is determined by the crystal manufacturer and board design.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

9 Proper PC board layout procedures must be followed to achieve specifications.

10 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

11 Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.13 16 MHz RC oscillator electrical characteristics

Table 23. RC oscillator electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	f_{RC}	CC	RC oscillator frequency	27 °C, 1.2 V trimmed	—	16	—	MHz
2	Δ_{RCMVAR}	CC	Frequency spread: The variation in output frequency from PTF[1] across temperature and supply voltage range	—	—	—	±5	%
3	$\Delta_{IRCTRIM}$	CC	Internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

NOTES:
1 PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature.

3.14 ADC electrical characteristics

The PXS30 provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

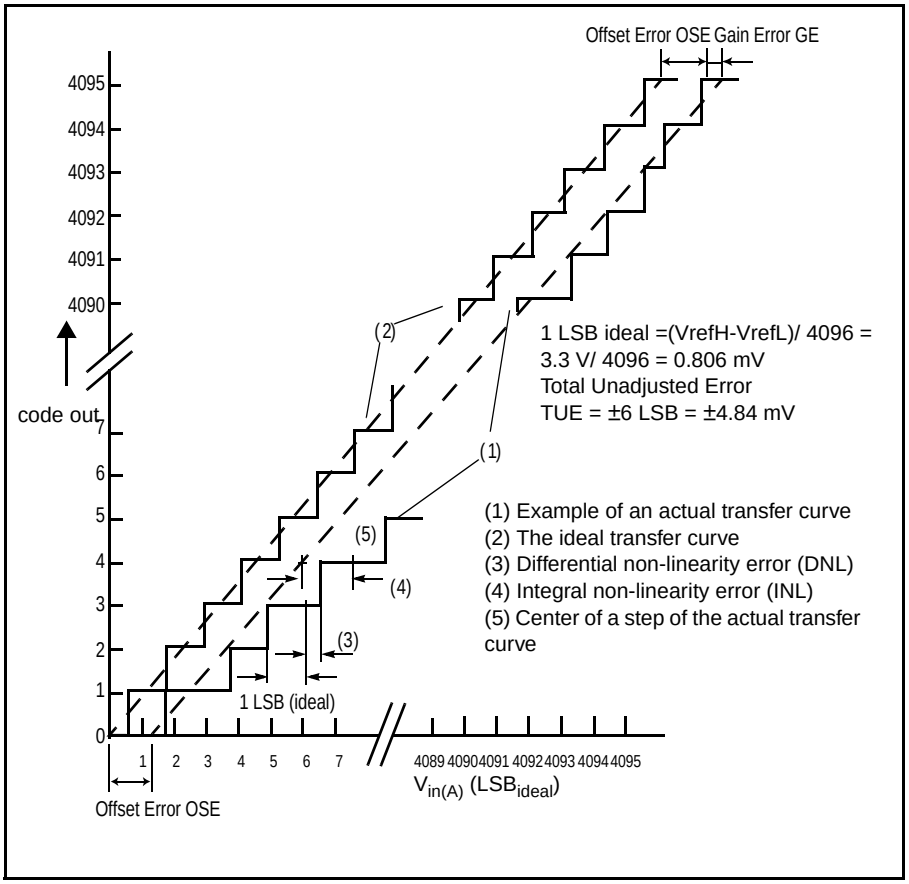


Figure 8. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_C \times C_S)$, where f_C represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 9:

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 9}$$

Equation 9 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

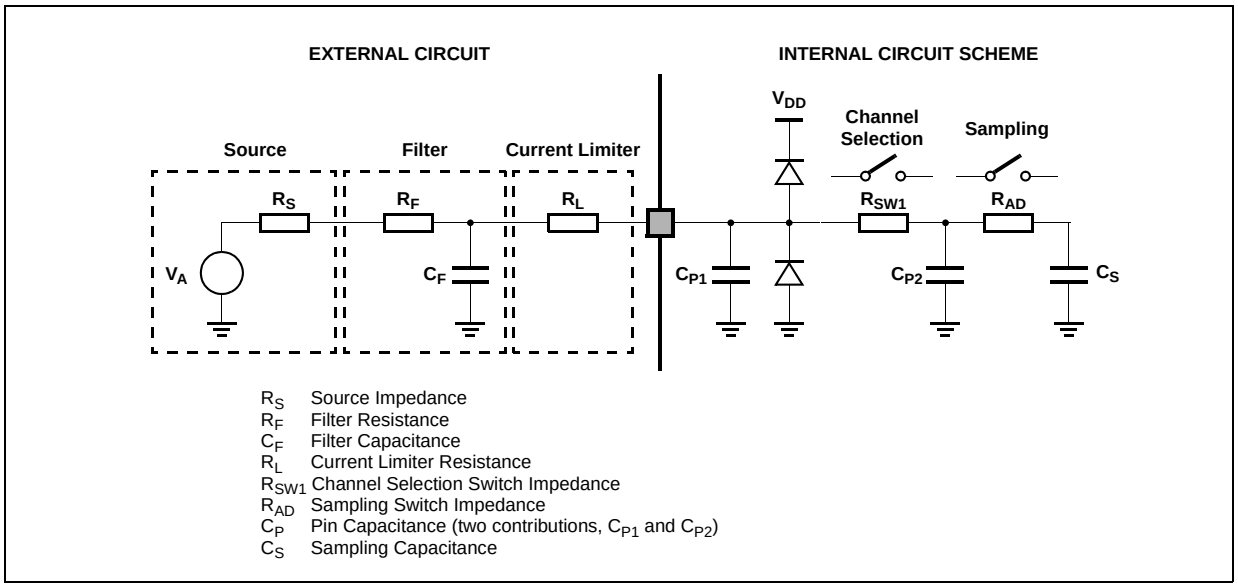


Figure 10. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1}, and C_{P2} are initially charged at the source voltage V_A (please see the equivalent circuit in Figure 10): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch is closed).

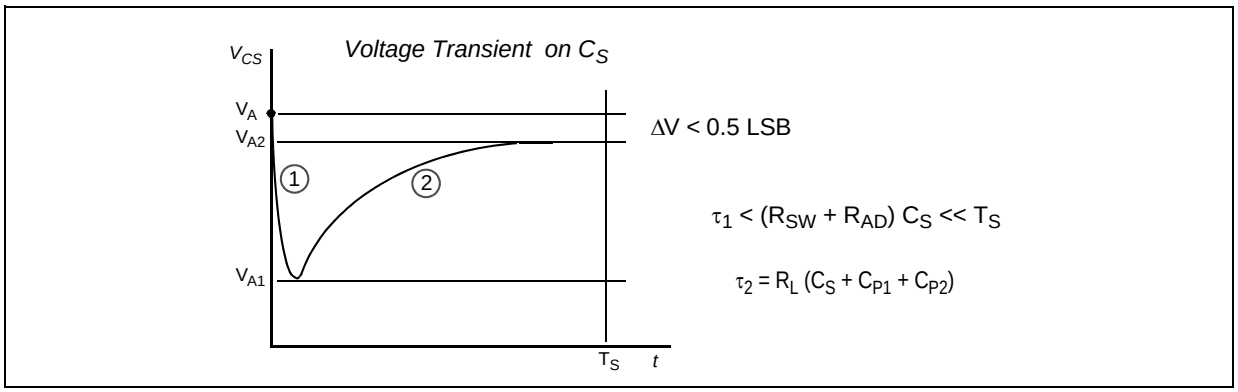


Figure 11. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is:

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 12}$$

  Equation 12 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S \qquad \textit{Eqn. 13}$$

  The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 14:

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2}) \qquad \textit{Eqn. 14}$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2}) \qquad \textit{Eqn. 15}$$

  In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S \qquad \textit{Eqn. 16}$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 17 must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S) \qquad \textit{Eqn. 17}$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

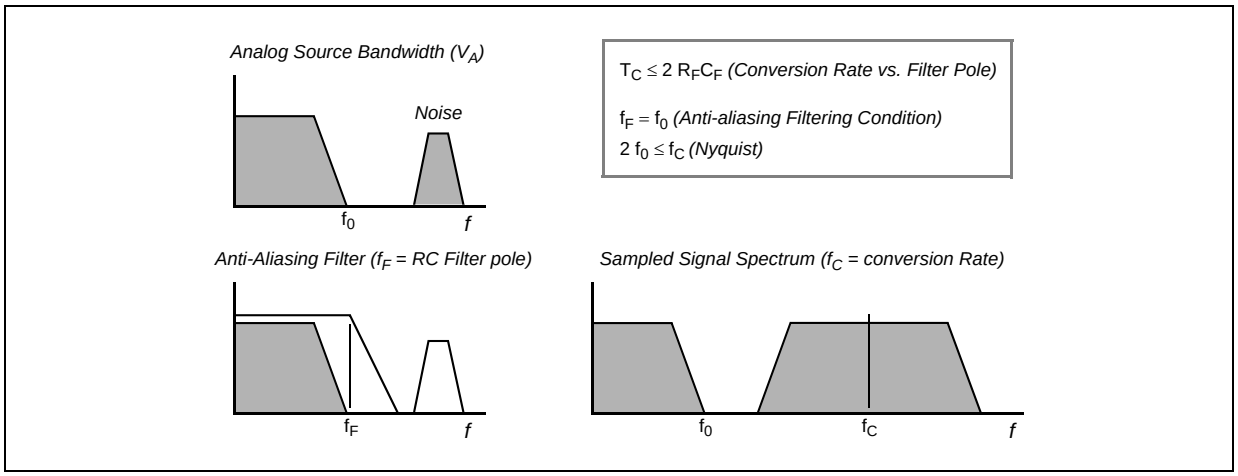


Figure 18. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 19 between the ideal and real sampled voltage on C_S:

Eqn. 19

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

$$C_F > 8192 \bullet C_S \qquad \textit{Eqn. 20}$$

Table 24. ADC conversion characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	f_{CK}	SR	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
2	f_s	SR	Sampling frequency	—	—	—	959	kHz
3	t_{ADC_S}	D	Sample time[3]	60 MHz	383	—	—	ns
4	t_{ADC_E}	P	Evaluation time[4]	TBD	600	—	—	ns
5	C_S[5]	D	ADC input sampling capacitance	—	—	—	7.32	pF
6	C_{P1}[5]	D	ADC input pin capacitance 1	—	—	—	2.5	pF
7	C_{P2}[5]	D	ADC input pin capacitance 2	—	—	—	TBD	pF
8	R_{SW1}[5]	D	Channel selection switch resistance	V_{REF} range = 4.5 to 5.5 V	—	—	1.0	kΩ
9				V_{REF} range = 3.0 to 3.6 V	—	—	1.2	kΩ
10	R_{AD}[5]	D	Sample switching resistance	—	—	—	825	Ω
11	I_{INJ}	T	Current injection	Current injection on one ADC input channel, different from the converted one. Other parameters stay within specified limits as long as the ADC supply stays within its specified limits due to the current injection.	–3	—	3	mA
12	INL	P	Integral non linearity	—	–3	—	3	LSB
13	DNL	P	Differential non linearity[6]	—	–1.0	—	1.0	LSB
14	OFS	T	Offset error	—	–4	—	4	LSB
15	GNE	T	Gain error	—	–4	—	4	LSB
16	TUE	P	Total unadjusted error	—	–6	—	6	LSB
17	TUE	T	Total unadjusted error with current injection	—	TBD	—	TBD	LSB
18	SNR	T	Signal-to-noise ratio	—	69	—	—	dB
19	THD	T	Total harmonic distortion	—	TBD	—	—	dB
20	SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
21	ENOB	T	Effective number of bits	—	10.5	—	—	bits

NOTES:
1 V_{DD} = 3.3 V, T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}
2 AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

4 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.

5 See Figure 10.

6 No missing codes.

3.15 Flash memory electrical characteristics

3.15.1 Program/Erase characteristics

Table 25 shows the Code flash memory program and erase characteristics.

Table 25. Code flash program and erase electrical specifications

No.	Symbol		Parameter	Min	Typ[1]	Initial Max[2]	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	CC	Double Word (64 bits) program time[4]	—	18	50	500	µs
3	$T_{16KPPERASE}$	CC	16 KB block pre-program and erase time	—	200	500	5000	ms
4	$T_{32KPPERASE}$	CC	32 KB block pre-program and erase time	—	300	600	5000	ms
5	$T_{64KPPERASE}$	CC	64 KB block pre-program and erase time	—	400	900	5000	ms
6	$T_{128KPPERASE}$	CC	128 KB block pre-program and erase time	—	600	1300	7500	ms

NOTES:
1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are verified at production test.
3 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.
4 Actual hardware programming times. This does not include software overhead.

Table 26 shows the Data flash memory program and erase characteristics.

Table 26. Data flash program and erase electrical specifications

No.	Symbol		Parameter	Min	Typ[1]	Initial Max[2]	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	CC	Double Word (64 bits) program time[4]	—	30	70	300	µs
3	$T_{16KPPERASE}$	CC	16 KB block pre-program and erase time	—	700	800	1500	ms

NOTES:
1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are verified at production test.
3 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.
4 Actual hardware programming times. This does not include software overhead.

Table 27. Flash module life

No.	Symbol		Parameter	Condition	Value			Unit
					Min	Typ[1]	Max	
1a	P/E	CC	Number of program/erase cycles per block for over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
1b				32 KB and 64 KB blocks	10,000	100,000	—	cycles
1c				128 KB blocks	1,000	100,000	—	cycles
2	Retention	CC	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

NOTES:
1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*
2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.15.2 Read access timing

Table 28. Code flash read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
2	f_{READ}	CC	Maximum frequency for Flash reading (system clock frequency SYS_CLK)	4 wait states	90	MHz
3				3 wait states	60	MHz

Table 29. Data flash read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
2	f_{READ}	CC	Maximum frequency for Flash reading (system clock frequency SYS_CLK)	12 wait states	90	MHz
3				8 wait states	60	MHz

3.15.3 Write access timing

Table 30. Code flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
2	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	TBD	90	MHz
3				TBD	60	MHz

Table 31. Data flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
2	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	TBD	90	MHz
3				TBD	60	MHz

3.16 SRAM memory electrical characteristics

3.16.1 Read access timing

Table 32. System SRAM memory read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
2	s_{READ}	CC	Maximum frequency for system SRAM reading (system clock frequency SYS_CLK)	1 wait state	90	MHz
3				1 wait state	60	MHz

3.16.2 Write access timing

Table 33. System SRAM memory write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
2	s_{WRITE}	CC	Maximum frequency for system SRAM writing (system clock frequency SYS_CLK)	TBD	90	MHz
3				TBD	60	MHz

3.17 GP pads specifications

This section specifies the electrical characteristics of the GP pads. Please refer to the tables in Section 2.2, Pin descriptions," for a cross reference between package pins and pad types.

3.17.1 GP pads DC specifications

Table 34 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V).

Table 34. GP pads DC electrical characteristics[1,2]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	V_{IL}	SR	Low level input voltage	—	–0.1[3]	0.35 $V_{DD\_HV\_IO}$	V
2	V_{IH}	SR	High level input voltage	—	0.65 $V_{DD\_HV\_IO}$	$V_{DD\_HV\_IO}$ + 0.1[3]	V
3	V_{HYS}	CC	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	V
4	V_{OL_S}	CC	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
5	V_{OH_S}	CC	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IO}$ – 0.8	—	V
6	V_{OL_M}	CC	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
7	V_{OH_M}	CC	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IO}$ – 0.8	—	V
8	V_{OL_F}	CC	Fast, high level output voltage	I_{OL} = 11 mA	—	0.5	V
9	V_{OH_F}	CC	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IO}$ – 0.8	—	V
10	V_{OL_SYM}	CC	Symmetric, high level output voltage	I_{OL} = 5 mA	—	0.5	V
11	V_{OH_SYM}	CC	Symmetric, high level output voltage	I_{OH} = –5 mA	$V_{DD\_HV\_IO}$ – 0.8	—	V
12	I_{PU}	CC	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
				V_{IN} = V_{IH}	—	–10	
13	I_{PD}	CC	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
				V_{IN} = V_{IH}	—	130	
14	I_{IL}	CC	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
15	I_{IL}	CC	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
16	V_{ILR}	SR	$\overline{\text{RESET}}$, low level input voltage	—	–0.4[3]	0.35 $V_{DD\_HV\_IO}$	V
17	V_{IHR}	SR	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IO}$	$V_{DD\_HV\_IO}$+0.4[3]	V
18	V_{HYSR}	CC	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	V
19	V_{OLR}	CC	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	0.5	V
20	I_{PD}	CC	$\overline{\text{RESET}}$, equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
				V_{IN} = V_{IH}	—	130	

NOTES:
1 These specifications are design targets and subject to change per device characterization.
2 The values provided in this table are not applicable for PDI and EBI/DRAM interface.
3 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 11.

3.17.2 GP pads AC specifications

Table 35. GP pads AC electrical characteristics[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	7	—	40	50
		1	—	6	3	—	12	—	—	40	7	—	40	100
		1	—	6	5	—	18	—	—	25	7	—	40	200
4	Symmetric	1	—	8	1	—	5	—	—	50	3	—	25	25
5	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

NOTES:
1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.
2 Slope at rising/falling edge.
3 Data based on characterization results, not tested in production.

3.18 PDI pads specifications

This section specifies the electrical characteristics of the PDI pads. Please refer to the tables in Section 2.2, Pin descriptions," for a cross reference between package pins and pad types.

PDI pads feature list:

- Direction
  - — Input
  - — Output
  - — Bidirectional
- Driver
  - — Push/Pull/Open Drain
  - — Configurable Four Drive Strengths on Fast driver pads

— Configurable No Slew-Rate, Slow Slew-Rate, and Fast Slew-Rate on Slow, Medium, and SLR driver pads

— VDD_HV_PDI NOTE: All pads are NOT 5 V TOLERANT. Pads are not capable of driving to or from voltages above their respective VDD_HV_PDI. In other words, you cannot connect a 3.3V external device to a pad supplied with 2.5 V. If a pad must be connected to a 3.3V device, its local VDD_HV_PDI must be 3.3 V. Injection current is then handled by the intrinsic diodes from the pad transistors and by the ESD diodes.

— VDD_HV_PDI range

– 1.8 V nominal

– 2.5 V nominal

– 3.3 V nominal

- Receiver
  - — Selectable hysteresis Input Buffer.
  - — CMOS Input Buffer

The electrical data provided in Section 3.18, PDI pads specifications," applies to the pads listed in Table 36.

Table 36. PDI I/O pads

No.	Name	Volt.	Used For	Notes
1	PDI Fast	1.62 V-3.6 V	I/O	Enhanced operating voltage range fast slew-rate output with four selectable slew-rates. Contains an input buffer and weak pullup/pulldown.
2	PDI Medium	1.62 V-3.6 V	I/O	Enhanced operating voltage range medium slew-rate output with four selectable slew-rates. Contains an input buffer and weak pullup/pulldown.

3.18.1 PDI pads electrical specifications ($V_{DD\_HV\_PDI}$ = 3.3 V)

Table 37. PDI pads DC electrical characteristics ($V_{DD\_HV\_PDI}$ = 3.3 V)

No.	Symbol		Parameter	Min	Max	Unit
1	$V_{DD\_HV\_PDI}$	SR	I/O supply voltage	3.0	3.6	V
2	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis enabled)	0.65 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V
3	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis disabled)	0.51 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V
4	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis enabled)	V_{SS} – 0.3	0.35 × $V_{DD\_HV\_PDI}$	V
5	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis disabled)	V_{SS} – 0.3	0.42 × $V_{DD\_HV\_PDI}$	V
6	V_{HYS_C}	CC	CMOS input buffer hysteresis	0.1 × $V_{DD\_HV\_PDI}$		V
7	I_{ACT_S}	CC	Selectable weak pullup/pulldown current[3]	25	150	µA
9	V_{OH}	CC	Output high voltage	0.8 × $V_{DD\_HV\_PDI}$	—	V
10	V_{OL}	CC	Output low voltage	—	0.2 × $V_{DD\_HV\_PDI}$	V

Table 38. Drive Current, $V_{DD\_HV\_PDI}$ = 3.3 V (±10%)

Pad	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
PDI Fast	All	84.4	137
PDI Medium	All	61.9	83.6

NOTES:
1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 39. PDI pads AC electrical characteristics ($V_{DD\_HV\_PDI}$ = 3.3 V)

No.	Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	PDI Medium	—	4.0/4.5	—	1.02/1.4	50	11
			7.3/8.3		3.5/4.2	200	
			24/22		9.1/10.3	50	10
			33/31		14/15	200	
			49/44		18/21	50	01
			60/53		24/25	200	
			332/302		126/151	50	00
			362/325		136/158	200	
2	PDI Fast	—	5/5	—	1.1/1.1	50	11
			8/8		2.6/2.6	200	
			8/8		2.4/2.4	50	10
			12/12		5/5	200	
			13/13		5/5	50	01
			19/19		8/8	200	
			40/40		16/16	50	00
			50/50		21/21	200	

NOTES:
1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.18.2 PDI pads electrical specifications ($V_{DD\_HV\_PDI}$ = 2.5 V)

Table 40. PDI pads DC electrical specifications ($V_{DD\_HV\_PDI}$ = 2.5 V)

No.	Symbol		Parameter	Min	Max	Unit
1	$V_{DD\_HV\_PDI}$	SR	I/O supply voltage	2.3	2.7	V
2	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis enabled)	0.65 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V

Table 40. PDI pads DC electrical specifications ($V_{DD\_HV\_PDI}$ = 2.5 V) (continued)

No.	Symbol		Parameter	Min	Max	Unit
3	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis disabled)	0.54 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V
4	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis enabled)	Vss – 0.3	0.35 × $V_{DD\_HV\_PDI}$	V
5	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis disabled)	Vss – 0.3	0.42 × $V_{DD\_HV\_PDI}$	V
6	V_{HYS_C}	CC	CMOS input buffer hysteresis	0.1 × $V_{DD\_HV\_PDI}$		V
7	I_{ACT_S}	CC	Selectable weak pullup/pulldown current[1]	25	150	µA
9	V_{OH}	CC	Output high voltage	0.8 × $V_{DD\_HV\_PDI}$	—	V
10	V_{OL}	CC	Output low voltage	—	0.2 × $V_{DD\_HV\_PDI}$	V

Table 41. Drive Current @ $V_{DD\_HV\_PDI}$ = 2.5 V (±10%)

Pad	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
PDI Fast	All	51.5	111
PDI Medium	All	52.6	78.1

NOTES:
1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}. PDI

Table 42. PDI pads AC electrical specifications ($V_{DD\_HV\_PDI}$ = 2.5 V)

No.	Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	PDI Medium	0.8/0.7 -------- 1.1/1.08	4.5/4	1.3/1	—	50	11
			9/7	4.8/3.2		200	
			34/19	10.5/7.9		50	10
			44/26	16.3/12		200	
			70/38	21/16		50	01
			83/45	28/20		200	
			491/254	142/115		50	00
			528/279	154/122		200	

Table 42. PDI pads AC electrical specifications ($V_{DD\_HV\_PDI}$ = 2.5 V) (continued)

No.	Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
2	PDI Fast	0.8/0.7 -------- 1.1/1.08	5/5	1.5/1.5	—	50	11
			8.4/8.4	3.5/3.5		200	
			8.6/8.6	3/3		50	10
			14/14	5.6/5.6		200	
			15.5/15.5	5.7/5.7		50	01
			22/22	9.5/9.5		200	
			48/48	19/19		50	00
			60/60	25/25		200	

NOTES:
1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.18.3 PDI pads electrical specifications ($V_{DD\_HV\_PDI}$ = 1.8 V)

Table 43. PDI pads DC electrical specifications ($V_{DD\_HV\_PDI}$ = 1.8 V)

No.	Symbol		Parameter	Min	Max	Unit
1	$V_{DD\_HV\_PDI}$	SR	I/O supply voltage	1.62	1.98	V
2	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis enabled)	0.65 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V
3	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis disabled)	0.58 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V
4	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis enabled)	Vss – 0.3	0.35 × $V_{DD\_HV\_PDI}$	V
5	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis disabled)	Vss – 0.3	0.44 × $V_{DD\_HV\_PDI}$	V
6	V_{HYS_C}	CC	CMOS input buffer hysteresis	0.1 × $V_{DD\_HV\_PDI}$	—	V
7	I_{ACT_S}	CC	Selectable weak pullup/pulldown current[1]	25	150	µA
9	V_{OH}	CC	Output high voltage	0.8 × $V_{DD\_HV\_PDI}$	—	V
10	V_{OL}	CC	Output low voltage	—	0.2 × $V_{DD\_HV\_PDI}$	V

Table 44. Drive current @ $V_{DD\_HV\_PDI}$ = 1.8 V (±10%)

Pad	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
PDI Fast	All	26.2	84.8
PDI Medium	All	19.2	52.1

NOTES:
1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 45. PDI pads AC electrical specifications ($V_{DD\_HV\_PDI}$ = 1.8 V)

No.	Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	PDI Medium	—	5.5/3.5	2/1	—	50	11
			12/5.5	7.2/2.3		200	
			49/17	13/6		50	10
			60/23	21/9.2		200	
			102/32	26/12		50	01
			119/39	35/16		200	
			722/216	172/85		50	00
			772/237	191/90		200	
2	PDI Fast	—	10/10	2/2	—	50	11
			15/15	6.2/6.2		200	
			15/15	4.5/4.5		50	10
			22/22	7.1/7.1		200	
			24/24	7.5/7.5		50	01
			33/33	12/12		200	
			66/66	24/24		50	00
			84/84	31/31		200	

NOTES:
1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19 DRAM pad specifications

This section specifies the electrical characteristics of the DRAM pads. Please refer to the tables in Section 2.2, Pin descriptions," for a cross reference between package pins and pad types.

DRAM pads feature list:

- Driver
  - Configurable to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR modes.
  - VDD_HV_DRAM Range of
    - 1.8 V nominal
    - 2.5 V nominal
    - 3.3 V nominal
- Receiver
  - Differential or pseudo-differential input buffer in all DRAM pads

— All inputs are tolerant up to their VDD_HV_DRAM Absolute Maximum Rating
— Data and strobe pads can be configured to support four signal termination options
  – Infinite/no termination
  – 50 Ohms
  – 75 Ohms
  – 150 Ohms

The electrical data provided in Section 3.19, DRAM pad specifications," applies to the pads listed in Table 46.

Table 46. DRAM pads

Name	Voltage	Used For	Notes[1]
DRAM ACC	1.62 V–3.6 V	I/O	Bidirectional DDR pad
DRAM CLK	1.62 V–3.6 V	O	Output only differential clock driver pad
DRAM DQ	1.62 V–3.6 V	I/O	Bidirectional DDR pad with integrated ODT

NOTES:
1 All pads can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.

All three pad types can be configured to support SDR, DDR, DDR2 half and full strength, and LPDDR half and full strength modes, according to Table 47.

Table 47. Mode configuration for DRAM pads

Configuration[1]	Mode
000	1.8 V LPDDR Half Strength
001	1.8 V LPDDR Full Strength
010	1.8 V DDR2 Half Strength
011	2.5 V DDR
100	Not supported
101	Not supported
110	1.8 V DDR2 Full Strength
111	SDR

NOTES:
1 Configuration is selected in the corresponding PCR registers of the SIUL.

3.19.1 DRAM pads electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

Table 48. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	3.0	3.6	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	1.3	1.7	V

Table 48. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ (continued) = 3.3 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ × 0.05	$V_{DD\_HV\_DRAM\_VREF}$ + 0.05	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.20	—	V
5	V_{IL}	CC	Input low voltage	—		$V_{DD\_HV\_DRAM\_VREF}$ × 0.2	V
6	V_{OH}	CC	Output high voltage	ODT enabled[2]	$V_{DD\_HV\_DRAM\_VTT}$ + 0.8	—	V
				ODT disabled[3]	0.8 × $V_{DD\_HV\_DRAM}$	—	V
7	V_{OL}	CC	Output low voltage	ODT enabled[2]	—	$V_{DD\_HV\_DRAM\_VTT}$ × 0.8	V
				ODT disabled[3]	—	$V_{DD\_HV\_DRAM}$ × 0.2	V

NOTES:
1. BGA473: Termination voltage can be supplied via package pins. BGA257 Termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT
2. Termination voltage is supplied by $V_{DD\_HV\_DRAM\_VTT}$.
3. Tie $V_{DD\_HV\_DRAM\_VTT}$ to V_{SS} and disable ODT

Table 49. Output drive current @ V_{DDE} = 3.3 V (±10%)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	111	–16	16
2	DRAM DQ			
3	DRAM CLK			

NOTES:
1. I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2. I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 50. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Output Slew rate Rise/Fall (V/ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
2	DRAM DQ	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
3	DRAM CLK	1.4/1.4	2.4/2.4	3.1/2.5	5.7/5.7	5	111
		1.6/1.6	2.6/2.6	1.1/1.3	2.3/2.3	20	111

NOTES:
1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19.2 DRAM pads electrical specification ($V_{DD\_HV\_DRAM}$ = 2.5 V)

Table 51. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 2.5 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	2.3	2.7	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	0.49 × $V_{DD\_HV\_DRAM}$	0.51 × $V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ - 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.15	—	V
5	V_{IL}	CC	Input low voltage	—	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.15	V
6	V_{OH}	CC	Output high voltage	ODT enabled[2]	$V_{DD\_HV\_DRAM\_VTT}$ + 0.81	—	V
				ODT disabled[3]	0.8 × $V_{DD\_HV\_DRAM}$	—	V
7	V_{OL}	CC	Output low voltage	ODT enabled[2]	—	$V_{DD\_HV\_DRAM\_VTT}$ – 0.81	V
				ODT disabled[3]	—	0.2 × $V_{DD\_HV\_DRAM}$	V

NOTES:
1 473 MAPBGA: Termination voltage can be supplied via package pins. 257 MAPBGA Termination voltage internally tied as the 257 MAPBGA does not provide DRAM interface. Disable ODT
2 Termination voltage is supplied by VDD_HV_DRAM_VTT.
3 Tie $V_{DD\_HV\_DRAM\_VTT}$ to V_{SS} and disable ODT

Table 52. Output drive current @ V_{DDE} = 2.5 V (±200 mV)

Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
DRAM ACC	011	–16.2	16.2
DRAM DQ	011		
DRAM CLK	011		

NOTES:
1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 53. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 2.5 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.5	2.5/2.4	2.1/2.1	4.3/4.1	5	011
		1.7/1.7	2.8/2.7	0.6/0.7	1.1/1.3	20	
2	DRAM DQ	1.4/1.5	2.5/2.4	2.1/2.1	4.3/4.1	5	011
		1.7/1.7	2.8/2.7	0.6/0.7	1.1/1.3	20	
3	DRAM CLK	1.4/1.4	2.4/2.4	2.1/2.1	4.4/4.1	5	011
		1.6/1.6	2.7/2.7	0.6/0.7	1.6/1.8	20	

NOTES:
1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19.3 DRAM pads electrical specification ($V_{DD\_HV\_DRAM}$ = 1.8 V)

Table 54. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	1.7	1.9	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	0.49 × $V_{DD\_HV\_DRAM}$	0.51 × $V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.125	—	V
5	V_{IL}	CC	Input low voltage	—	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.125	V
6	V_{OH}	CC	Output high voltage	ODT enabled[2]	$V_{DD\_HV\_DRAM\_VTT}$ + 0.81	—	V
				ODT disabled[3]	0.8 × $V_{DD\_HV\_DRAM}$	—	V
7	V_{OL}	CC	Output low voltage	ODT enabled[2]	—	$V_{DD\_HV\_DRAM\_VTT}$ – 0.81	V
				ODT disabled[3]	—	0.2 × $V_{DD\_HV\_DRAM}$	V

NOTES:
1 BGA473: Termination voltage can be supplied via package pins. BGA257 Termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT
2 Termination voltage is supplied by VDD_HV_DRAM_VTT.
3 Tie $V_{DD\_HV\_DRAM\_VTT}$ to V_{SS} and disable ODT

Table 55. Output drive current @ V_{DDE} = 1.8 V (±100 mV)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
2	DRAM DQ	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
3	DRAM CLK	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4

NOTES:
1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 56. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	

Table 56. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ (continued) = 1.8 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
2	DRAM DQ	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	
3	DRAM CLK	1.4/1.4	2.4/2.4	0.4/0.6	2.7/2.7	5	000
		1.6/1.6	2.7/2.7	0.7/0.9	1.8/3.4	20	
		1.4/1.4	2.4/2.4	1.1/1.1	3.0/2.8	5	001
		1.7/1.7	2.7/2.7	0.3/0.4	1.0/1.1	20	
		1.4/1.4	2.4/2.4	0.9/1.1	3.0/2.8	5	010
		1.6/1.6	2.7/2.7	0.3/0.4	0.9/1.0	20	
		1.4/1.4	2.5/2.5	1.5/1.2	3.2/2.6	5	110
		1.7/1.7	2.7/2.7	0.4/0.4	1.1/1.2	20	

NOTES:
1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.20 $\overline{\text{RESET}}$ characteristics

3.20.1 $\overline{\text{RESET}}$ pin characteristics

Table 57. $\overline{\text{RESET}}$ pin characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	W_{FRST}	SR	$\overline{\text{RESET}}$ pulse is sure to be filtered	—	—	70	ns
2	W_{NFRST}	SR	$\overline{\text{RESET}}$ pulse is sure not to be filtered	—	400	—	ns

3.21 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences depending on internal or external VREG mode.

3.21.1 Reset sequence duration

Table 58 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Section 3.21.2, Reset sequence description."

Table 58. RESET sequences

No.	Symbol		Parameter	T_{Reset}			Unit
				Min	Typ	Max[1]	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled	60	65	70	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	40	400	1000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled	60	65	70	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	40	300	600	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	1	3	10	µs

NOTES:
1 The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

3.21.2 Reset sequence description

The figures in this section show the internal states of the PXS30 during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 58. The start point and end point conditions as well as the reset trigger mapping to the different reset sequences is specified in Section 3.21.3, Reset sequence trigger mapping."

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the PXS30 during the execution of the reset sequence and the possible states of the $\overline{\text{RESET}}$ signal pin.

NOTE

$\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the PXS30 internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 58 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

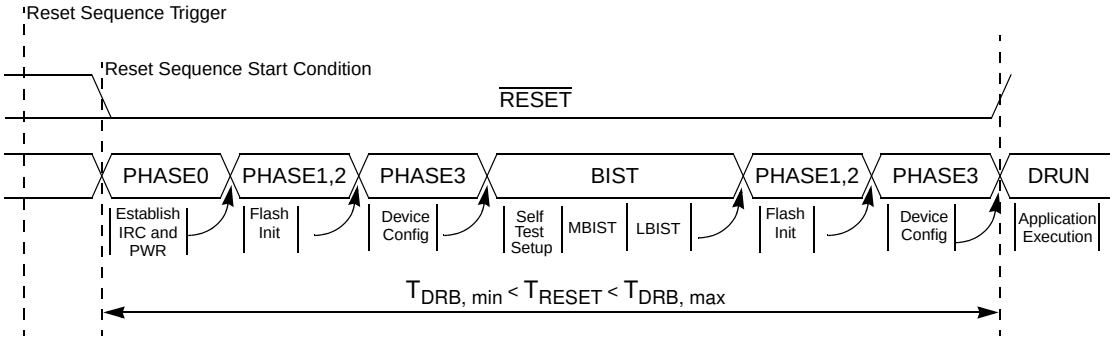


Figure 21. Destructive reset sequence, BIST enabled

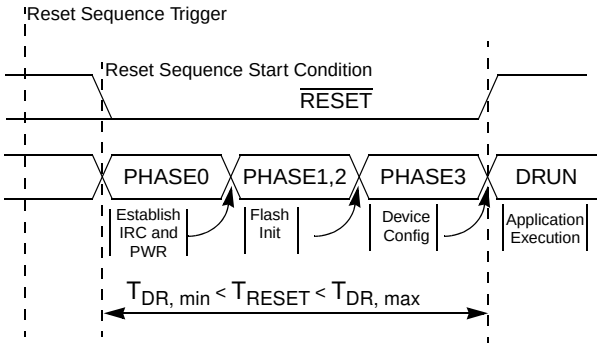


Figure 22. Destructive reset sequence, BIST disabled

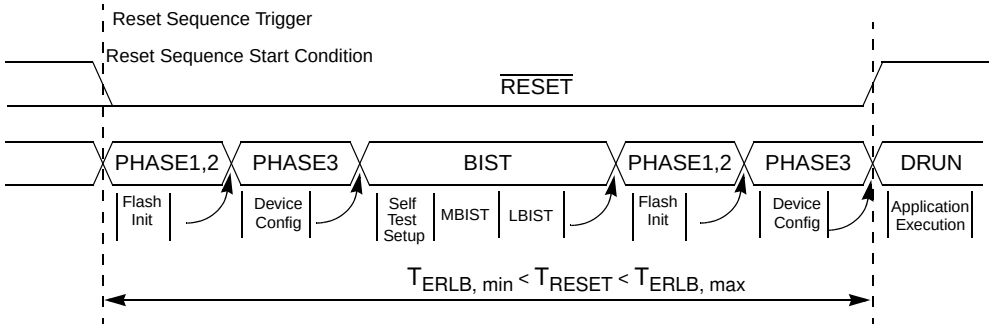


Figure 23. External reset sequence long, BIST enabled

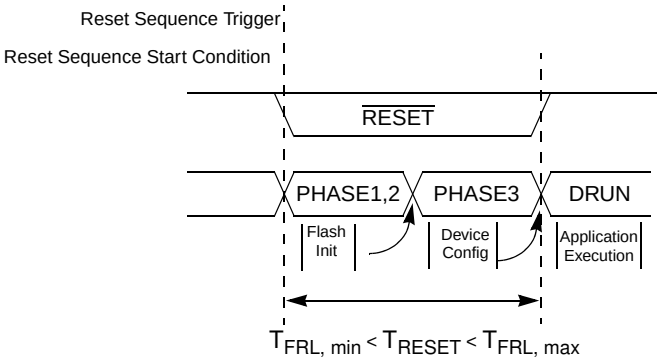


Figure 24. Functional reset sequence long

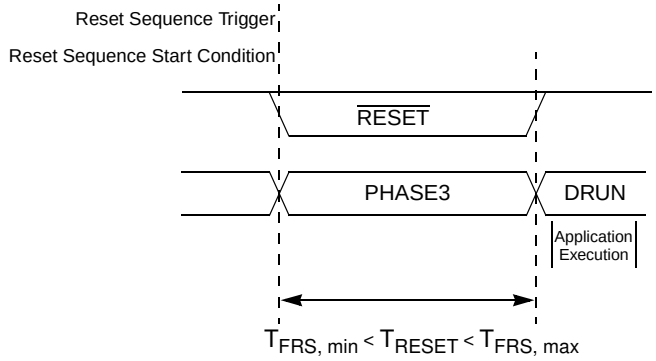


Figure 25. Functional reset sequence short

The reset sequences shown in Figure 24 and Figure 25 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence. See the RGM_FBRE register in the *PXS30 Reference Manual (PXS30RM)* for more information.

3.21.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences, depending on the VREG mode (external or internal). It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 58.

Table 59. Reset sequence trigger—reset sequence

Reset Sequence Trigger	VREG Mode[1]	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
				Destructive Reset Sequence, BIST enabled[2]	*Destructive Reset Sequence, BIST disabled*[2]	*External Reset Sequence Long, BIST enabled*	*Functional Reset Sequence Long*	*Functional Reset Sequence Short*
All active internal destructive reset sources (LVDs or internal HVD during power-up and during operation)	I	Section 3.21.4.1, Internal VREG mode"	Release of $\overline{\text{RESET}}$[3]	triggers		cannot trigger	cannot trigger	cannot trigger
	E	Section 3.21.4.2, External VREG mode"				cannot trigger	cannot trigger	cannot trigger
Assertion of $\overline{\text{RESET}}$_SUP[4]								
Assertion of $\overline{\text{RESET}}$[5]	I/E	Section 3.21.4.3, external Reset via RESET"		cannot trigger		triggers[6]	triggers[7]	triggers[8]
All internal functional reset sources configured for long reset	I/E	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$[9]	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset	I/E			cannot trigger		cannot trigger	cannot trigger	triggers

NOTES:
1 VREG Mode: I = Internal VREG Mode, E = External VREG Mode.

2 Whether BIST is executed or not depends on device configuration data stored in the shadow sector of the NVM.

3 End of the internal reset sequence (as specified in Table 58) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 until $\overline{\text{RESET}}$ is released externally.

4 In external VREG mode only.

5 The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).

6 If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is enabled via device configuration data stored in the shadow sector of the NVM.

7 If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is disabled via device configuration data stored in the shadow sector of the NVM.

8 If $\overline{\text{RESET}}$ is configured for short reset.

9 Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.21.4 Reset sequence—start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.21.4.1 Internal VREG mode

Figure 26 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*. The last voltage rail crossing the levels shown in Figure 26 determines the start of the reset times specified in Table 58.

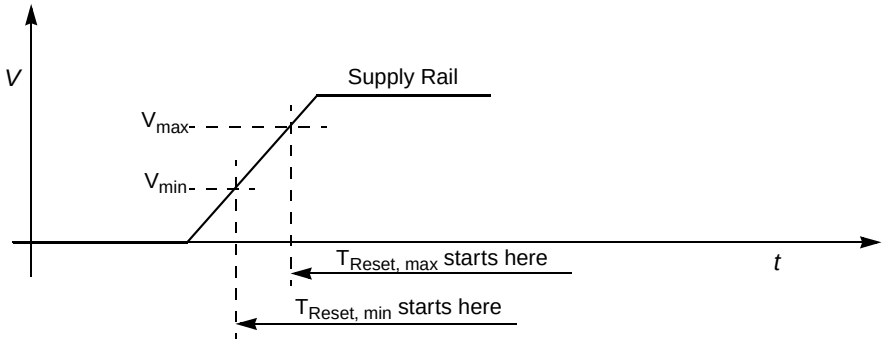


Figure 26. Reset sequence start in internal VREG mode

Table 60. Voltage thresholds

Variable name	Value
V_{min}	LvdReg – 3.5%
V_{max}	LvdReg + 3.5%
Supply Rail	VDD_HV_PMU VDD_HV_IO VDD_HV_FLASH VDD_HV_ADV

3.21.4.2 External VREG mode

Figure 27 and Figure 28 show the voltage thresholds that determine the start of the Destructive Reset Sequence, BIST enabled and the start for the Destructive Reset Sequence, BIST disabled.

NOTE

$\overline{\text{RESET\_SUP}}$ must not be released unless $V_{DD\_LV\_xxx}$ is within its valid range of operation.

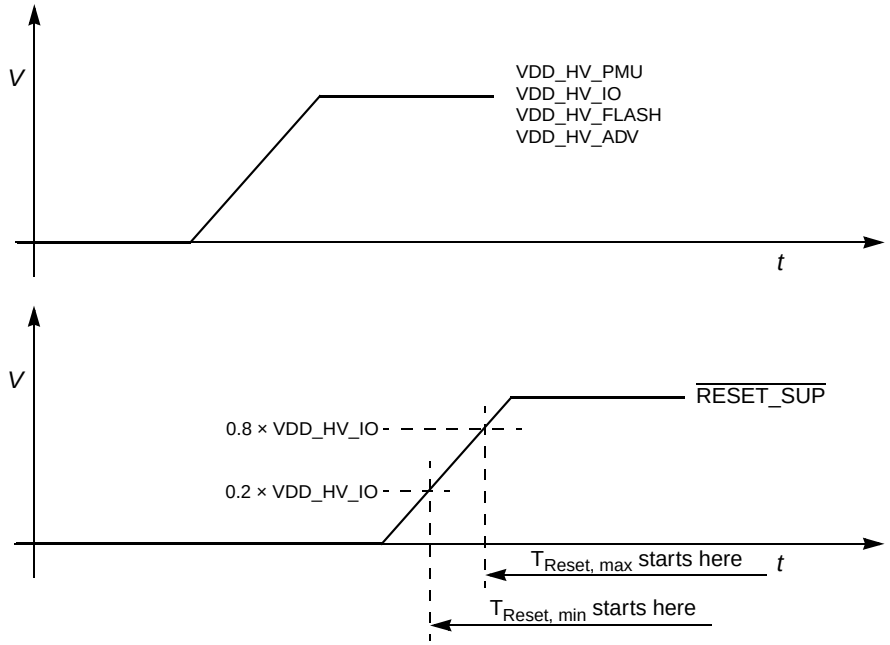


Figure 27. External VREG mode, $\overline{\text{RESET\_SUP}}$ rises after $V_{DD\_HV\_xxx}$ are stable

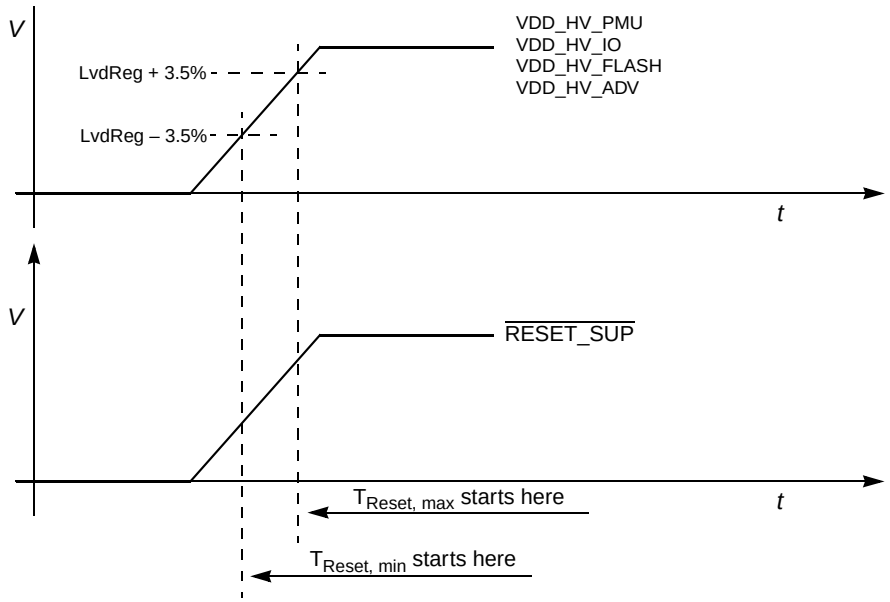


Figure 28. External VREG mode, $\overline{\text{RESET\_SUP}}$ rises with $V_{DD\_HV\_xxx}$

NOTE

In case $\overline{\text{RESET\_SUP}}$ has reached a valid high level before $V_{DD\_HV\_IO}$ is stable, the reset sequence will start as documented in Figure 28 as the $\overline{\text{RESET\_SUP}}$ input circuitry needs a valid $V_{DD\_HV\_IO}$ rail in order to detect a high level on $\overline{\text{RESET\_SUP}}$.

3.21.4.3 external Reset via $\overline{\text{RESET}}$

Figure 29 shows the voltage thresholds that determine the start of the reset sequences initiated by the assertion of $\overline{\text{RESET}}$ as specified in Table 59.

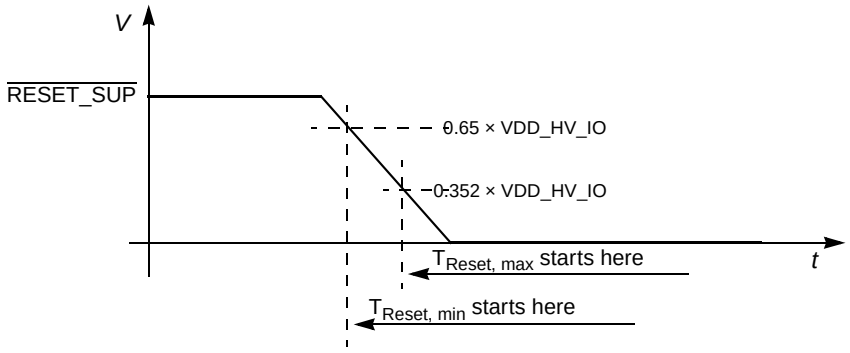


Figure 29. Reset sequence start via $\overline{\text{RESET}}$ assertion

3.21.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in Section 3.21, Reset sequence can be used to determine the correct positioning of the trigger window for the external watchdog. Figure 30 shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

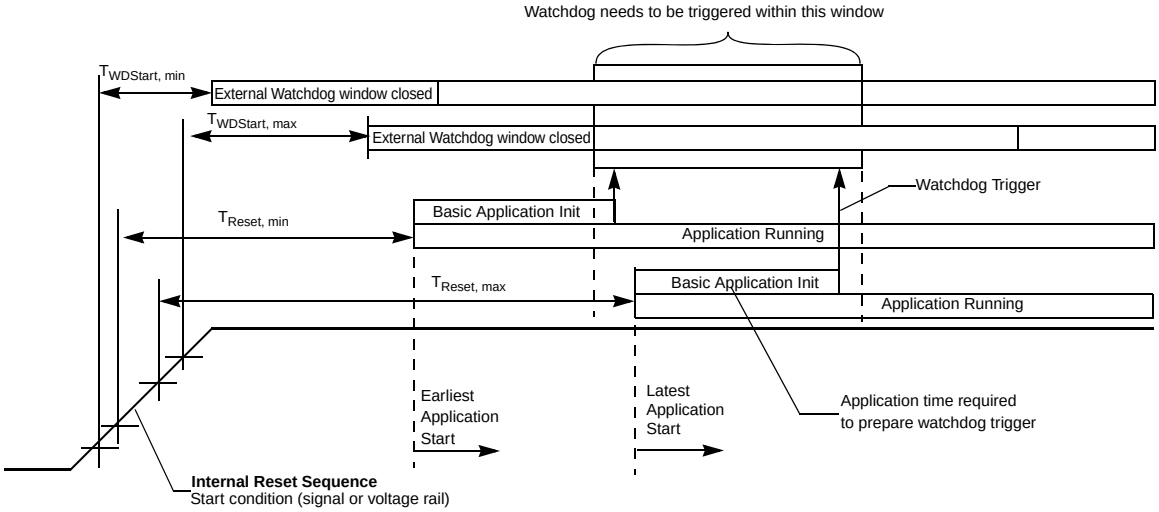


Figure 30. Reset sequence—external watchdog trigger window position

3.22 Peripheral timing characteristics

3.22.1 SDRAM (DDR)

The PXS30 memory controller supports three types of DDR devices:

- DDR-1 (SSTL_2 class II interface)
- DDR-2 (SSTL_18 interface)
- LPDDR/Mobile-DDR (1.8V I/O supply voltage)

JEDEC standards define the minimum set of requirements for compliant memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, MAY 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The PXS30 supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strength (intended for lighter loads or point-to-point environments)

The PXS30 memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the Section 3.19, DRAM pad specifications."

3.22.1.1 DDR and DDR2 SDRAM AC timing specifications

Table 61. DDR and DDR2 (DDR2-400) SDRAM timing specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

No.	Symbol		Parameter	Min	Max	Unit
1	t_{CK}	CC	Clock cycle time, CL = *x*	—	90	MHz
2	V_{IX-AC}	CC	MCK AC differential crosspoint voltage[1]	$V_{DD\_MEM\_IO}$ × 0.5 – 0.1	$V_{DD\_MEM\_IO}$ × 0.5 + 0.1	V
3	t_{CH}	CC	CK HIGH pulse width[1, 2]	0.47	0.53	t_{CK}
4	t_{CL}	CC	CK LOW pulse width[1, 2]	0.47	0.53	t_{CK}
5	t_{DQSS}	CC	Skew between MCK and DQS transitions[2, 3]	–0.25	0.25	t_{CK}
8	$t_{OS(base)}$	CC	Address and control output setup time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)		ps
9	$t_{OH(base)}$	CC	Address and control output hold time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)	—	ps
11	$t_{DS1(base)}$	CC	DQ and DM output setup time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
12	$t_{DH1(base)}$	CC	DQ and DM output hold time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps

Table 61. DDR and DDR2 (DDR2-400) SDRAM timing specifications (continued)

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

No.	Symbol		Parameter	Min	Max	Unit
14	t_{DQSQ}	CC	DQS-DQ skew for DQS and associated DQ inputs[2]	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps
15	t_{DQSEN}	CC	DQS window start position related to CAS read command[1, 2, 3, 4, 5]	TBD	TBD	ps

NOTES:
1. Measured with clock pin loaded with differential 100 ohm termination resistor.
2. All transitions measured at mid-supply ($V_{DD\_MEM\_IO}$/2).
3. Measured with all outputs except the clock loaded with 50 ohm termination resistor to $V_{DD\_MEM\_IO}$/2.
4. In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.
5. Window position is given for t_{DQSEN} = 2.0 t_{CK}. For other values of t_{DQSEN}, window position is shifted accordingly.

Figure 31 shows the DDR SDRAM write timing.

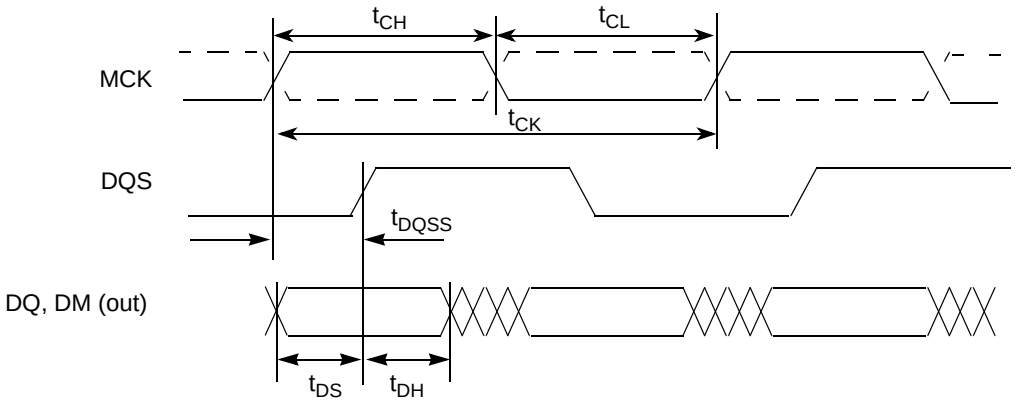


Figure 31. DDR write timing

Figure 32 and Figure 33 show the DDR SDRAM read timing.

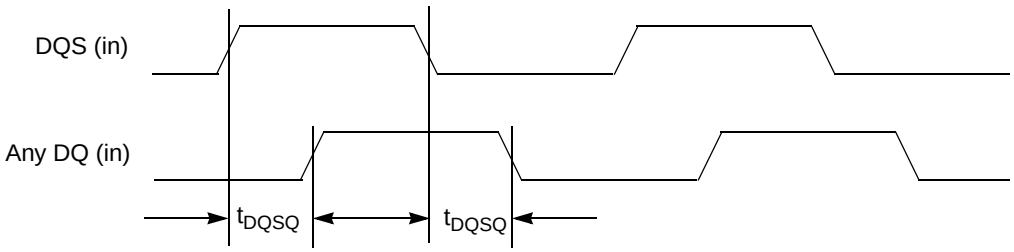


Figure 32. DDR read timing, DQ vs. DQS

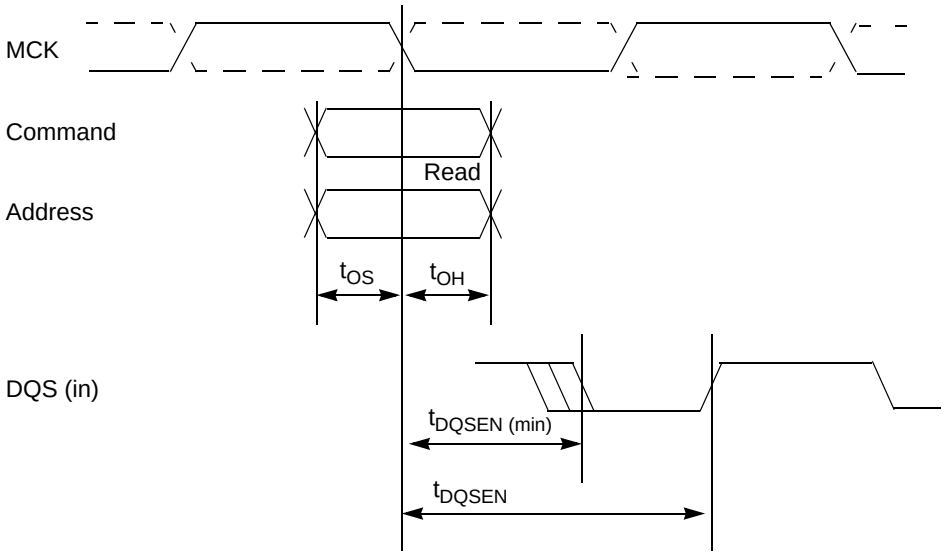


Figure 33. DDR read timing, DQSEN

Figure 34 provides the AC test load for the DDR bus.

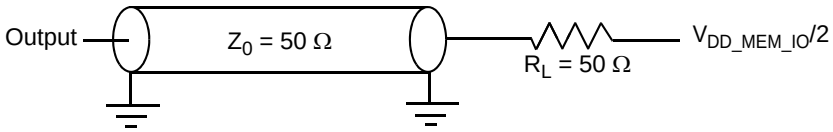


Figure 34. DDR AC test load

3.22.2 IEEE 1149.1 (JTAG) interface timing

Table 62. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	100	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

NOTES:
1 $f_{TCK} = 1/t_{TCK}$. f_{TCK} needs to be smaller than or equal to the system clock (SYS_CLK).

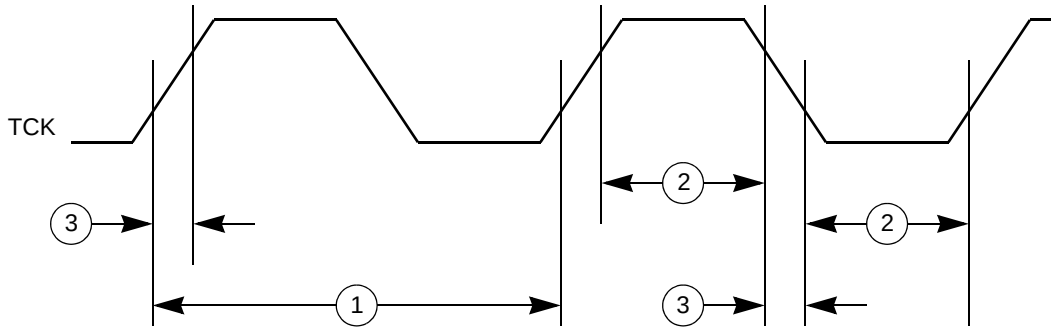


Figure 35. JTAG test clock input timing

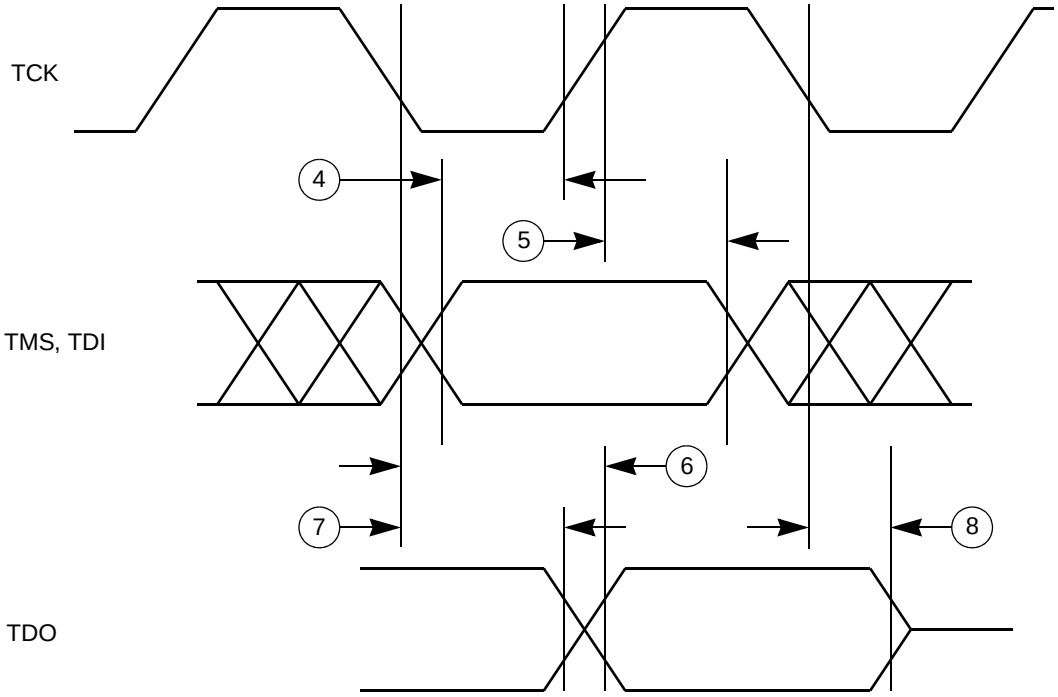


Figure 36. JTAG test access port timing

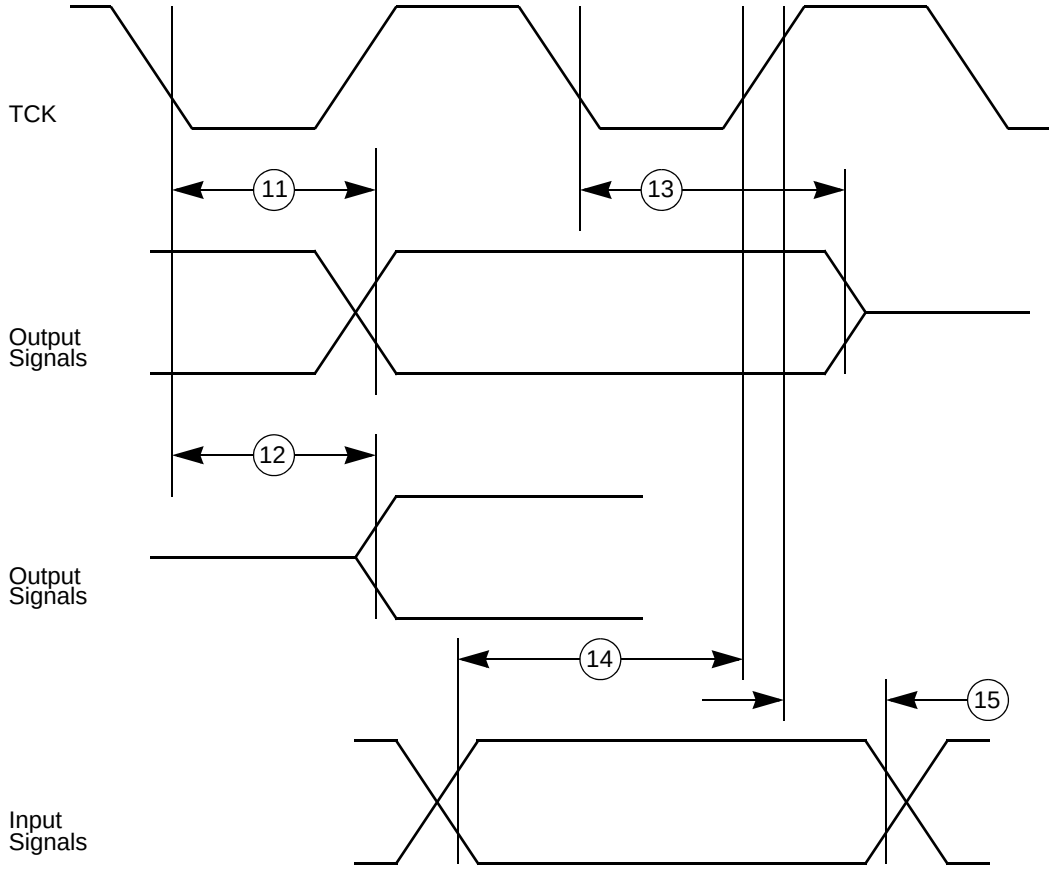


Figure 37. JTAG boundary scan timing

3.22.3 Nexus timing

Table 63. Nexus debug port timing[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCKO}	CC	MCKO cycle time	—	15.75	—	ns
2	t_{MDC}	CC	MCKO duty cycle	—	33	66	%
3	t_{MDOV}	CC	MCKO Low to MDO, $\overline{MSEO}$, $\overline{EVTO}$ data valid[2]	—	$(-0.1)t_{MCKO}$	$(0.2)t_{MCKO}$	ns
4	t_{EVTIPW}	CC	$\overline{EVTI}$ pulse width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	CC	$\overline{EVTO}$ pulse width	—	1	—	t_{MCYC}
6	t_{TCYC}	CC	TCK cycle time[3]	—	60	—	ns
7	t_{TDC}	CC	TCK duty cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	CC	TDI, TMS data setup time	—	12	—	ns
9	t_{NTDIH}, t_{NTMSH}	CC	TDI, TMS data hold time	—	6	—	ns
10	t_{JOV}	CC	TCK low to TDO data valid	—	0	18	ns
11	t_{JOIV}	CC	TCK low to TDO data invalid	—	6	—	ns

NOTES:
1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3 The system clock frequency needs to be three times faster than the TCK frequency.

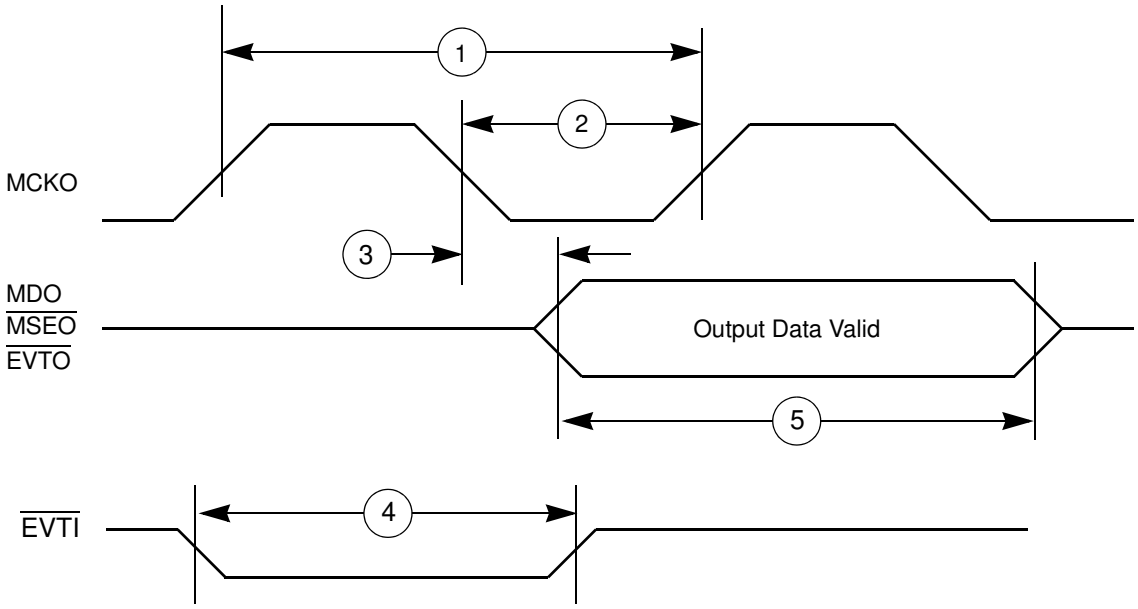


Figure 38. Nexus output timing

3.22.4 External interrupt timing (IRQ pins)

Table 64. External interrupt timing (NMI IRQ)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	SR	IRQ pulse width low	—	TBD	—	ns
2	t_{IPWH}	SR	IRQ pulse width high	—	TBD	—	ns
3	t_{ICYC}	SR	IRQ edge to edge time[1]	—	TBD	—	ns

NOTES:
1 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Table 65. External interrupt timing (GPIO IRQ)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	SR	IRQ pulse width low	—	TBD	—	ns
2	t_{IPWH}	SR	IRQ pulse width high	—	TBD	—	ns
3	t_{ICYC}	SR	IRQ edge to edge time[1]	—	TBD	—	ns

NOTES:
1 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

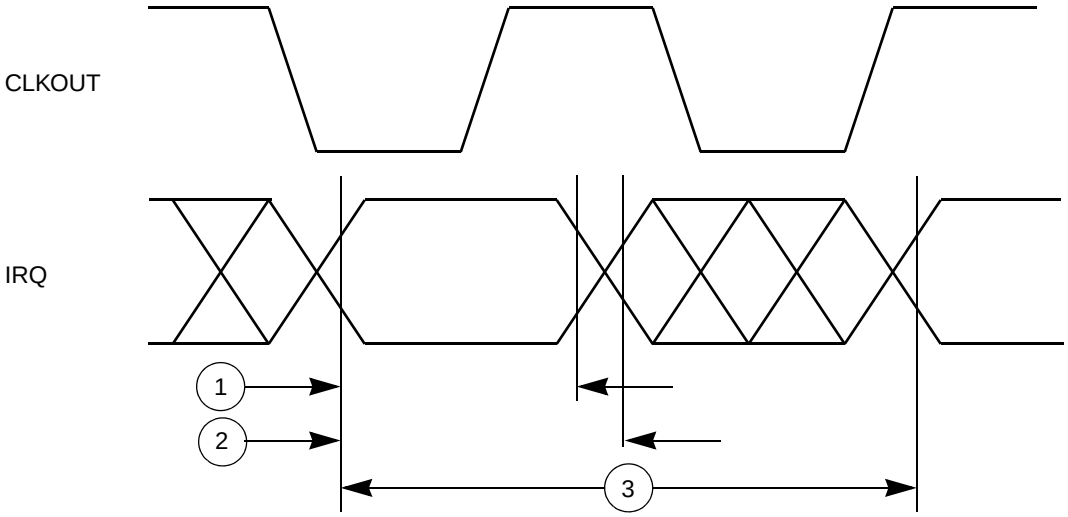


Figure 39. External interrupt timing

3.22.5 FlexCAN timing

Table 66. FlexCAN timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	f_{CAN_TX}	CC	FlexCAN design target transmit data rate	—	10	—	MBit/s
2	f_{CAN_RX}	CC	FlexCAN design target receive data rate	—	10	—	MBit/s

3.22.6 DSPI timing

Table 67. DSPI timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	DSPI cycle time	Master (MTFE = 0)	62	—	ns
				Slave (MTFE = 0)	62	—	
				Slave receive only mode[1]	16	—	
2	t_{CSC}	CC	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	After SCK delay	—	16	—	ns
4	t_{SDC}	CC	SCK duty cycle	—	0.4 × t_{SCK}	0.6 × t_{SCK}	ns
5	t_A	CC	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	CC	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	CC	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	$\overline{PCSS}$ to PCS*x* time	—	13	—	ns

Table 67. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
9	t_{SUI}	CC	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	CC	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	11	
				Master (MTFE = 1, CPHA = 1)	—	5	
12	t_{HO}	CC	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	
13	t_{DT}	CC	Delay after Transfer (minimum $\overline{CS}$ negation time)	Continuous mode Non-continuos mode[2]	62 134	— —	ns

NOTES:

1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. Note that in this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

2 In non-continuous mode, this value is always t_{SCK} × DSPI_CTAR*n*[DT] × DSPI_CTAR*n*[PDT]. The minimum permissible value of DT is 2 and the minimum permissible value of PDT is 1. See the DSPI chapter of the *PXS30 Reference Manual (PXS30RM)* for more information.

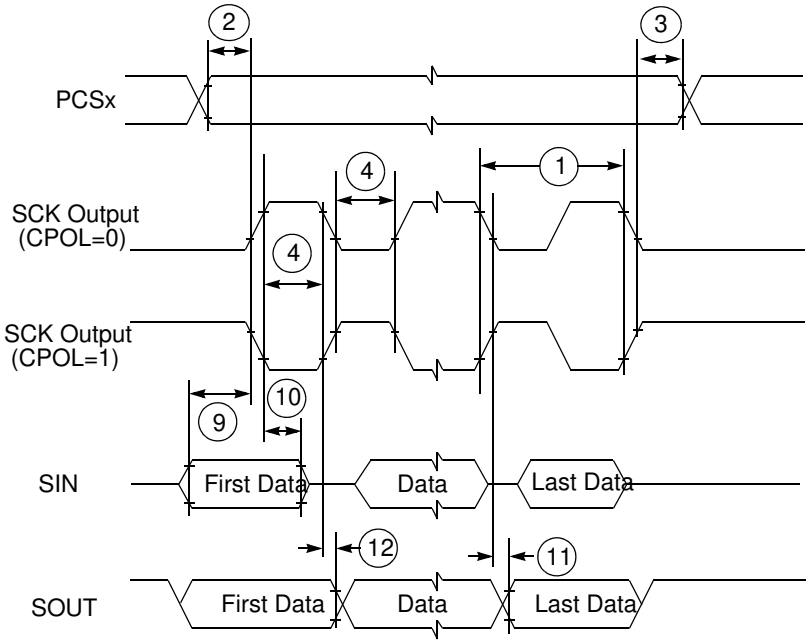


Figure 40. DSPI classic SPI timing—master, CPHA = 0

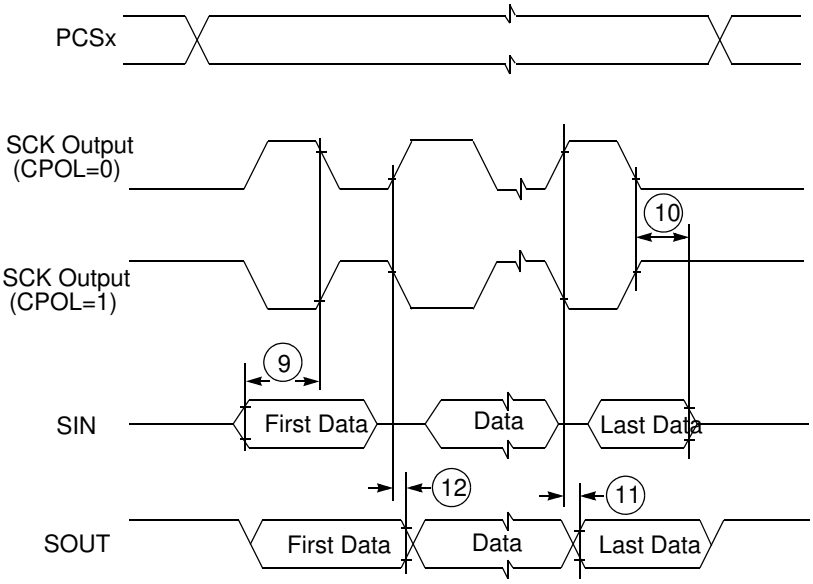


Figure 41. DSPI classic SPI timing—master, CPHA = 1

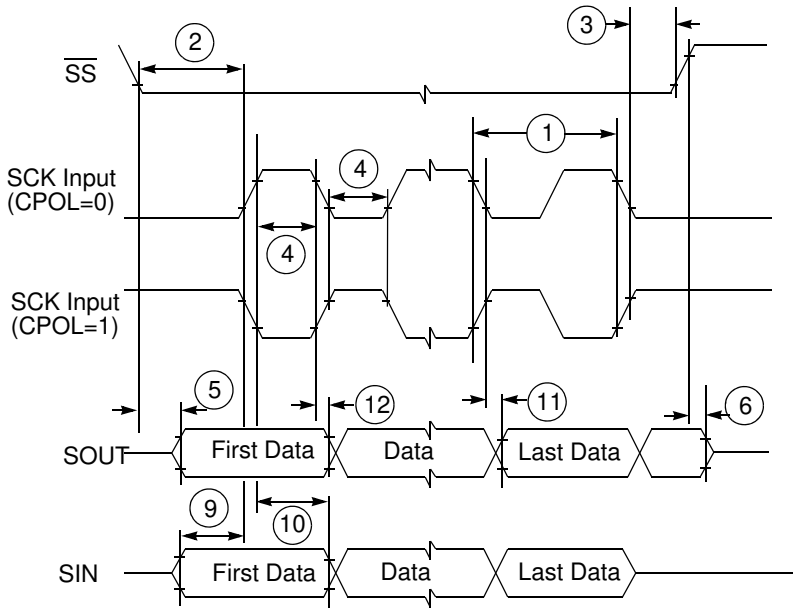


Figure 42. DSPI classic SPI timing—slave, CPHA = 0

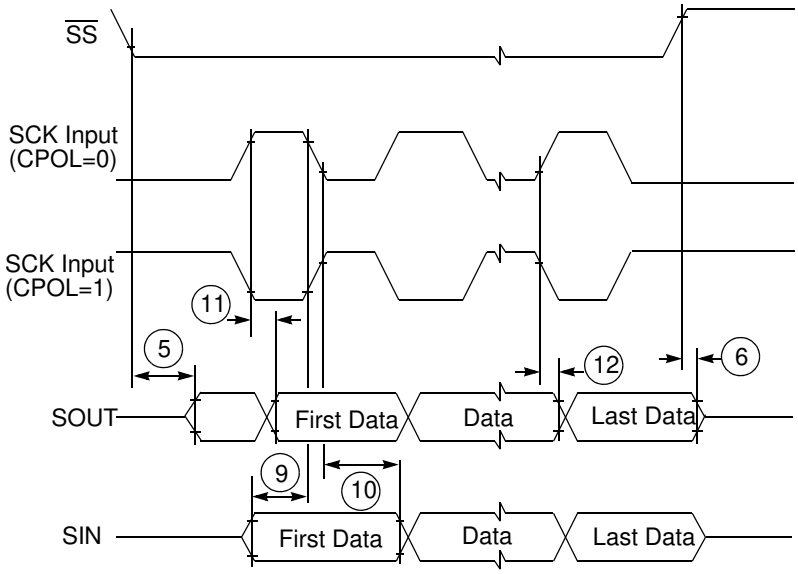


Figure 43. DSPI classic SPI timing—slave, CPHA = 1

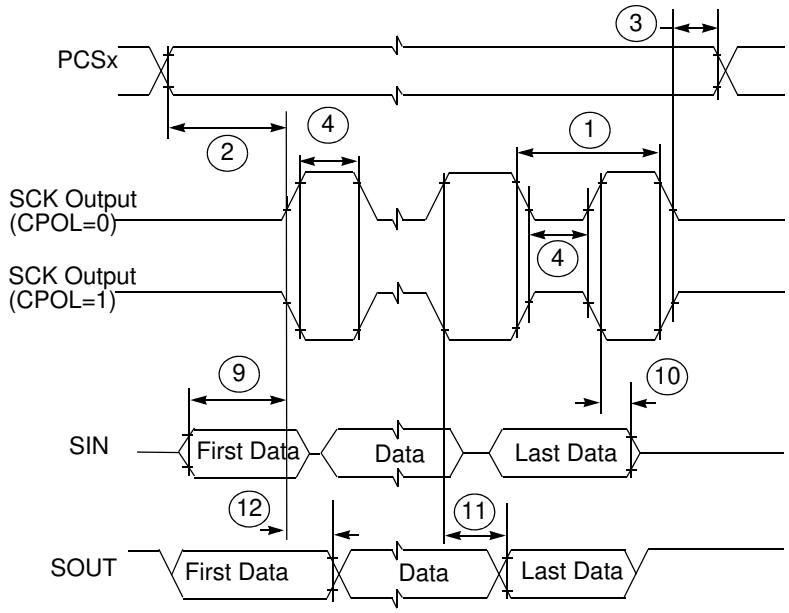


Figure 44. DSPI modified transfer format timing—master, CPHA = 0

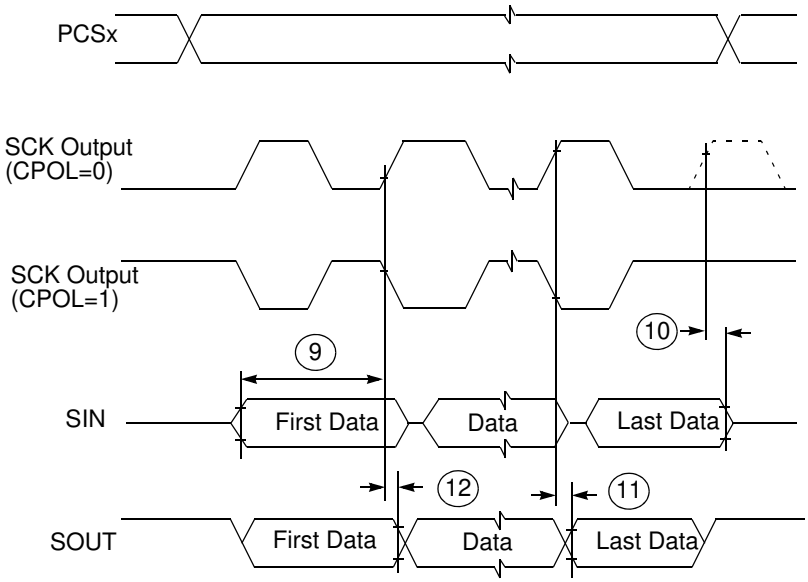


Figure 45. DSPI modified transfer format timing—master, CPHA = 1

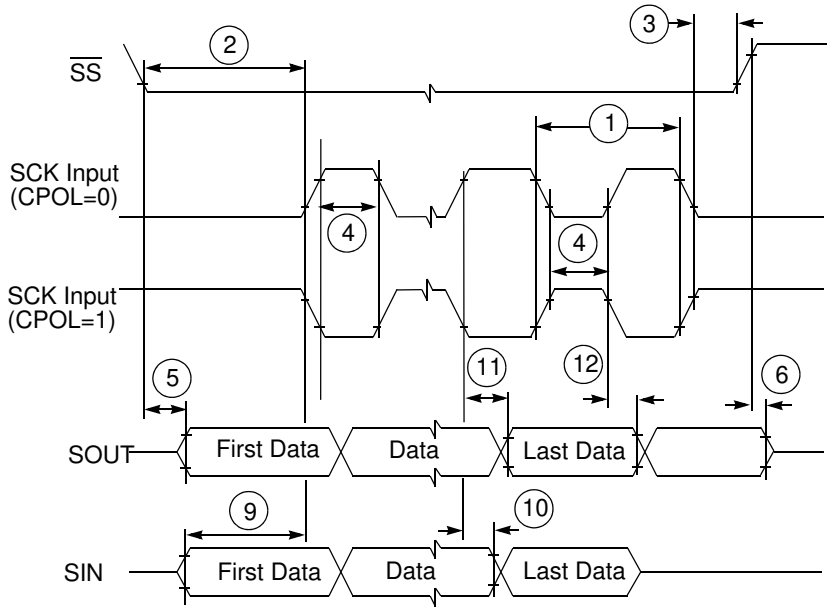


Figure 46. DSPI modified transfer format timing—slave, CPHA = 0

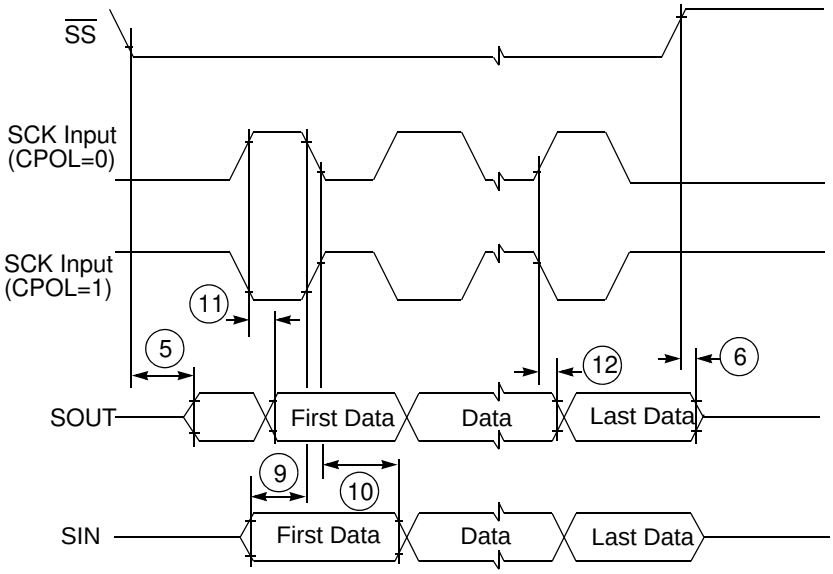


Figure 47. DSPI modified transfer format timing—slave, CPHA = 1

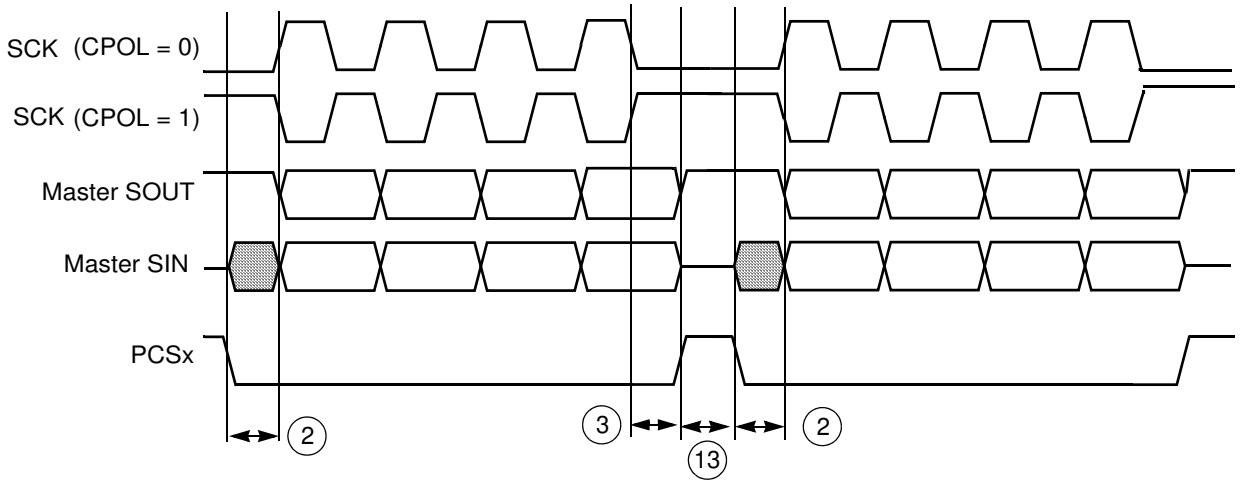


Figure 48. Example of non-continuous format (CPHA = 1, CONT = 0)

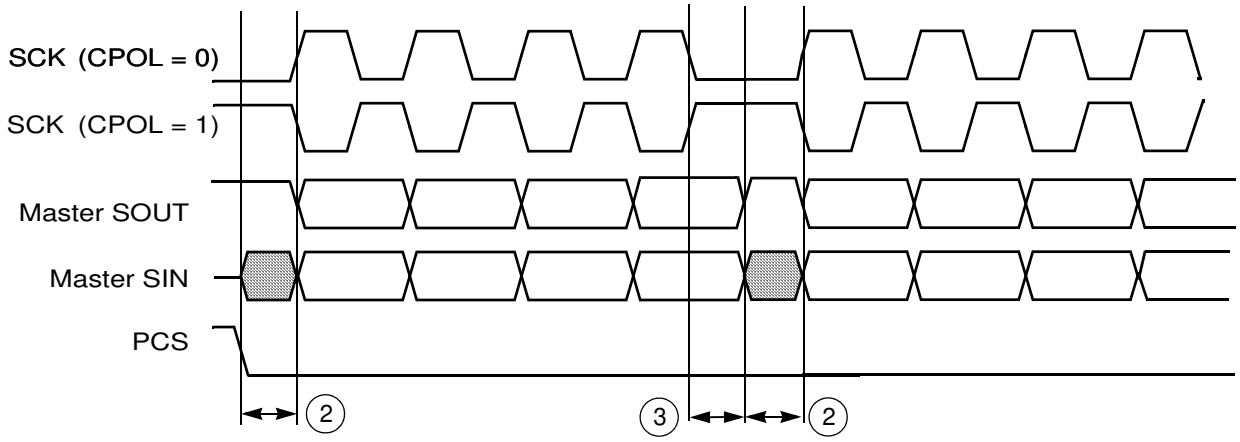


Figure 49. Example of continuous transfer (CPHA = 1, CONT = 1)

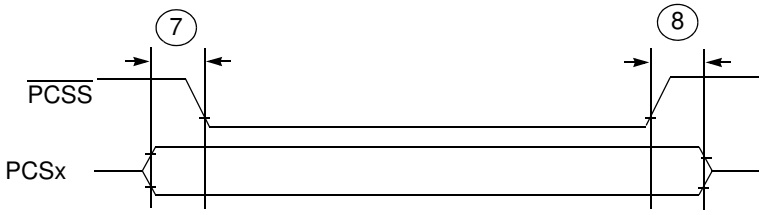


Figure 50. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.22.7 PDI timing

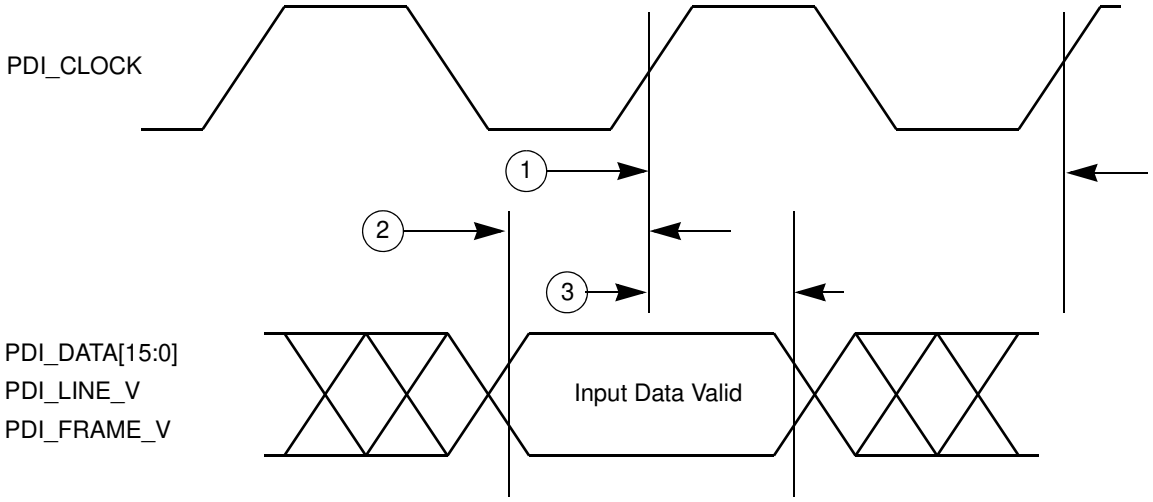
Table 68. PDI electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{PDI_CLOCK}	SR	PDI clock period	—	15	—	ns

Table 68. PDI electrical characteristics (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
2	t_{PDI_IS}	SR	Input setup time[1]	—	3	—	ns
3	t_{PDI_IH}	SR	Input hold time[1]	—	3	—	ns

NOTES:
1 Data can be captured at both launching and capturing edge of PDI_CLK.



PDI timing

3.22.8 Fast ethernet interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

3.22.8.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 69. MII receive signal timing

No.	Parameter	Min	Max	Unit
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
3	RX_CLK pulse width high	40%	60%	RX_CLK period
4	RX_CLK pulse width low	40%	60%	RX_CLK period

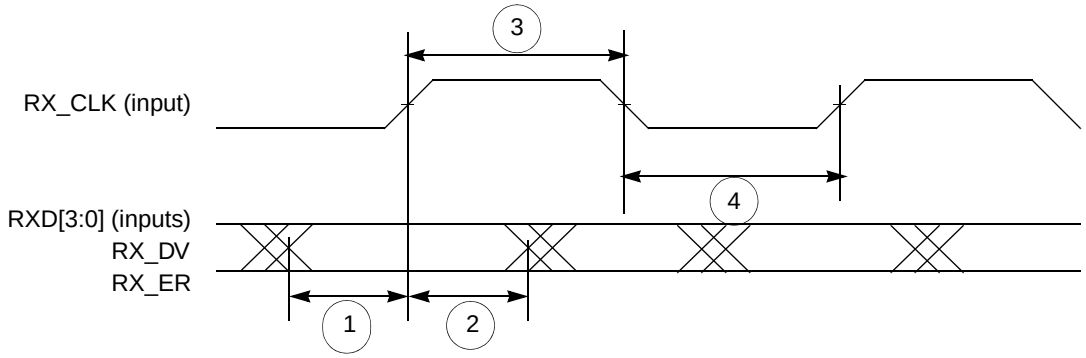


Figure 51. MII receive signal timing diagram

3.22.8.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 70. MII transmit signal timing[1]

No.	Parameter	Min	Max	Unit
5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
7	TX_CLK pulse width high	40%	60%	TX_CLK period
8	TX_CLK pulse width low	40%	60%	TX_CLK period

NOTES:
1 Output pads configured with SRC = 0b11.

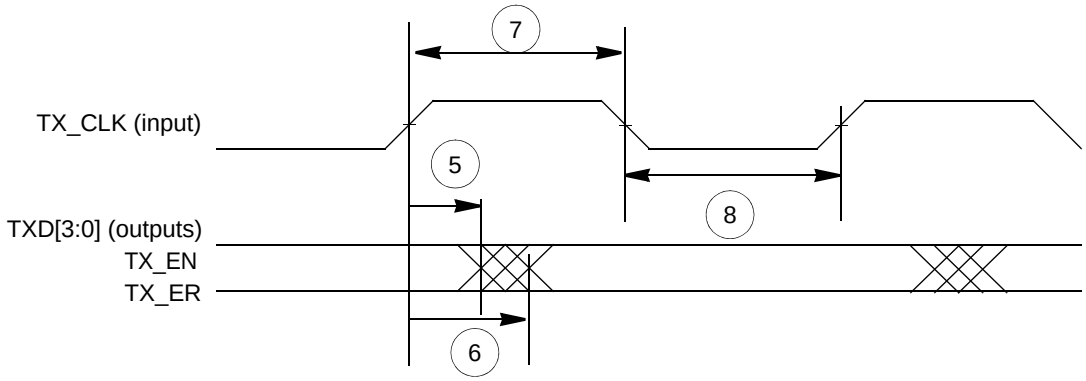


Figure 52. MII transmit signal timing diagram

3.22.8.3 MII async inputs signal timing (CRS and COL)

Table 71. MII async inputs signal timing[1]

No.	Parameter	Min	Max	Unit
9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

NOTES:
1 Output pads configured with SRC = 0b11.

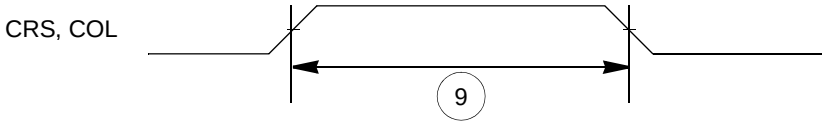


Figure 53. MII async inputs timing diagram

3.22.8.4 MII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 5 MHz.

Table 72. MII serial management channel timing[1]

No.	Parameter	Min	Max	Unit
10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
12	MDIO (input) to MDC rising edge setup	10	—	ns
13	MDIO (input) to MDC rising edge hold	0	—	ns
14	MDC pulse width high	40%	60%	MDC period
15	MDC pulse width low	40%	60%	MDC period

NOTES:
1 Output pads configured with SRC = 0b11.

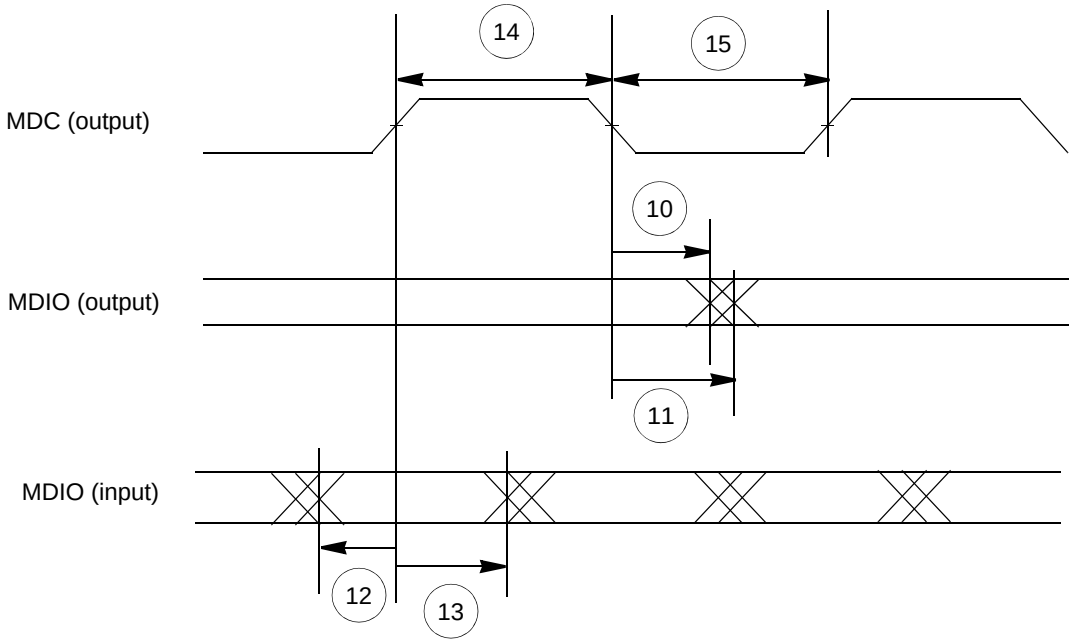


Figure 54. MII serial management channel timing diagram

3.22.9 External Bus Interface (EBI) timing

Table 73. EBI timing

No.	Symbol		Parameter	45 MHz (Ext. Bus Freq)[1]		Unit	Notes
				Min	Max		
1	t_C	CC	D_CLKOUT period	22.2	—	ns	Signals are measured at 50% V_{DDE}.
2	t_{CDC}	CC	D_CLKOUT duty cycle	45%	55%	t_C	—
3	t_{CRT}	CC	D_CLKOUT rise time	—	—	ns	—
4	t_{CFT}	CC	D_CLKOUT fall time	—	—	ns	—
5	t_{COH}	CC	D_CLKOUT posedge to output signal invalid or high Z (hold time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] $\overline{\text{D\_OE}}$ $\overline{\text{D\_RD\_WR}}$ D_TA $\overline{\text{D\_TS}}$ $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]	1.0	—	ns	—

Table 73. EBI timing (continued)

No.	Symbol		Parameter	45 MHz (Ext. Bus Freq)[1]		Unit	Notes
				Min	Max		
6	t_{COV}	CC	D_CLKOUT posedge to output signal valid (output delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] $\overline{\text{D\_OE}}$ $\overline{\text{D\_RD\_WR}}$ D_TA $\overline{\text{D\_TS}}$ $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]	—	10	ns	—
7	t_{CIS}	CC	Input signal valid to D_CLKOUT posedge (setup time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	7.5	—	ns	—
8	t_{CIH}	CC	D_CLKOUT posedge to input signal invalid (hold time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	1.0	—	ns	—
9	t_{APW}	CC	D_ALE pulse width	6.5	—	ns	The timing is for Asynchronous external memory system.
10	t_{AAI}	CC	D_ALE negated to address invalid	1.5	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

NOTES:
1 Speed is the nominal maximum frequency. Maximum core speed allowed is 180 MHz plus frequency modulation (FM).

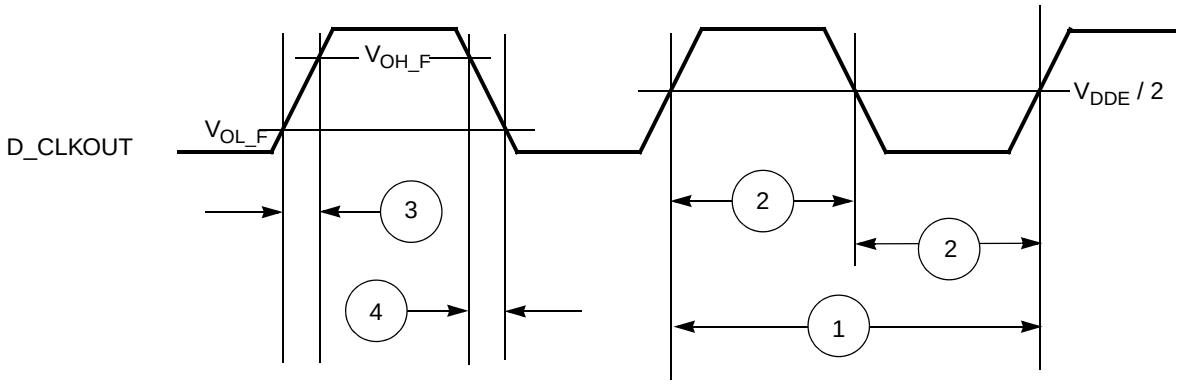


Figure 55. D_CLKOUT timing

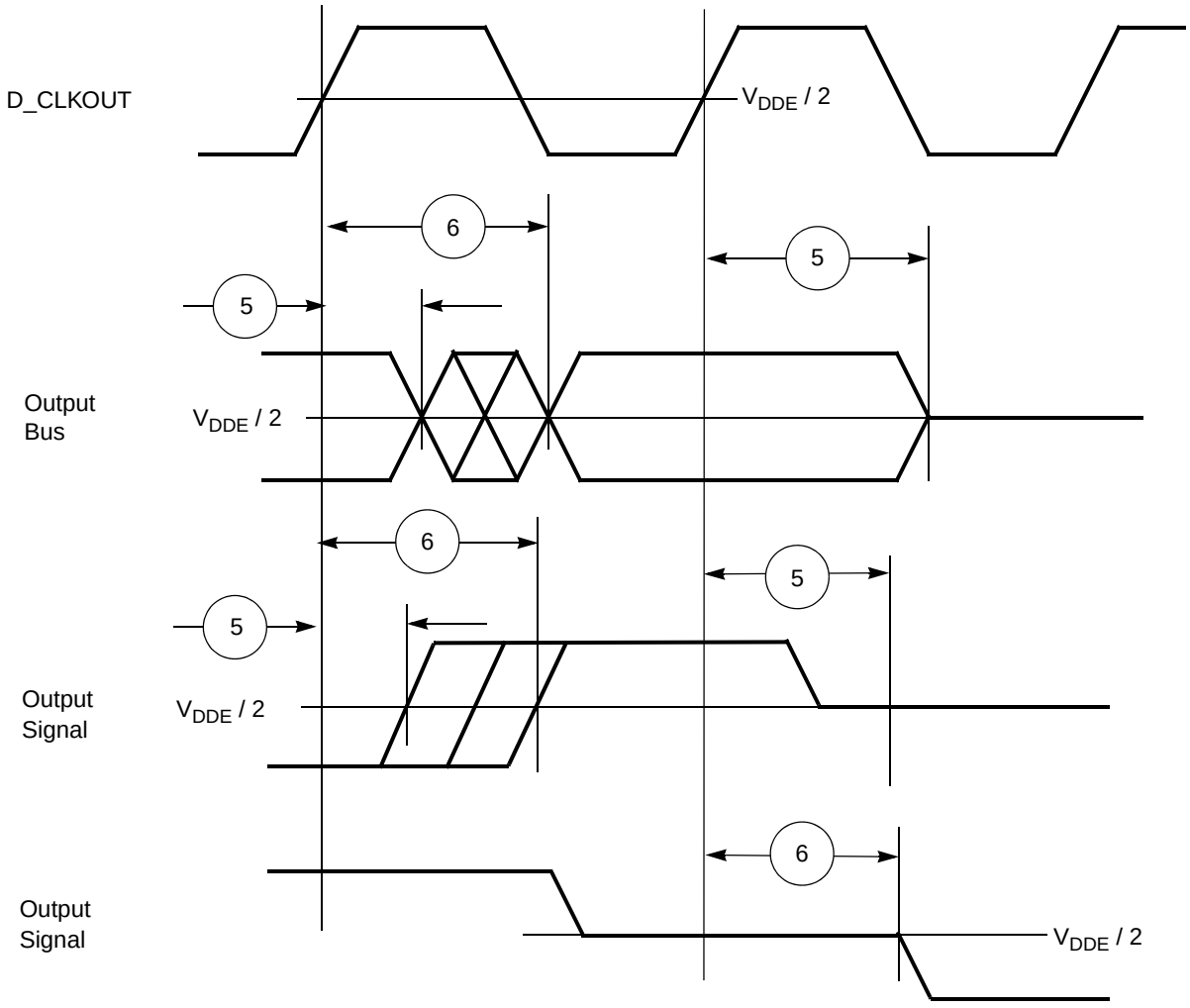


Figure 56. Synchronous output timing

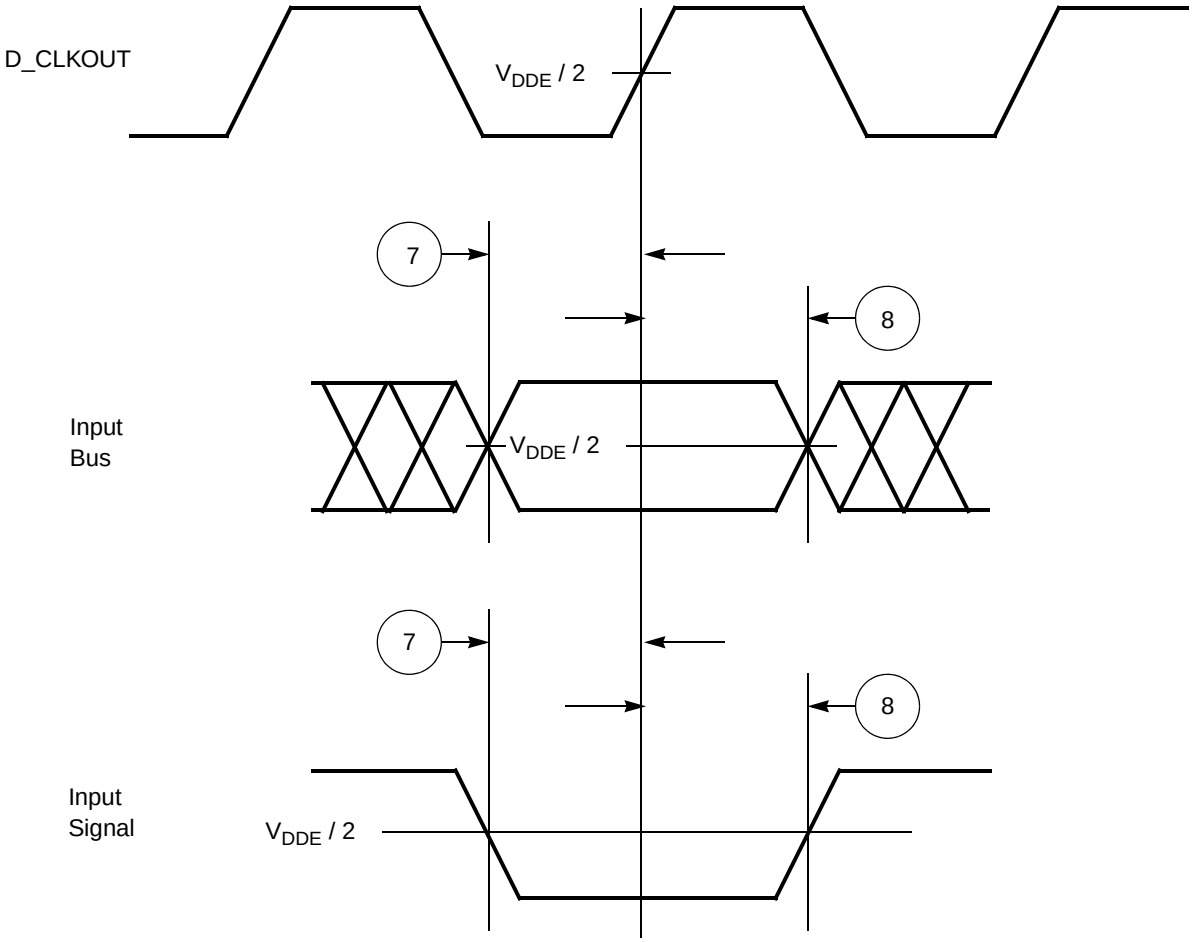


Figure 57. Synchronous input timing

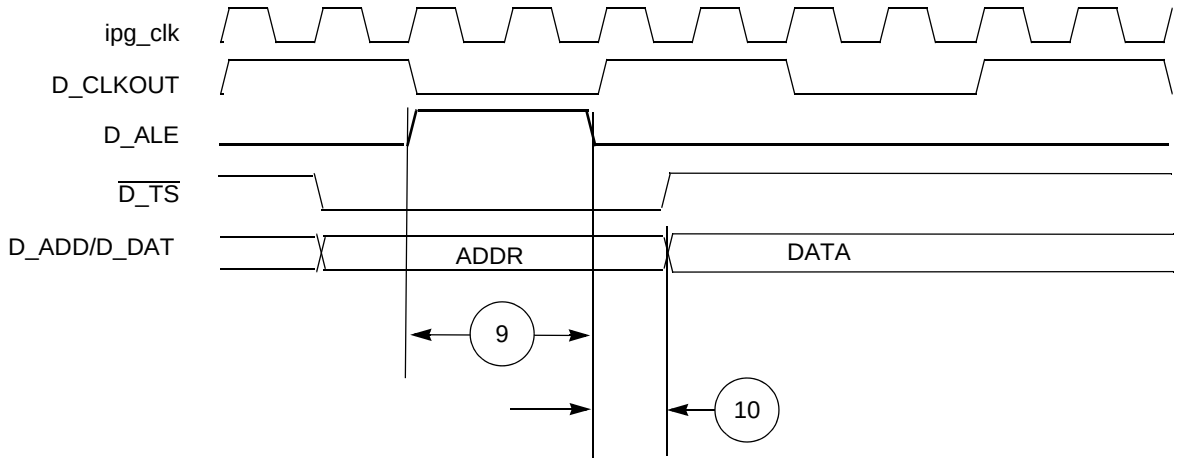


Figure 58. ALE signal timing

3.22.10 I²C Timing

Table 74. I²C SCL and SDA input timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	D	Start condition hold time	2	—	IP bus cycle[1]
2	—	D	Clock low time	8	—	IP bus cycle[1]
4	—	D	Data hold time	0.0	—	ns
6	—	D	Clock high time	4	—	IP bus cycle[1]
7	—	D	Data setup time	0.0	—	ns
8	—	D	Start condition setup time (for repeated start condition only)	2	—	IP bus cycle[1]
9	—	D	Stop condition setup time	2	—	IP bus cycle[1]

NOTES:
1 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

Table 75. I²C SCL and SDA output timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1[1]	—	D	Start condition hold time	6	—	IP bus cycle[2]
2[1]	—	D	Clock low time	10	—	IP bus cycle[1]
3[3]	—	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	D	Data hold time	7	—	IP bus cycle[1]
5[1]	—	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	D	Clock high time	10	—	IP bus cycle[1]
7[1]	—	D	Data setup time	2	—	IP bus cycle[1]
8[1]	—	D	Start condition setup time (for repeated start condition only)	20	—	IP bus cycle[1]
9[1]	—	D	Stop condition setup time	10	—	IP bus cycle[1]

NOTES:
1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.
2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.
3 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

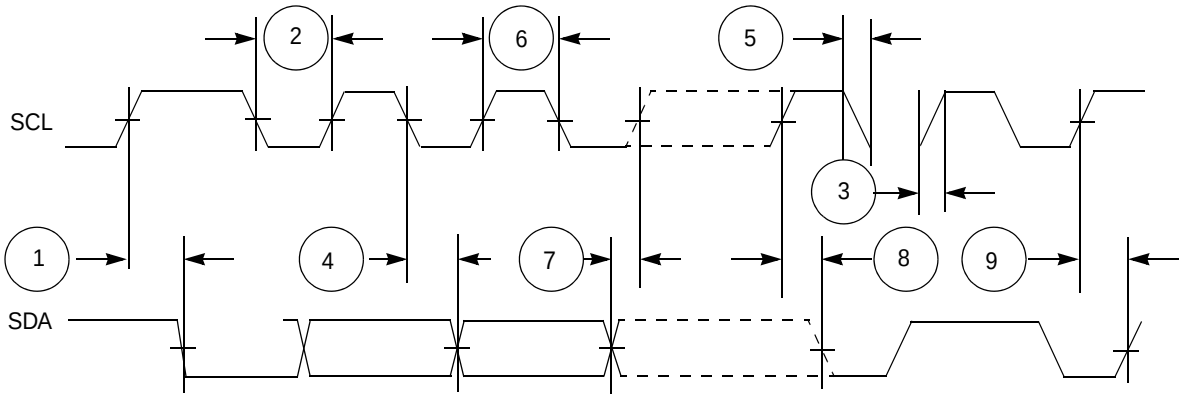


Figure 59. I²C input/output timing

3.22.11 LINFlex timing

The maximum bit rate is 1.875 MBit/s.

4 Package characteristics

4.1 Package mechanical data

4.1.1 257 MAPBGA

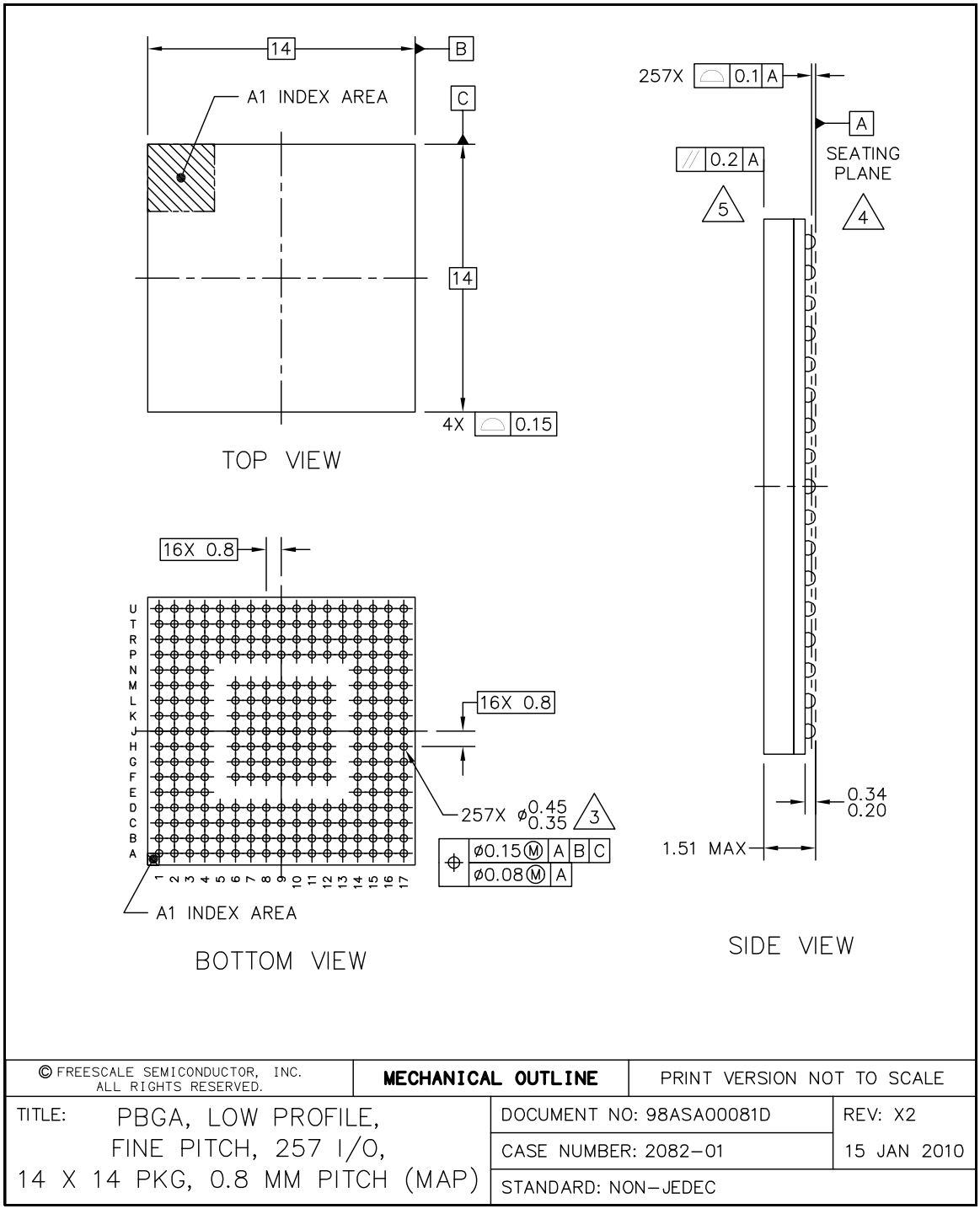


Figure 60. 257 MAPBGA mechanical data (1 of 2)

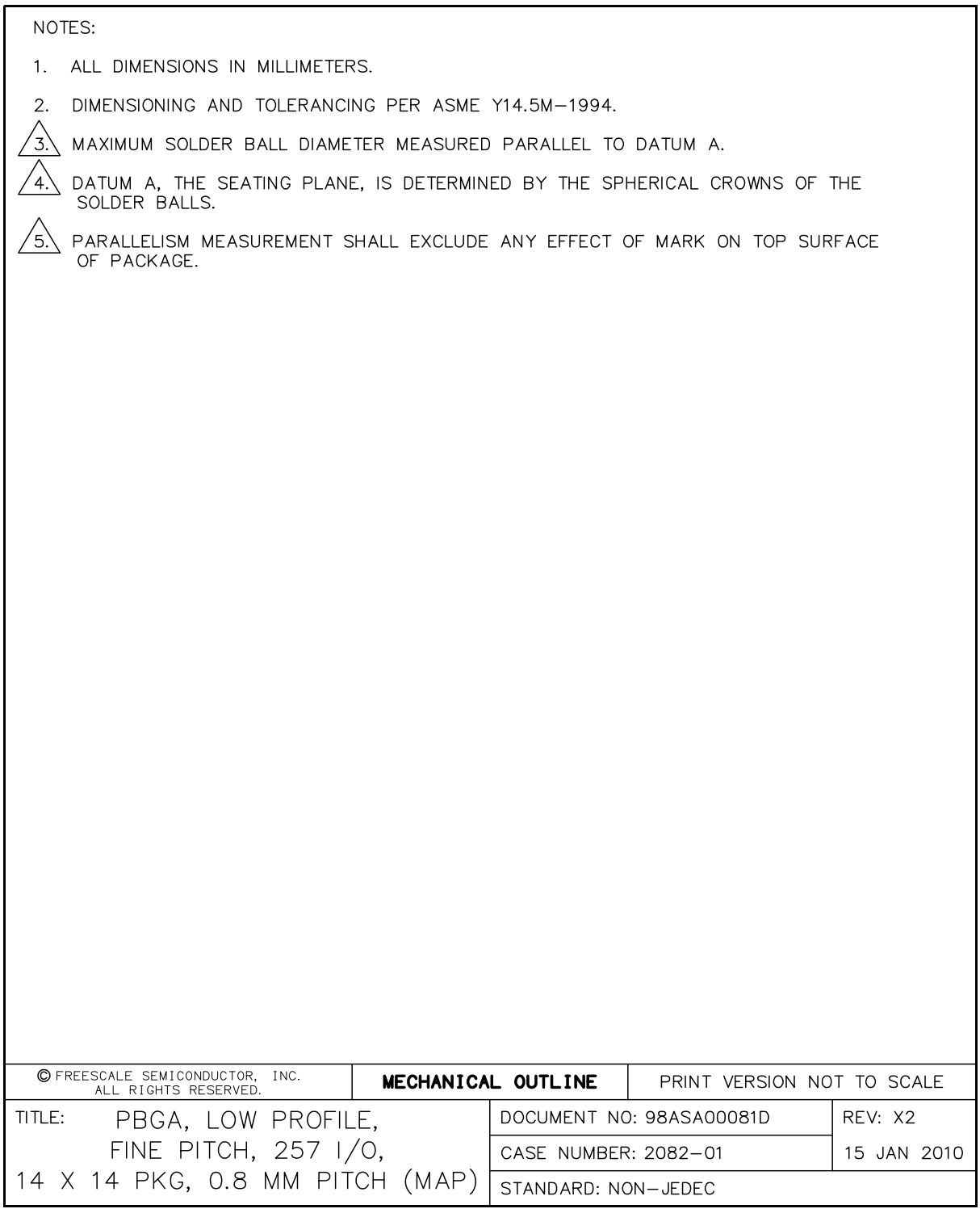


Figure 61. 257 MAPBGA mechanical data (2 of 2)

4.1.2 473 MAPBGA

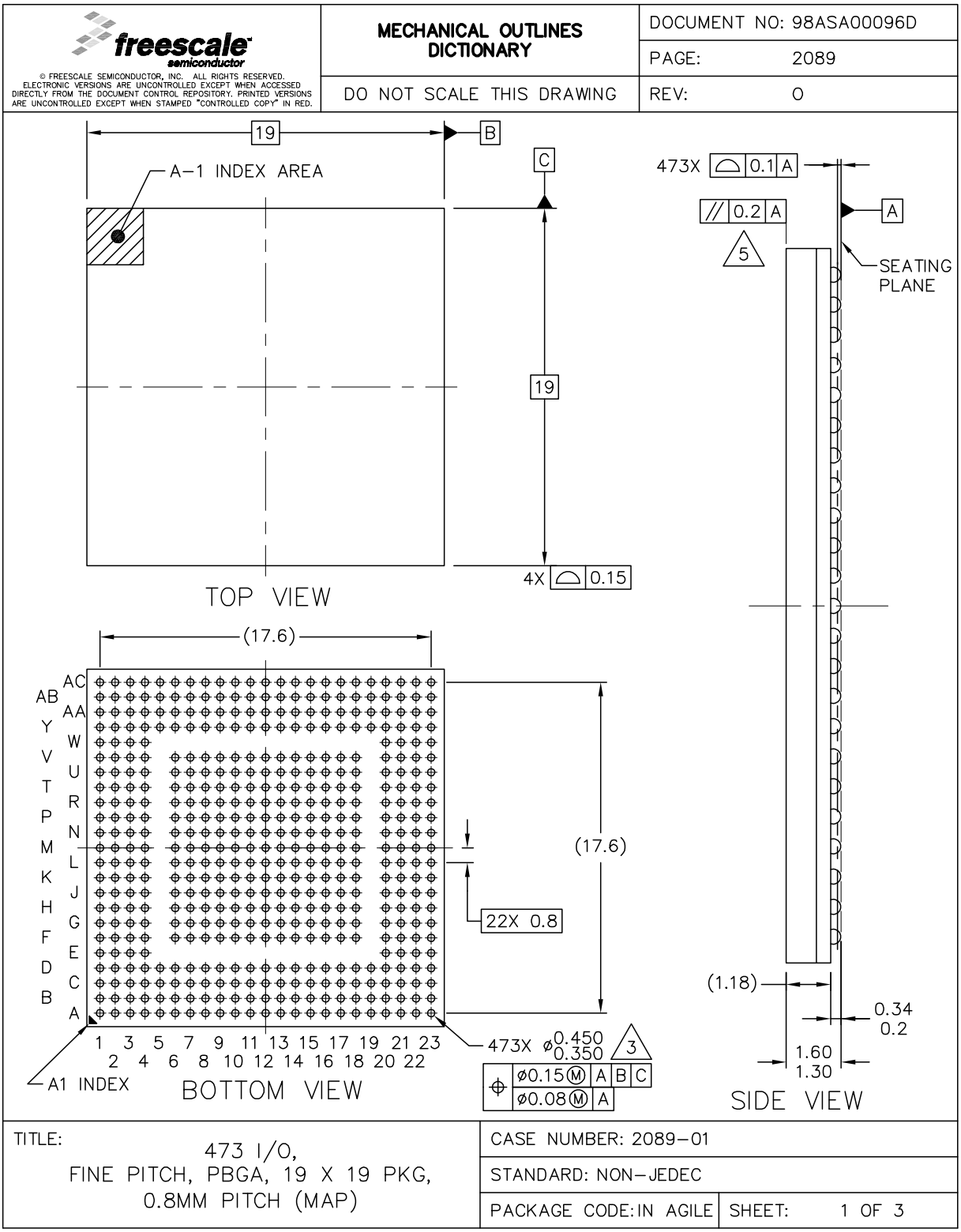


Figure 62. 473 MAPBGA package mechanical data (1 of 3)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00096D
		PAGE: 2089
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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 473 I/O, FINE PITCH, PBGA, 19 X 19 PKG, 0.8MM PITCH (MAP)	CASE NUMBER: 2089–01	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: IN AGILE	SHEET: 2

Figure 63. 473 MAPBGA package mechanical data (2 of 3)

REVISION HISTORY

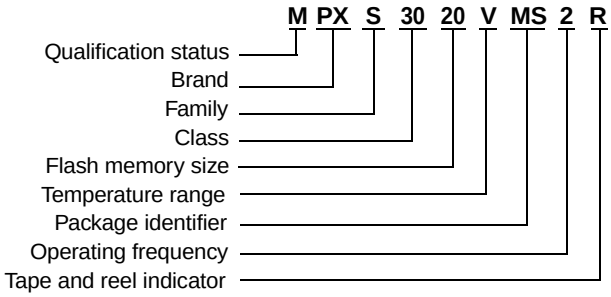
DOCUMENT NO: 98ASA00096D
PAGE: 2089
REV: O

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	D. VO	RELEASED FOR PRODUCTION	DSS	08 JUN 2009

TITLE:	CASE NUMBER: 2089–01	
473 I/O, FINE PITCH, PBGA, 19 X 19 PKG, 0.8MM PITCH (MAP)	STANDARD: NON–JEDEC	
	PACKAGE CODE: IN AGILE	SHEET: 3

Figure 64. 473 MAPBGA package mechanical data (3 of 3)

5 Orderable parts



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Tiime Control
S = Safety

Flash Memory Size
10 = 1 MB
15 = 1.5 MB
20 = 2 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
MM = 257 BGA
MS = 473 BGA

Operating frequency
1 = 150 MHz
2 = 180 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 76 for more information.

Figure 65. PXS30 orderable part number description

Table 76. PXS30 orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXS3010VMM150	1 MB/256 KB	257 MAPBGA (14 mm x 14 mm)	150
MPXS3015VMS180	1.5 MB/384 KB	473 MAPBGA (19 mm x 19 mm)	180
MPXS3020VMS180	2 MB/512 KB	473 MAPBGA (19 mm x 19 mm)	180

6 Reference documents

1. Nexus (IEEE-ISTO 5001™—2008)
2. Measurement of emission of ICs—IEC 61967-2
3. Measurement of emission of ICs—IEC 61967-4
4. Measurement of immunity of ICs—IEC 62132-4
5. Semiconductor Equipment and Materials International
   3081 Zanker Road
   San Jose, CA 95134 USA
   (408) 943-6900
6. JEDEC specifications are available at http://www.jedec.org
7. MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

8. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
9. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
10. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

7 Document revision history

Table 77 summarizes revisions to this document.

Table 77. Revision history

Revision	Date	Description of Changes
1	30 Sep 2011	Initial release.

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Document Number: PXS30
Rev. 1
October 3, 2011 1:35 pm