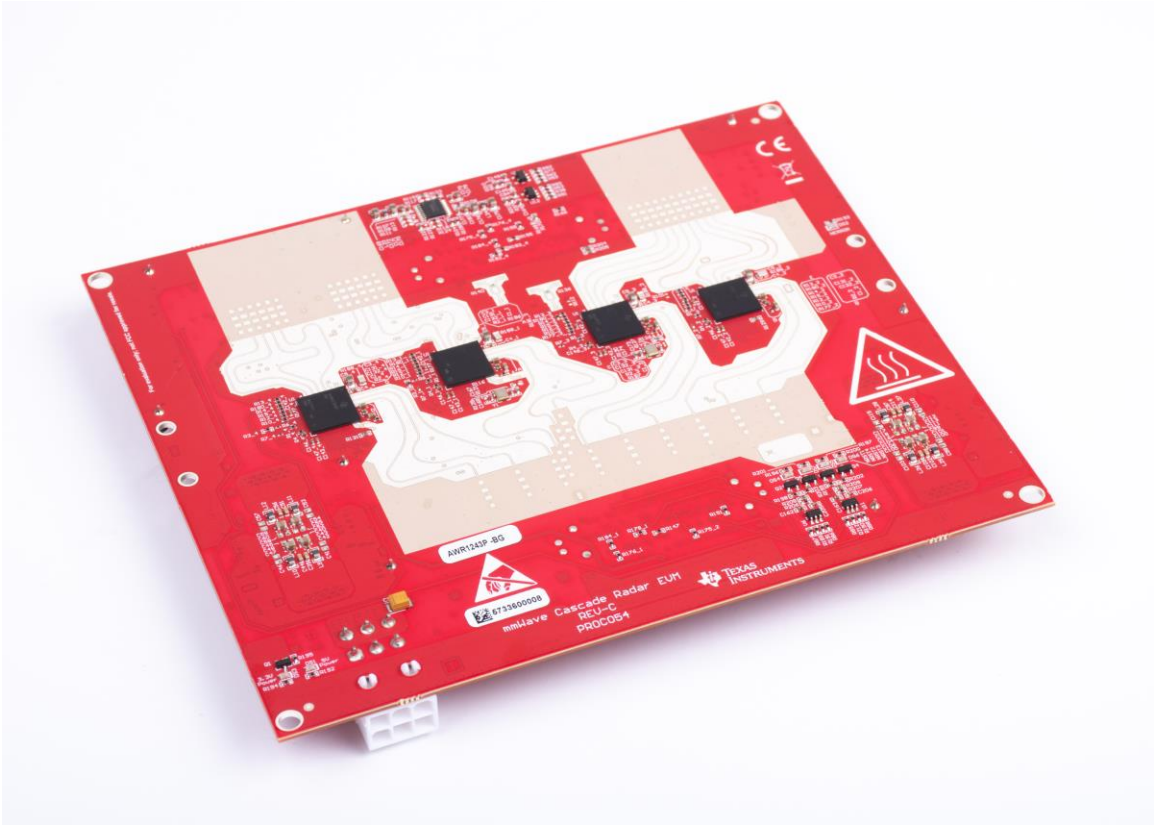
User's Guide
SWRU553A–September 2019–Revised February 2020

# AWRx Cascaded Radar RF Evaluation Module (MMWCAS-RF-EVM)



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# 1 Getting Started

## 1.1 Introduction

The AWRx Cascaded Radar RF evaluation board is an AWRx based mmWave sensing solution from TI implementing a 4-device, cascaded, array of AWRx mmWave devices. In this cascaded radar configuration, a single master device distributes a 20 GHz LO signal between all 4 devices, allowing these 4 devices to operate as a single RF transceiver. This enables support for up to 12 TX and 16 RX antenna elements. In TX beam-forming, beam-steering and MIMO/SIMO use-cases the larger number of antenna elements allows for higher SNR and higher angular resolution compared to a single-device system.

The Cascade Radar evaluation board interfaces to a companion TI TDA2x based Host/Data Capture board that is responsible for controlling the AWRx devices and receiving captured IF ADC samples. The TI TDA2x Host/Data Capture board includes SSD storage for supporting longer term data capture scenarios and 1Gigabit Ethernet connectivity for control and offloading captured data.

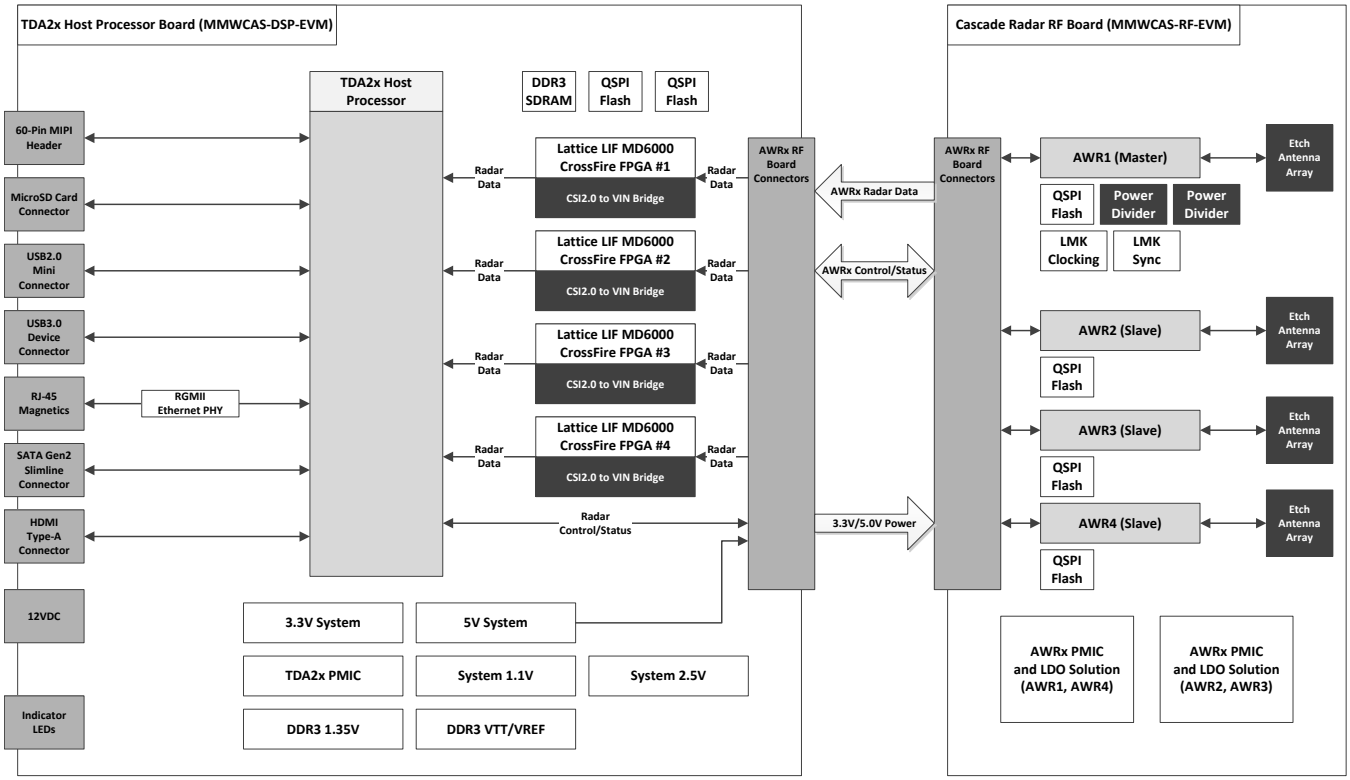


**Figure 1. Cascade RF EVM and companion TDA2x Host Processor Board Block Diagram**

The Cascade Radar evaluation board, when combined with a compatible host/data capture board, contains everything needed to start evaluating a single-device, or 2-device, 3-device or 4-device cascaded radar solution.

## 1.2 EVM Revisions

Multiple revisions of this EVM have been released. Please see below descriptions. This user guide is applicable to all of these EVM revisions. Usage of AWRx refers to either AWR1243P or AWR2243P throughout this document.

- **MMWCAS-RF-EVM, PROC054C** - Release based on AWR1243P. AWR1243P is not recommended for new designs.
- **MMWCAS-RF-EVM, PROC054D** - Release based on AWR2243P. AWR2243P is recommended for new designs.



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## 1.3 Key Features

**Table 1. Key Features**

| | Cascade Radar RF Board |
|---|---|
| 4x AWRx 76-81GHz Radar SoC | Integrated VCO, LO distribution, PA, LNA, ADC, 3 TX and 4 RX ARM MCU R4 Controller |
| **AWRx RF/LO Peripherals** | |
| 12x TX, 16x RX Antennas | • 12 total transmitters across all 4 AWRx devices<br>• 16 total receivers across all 4 AWRx devices<br>• 86 non-overlapping Azimuth virtual array (lambda/2)<br>• 4 minimum redundancy array (MRA) Elevation |
| Embedded Antenna | • 4-element series-fed patch antenna, 12dBi<br>• ± 60 deg Azimuth 3dB<br>• ± 30 deg Elevation 3dB |
| 20 GHz LO Star-Network Distribution | 2x Wilkinson power dividers fed by the Master AWRx device LO output to Master and Slave AWRx devices |
| **AWR Digital Peripherals** | |
| CSI2.0 4-lane | 600Mbps/Lane for 2.4 Gbps ADC IF data per device |
| QSPI Flash | 16 Mbit QSPI flash for AWR firmware updates/deveopment |
| Serial Peripherals | SPI, I2C, UART, GPIO |
| System Temperature | TMP112 I2C Temperature Sensors |
| **Power** | |
| Radar Power Management IC (PMIC) Solution | • 2x LP87524P Quad-Channel, Integrated FET, Buck Converters, secondary LC filtering solution powering all 4 AWRx devices<br>• TPS73733 LDO generating 3.3V system power |

## 1.4 What is Included

### 1.4.1 Kit Hardware Contents

- MMWAVCAS-RF-EVM PCB assembly
- Mounting standoffs and screws

**NOTE:** The MMWAVCAS-RF-EVM is designed to be mounted to the companion TI TDA2x Cascade Radar Host/Capture board (MMWAVCAS-DSP-EVM). The combination MMWAVCAS-RF-EVM and MMWAVCAS-RF-EVM kit is mastered through a host PC over Ethernet and USB and the mmWave Studio software suite.

For more information on assembling, powering and configuring the full two-board system, see the mmWave Studio and MMWAVCAS-DSP-EVM documentation. All necessary mounting hardware and peripheral cables are expected to be provided by the host board system.

### 1.4.2 mmWave Studio and Matlab Post Processing

TI provides the following evalution software to get started with the Cascade Radar evaluation module.

- mmWave Studio GUI and Lua scriptable configuration environment
- TDA2x ADC IF data capture application running on the MMWAVCAS-DSP-EVM
- Matlab post processing sample codes for reading captured ADC IQ sample datasets and example TDMA-MIMO and TX-Beamforming use modes

For details on getting started with these demos, see the mmWave Studio User's Guide. This is part of the mmWave Studio 2.1 release (and later).


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## 2 Hardware Description

Figure 2 and Figure 3 show the front and rear views of the evaluation board, respectively. The front (top layer) of the board primarily includes the AWRx devices and the embedded antenna arrays and 20 GHz LO splitters. The back (bottom layer) of the board primarily includes the host board connectors, power supplies (PMIC), most other support IC and most passives.

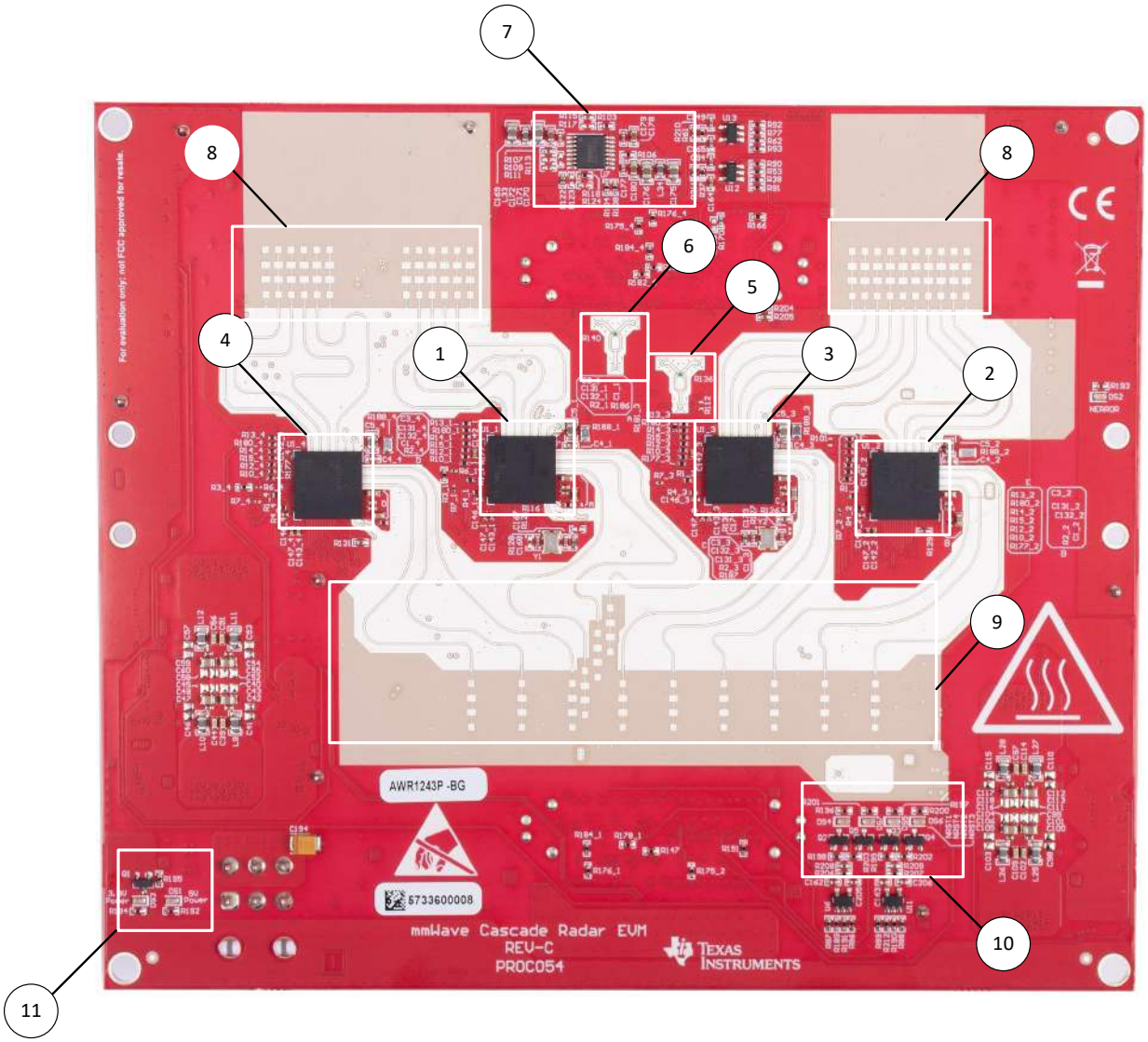


**Figure 2. MMWAVCAS-RF-EVM Front View**

Front View Callouts:

1. AWRx #1 “Master” (U1_1)
2. AWRx #2 “Slave 1” (U1_2)
3. AWRx #4 “Slave 3” (U1_4)
4. AWRx #3 “Slave 2” (U1_3)
5. 20 GHz LO Wilkinson Power Divider #1 (FMCW_CLKOUT) AWR #1 and AWR #2
6. 20 GHz LO Wilkinson Power Divider #2 (FMCW_SYNCOUT) AWR #3 and AWR #4
7. LMK00804B (U4) AWRx 40 MHz clock distribution buffer
8. Receive antenna array
9. Transmit antenna array



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10. AWRx reset LED indicators
11. System 5.0 V and 3.3 V power status indicators

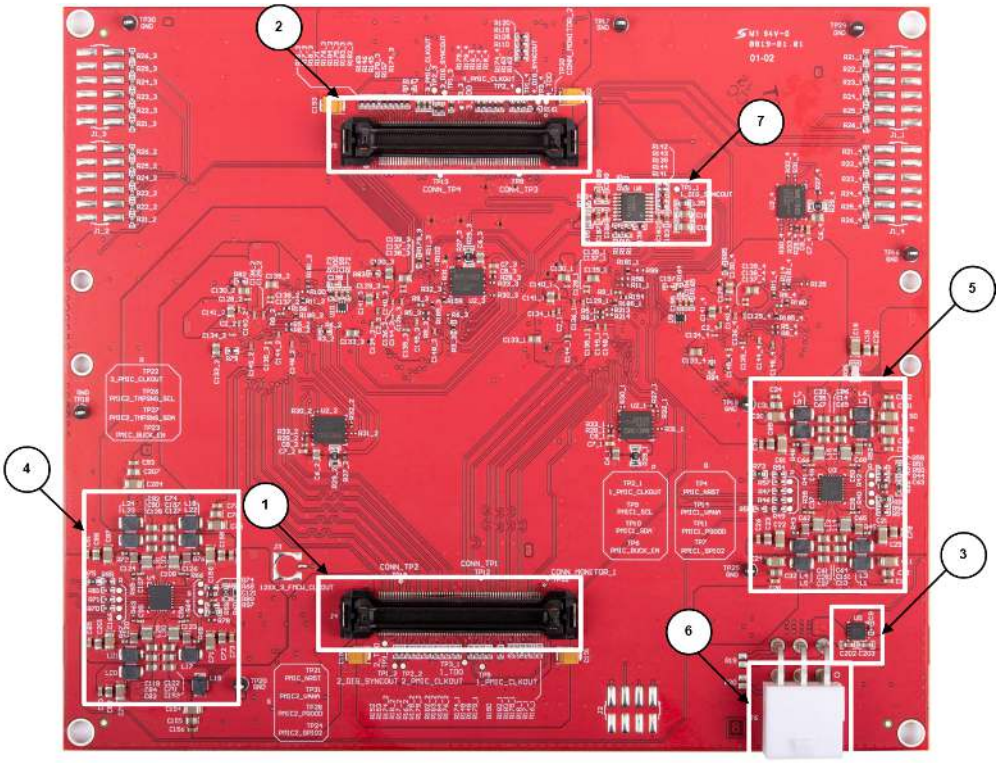


**Figure 3. MMWAVCAS-RF-EVM Back View**

Back View Callouts:

1. Host Board Connector #1 (J4) 5.0 V power, interfaces for AWRx #1, AWRx #2
2. Host Board Connector #2 (J5) 5.0 V power, interfacesAWRx #3, AWRx #4
3. LP87524P PMIC #2 (U4) powersAWRx #2 and AWRx #3
4. LP87524P PMIC #1 (U3) powersAWRx #1 and AWRx #4
5. TPS73733 5.0V to 3.3 V LDO (U5) provides system 3.3 V power
6. Bench 5.0 V power connector (J6)
7. LMK00804B (U8) AWRx digital synchronization distribution buffer


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## 2.1 Block Diagram

The MMWAVCAS-RF-EVM consists of four AWR mmWave SoC and their associated power, clocking, synchronization, LO and RF TX and RX circuits. Each AWRx RF TX and RX port is routed to an etched, series-fed, patch antenna element. Each AWRx on the RF board has a 4-port CSI2.0 transmitter which is used for sending radar IQ ADC data samples to an attached host processor CSI2.0 receiver set. All of the AWRx configuration, control and reset lines are made available on two host interface connectors (J4 and J5) implemented with Hirose FX23-120 connectors.

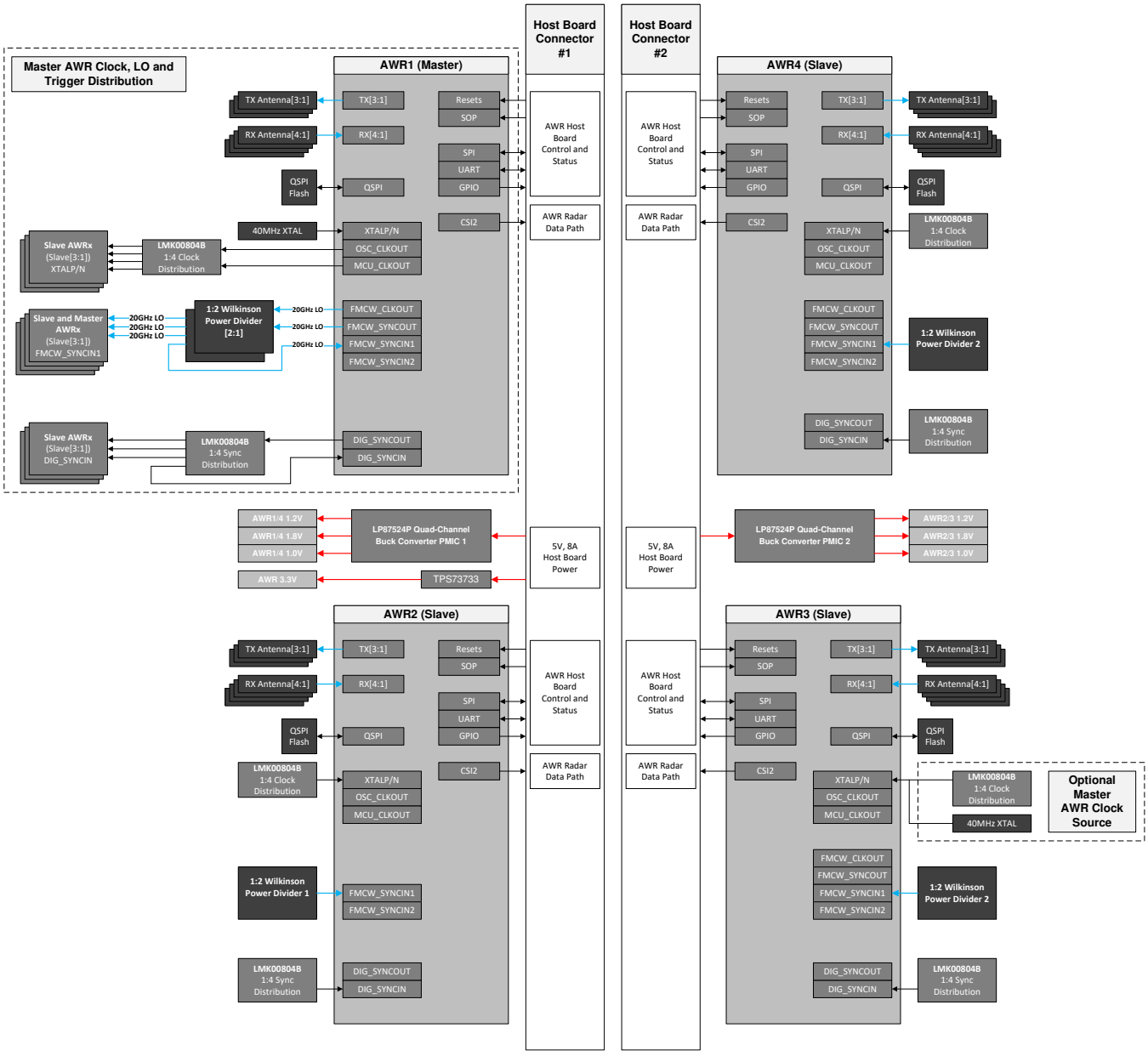


**Figure 4. MMWAVCAS-RF-EVM System Block Diagram**

The AWR devices are separated into Master and Slave classes of devices. AWRx #1, the Master device, utilizes the AWRx architecture built in VCO, LO distribution, clock distribution and frame synchronization distribution to provide 40 MHz clock, 20 GHz LO and frame synchronization to the other three Slave devices – AWRx #2, AWRx #3 and AWRx #4. This allows the system to generate and receive synchronous FMCW chirps across the four device AWRx array of transmitters and receivers.



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The LO distribution follows the star-network configuration described in *AWR2243 Cascade*. The master AWRx feeds a network of two Wilkinson power dividers, which in turn provide synchronous LO for the Master and Slave PA and mixer subsystems. All clock distribution, synchronization distribution and LO distribution requirements are documented in this referenced application note.

The Cascade RF board accepts 5V DC, 8A (max) power primarily through the host board connectors J4 and J5. A separate 6-pin power connector (J6) is available as an alternate power path. The primary 5V system rail provided by the host board is converted into the variousAWRx device rails by the LP87524P quad-channel, monolithic, buck-converter.

## 2.2 Attaching the MMWAVCAS-RF-EVM to the MMWAVCAS-DSP-EVM

The MMWAVCAS-RF-EVM is designed to operate attached to the companion MMWAVCAS-DSP-EVM host board. The MMWAVCAS-DSP-EVM host board provides 5.0 V power and all necessary control signals to reset, boot and loadAWRx firmware.

The two boards are attached and aligned through the the Host Board Connector #1 (J4) and Host Board Connector #2 (J5). These two connectors are keyed to prevent incorrect, 180°, opposite orientation. Also, the four corner mounting holes and the overall board outlines match between the MMWAVCAS-RF-EVM and MMWAVCAS-DSP-EVM host board. Simply depressing the J4 and J5 connectors into their opposing connector pairs on the MMWAVCAS-DSP-EVM will connect the two EVM. Additional 25 mm mounting stand-offs and screws should be used to secure the two boards together into a single assembly.

Section 2.5.1 discusses the host board connectors.

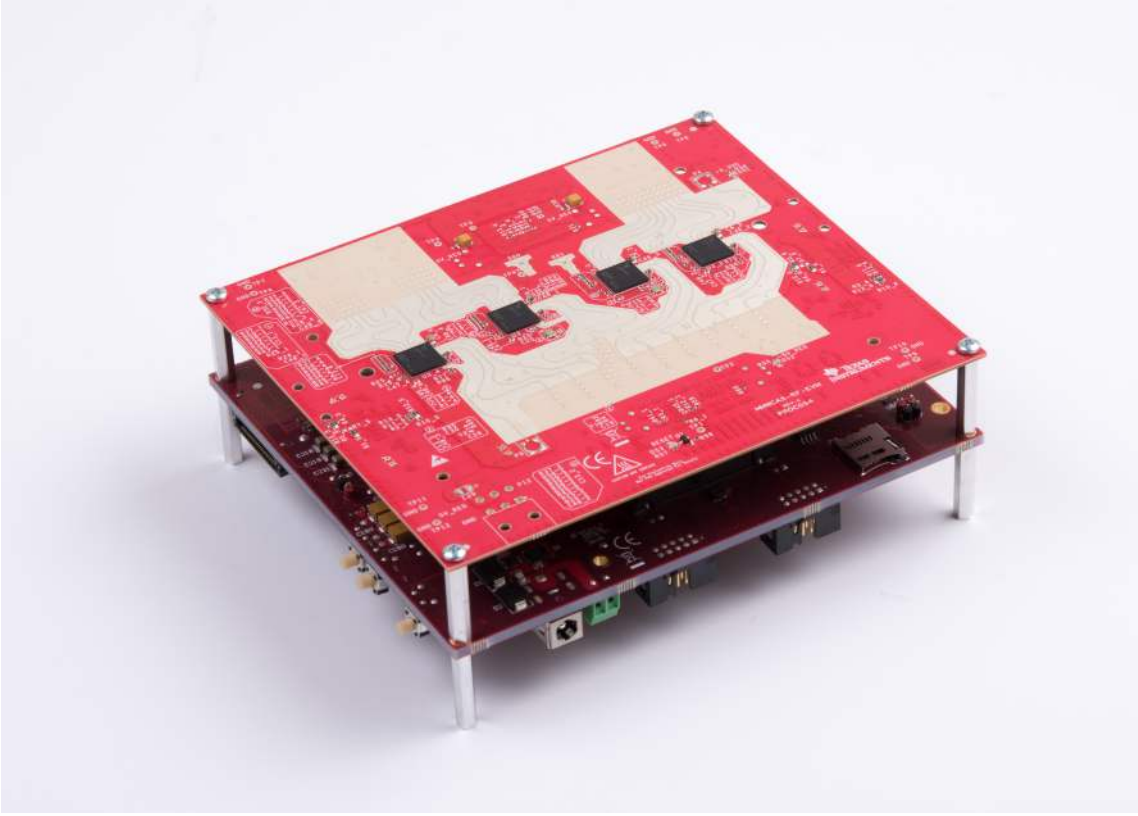

**Figure 5. MMWAVCAS-RF-EVM (top) attached to the MMWAVCAS-DSP-EVM (bottom)**

For additional information on the MMWAVCAS-DSP-EVM, see the MMWAVCAS-DSP-EVM User's Guide on the associated technical documents collateral.


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## 2.3 Power Status LED Indicators

The MMWAVCAS-RF-EVM board provides two LED for visually evaluating 5.0 V and 3.3 V system power status. The 5.0 V LED will be enabled as soon as 5 V power is provided to the system through either the primary host connectors (J4, J5) or through the bench power connector J6. The 3.3 V LED will be enabled as soon as the TPS73733 LDO (U5) output is enabled. TPS73733 3.3 V power is enabled through the GPIO2 output of LP87524P PMIC #1 (U3) as the last stage of the PMIC power on sequence.

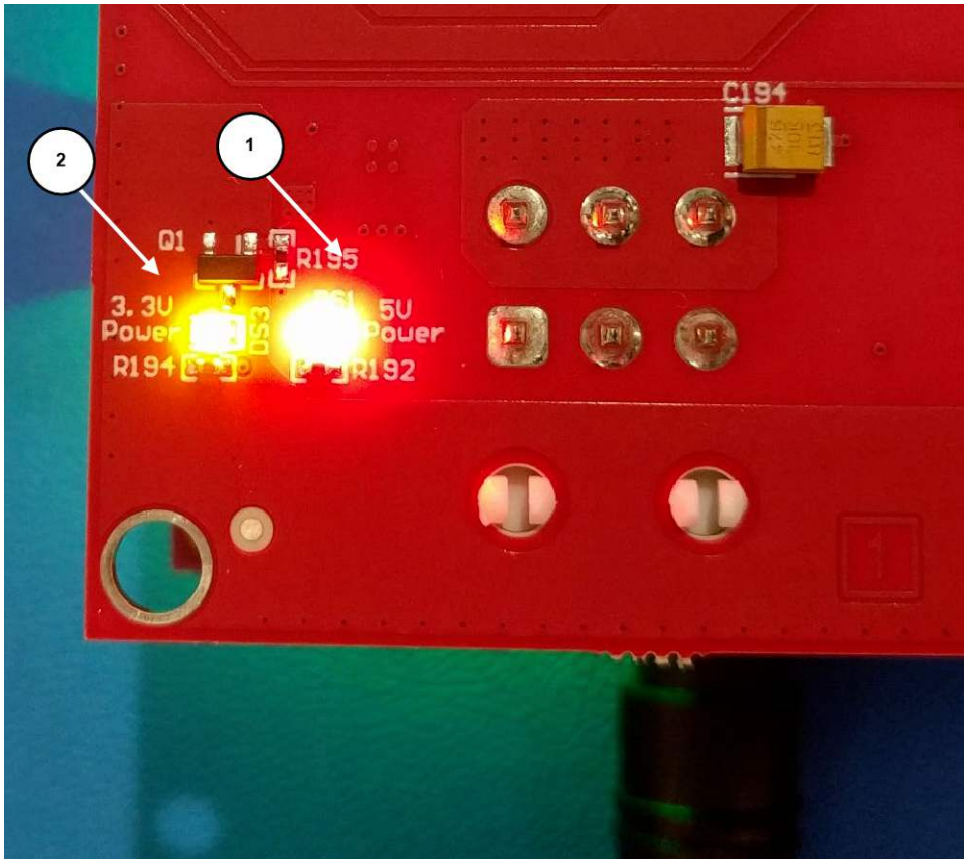


**Figure 6. MMWAVCAS-RF-EVM Power Status LED Indicators**

Power Satus LED Callouts:

1. 5 V Power On LED (DS1) - Red LED active when 5 V power is available to MMWAVCAS-RF-EVM board
2. 3.3 V Power On LED (DS3) - Amber LED active when TPS73733 LDO (U5) 3.3V output is enabled



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## 2.4 Reset LED Indicators

The MMWAVCAS-RF-EVM board provides four LED for visually evalutingAWRx NRESET status. The NRESET is generated from a combination of PMIC #1 and PMIC #2 power good outputs and host board NRESET signals. When powering on the MMWAVCAS-RF-EVM from the MMWAVCAS-DSP-EVM the NRESET signals will be initially de-asserted. A full reset sequence will be driven later by the TDA2 host processor to initialize the AWRx devices.

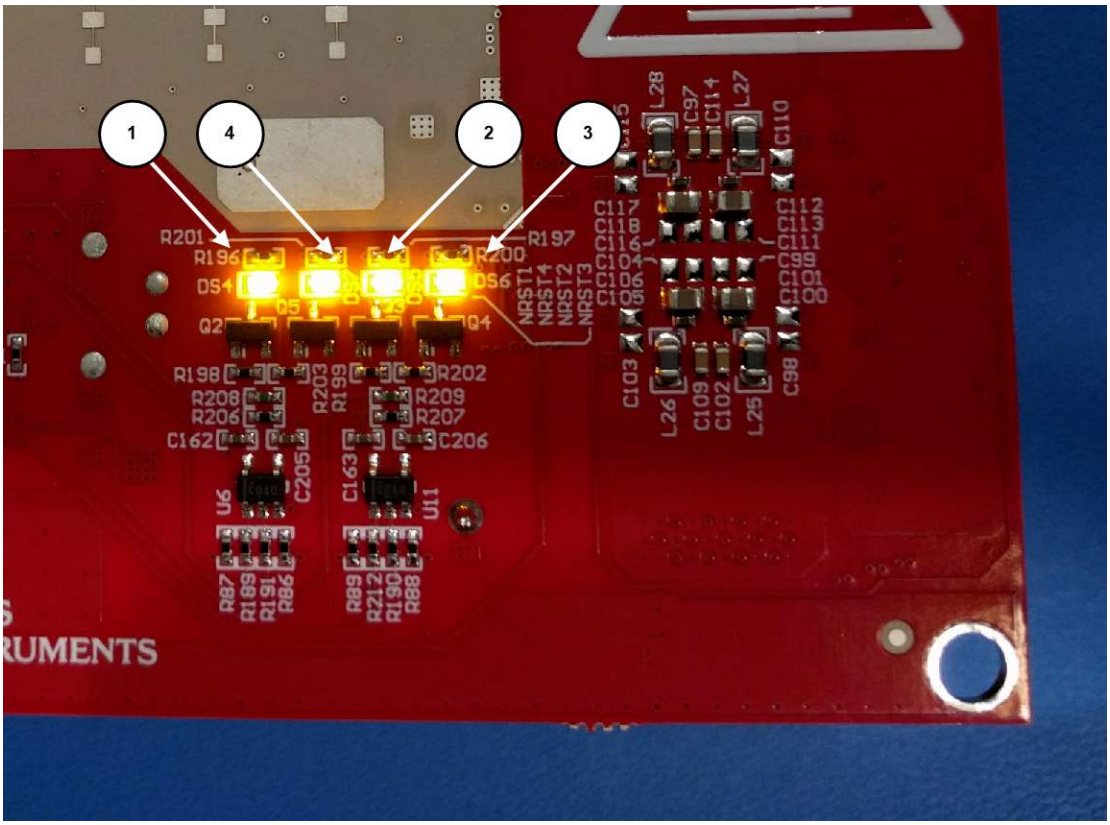


**Figure 7. MMWAVCAS-RF-EVM AWRx NRESET Status LED Indicators**

Reset Status LED Callouts:

1. AWRx #1 NRESET LED (DS4) - Amber LED active when NRESET is de-asserted (logic high)
2. AWRx #2 NRESET LED (DS5) - Amber LED active when NRESET is de-asserted (logic high)
3. AWRx #3 NRESET LED (DS6) - Amber LED active when NRESET is de-asserted (logic high)
4. AWRx #4 NRESET LED (DS7) - Amber LED active when NRESET is de-asserted (logic high)


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## 2.5 Connectors

To keep out of the field of view of the etched antenna array on the top layer (front) of the board, all connectors are placed on the bottom layer (back) of the board.

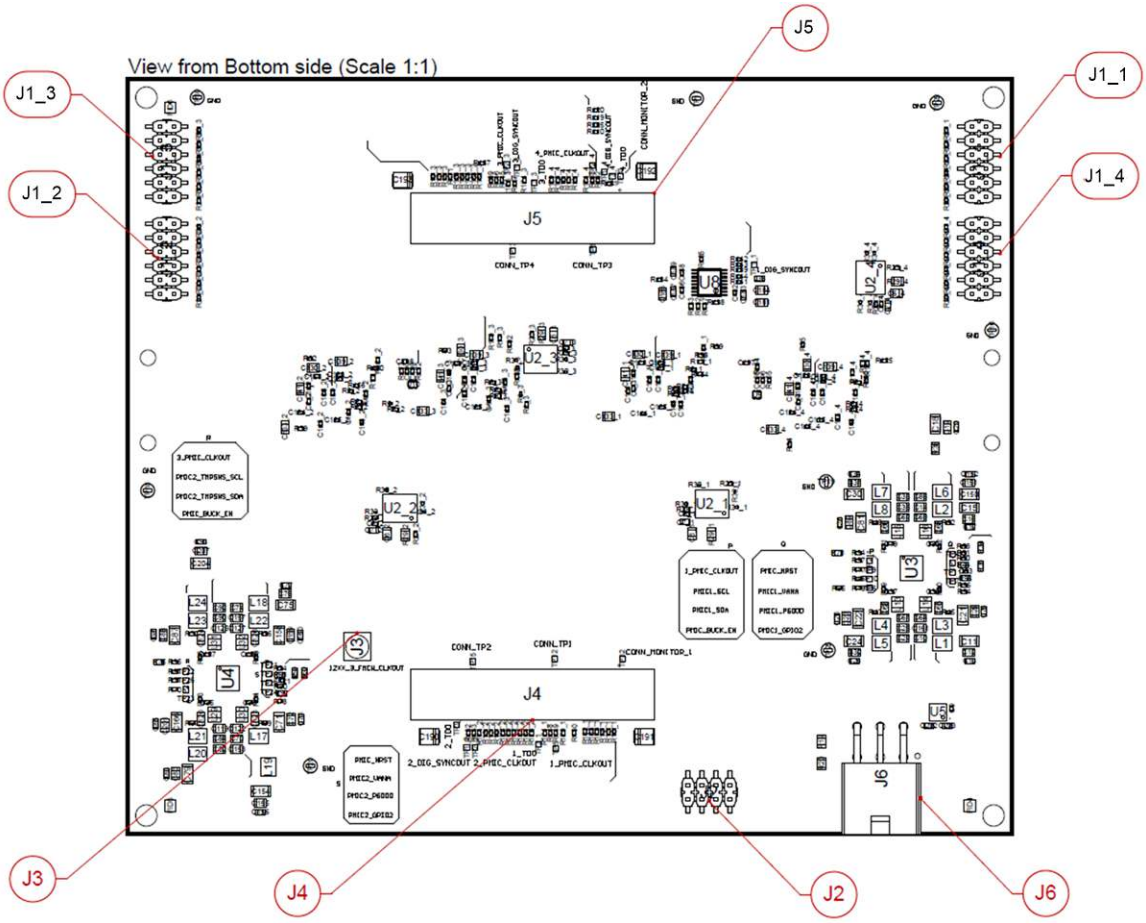


**Figure 8. MMWCAS-RF-EVM (Bottom-View) Connector Placements and Callouts**

Connector Callouts

- J6 - Auxillary Power Connector
- J4 - Host Board Connector (AWRx #1, AWRx #2)
- J5 - Host Board Connector (AWRx #3, AWRx #4)
- J3 - 20 GHz LO Debug Connecctor
- J2 - AWR OSC_CLKOUT Debug Header
- J1_1 - AWRx #1 Debug Header
- J1_2 - AWRx #2 Debug Header
- J1_3 - AWRx #3 Debug Header
- J1_4 - AWRx #4 Debug Header



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### 2.5.1 Host Board Connectors(J4, J5)

The primary connector set on the MMWAVCAS-RF-EVM is the host board connector #1 (J4) and host board connector #2 (J5). These connectors are each implemeted with a Hirose FX23-120P-0.5SV15 Header. Connector #1 pinout containss all of the reset, boot, digital control and CSI2.0 data paths forAWRx #1 and AWRx #2. Connector #2 pinout contains the same for AWRx #3 and AWRx #4. Both connectors share a common 5.0 V power and GND return path. Primary power to the MMWCAS-RF-EVM is expected to be provided from a compatible host board through these connectors.

**WARNING**

**It is required that any attached host board provide 5.0 V power conditioning. No 5.0 V power rail protection exists on the MMWAVCAS-RF-EVM design itself. The attached host board is expected to provide reverse polarity protectionand turn-on/off transient suppression. This is especially import to note when testing in an automotive alternator/battery powered system. The MMWAVCAS-DSP-EVM host board includes an automotive 12 V input supply rail for this purpose.**


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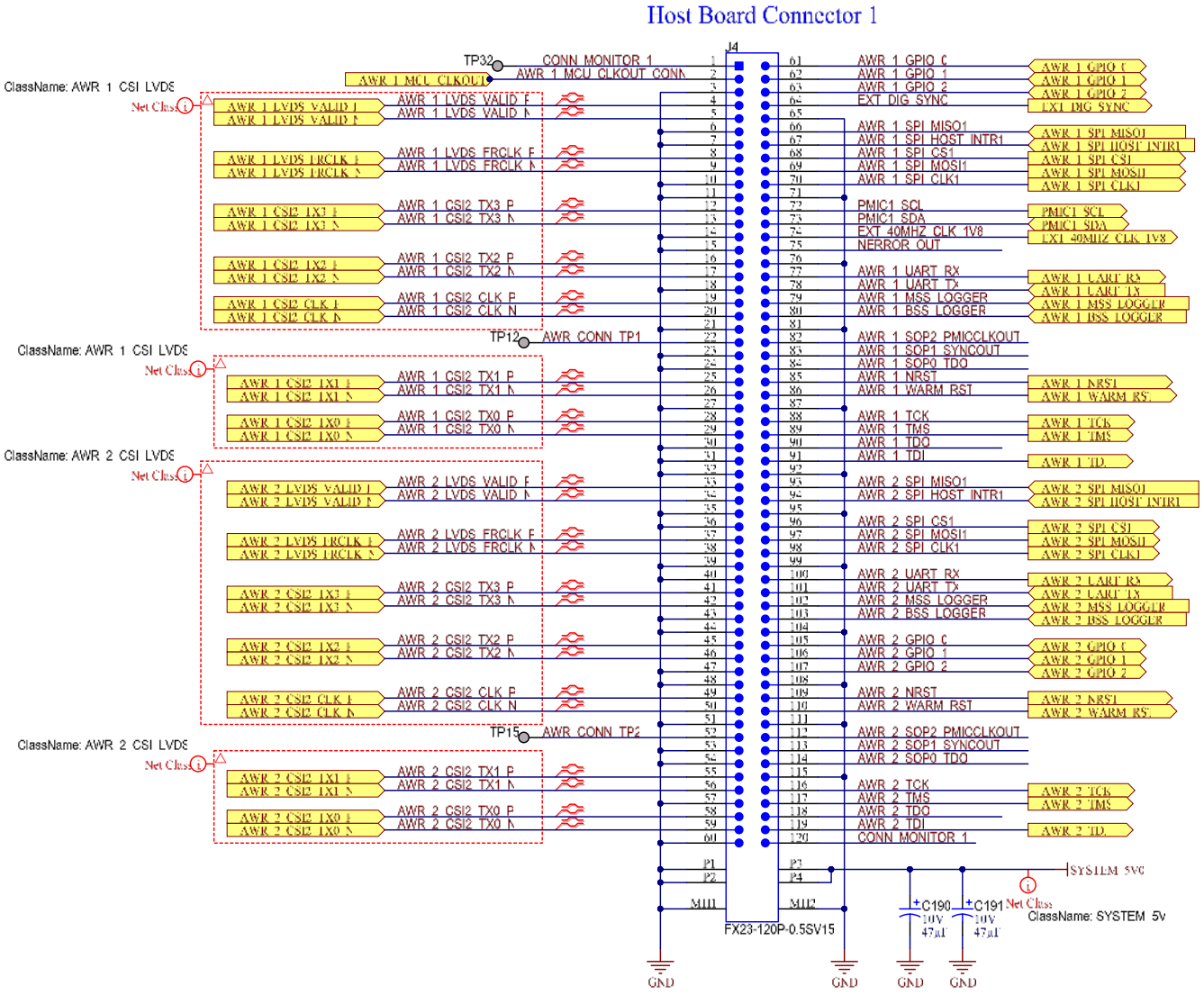


**Figure 9. Host Board Connector #1 (J4), Schematic Excerpt**



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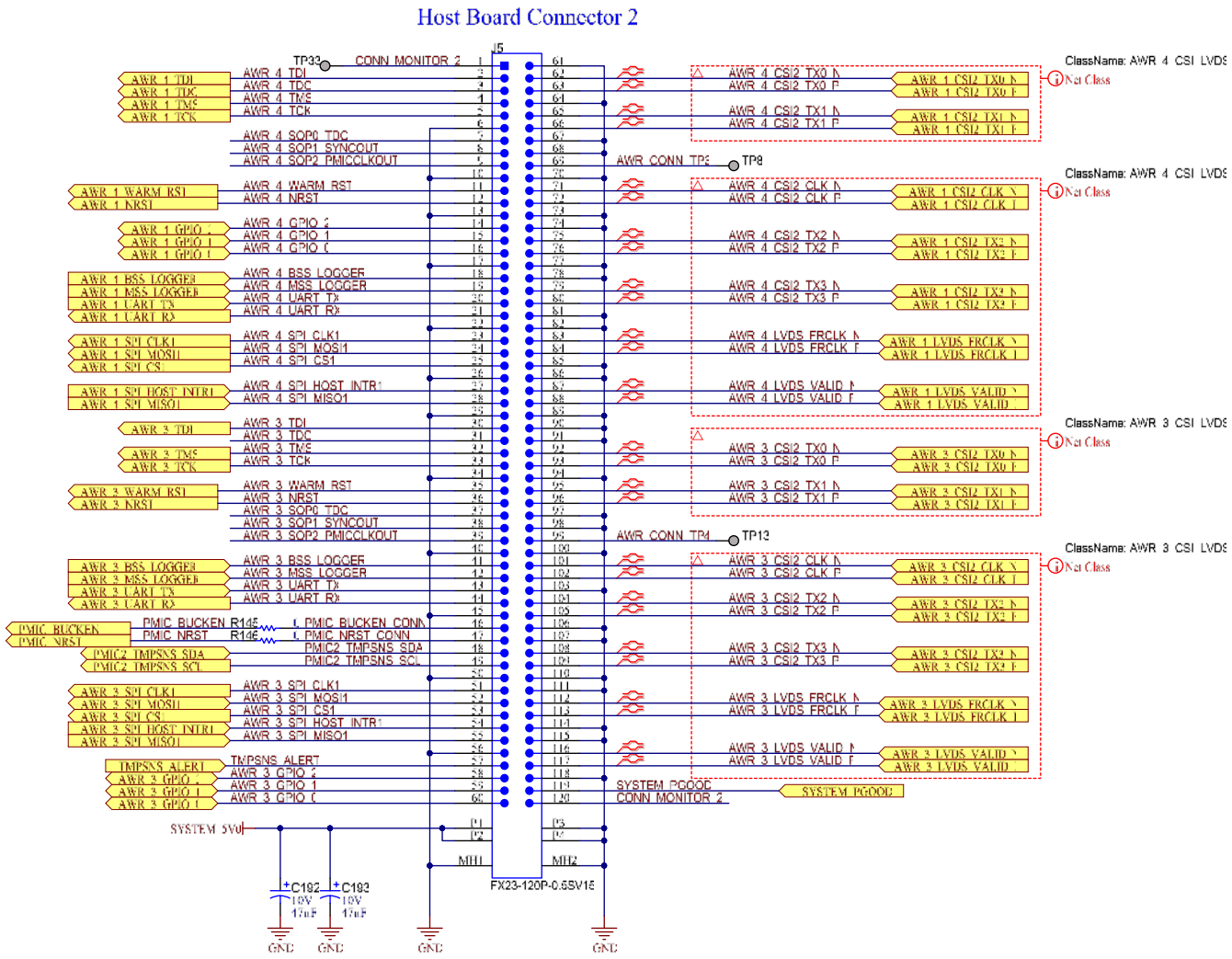


**Figure 10. Host Board Connector #2 (J5), Schematic Excerpt**

**Table 2. Host Board Connector #1 (J4) Connector Definition**

| Pin Number | Pin Name | Pin Type [1] | Pin Description |
|---|---|---|---|
| 1 | CONN_MONITOR_1 | Passive | Connection monitor - To be used with pin 120 |
| 2 | AWR_1_MCU_CLKOUT_CONN | Passive | AWR #1 MCU_CLKOUT |
| 3 | GND | Power | System ground return |
| 4 | AWR_1_LVDS_VALID_P | Output | AWR #1 LVDS |
| 5 | AWR_1_LVDS_VALID_N | Output | AWR #1 LVDS |
| 6 | GND | Power | System ground return |
| 7 | GND | Power | System ground return |
| 8 | AWR_1_LVDS_FRCLK_P | Output | AWR #1 LVDS |
| 9 | AWR_1_LVDS_FRCLK_N | Output | AWR #1 LVDS |
| 10 | GND | Power | System ground return |
| 11 | GND | Power | System ground return |
| 12 | AWR_1_CSI2_TX3_P | Output | AWR #1 CSI2 TX3 |
| 13 | AWR_1_CSI2_TX3_P | Output | AWR #1 CSI2 TX3 |


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**Table 2. Host Board Connector #1 (J4) Connector Definition (continued)**

| Pin Number | Pin Name | Pin Type [1] | Pin Description |
|---|---|---|---|
| 14 | GND | Power | System ground return |
| 15 | GND | Power | System ground return |
| 16 | AWR_1_CSI2_TX2_P | Output | AWR #1 CSI2 TX2 |
| 17 | AWR_1_CSI2_TX2_N | Output | AWR #1 CSI2 TX2 |
| 18 | GND | Power | System ground return |
| 19 | AWR_1_CSI2_CLK_P | Output | AWR #1 CSI2 Clock |
| 20 | AWR_1_CSI2_CLK_N | Output | AWR #1 CSI2 Clock |
| 21 | GND | Power | System ground return |
| 22 | XWR_CONN_TP1 | Passive | Unused |
| 23 | GND | Power | System ground return |
| 24 | GND | Power | System ground return |
| 25 | AWR_1_CSI2_TX1_P | Output | AWR #1 CSI2 TX1 |
| 26 | AWR_1_CSI2_TX1_N | Output | AWR #1 CSI2 TX1 |
| 27 | GND | Power | System ground return |
| 28 | AWR_1_CSI2_TX0_P | Output | AWR #1 CSI2 TX0 |
| 29 | AWR_1_CSI2_TX0_N | Output | AWR #1 CSI2 TX0 |
| 30 | GND | Power | System ground return |
| 31 | GND | Power | System ground return |
| 32 | GND | Power | System ground return |
| 33 | AWR_2_LVDS_VALID_P | Output | AWR #2 LVDS |
| 34 | AWR_2_LVDS_VALID_N | Output | AWR #2 LVDS |
| 35 | GND | Power | System ground return |
| 36 | GND | Power | System ground return |
| 37 | AWR_2_LVDS_FRCLK_P | Output | AWR #2 LVDS |
| 38 | AWR_2_LVDS_FRCLK_N | Output | AWR #2 LVDS |
| 39 | GND | Power | System ground return |
| 40 | GND | Power | System ground return |
| 41 | AWR_2_CSI2_TX3_P | Output | AWR #2 CSI2 TX3 |
| 42 | AWR_2_CSI2_TX3_N | Output | AWR #2 CSI2 TX3 |
| 43 | GND | Power | System ground return |
| 44 | GND | Power | System ground return |
| 45 | AWR_2_CSI2_TX2_P | Output | AWR #2 CSI2 TX2 |
| 46 | AWR_2_CSI2_TX2_N | Output | AWR #2 CSI2 TX2 |
| 47 | GND | Power | System ground return |
| 48 | GND | Power | System ground return |
| 49 | AWR_2_CSI2_CLK_P | Output | AWR #2 CSI2 Clock |
| 50 | AWR_2_CSI2_CLK_N | Output | AWR #2 CSI2 Clock |
| 51 | GND | Power | System ground return |
| 52 | XWR_CONN_TP2 | Passive | Unused |
| 53 | GND | Power | System ground return |
| 54 | GND | Power | System ground return |
| 55 | AWR_2_CSI2_TX1_P | Output | AWR #2 CSI2 TX1 |
| 56 | AWR_2_CSI2_TX1_N | Output | AWR #2 CSI2 TX1 |
| 57 | GND | Power | System ground return |
| 58 | AWR_2_CSI2_TX0_P | Output | AWR #2 CSI2 TX0 |
| 59 | AWR_2_CSI2_TX0_P | Output | AWR #2 CSI2 TX0 |
| 60 | GND | Power | System ground return |



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**Table 2. Host Board Connector #1 (J4) Connector Definition (continued)**

| Pin Number | Pin Name | Pin Type [1] | Pin Description |
|---|---|---|---|
| 61 | AWR1_GPIO0 | Bidirectional | AWR #1 GPIO0 |
| 62 | AWR1_GPIO1 | Bidirectional | AWR #1 GPIO1 |
| 63 | AWR1_GPIO2 | Bidirectional | AWR #1 GPIO2 |
| 64 | EXT_DIG_SYNC | Input | Alternative input to AWRx digital sync fanout buffer (U8) |
| 65 | GND | Power | System ground return |
| 66 | AWR_1_SPI_MISO1 | Output | AWR#1 SPI Slave MISO |
| 67 | AWR_1_SPI_HOST_INTR1 | Output | AWR#1 SPI Slave Interrupt |
| 68 | AWR_1_SPI_CS1 | Input | AWR#1 SPI Slave CS0N |
| 69 | AWR_1_SPI_MOSI1 | Input | AWR#1 SPI Slave MOSI |
| 70 | AWR_1_SPI_CLK1 | Input | AWR#1 SPI Slave SCLK |
| 71 | GND | Power | System ground return |
| 72 | PMIC1_SCL | Input | LP8752 4P (U3) PMIC I2C |
| 73 | PMIC1_SDA | Bidirectional | LP8752 4P (U3) PMIC I2C |
| 74 | EXT_40MHZ_CLK_1V8 | Input | Optional 40 MHz clock input for AWR #1 (U1_1) CLKP. |
| 75 | NERROR_OUT | Input | Open-Drain Logic OR ERROR_OUT from AWR#1, 2, 3 and 4 |
| 76 | GND | Power | System ground return |
| 77 | AWR_1_UART_RX | Input | AWR#1 UART RX |
| 78 | AWR_1_UART_TX | Output | AWR#1 UART TX |
| 79 | AWR_1_MSS_LOGGER | Output | AWR #1 MSS debug log UART output |
| 80 | AWR_1_BSS_LOGGER | Output | AWR #1 MSS debug log UART output |
| 81 | GND | Power | System ground return |
| 82 | AWR_1_SOP2_PMICCLKOUT | Input | AWR#1 PMICCLKOUT/SOP2 |
| 83 | AWR_1_SOP1_SYNCOUT | Input | AWR#1 SYNCOUT/SOP1 signal |
| 84 | AWR_1_SOP0_TDO | Input | AWR#1 TDO/SOP0 signal |
| 85 | AWR_1_NRST | Input | AWR#1 NRESET signal |
| 86 | AWR_1_WARM_RST | Input | AWR#1 WARM_RESET signal |
| 87 | GND | Power | System ground return |
| 88 | AWR_1_TCK | Input | AWR #1 JTAG |
| 89 | AWR_1_TMS | Input | AWR #1 JTAG |
| 90 | AWR_1_TDO | Output | AWR #1 JTAG |
| 91 | AWR_1_TDI | Input | AWR #1 JTAG |
| 92 | GND | Power | System ground return |
| 93 | AWR_2_SPI_MISO1 | Output | AWR#2 SPI Slave MISO |
| 94 | AWR_2_SPI_HOST_INTR1 | Input | AWR#2 SPI Slave Interrupt |
| 95 | GND | Power | System ground return |
| 96 | AWR_2_SPI_CS1 | Input | AWR#2 SPI Slave CS |
| 97 | AWR_2_SPI_MOSI1 | Input | AWR#2 SPI Slave MOSI |
| 98 | AWR_2_SPI_CLK1 | Input | AWR#2 SPI Slave SCLK |
| 99 | GND | Power | System ground return |
| 100 | AWR_2_UART_RX | Output | AWR#2 UART RX - TDA2x TX to AWR RX |
| 101 | AWR_2_UART_TX | Input | AWR#2 UART TX - AWR TX to TDA2x RX |


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**Table 2. Host Board Connector #1 (J4) Connector Definition (continued)**

| Pin Number | Pin Name | Pin Type [1] | Pin Description |
|---|---|---|---|
| 102 | AWR_2_MSS_LOGGER | Output | AWR #1 MSS debug log UART output |
| 103 | AWR_2_BSS_LOGGER | Output | AWR #1 BSS debug log UART output |
| 104 | GND | Power | System ground return |
| 105 | AWR_2_GPIO_0 | Bidirectional | AWR #1 GPIO0 |
| 106 | AWR_2_GPIO_1 | Bidirectional | AWR #1 GPIO1 |
| 107 | AWR_2_GPIO_2 | Bidirectional | AWR #1 GPIO2 |
| 108 | GND | Power | System ground return |
| 109 | AWR_2_NRST | Output | AWR#2 NRESET signal |
| 110 | AWR_2_WARM_RST | Output | AWR#2 WARM_RESET signal |
| 111 | GND | Power | System ground return |
| 112 | AWR_2_SOP2_PMICCLKOUT | Output | AWR#2 PMICCLKOUT/SOP2 |
| 113 | AWR_2_SOP1_SYNCOUT | Output | AWR#2 SYNCOUT/SOP1 signal |
| 114 | AWR_2_SOP0_TDO | Output | AWR#2 TDO/SOP0 signal |
| 115 | GND | Power | System ground return |
| 116 | AWR_2_TCK | Input | AWR #2 JTAG |
| 117 | AWR_2_TMS | Input | AWR #2 JTAG |
| 118 | AWR_2_TDO | Output | AWR #2 JTAG |
| 119 | AWR_2_TDI | Input | AWR #2 JTAG |
| 120 | CONN_MONITOR_1 | Passive | Connection monitor - To be used with pin 1 |
| P1 | GND | Power | Ground return |
| P2 | GND | Power | Ground return |
| P3 | EVM_5V0 | Power | System 5.0V power |
| P4 | EVM_5V0 | Power | System 5.0V power |
| MH1 | GND | Power | Plated mounting hole used for additional ground return |
| MH2 | GND | Power | Plated mounting hole used for additional ground return |

(1) Pin direction relative to the MMWAVCAS-RF-EVM. Output are signals generated by transmitters on the MMWCAS-RF-EVM. Inputs are signal intended for receivers on the MMWCAS-RF-EVM.

**Table 3. Host Board Connector #2 (J5) Connector Definition**

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | CONN_MONITOR_2 | Passive | Connection monitor - To be used with pin 120 |
| 2 | AWR_4_TDI | Input | AWR #4 JTAG |
| 3 | AWR_4_TDO | Output | AWR #4 JTAG |
| 4 | AWR_4_TMS | Input | AWR #4 JTAG |
| 5 | AWR_4_TCK | Input | AWR #4 JTAG |
| 6 | GND | Power | Ground return |
| 7 | AWR_4_SOP0_TDO | Input | AWR#4 TDO/SOP0 |
| 8 | AWR_4_SOP1_SYNCOUT | Input | AWR#4 SYNCOUT/SOP1 |
| 9 | AWR_4_SOP2_PMICCLKOUT | Input | AWR#4 PMICCLKOUT/SOP2 |
| 10 | GND | Power | Ground return |
| 11 | AWR_4_WARM_RST | Input | AWR#4 WARM_RESET signal |


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**Table 3. Host Board Connector #2 (J5) Connector Definition (continued)**

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 12 | AWR_4_NRST | Input | AWR#4 NRESET signal |
| 13 | GND | Power | Ground return |
| 14 | AWR_4_GPIO_2 | Bidirectional | AWR #4 GPIO2 |
| 15 | AWR_4_GPIO_1 | Bidirectional | AWR #4 GPIO1 |
| 16 | AWR_4_GPIO_0 | Bidirectional | AWR #4 GPIO0 |
| 17 | GND | Power | Ground return |
| 18 | AWR_4_BSS_LOGGER | Passive | AWR #4 BSS debug log UART output |
| 19 | AWR_4_MSS_LOGGER | Passive | AWR #4 MSS debug log UART output |
| 20 | AWR_4_UART_TX | Output | AWR #4 UART TX |
| 21 | AWR_4_UART_RX | Input | AWR #4 UART RX |
| 22 | GND | Power | Ground return |
| 23 | AWR_4_SPI_CLK1 | Output | AWR #4 SPI CLK |
| 24 | AWR_4_SPI_MOSI1 | Output | AWR #4 SPI MOSI |
| 25 | AWR_4_SPI_CS1 | Output | AWR #4 SPI CS |
| 26 | GND | Power | Ground return |
| 27 | AWR_4_SPI_HOST_INTR1 | Input | AWR #4 SPI Host Interrupt |
| 28 | AWR_4_SPI_MISO1 | Input | AWR #4 SPI MISO |
| 29 | GND | Power | Ground return |
| 30 | AWR_3_TDI | Input | AWR #3 JTAG |
| 31 | AWR_3_TDO | Output | AWR #3 JTAG |
| 32 | AWR_3_TMS | Input | AWR #3 JTAG |
| 33 | AWR_3_TCK | Input | AWR #3 JTAG |
| 34 | GND | Power | Ground return |
| 35 | AWR_3_WARM_RST | Input | AWR#4 WARM_RESET signal |
| 36 | AWR_3_NRST | Input | AWR#4 NRESET signal |
| 37 | AWR_3_SOP0_TDO | Input | AWR #3 TDO/SOP0 |
| 38 | AWR_3_SOP1_SYNCOUT | Input | AWR #3 SYNCOUT/SOP1 |
| 39 | AWR_3_SOP2_PMICCLKOUT | Input | AWR #3 MICCLKOUT /SOP2 |
| 40 | GND | Power | Ground return |
| 41 | AWR_3_BSS_LOGGER | Passive | AWR #3 BSS debug log UART output |
| 42 | AWR_3_MSS_LOGGER | Passive | AWR #3 MSS debug log UART output |
| 43 | AWR_3_UART_TX | Input | AWR #3 UART TX |
| 44 | AWR_3_UART_RX | Output | AWR #3 UART RX |
| 45 | GND | Power | Ground return |
| 46 | PMIC_BUCKEN_CONN | PassInputive | LP87524P (U3) and (U4) power enable input |
| 47 | PMIC_NRST_CONN | Passive | LP87524P (U3) and (U4) reset input |
| 48 | PMIC2_TMPSNS_SDA | Bidirectional | LP87524P (U4) and TMP112 (U9, U10) I2C |
| 49 | PMIC2_TMPSNS_SCL | Input | LP87524P (U4) and TMP112 (U9, U10) I2C |
| 50 | GND | Power | Ground return |
| 51 | AWR_3_SPI_CLK1 | Input | AWR #3 SPI CLK |
| 52 | AWR_3_SPI_MOSI1 | Input | AWR #3 SPI MOSI |


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**Table 3. Host Board Connector #2 (J5) Connector Definition (continued)**

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 53 | AWR_3_SPI_CS1 | Input | AWR #3 SPI CS |
| 54 | AWR_3_SPI_HOST_INTR1 | Output | AWR #3 SPI Host Interupt |
| 55 | AWR_3_SPI_MISO1 | Output | AWR #3 SPI MISO |
| 56 | GND | Power | Ground return |
| 57 | TMPSNS_ALERT | Output | TMP112 (U9, U10) I2C temperature alert (3.3V open-drain) |
| 58 | AWR_3_GPIO_2 | Bidirectional | AWR #3 GPIO2 |
| 59 | AWR_3_GPIO_1 | Bidirectional | AWR #3 GPIO1 |
| 60 | AWR_3_GPIO_0 | Bidirectional | AWR #3 GPIO0 |
| 61 | GND | Power | Ground return |
| 62 | AWR_4_CSI2_TX0_N | Output | AWR #4 CSI2 TX0 |
| 63 | AWR_4_CSI2_TX0_P | Output | AWR #4 CSI2 TX0 |
| 64 | GND | Power | Ground return |
| 65 | AWR_4_CSI2_TX1_N | Output | AWR #4 CSI2 TX1 |
| 66 | AWR_4_CSI2_TX1_P | Output | AWR #4 CSI2 TX1 |
| 67 | GND | Power | Ground return |
| 68 | GND | Power | Ground return |
| 69 | XWR_CONN_TP3 | Passive | Unused |
| 70 | GND | Power | Ground return |
| 71 | AWR_4_CSI2_CLK_N | Output | AWR #4 CSI2 Clock |
| 72 | AWR_4_CSI2_CLK_P | Output | AWR #4 CSI2 Clock |
| 73 | GND | Power | Ground return |
| 74 | GND | Power | Ground return |
| 75 | AWR_4_CSI2_TX2_N | Output | AWR #4 CSI2 TX2 |
| 76 | AWR_4_CSI2_TX2_P | Output | AWR #4 CSI2 TX2 |
| 77 | GND | Power | Ground return |
| 78 | GND | Power | Ground return |
| 79 | AWR_4_CSI2_TX3_P | Output | AWR #4 CSI2 TX3 |
| 80 | AWR_4_CSI2_TX3_P | Output | AWR #4 CSI2 TX3 |
| 81 | GND | Power | Ground return |
| 82 | GND | Power | Ground return |
| 83 | AWR_4_LVDS_FRCLK_N | Output | AWR #4 LVDS |
| 84 | AWR_4_LVDS_FRCLK_P | Output | AWR #4 LVDS |
| 85 | GND | Power | Ground return |
| 86 | GND | Power | Ground return |
| 87 | AWR_4_LVDS_VALID_N | Output | AWR #4 LVDS |
| 88 | AWR_4_LVDS_VALID_P | Output | AWR #4 LVDS |
| 89 | GND | Power | Ground return |
| 90 | GND | Power | Ground return |
| 91 | GND | Power | Ground return |
| 92 | AWR_3_CSI2_TX0_N | Output | AWR #3 CSI2 TX |
| 93 | AWR_3_CSI2_TX0_P | Output | AWR #3 CSI2 TX0 |
| 94 | GND | Power | Ground return |
| 95 | AWR_3_CSI2_TX1_N | Output | AWR #3 CSI2 TX1 |
| 96 | AWR_3_CSI2_TX1_P | Output | AWR #3 CSI2 TX1 |
| 97 | GND | Power | Ground return |



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**Table 3. Host Board Connector #2 (J5) Connector Definition (continued)**

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 98 | GND | Power | Ground return |
| 99 | XWR_CONN_TP4 | Passive | Unused |
| 100 | GND | Power | Ground return |
| 101 | AWR_3_CSI2_CLK_N | Output | AWR #3 CSI2 TX2 |
| 102 | AWR_3_CSI2_CLK_P | Output | AWR #3 CSI2 TX2 |
| 103 | GND | Power | Ground return |
| 104 | AWR_3_CSI2_TX2_N | Input | AWR #3 CSI2 TX2 |
| 105 | AWR_3_CSI2_TX2_P | Input | AWR #3 CSI2 TX2 |
| 106 | GND | Power | Ground return |
| 107 | GND | Power | Ground return |
| 108 | AWR_3_CSI2_TX3_N | Input | AWR #3 CSI2 TX3 |
| 109 | AWR_3_CSI2_TX3_P | Input | AWR #3 CSI2 TX3 |
| 110 | GND | Power | Ground return |
| 111 | GND | Power | Ground return |
| 112 | AWR_3_LVDS_FRCLK_N | Passive | AWR #3 LVDS |
| 113 | AWR_3_LVDS_FRCLK_P | Passive | AWR #3 LVDS |
| 114 | GND | Power | Ground return |
| 115 | GND | Power | Ground return |
| 116 | AWR_3_LVDS_VALID_N | Passive | AWR #3 LVDS |
| 117 | AWR_3_LVDS_VALID_P | Passive | AWR #3 LVDS |
| 118 | GND | Power | Ground return |
| 119 | SYSTEM_PGOOD | Output | System power good. Wired logic OR from LP87524P (U3, U4) PMIC. |
| 120 | CONN_MONITOR_2 | Passive | Connection monitor - To be used with pin 1 |
| P1 | SYSTEM_5V0 | Power | System 5.0V power |
| P2 | SYSTEM_5V0 | Power | System 5.0V power |
| P3 | GND | Power | Ground return |
| P4 | GND | Power | Ground return |
| MH1 | GND | Power | Ground return |
| MH2 | GND | Power | Ground return |


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### 2.5.2 Bench Power Connector(J6)

A separate, 6-pin, Molex Minifit Jr connector provides for the connection of bench 5.0 V power to the MMWAVCAS-RF-EVM. 5.0 V power, GND return and a 5.0 V sense and GND sense path are also provided for a 4-terminal, "Kelvin" connection.

**NOTE:** The Host Board Connectors, J4, and J5 are the primary 5.0 V power inputs to the MMWCAS-RF-EVM. If this bench power connector, J6, is to be used, an attached host board should ensure that either the J4, J5, 5.0 V nets are being supplied from the same supply sourcing J6, **or** that the 5.0 V nets on J4 and J5 are open and not providing 5.0 V power to the MMWCAS-RF-EVM.

The MMWCAS-DSP-EVM host board has no method of disconnecting these 5.0 V power nets and therefore it is incompatible with this J6 bench power connector.

**WARNING**

**It is required that any attached host board provide 5.0V power conditioning. No 5.0 V rail protection exists on the MMWAVCAS-RF-EVM design itself. The attached host board is expected to provide reverse polarity protection and turn-on/off transient suppression. This is especially import to note when testing in an automotive alternator/battery powered system.**

**Table 4. Bench Power Connector (J6)**

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | GND_SENSE | Power | GND return sense path |
| 2 | GND | Power | GND return |
| 3 | GND | Power | GND return |
| 4 | SYSTEM_5V0_SENSE | Power | 5.0V sense path |
| 5 | SYSTEM_5V0 | Power | 5.0V System Power |
| 6 | SYSTEM_5V0 | Power | 5.0V System Power |

### 2.5.3 20 GHz LO Debug Connector (J3)

J3 is a footprint for a Rosenberger model 19S101-40ML5, 50-Ω, SMP connector capable of 26 GHz operation with very low loss and reflection. This connector exposes the AWR_3_FMCW_CLKOUT 20 GHz local oscillator (LO) net from AWR #3. Depending on how the AWR #3 is configured, this connector allows the user to sample an example AWR master-mode or slave-mode LO output signal. This connector is not installed by default.

### 2.5.4 AWR OSC_CLKOUT Debug Header (J2)

A footprint for terminal strip of 25 mil square posts, 100 mil pitch, are provided to enable sampling of the AWR #1, #2, #3 and #4 OSC_CLKOUT paths. These terminal strips are not installed by default.

### 2.5.5 AWR Debug Headers (J1_1, J1_2, J1_3, J1_4)

A footprint for terminal strip of 25 mil square posts, 100 mil pitch, are provided to enable sampling of the AWR #1, #2, #3 and #4 GPADC debug headers. These terminal strips are not installed by default.



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## 2.6 Antennas

Each of the 12 TX channels and 16 RX channels (across the four AWRx cascaded radar devices) is routed to an etched antenna element. This antenna array allows for the creation of MIMO and TX-Beamforming array generation, allowing for high angular resolution and longer range detection of targets in a 3D space.

The antenna array axes are defined such that the azimuth axis is along the XZ-plane with azimuth bore-sight along the +Z-axis. Likewise, the elevation axis is along the YZ-plane with elevation bore-sight along the +Z-axis. Antenna patterns presented are relative to these axes as well. The E-plane defined polarization (Phi = 90 in spherical coordinates) being along the YZ-plane and the H-plane being (Phi = 0 in spherical coordinates) along the XZ-plane.

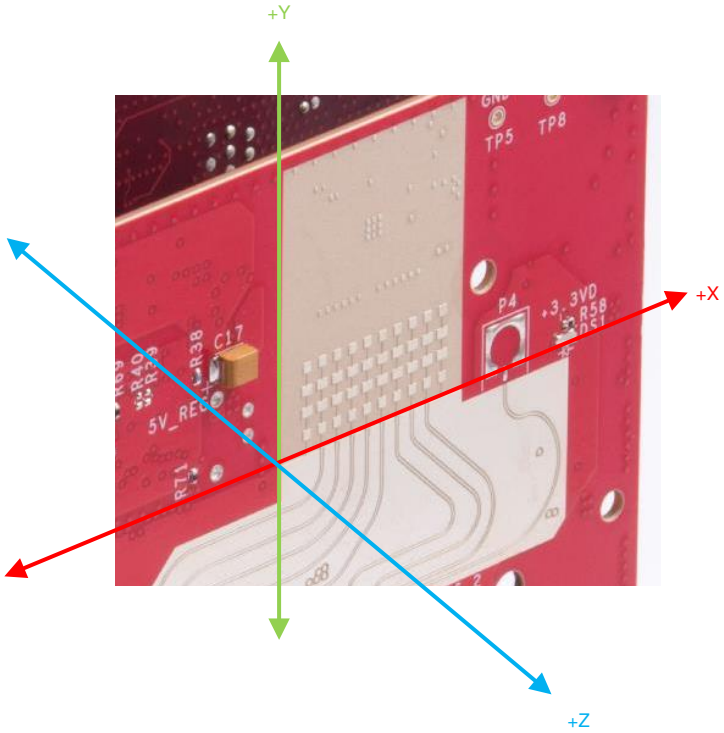


**Figure 11. Antenna Axes Definition**


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### 2.6.1 TX and RX Antenna Arrays

The following sections describe the TX and RX antenna array structures included on the board. The element spacing information can be used to form the necessary processing models of the MIMO virtual array and Beam-Forming phased array.

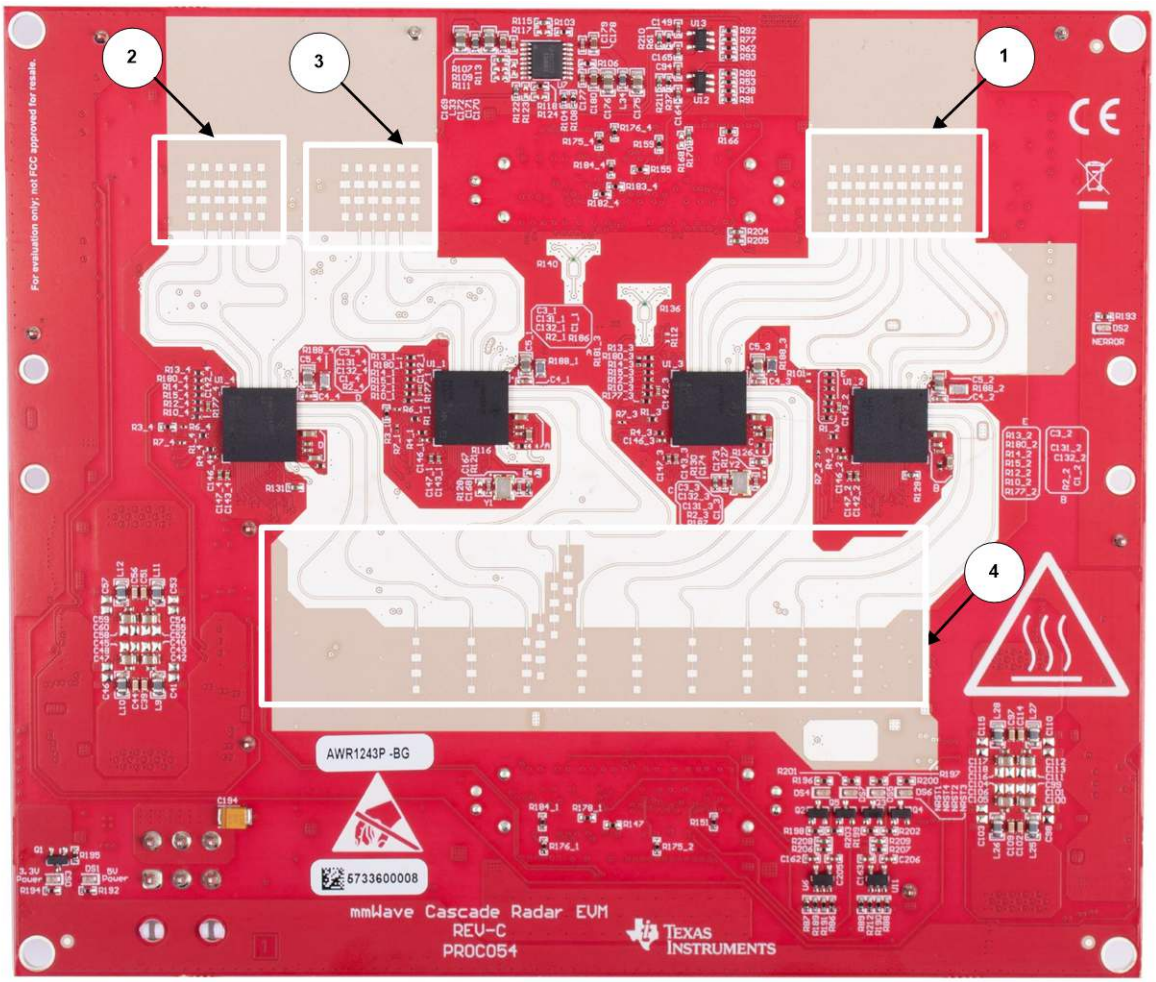


**Figure 12. PCB Antenna Arrays**

Reset Status LED Callouts:

1. RX Array A - 8, lambda/2, linear elements - azimuth displacement only
2. RX Array B – 4, lambda/2, linear elements - azimuth displacement only
3. RX Array C – 4, lambda/2, linear elements - azimuth displacement only
4. TX array – 9, lambda × 2, linear elements in azimuth. 4 minimum redundancy array (MRA) elements in elevation.



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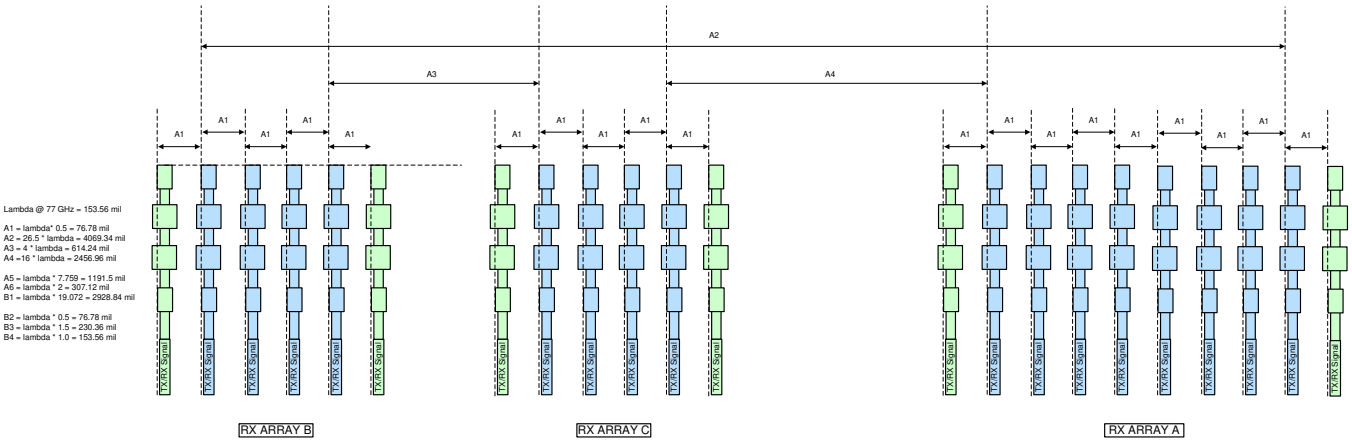


**Figure 13. RX Antenna Array Dimensions**

**Table 5. RX Antenna Array Dimensions**

| Dimension Label | Dimension (mils) | Dimension (78.5 GHz lambda) |
|---|---|---|
| A1 | 76.78 | 0.5 |
| A2 | 4069.34 | 26.5 |
| A3 | 614.24 | 4.0 |
| A4 | 2456.96 | 16.0 |

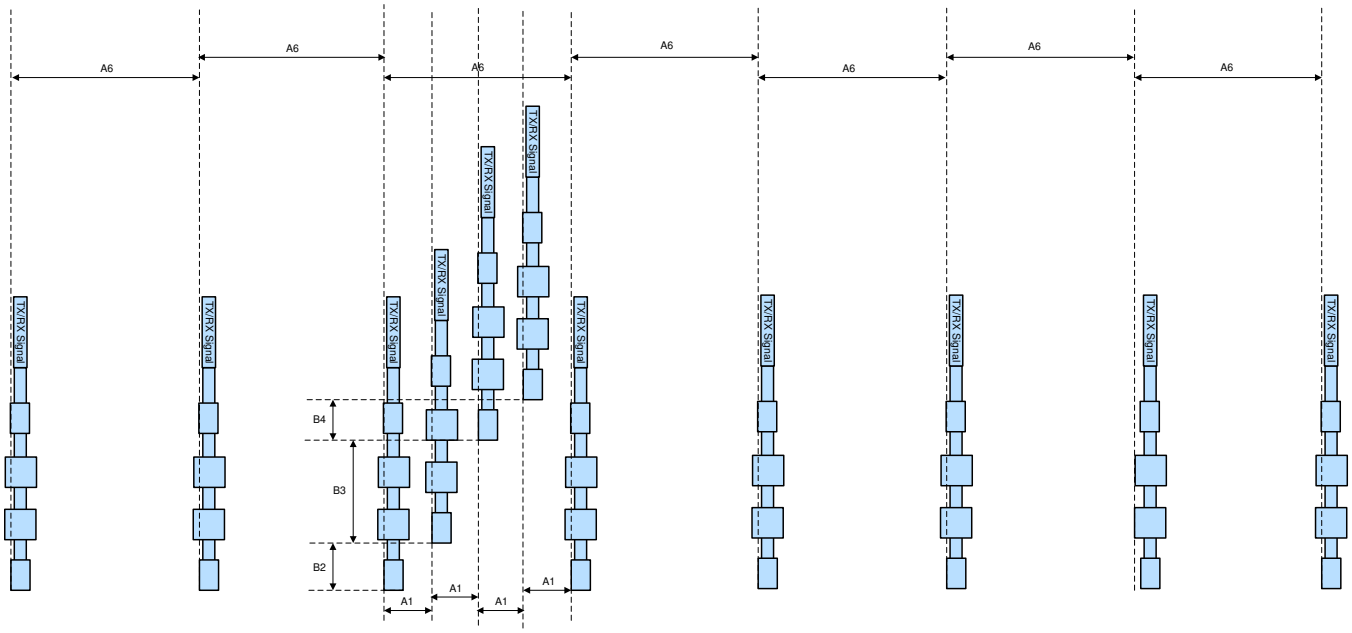


**Figure 14. TX Antenna Array Dimensions**

**Table 6. TX Antenna Array Dimensions**

| Dimension Label | Dimension (mils) | Dimension (77 GHz lambda) |
|---|---|---|
| A1 | 76.78 | 0.5 |
| A5 | 1191.5 | 7.759 |
| A6 | 307.12 | 2.0 |



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**Table 6. TX Antenna Array Dimensions (continued)**

| Dimension Label | Dimension (mils) | Dimension (77 GHz lambda) |
|---|---|---|
| B1 | 2928.84 | 19.072 |
| B2 | 76.78 | 0.5 |
| B3 | 230.36 | 1.5 |
| B4 | 153.56 | 1.0 |

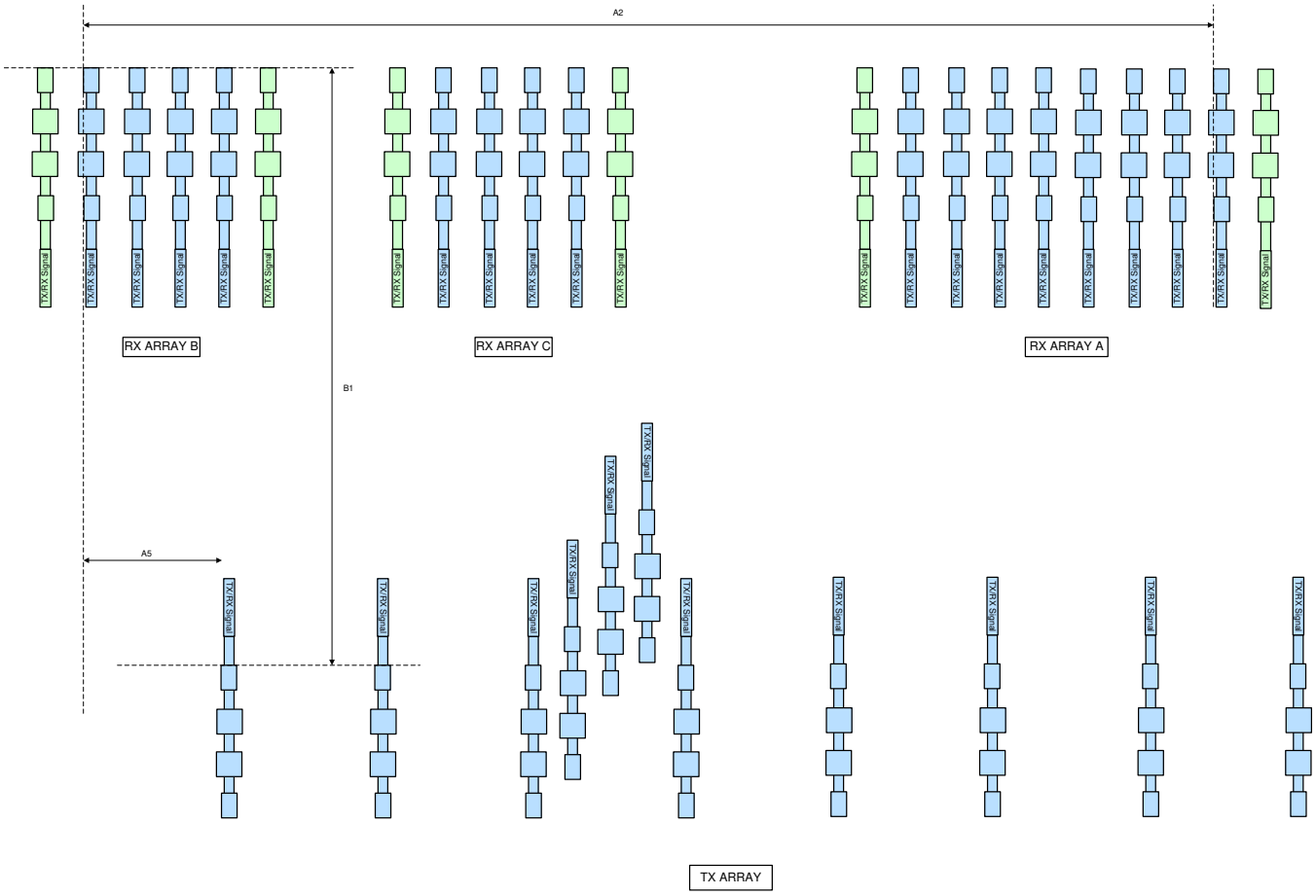


**Figure 15. TX and RX Antenna Array Relative Dimensions**



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### 2.6.2 PCB Antenna Element

Each TX/RX antenna element is implemented as a series-fed, Microstrip patch array. The following figures and tables describe this antenna element. The element is implemted with a GCPW feed to Microstrip transition, and then Microstrip stub matching into the first patch of the seried-fed array.

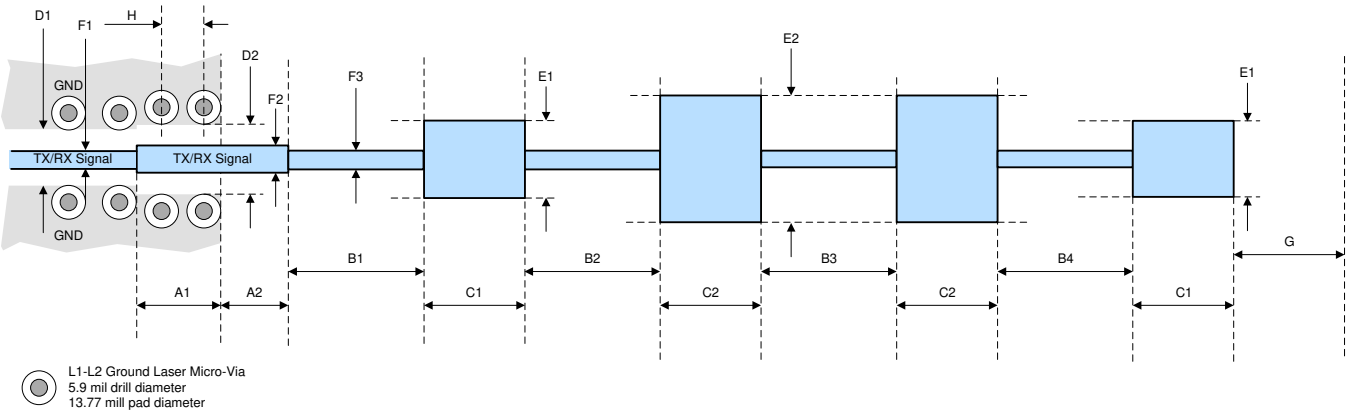


**Figure 16. Cascade RF Series-Fed, Microstrip Patch Array Antenna Element Dimensions**

**Table 7. Cascade RF Series-Fed, Microstrip Patch Array Antenna Element Dimensions**

| Dimension Label | Dimension (mils) |
|---|---|
| A1 | 27.568 |
| A2 | 11.802 |
| B1 | 47.24 |
| B2 | 49.21 |
| B3 | 45.27 |
| B4 | 49.21 |
| C1 | 42.52 |
| C2 | 40.95 |
| D1 | 16.722 |
| D2 | 20.002 |
| E1 | 39.38 |
| E2 | 55.12 |
| F1 | 8.4 |
| F2 | 10.62 |
| F3 | 3.94 |
| G (1) | > 78.7402 |
| H | <= 20.67 |

(1) Dimension G is the is the minimum keepout from any structure adjacent to the antenna (vias, traces, copper pours, and so forth).


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#### 2.6.2.1 RX Antenna Element Performance

Simulated RX antenna performance from RX Array A is shown below. Three different RX antenna were excerpted to show the overall performance across the array. These excerpted antenna are labeled RX1, RX4 and RX8 shown. This selection is meant to highlight behavior of the RX antenna near the edge of the RX antenna rrays and near the center of the arrays. Due to coupling between antenna, the performance near the edge of the array changes from the performance near the center of the array.

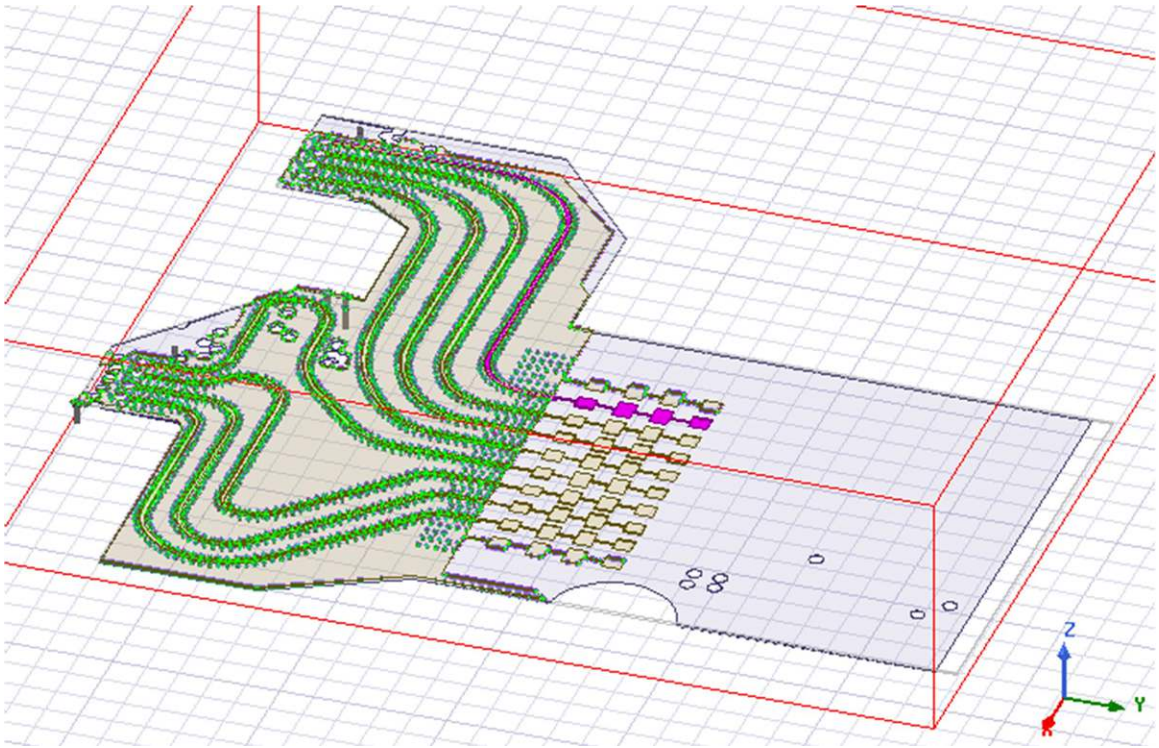


**Figure 17. RX Array A Execerpt for Simulation (RX1 at the "top" of the image, RX8 at the "bottom" of the image. RX1 highlighted in purple.)**



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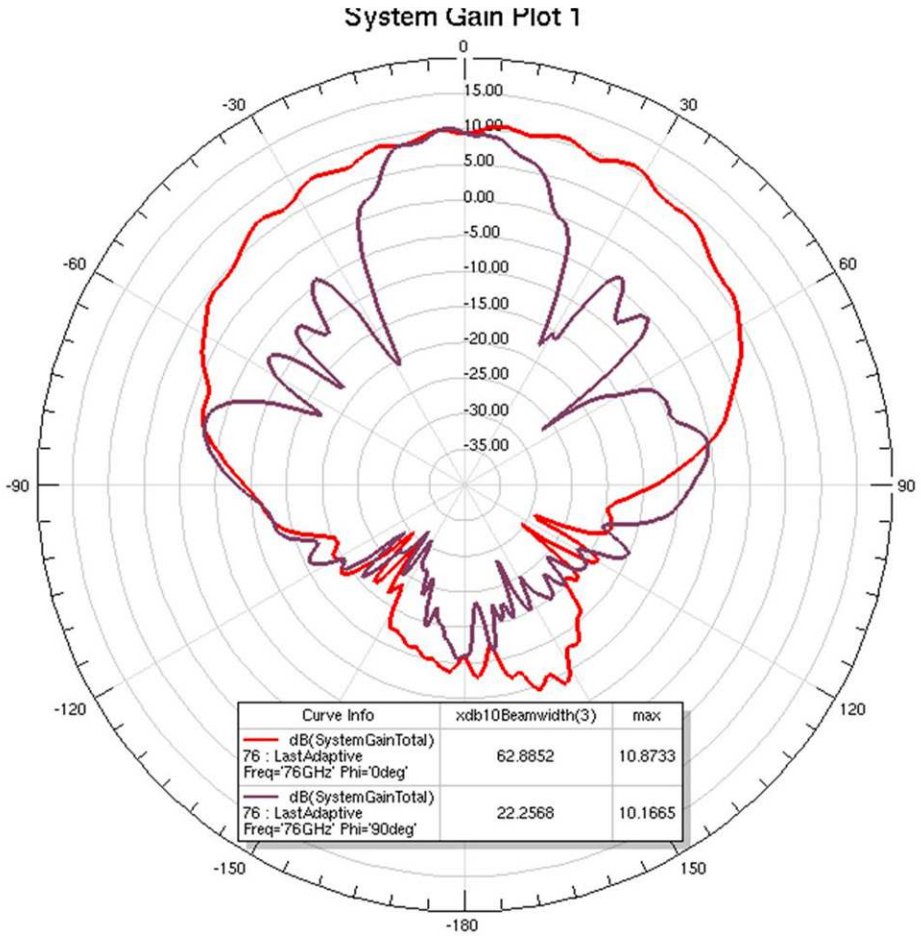


**Figure 18. RX Array A, RX1, 76 GHz Operation (Maximum E-plane (Phi = 90) and H-plane (Phi = 0) slices shown. 3dB beamwidths shown.)**


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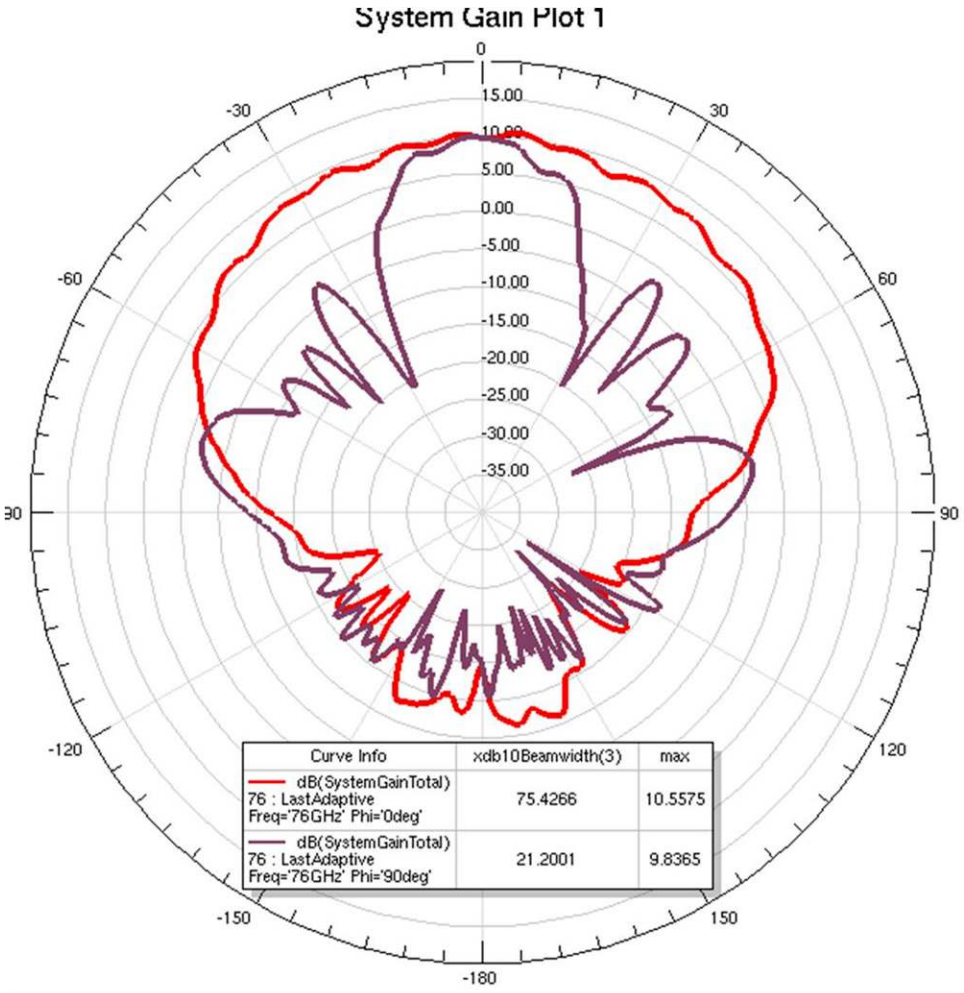


**Figure 19. RX Array A, RX4, 76 GHz Operation (Maximum E-plane (Phi = 90) and H-plane (Phi = 0) slices shown. 3dB beamwidths shown.)**



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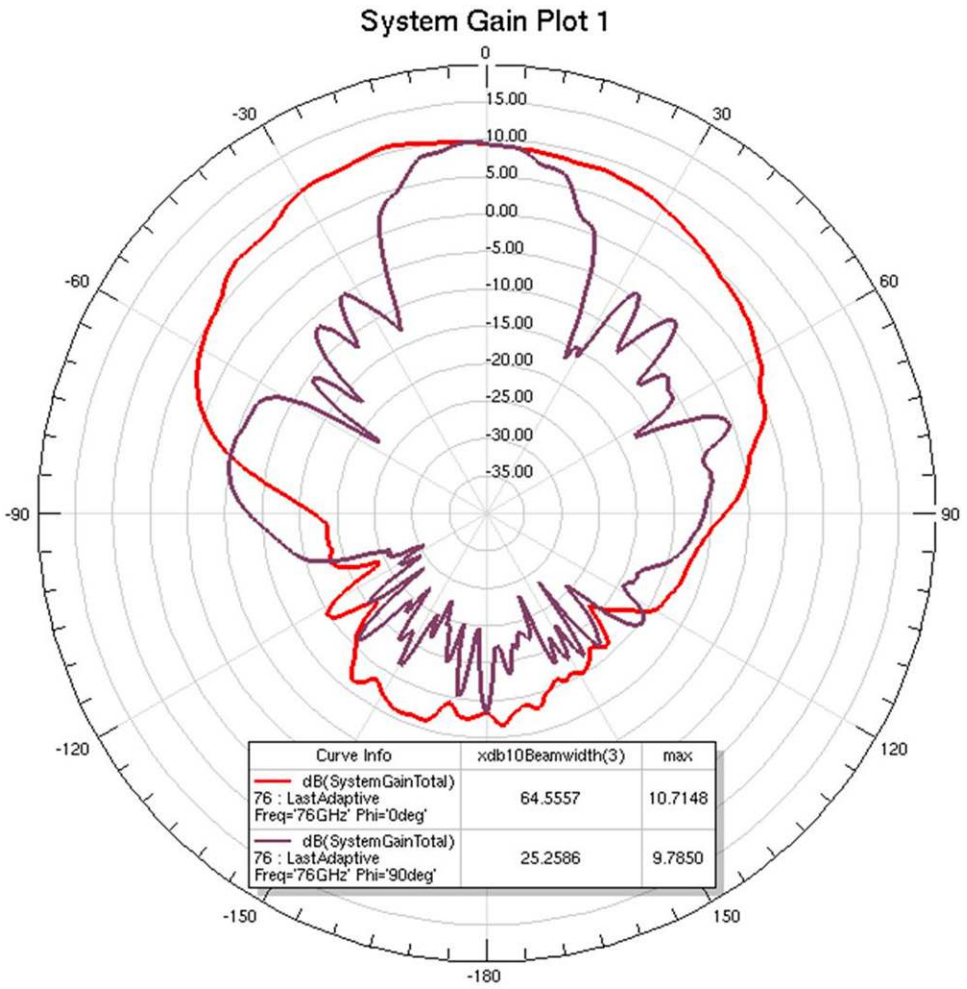


**Figure 20. RX Array A, RX8, 76 GHz Operation (Maximum E-plane (Phi = 90) and H-plane (Phi = 0) slices shown. 3dB beamwidths shown.)**


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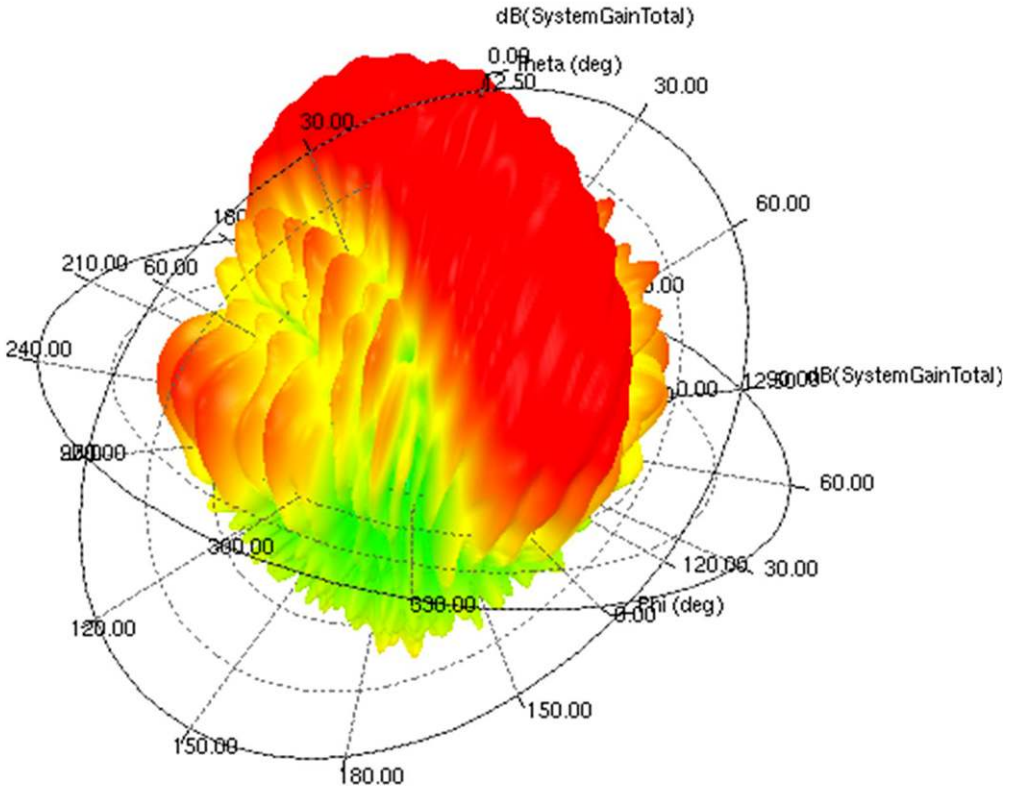


**Figure 21. RX Array A, RX4, 76 GHz Operation (3D Antenna Gain Pattern)**



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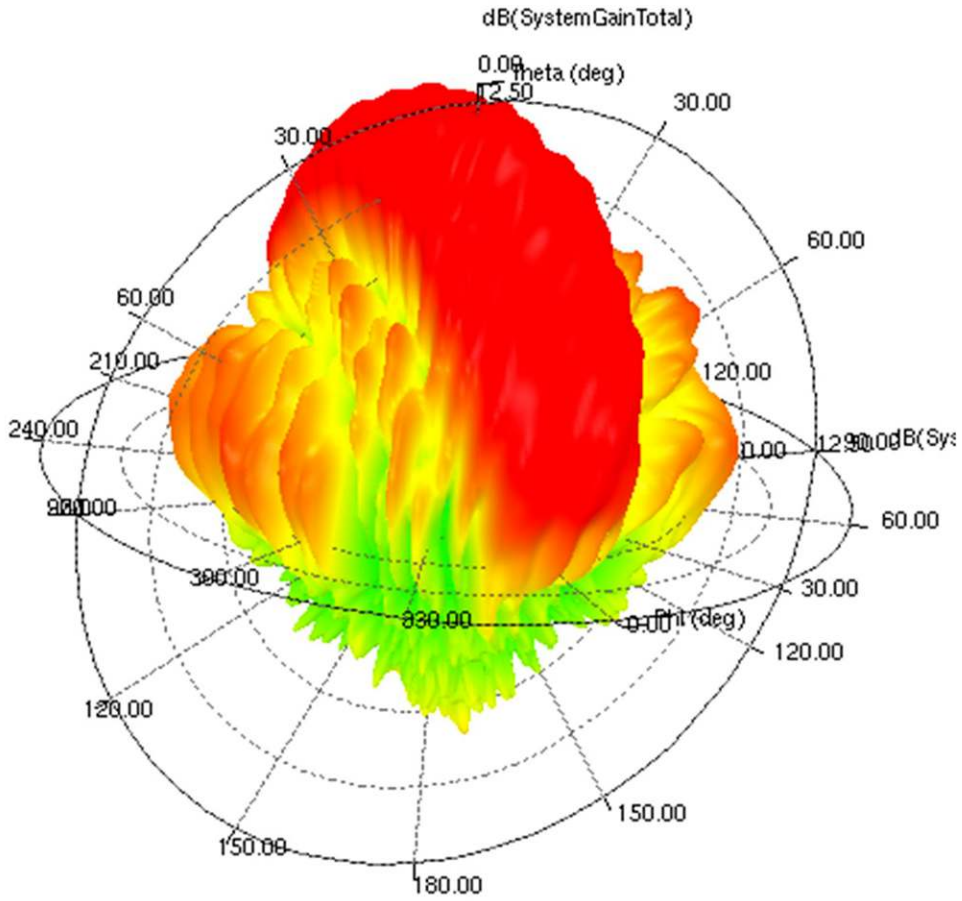


**Figure 22. RX Array A, RX4, 78.5 GHz Operation (3D Antenna Gain Pattern)**


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#### 2.6.2.2 TX Antenna Element Performance

Simulated TX antenna performance from center of the TX Array is shown below. Six different TX antenna were excerpted to show the overall performance across the array. These excerpted antenna are labeled TX1 and TX2. Like the RX antenna simulations, the TX selected here are meant to highlight the differences in performance between the more widely separated antenna and the more closely placed antenna.

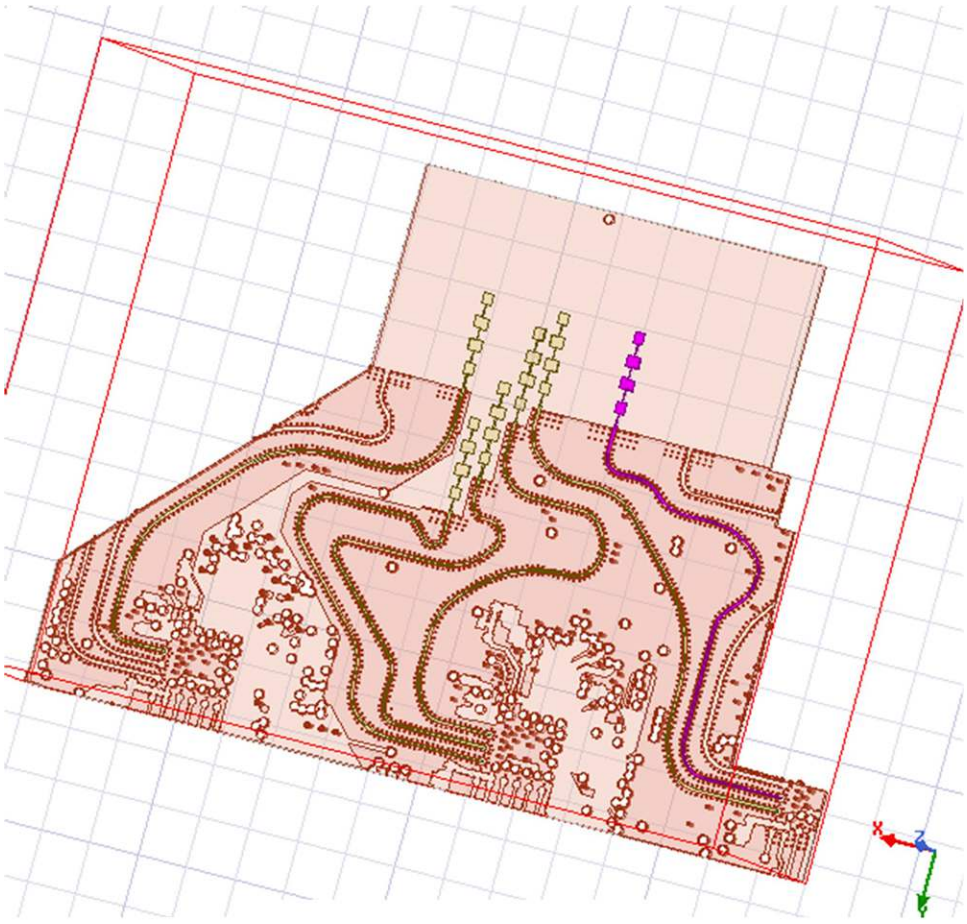


**Figure 23. TX array Excerpt for Simulation (TX1 at the "right" of the image and TX2 adjacent to TX1 to the left. TX1 highlighted in purple.)**



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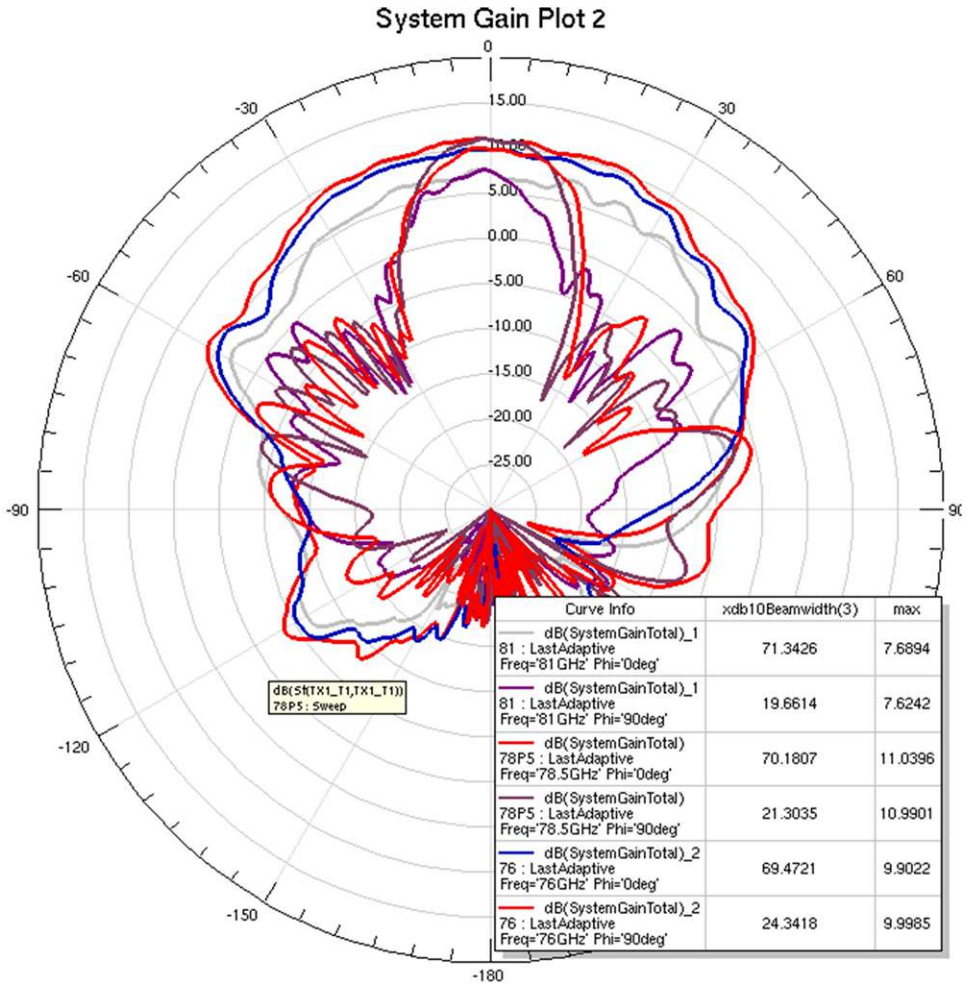


**Figure 24. Combined TX Array TX1, TX2, 76 GHz, 78.5 GHz and 81 GHz Operation (Maximum E-plane (Phi = 90) and H-plane (Phi = 0) slices shown. 3dB beamwidths shown.)**


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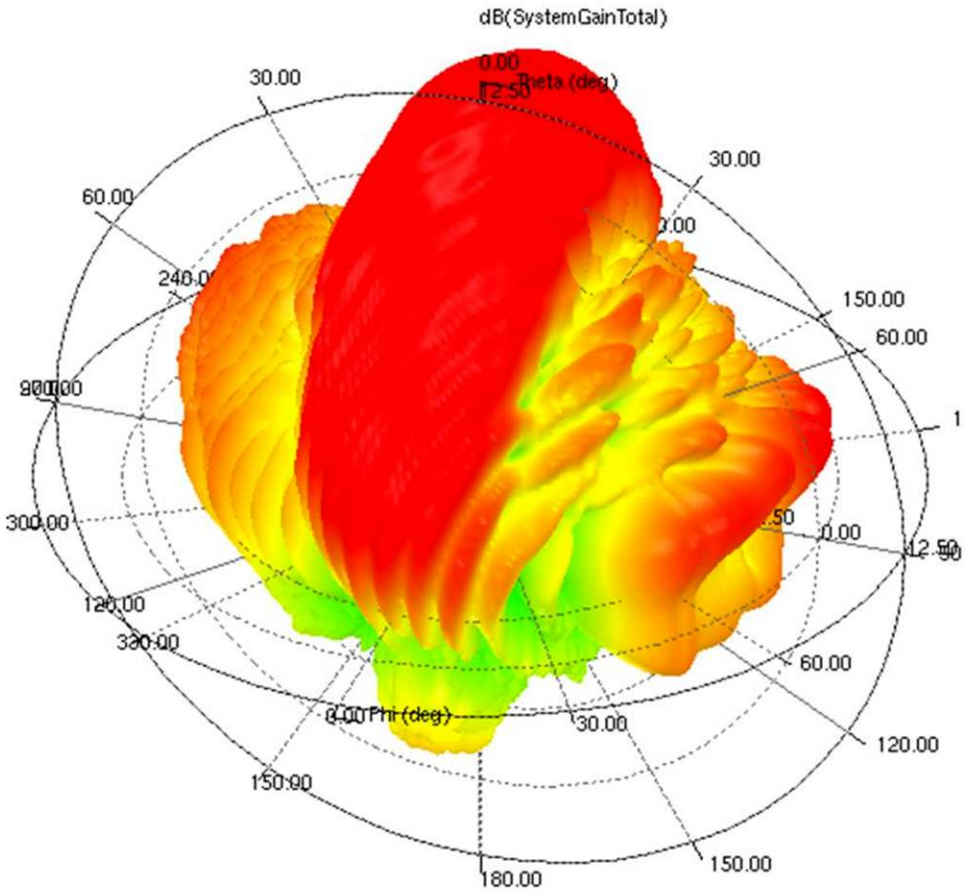


**Figure 25. TX Array, TX2, 78.5 GHz Operation (3D Antenna Pattern)**

### 2.6.3 Virtual Antenna Array

The TX and RX antenna placement described above can be used to create a large, 192- element (12 TX x 16 RX) virtual antenna array. Figure 26 and Figure 27 describe the RX, TX and resulting combined virtual antenna array offsets in terms of lambda offsets. This information is useful when constructing a TX beam-form or MIMO AWR chirp, profile and framing scenario.

All antenna position offsets are in terms of lambda. Where lambda is the free-space wavelength at 78.5 GHz, or 153.56 mils. This lambda was chosen as a compromise between the AWRx RF lower 76 GHz, and higher 81 GHz range.



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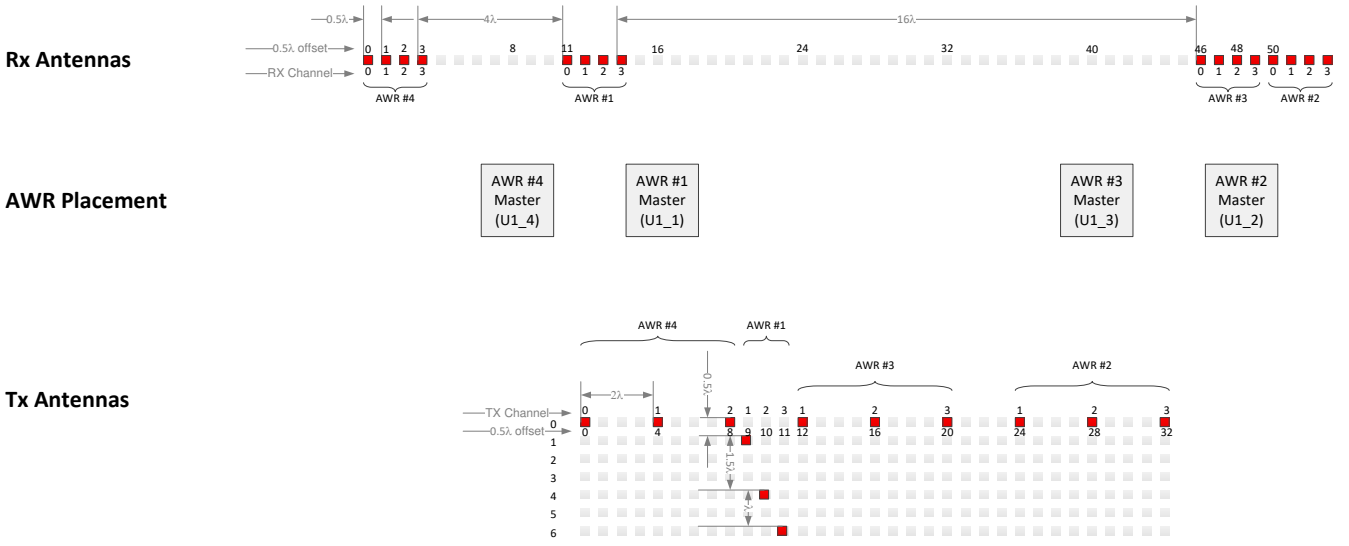


**Figure 26. RX/TX Antenna Offsets**

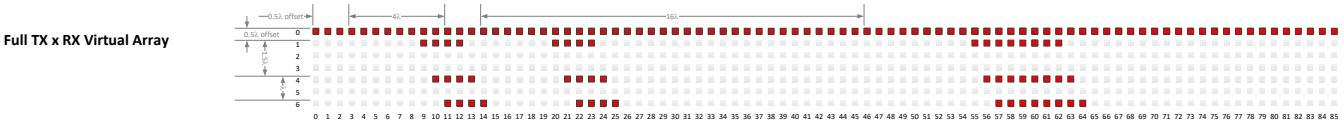


**Figure 27. Resulting Virtual Antenna Array**


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# 3 Design Files and Software Tools

## 3.1 Hardware Collateral

All PCB design documents for the MMWCAS-RF-EVM are available on ti.com enabling AWRx users to fabricate, modify and extend the MMWCAS-RF-EVM to suite their own specific use-case requirements. This design was created with Altium Designer 18.

MMWCAS-RF-EVM Rev C Design:

- *MMWCAS-RF-EVMCAD Files Revision C*
- *MMWCAS-RF-EVMCAD Files Revision D*

## 3.2 Software, Development Tools, and Example Codes for MMWCAS-RF-EVM

The Cascade Radar kit belongs to a larger TI ecosystem of hardware and software tools.

To enable immediate evaluation of the Cascade Radar kit TI provides the mmWave Studio RF evaluation GUI and Lua scripting environment. This mmWave Studio tool interfaces to the MMWCAS-RF-EVM through the MMWCAS-DSP-EVM host board and masters the TDA2Sx host processor, enabling configuration, control and data capture of the AWRx devices on the MMWCAS-RF-EVM. mmWave Studio includes example single-device, multi-device MIMO and multi-device TX-beamforming configurations. Example capture Lua scripts are also included.

A Matlab code base for MIMO and TX-Beamforming post-processing and calibration has also been developed and included in mmWave Studio. This post-processing code is designed to work on the raw captured ADC samples and includes examples of basic 1D, 2D and 3D-FFT processing for creating range-doppler and point-cloud datasets from the MIMO and TX-Beamforming data.

To enable development of an end application with single-device and cascaded AWRx, TI provides the device firmware packages (DFP).

The DFP includes the MSS and BSS firmware, or firmware patches, as well as the mmWave Link Framework and framework implementation examples. The mmWave Link Framework provides a C-source implementation of the AWRx Interface Control Document (ICD) defined API.

Links:

- MMWCAS-DSP-EVM
- mmWave Studio (MMWAVE-STUDIO)
- AWR1243 DFP (MMWAVE-DFP)
- RTOS Processor SDK for Radar
- PROCESSOR-SDK-VISION



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## 3.3 Critical AWRx Setup Notes

This section covers critical details concerning setup of the AWRx devices on the Cascade RF board.

### 3.3.1 LDO Bypass Requirement

The MMWCAS-RF-EVM use a 1.0-V supply on the RF1 and RF2 power rails of each AWRx device. To support simultaneous, 3 TX operations, the VOUT_PA output is shorted to the RF2 1.0 V power rail. For best performance and to prevent damage to the device, the on-die 1.3 V to 1.0 V LDO must be bypassed. This is done in a few different ways.

When using mmWave studio to configure theAWRx devices, select the 'RF LDO Bypass Enable' and 'PA LDO I/P Disable' options in the Static Configuration tab prior to RF initialization.

Likewise, when issuing DFP API commands to the device, the RF LDO bypass can be configured using the AWR_RF_LDO_BYPASS_SB API from the host processor. To enable the RF LDO Bypass and PA LDO I/P Disable through the API, issue an ar1.RfLdoBypassConfig(0x3) command.

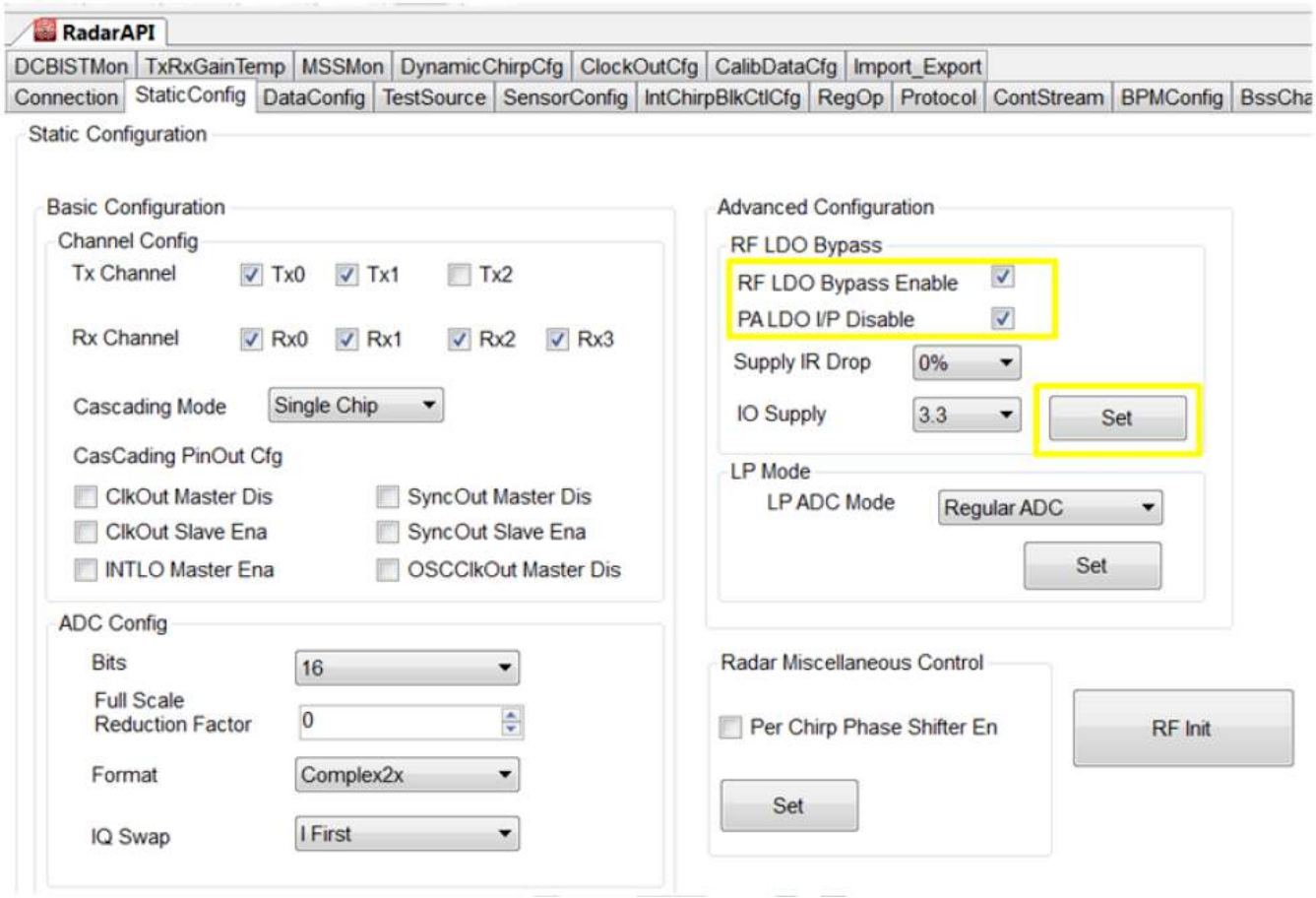


**Figure 28. LDO Bypass Enable Options in mmWave Studio**


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# 4 PCB Dimensions and Mounting Information

The field of view of the radar sensor is orthogonal to the PCB top layer where the etched antenna are placed. See the above antenna sections for more details on the antenna element gain patterns.

Mounting to the MMWCAS-DSP-EVM is accomplished through the 4, plated, through-holes in each corner of the PCB. An optional pattern of 4, plated through-hole are provided in the same lateral area as the AWRx devices and are meant to support a user-designed heat-sink plate across theAWRx packages.

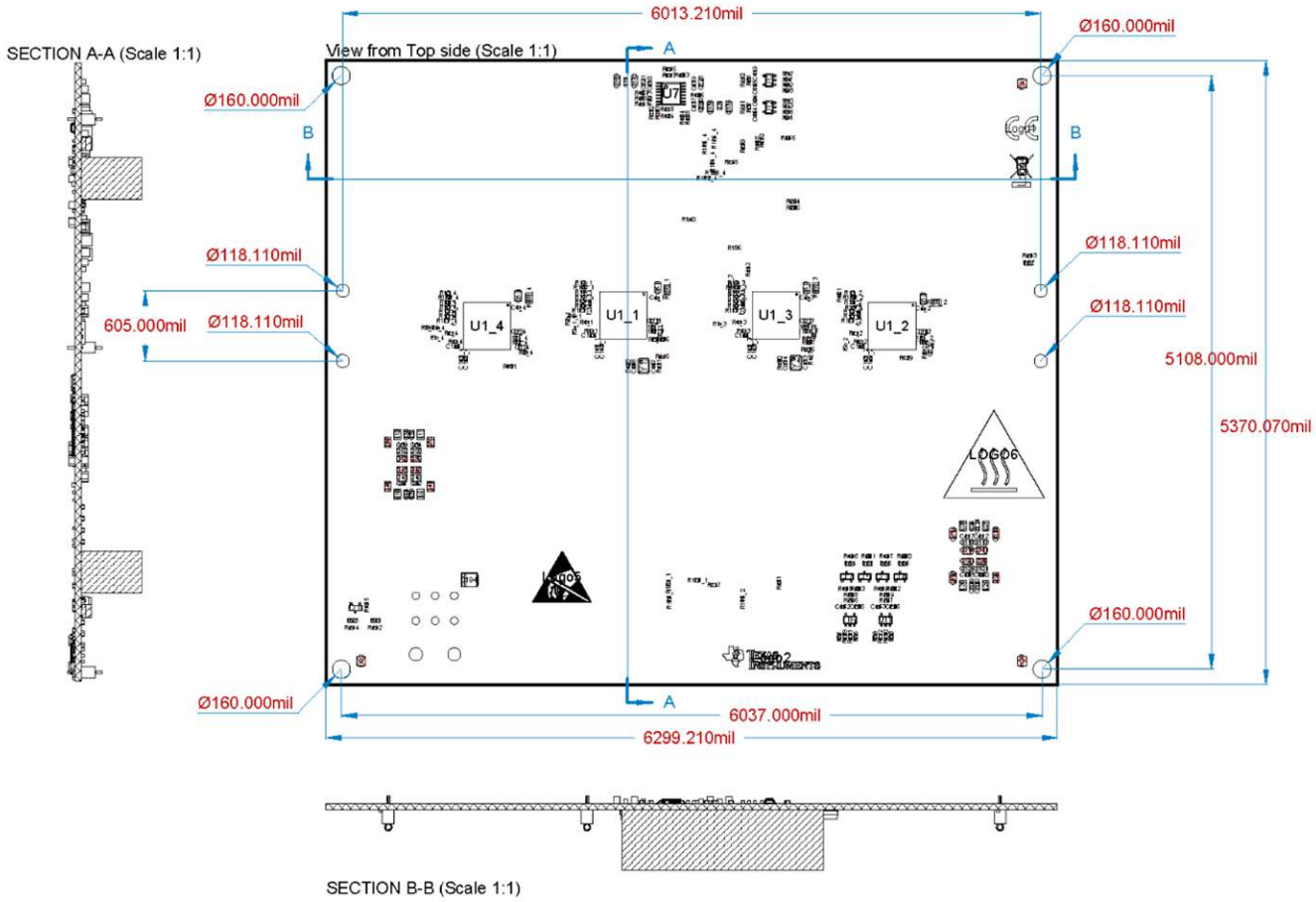


**Figure 29. MMWCAS-RF-EVM Overall Mechanical Dimensions and Mounting Drill Dimensions**

The MMWCAS-RF-EVM PCB is composed of an 8-layer, heterogenous, sequential lamination, stack-up. Rogers RO3003 is used for the Layer 1 RF GCPW routing, etched antenna structtures and the 20 GHz LO splitters. RO4450F prepreg and RO4835 LoPro are used to create Stripline routing on Layer 3 for 20 GHz LO distribution. The lower 4 core and prepreg layers are in Isola 370HR. These layers are dedicated to power distribution and high-speed digital routing.



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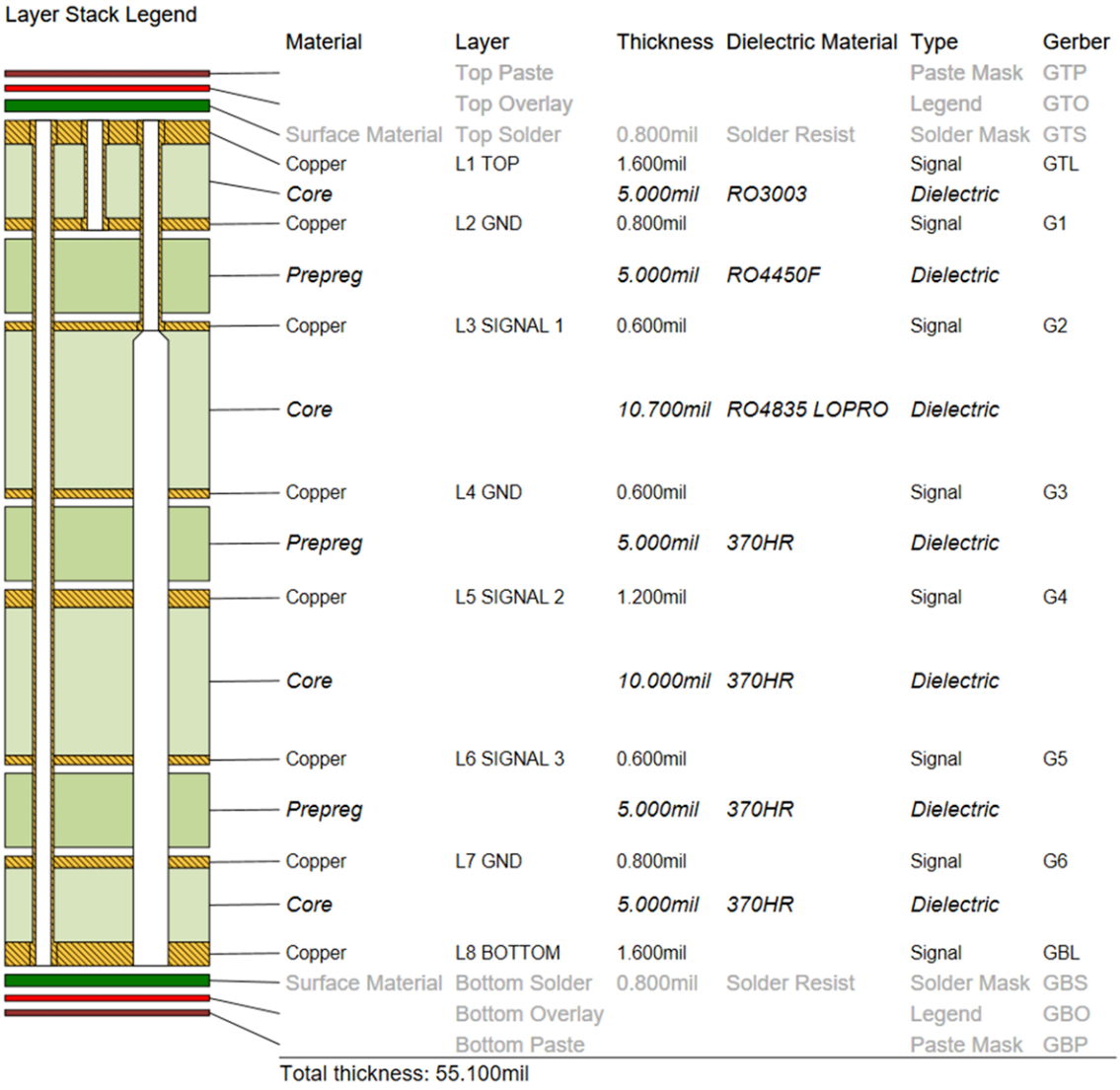


**Figure 30. MMWCAS-RF-EVM PCB and Drill Stack-Up Table**

Three via types are utilized throughout the design:

- L1-L8, 12.2mil drill, 22.4 mil pad - primary via used throughout the design for power and high-speed digital routing
- L1-L2, 5.9 mil drill, 13.77 mil pad (blind, micro-via) - L1 to L2 ground plane shorting for RF and LO routing distribution
- L1-L3, 12 mil drill, 24 mil pad, (backdrilled up to L3) - 20 GHz LO distribution L1 GCPW to L3 Stripline transition


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## 5 PCB Storage and Handling Recommendations

All of the 77-81GHz RF and 20 GHz LO transmission-line and antenna structures on this design have been left exposed on the top soldermask layer. An immersion silver finish is applied to these solder-mask free regions to protect the underlying copper. The immersion silver finish provides the RF structures with a more simple and controlled high-frequency finish compared to solder mask.

However, the immersion silver finish is also prone to oxidation in an open atmosphere environment. This oxidation causes the surface around the antenna region to blacken or tarnish as a layer of silver-oxide forms. To avoid this effect, store the PCB in an ESD cover and keep it at controlled room temperature with low humidity conditions. It should be noted though that transmission lines and antenna which are tarnished will not experience RF performance degredation.

All ESD precautions must be taken while using and handling the EVM.

## 6 References

- Texas Instruments: *AWR2243 Cascade*
- Texas Instruments: *MMWCAS-RF-EVMCAD Files Revision C*
- Texas Instruments: *MMWCAS-RF-EVMCAD Files Revision D*

## 7 Regulatory Information

No additional regulatory information is available for the MMWCAS-RF-EVM.



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# Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2019) to A Revision | Page |
|---|---|
| • Title of the document was updated. | 4 |
| • Added new Section 1.2. | 4 |
| • Updates were made in Section 2. | 6 |
| • Update was made in Section 2.1. | 8 |
| • Updates were made in Section 2.5.1. | 13 |
| • Added new Section 2.6.3. | 36 |


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