



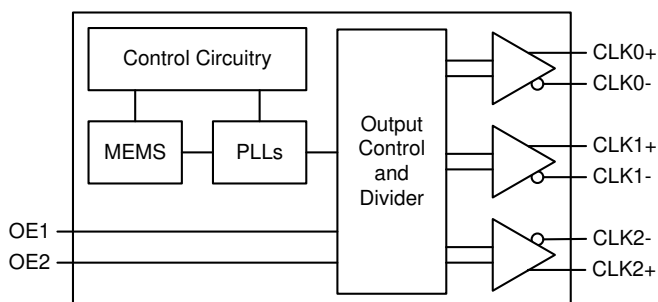
## Crystal-less™ Three Output PCIe Clock Generator

### General Description

The DSC557-04 is a Crystal-less™, three output PCI express clock generator meeting Gen1, Gen2, and Gen3 specifications. The clock generator uses proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, MEMS clock generators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC557-04 has an Output Enable / Disable feature allowing it to disable all outputs when OE1 and OE2 are low. OE1 controls CLK0 and OE2 controls CLK1/2. CLK1/2 are synchronous PCIe clocks. See the OE function diagram for more detail. The device is available in a 20 pin QFN. Additional output formats are in any combination of LVPECL, LVDS, and HCSL.

### Block Diagram



\* CLK0+/-, Clk1+/- and Clk2 +/- are 100 MHz as per PCIe standards. For other frequencies, please contact the factory.

### Features

- **Meets PCIe Gen1, Gen2 & Gen3 specs**
- **Available Output Formats:**
  - HCSL, LVPECL, or LVDS
  - Mixed Outputs: LVPECL/HCSL/LVDS
- **Wide Temperature Range**
  - Ext. Industrial: -40° to 105° C
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
  - 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **Available Footprints:**
  - 20 QFN
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**

### Applications

- **Communications/Networking**
  - Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FcoE
  - Routers and Switches
  - Gateways, VoIP, Wireless AP's
  - Passive Optical Networks
- **Storage**
  - SAN, NAS, SSD, JBOD
- **Embedded Applications**
  - Industrial, Medical, and Avionics
  - Security Systems and Office Automation
  - Digital Signage, POS and others
- **Consumer Electronics**
  - Smart TV, Bluray, STB

## Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

| Parameter   |                 | Condition   | Min.                 | Typ. | Max.                 | Unit |
|---|-----------------|---|----------------------|------|----------------------|------|
| Supply Voltage <sup>1</sup>                               | V <sub>DD</sub> |   | 2.25                 |      | 3.6                  | V    |
| Supply Current  | I <sub>DD</sub> | EN pin low – outputs are disabled   |                      | 42   | 46                   | mA   |
| Supply Current <sup>2</sup><br>(Two HCSL Outputs)         | I <sub>DD</sub> | EN pin high – outputs are enabled<br>R <sub>L</sub> =50 Ω, F <sub>O1</sub> =F <sub>O2</sub> =F <sub>O3</sub> =100 MHz |                      | 100  |                      | mA   |
| Frequency Stability                                       | Δf              | Includes frequency variations due to initial tolerance, temp. and power supply voltage                                |                      |      | ±100                 | ppm  |
|   |                 |   |                      |      | ±50                  |      |
| Startup Time <sup>3</sup>                                 | t <sub>SU</sub> | T=25°C  |                      |      | 5                    | ms   |
| Input Logic Levels<br>Input logic high<br>Input logic low | V <sub>IH</sub> |   | 0.75xV <sub>DD</sub> |      | -                    | V    |
|   | V <sub>IL</sub> |   | -                    |      | 0.25xV <sub>DD</sub> |      |
| Output Disable Time <sup>4</sup>                          | t <sub>DA</sub> |   |                      |      | 5                    | ns   |
| Output Enable Time  | t <sub>EN</sub> |   |                      |      | 20                   | ns   |
| Pull-Up Resistor <sup>2</sup>                             |                 | Pull-up on OE pin   |                      | 40   |                      | kΩ   |

| HCSL Outputs <sup>6</sup>                                     |                       |   |       |                  |                   |                   |
|---|-----------------------|---|-------|------------------|-------------------|-------------------|
| Parameter   |                       | Condition   | Min.  | Typ.             | Max.              | Unit              |
| Output Logic Levels<br>Output logic high<br>Output logic low  | V <sub>OH</sub>       | R <sub>L</sub> =50Ω   | 0.725 |                  | -                 | V                 |
|   | V <sub>OL</sub>       |   | -     |                  | 0.1               |                   |
| Pk to Pk Output Swing   |                       | Single-Ended  |       | 750              |                   | mV                |
| Output Transition time <sup>4</sup><br>Rise Time<br>Fall Time | t <sub>R</sub>        | 20% to 80%<br>R <sub>L</sub> =50Ω, C <sub>L</sub> = 2pF     | 200   |                  | 400               | ps                |
|   | t <sub>F</sub>        |   |       |                  |                   |                   |
| Frequency   | f <sub>0</sub>        | Single Frequency  | 2.3   | 100 <sup>7</sup> | 460               | MHz               |
| Output Duty Cycle   | SYM                   | Differential  | 48    |                  | 52                | %                 |
| Period Jitter <sup>5</sup>                                    | J <sub>PER</sub>      | F <sub>O1</sub> =F <sub>O2</sub> = F <sub>O3</sub> =100 MHz |       | 2.5              |                   | ps <sub>RMS</sub> |
| Jitter, Phase<br>(Common Clock<br>Architecture)               | T <sub>J</sub>        | PCIe Gen 1.1  |       | 22.7             | 86.0 <sup>8</sup> | ps <sub>p-p</sub> |
|   | J <sub>RMS-CCHF</sub> | PCIe Gen 2.1, 1.5MHz to Nyquist                             |       | 2.20             | 3.1 <sup>8</sup>  | ps <sub>RMS</sub> |
|   | J <sub>RMS-CCLF</sub> | PCIe Gen 2.1, 10 kHz to 1.5 MHz                             |       | 0.08             | 3.0 <sup>8</sup>  | ps <sub>RMS</sub> |
|   | J <sub>RMS-CC</sub>   | PCIe Gen 3.0  |       | 0.37             | 1.0 <sup>8</sup>  | ps <sub>RMS</sub> |
| Integrated Phase Noise<br>(Data Clock<br>Architecture)        | J <sub>RMS-DCHF</sub> | PCIe Gen 2.1, 1.5MHz to Nyquist                             |       | 2.15             | 4.0 <sup>8</sup>  | ps <sub>RMS</sub> |
|   | J <sub>RMS-DCLF</sub> | PCIe Gen 2.1, 10 kHz to 1.5 MHz                             |       | 0.06             | 7.5 <sup>8</sup>  | ps <sub>RMS</sub> |
|   | J <sub>RMS-DC</sub>   | PCIe Gen 3.0  |       | 0.32             | 1.0 <sup>8</sup>  | ps <sub>RMS</sub> |

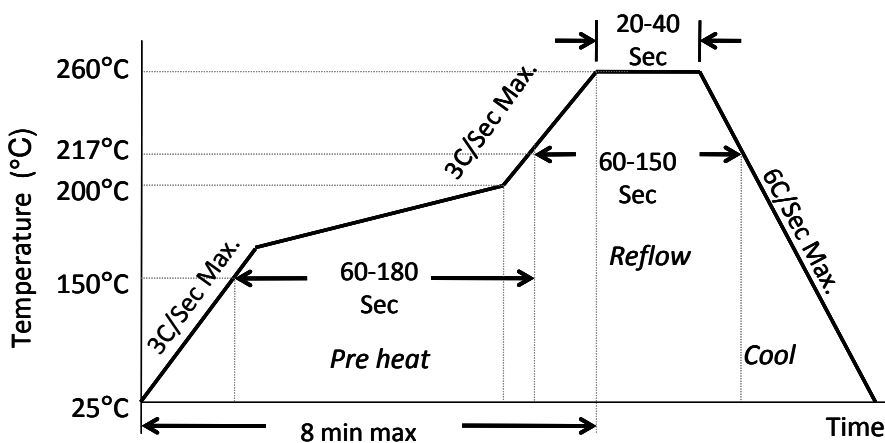
### Notes:

- V<sub>DD</sub> should be filtered with 0.01uf capacitor.
- Output is enabled if OE pin is floated or not connected.
- t<sub>SU</sub> is time to 100PPM stable output frequency after V<sub>DD</sub> is applied and outputs are enabled.
- Output Waveform and Connection Diagram define the parameters.
- Period Jitter includes crosstalk from adjacent output.
- Contact [Sales@Discera.com](mailto:Sales@Discera.com) for alternate output options (LVPECL, LVDS, LVCMOS).
- Contact [Sales@Discera.com](mailto:Sales@Discera.com) for alternative frequency options
- Jitter limits established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

## Absolute Maximum Ratings

| Item           | Min  | Max          | Unit | Condition  |
|----------------|------|--------------|------|------------|
| Supply Voltage | -0.3 | +4.0         | V    |            |
| Input Voltage  | -0.3 | $V_{DD}+0.3$ | V    |            |
| Junction Temp  | -    | +150         | °C   |            |
| Storage Temp   | -55  | +150         | °C   |            |
| Soldering Temp | -    | +260         | °C   | 40sec max. |
| ESD            | -    |              | V    |            |
| HBM            |      | 4000         |      |            |
| MM             |      | 400          |      |            |
| CDM            |      | 1500         |      |            |

## Solder Reflow Profile

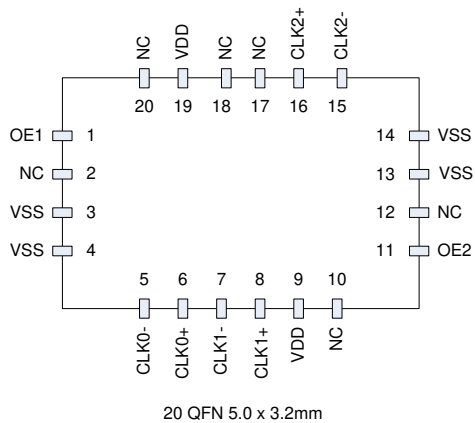


| 20 QFN MSL 1 @ 260°C refer to JSTD-020C |              |
|---|--------------|
| Ramp-Up Rate (200°C to Peak Temp)       | 3°C/Sec Max. |
| Preheat Time 150°C to 200°C             | 60-180 Sec   |
| Time maintained above 217°C             | 60-150 Sec   |
| Peak Temperature                        | 255-260°C    |
| Time within 5°C of actual Peak          | 20-40 Sec    |
| Ramp-Down Rate                          | 6°C/Sec Max. |
| Time 25°C to Peak Temperature           | 8 min Max.   |

## Pin Description (20 QFN)

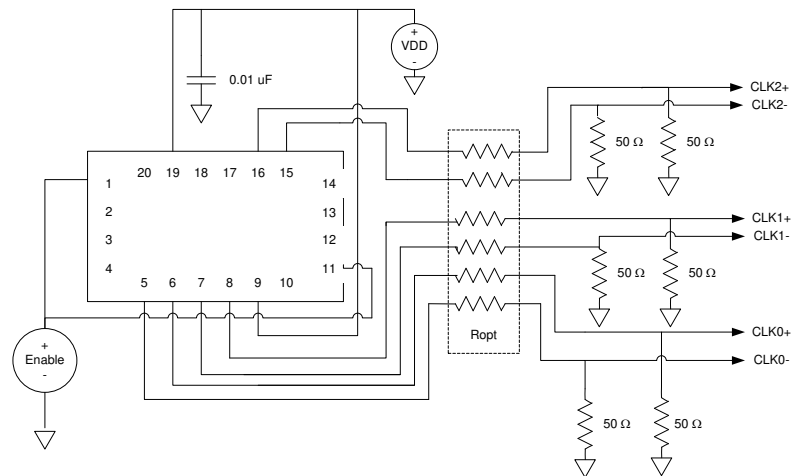
| Pin No. | Pin Name | Pin Type | Description   |
|---------|----------|----------|---|
| 1       | OE1      | I        | Output Enable; active high                          |
| 2       | NC       | NA       | Leave unconnected or grounded                       |
| 3       | VSS      | Power    | Ground  |
| 4       | VSS      | Power    | Ground  |
| 5       | CLK0-    | O        | Complement output of differential pair              |
| 6       | CLK0+    | O        | True output of differential pair                    |
| 7       | CLK1-    | O        | Complement output of differential pair              |
| 8       | CLK1+    | O        | True output of differential pair                    |
| 9       | VDD      | Power    | Power Supply  |
| 10      | NC       | NA       | Leave unconnected or grounded                       |
| 11      | OE2      | I        | Output Enable; active high                          |
| 12      | NC       | NA       | Leave unconnected or grounded                       |
| 13      | VSS      | Power    | Ground  |
| 14      | VSS      | Power    | Ground  |
| 15      | CLK2-    | O        | Complement output of differential pair              |
| 16      | CLK2+    | O        | True output of differential pair                    |
| 17      | NC       | NA       | Package pin is Not Connected to internal IC or MEMS |
| 18      | NC       | NA       | Package pin is Not Connected to internal IC or MEMS |
| 19      | VDD      | Power    | Power Supply  |
| 20      | NC       | NA       | Leave unconnected or grounded                       |

## Pin Diagram (20 QFN)

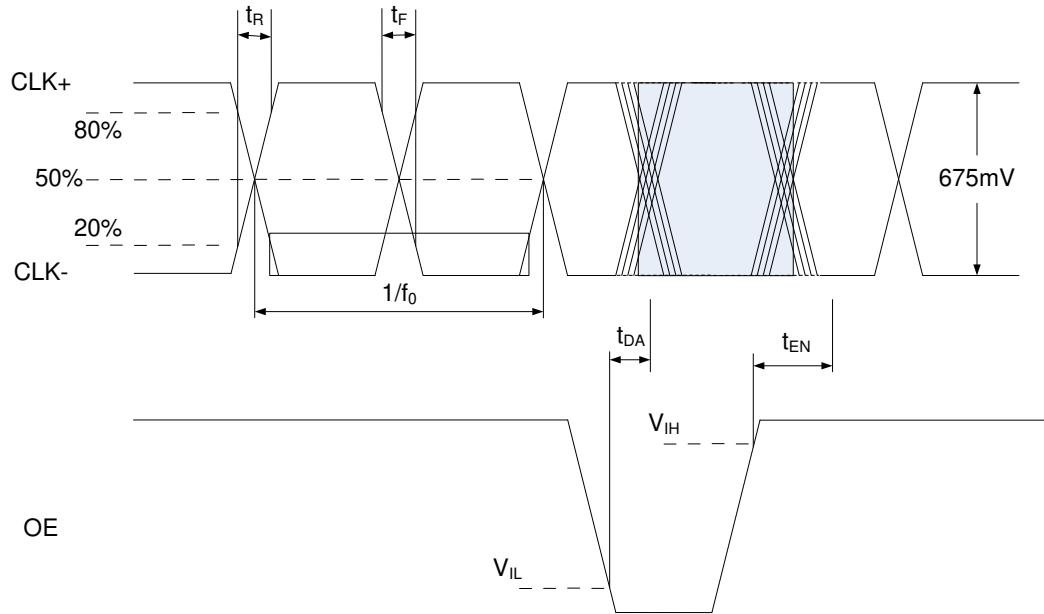


## Connection Diagram

### (20 QFN Three HCSL Outputs)

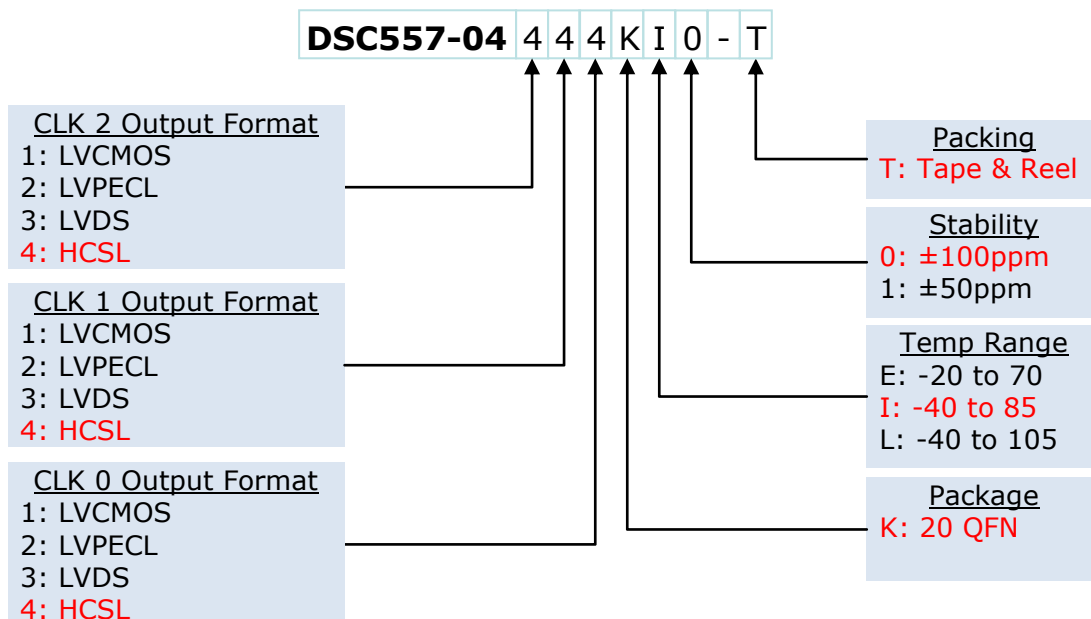


## OE Function and Output Waveform: HCSL



| OE1 | OE2 | CLK0 | Synchronous |      |
|-----|-----|------|-------------|------|
|     |     |      | CLK1        | CLK2 |
| 0   | 0   | Hi-Z | Hi-Z        | Hi-Z |
| 0   | 1   | Hi-Z | EN          | EN   |
| 1   | 0   | EN   | Hi-Z        | Hi-Z |
| 1   | 1   | EN   | EN          | EN   |

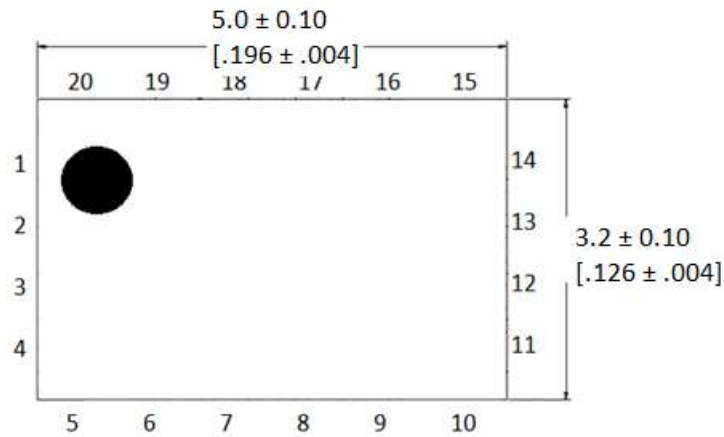
## Ordering Information



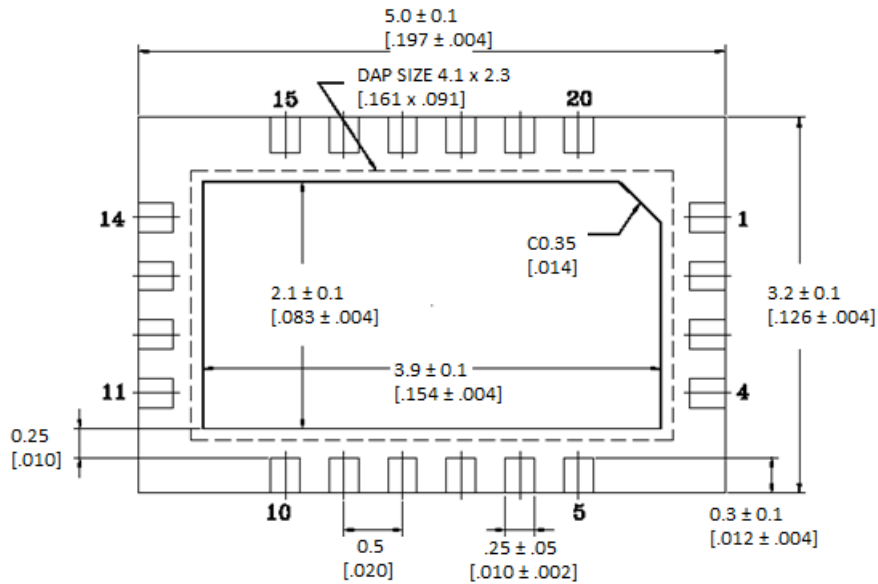
## Package Dimensions

### 20 QFN, 5.0 x 3.2 mm

#### Top View units: mm[inches]



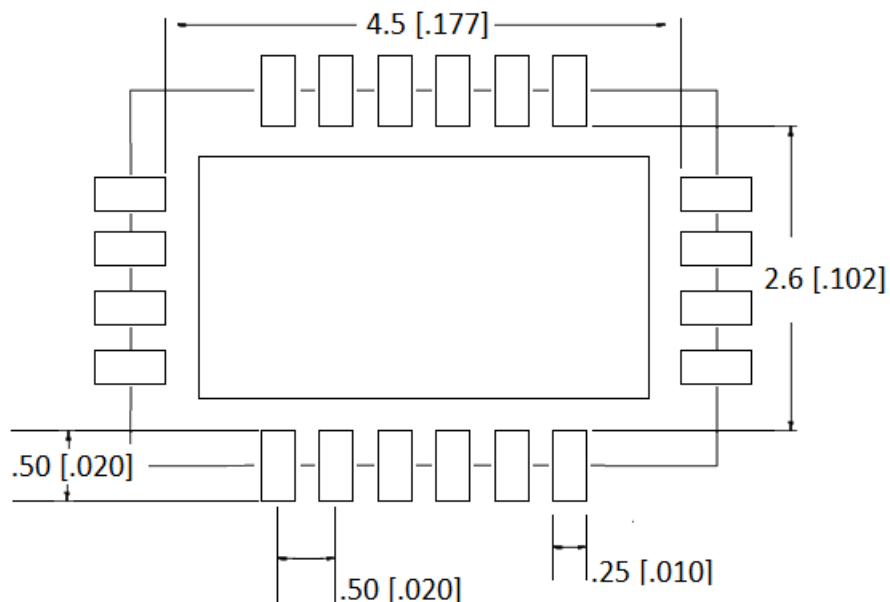
#### Bottom View units: mm[inches]±



**Side View**  
units: mm[inches]



**Recommended Solder Pad Layout**  
units: mm[inches]



\*Connect the center pad to VSS for best thermal performance

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