

MPR0712TE Power Supply

Input: 90VAC to 264VAC; Output: +12VDC, 700W; Auxiliary Voltage 12VDC @ 2A



The MPR0712 series is a 700W ACDC power supply with a power density of 23W/in³ at an efficiency of 94% @ 50% Load. The smaller depth of 9" would be conducive for mid plane system architectures and in applications that are limited in space. MPR0712 uses the industry standard PMBus[®] compliant I2C communications bus and offers a full range of control and monitoring capabilities. The SMBAlert signal pin automatically alerts customers of any state

Applications

- 12Vdc Distributed Power Architectures
- Mid-End Servers
- Blade Servers
- Advanced workstations
- Network Equipment
- Network Attached Storage
- Storage Area Networks
- Routers/Switches
- Enterprise Networks

Features

- Form factor: 9.0" (L) x 2.15" (W) x 1.57" (H)
- 12Vdc Regulation: set point $\pm 0.33\%$, overall $\pm 1\%$
- Active current share on 12V with internal OR'ing function
- Remote sense on the 12V main output
- Hot insertion/removal (hot plug)
- Hardware recoverable latched 12Vdc overvoltage
- Auto recoverable overload & over temperature
- Firmware adjustable overload set point of 12V output
- Operating temperature: -5C to 50C
- Digital status & control: PMBus[®] serial bus
- Compliant to REACH Directive (EC) No 1907/2006
- Compliant to RoHS II EU "Directive 2011/65/EU (-Z versions)
- Conducted EMI: Class A with 6dB margin
- Meets EN6100 immunity and transient standards
- Shock & vibration: NEBS GR-63-CORE, level 3
- Safety: UL, CAN/CSA, IEC, TUV, BSMI, CCC, KC

Technical Specifications

Absolute Maximum Ratings

Stresses over the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions over those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

| Parameter | Device | Min | Max | Unit |
|--|-----------|-----|-----------------|----------|
| Input Voltage: Continuous | V_{IN} | 90 | 264 | V_{DC} |
| Operating Ambient Temperature | T_A | -5 | 50 ¹ | °C |
| Storage Temperature | T_{STG} | -40 | 85 | °C |
| I/O Isolation voltage (100% factory Hi-Pot tested) | | | 3000 | V_{AC} |

¹ De-rating above 40C for reverse model

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

| Parameter | Device | Min | Typ | Max | Unit |
|--|----------|------|---------|-----|------------|
| Operational Range | V_{IN} | 90 | 115/230 | 264 | V_{AC} |
| Frequency range (ETSI 300-132-1 recommendation) | F_{IN} | 47 | 50/60 | 63 | Hz |
| Main Output Turn OFF | V_{IN} | 70 | | 80 | V_{AC} |
| Main Output Turn ON | V_{IN} | 74 | | 84 | V_{AC} |
| Hysteresis between turn OFF and turn ON | V_{IN} | 4 | | | V_{AC} |
| Efficiency ($T = 25^{\circ}C$, $V = 12V$) $V = 230V$, exc. fan | | | | | |
| 100% load | η | | 91.0 | | % |
| 50% load | η | | 94.0 | | % |
| 20% load | η | | 90.5 | | % |
| Maximum Input Current ($V_O = V_O, set$, $I_O = I_O, max$) | | | | | |
| $V_{IN} = 100V_{AC}$ | I_{IN} | | | 8.5 | A_{AC} |
| $V_{IN} = 180V_{AC}$ | I_{IN} | | | 4.6 | A_{AC} |
| Cold Start Inrush Current (between 0 to 200mSec) | I_{IN} | | | 25 | A_{PEAK} |
| Startup Time during AC ramp up. Note: Following a "turn off" of the 12V Main output (for any reason whatsoever) the output shall not be allowed to "turn on" again for 1sec (even if all necessary operating conditions are met). | | | | | |
| | | | | 3 | Sec |
| Power factor ($V_{AC} = 115/230V_{AC}$), | | | | | |
| $I_0 = 50\% I_{0, max}$ | PF | | 0.96 | | |
| $I_0 = 100\% I_{0, max}$ | PF | | 0.98 | | |
| Holdup time ($V_{out} \geq 10.8V$, $T_{amb} = 25^{\circ}C$, 650W) $V_{IN} = 100-230V_{AC}$ | | | | | |
| Early warning prior to output falling below regulation | T | 1 | | | ms |
| Ride through | | | 10 | | |
| Leakage current ($V = 250V$, $F = 60Hz$) | I_{IN} | | | 3 | mA_{RMS} |
| Isolation Input/Output | | 3000 | | | V_{RMS} |
| Input/Frame | | 1500 | | | V_{RMS} |
| Output/Frame | | 50 | | | V_{DC} |

Technical Specifications

Electrical Specifications (continued)

12Vdc MAIN OUTPUT

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|----------------|------|------|------------------|---------------------------------|
| Output Power 90 – 264 Vac, Cout 500-4000uF | W | 0 | - | 700 | W |
| Overall regulation (setpoint, line, load, temperature) | V _o | -2 | | +2 | % |
| Ripple and noise (20MHz bandwidth, 0.1uF ceramic+10uF tantalum connected) | V _o | - | | 120 ¹ | mVP-P |
| Turn-ON overshoot | V _o | | | +3 | % |
| Turn-ON delay | T | | | 2 | sec |
| Remote ON/OFF delay time | T | | | 150 | ms |
| Turn-ON rise time (10 – 90% of Vout) | T | | | 80 | ms |
| Transient response 50% step [10%-50%, 50% - 100%] (di/dt – 1A/μs, recovery 500μs) | T | -5 | | +5 | %V _o |
| Overvoltage protection, latched (recovery by cycling off/on via hardware or PMBUs®) | V _o | 13.0 | 13.8 | 14.5 | Overvoltage protection, latched |
| Output current 264 ≥ VIN ≥ 90 | I _o | 0 | | 58.3 | A _{DC} |
| Current limit— The output shall shutdown when an overcurrent condition is detected. It will auto restart after 1sec; however, if the overcurrent condition is redetected the output will once again shutdown. The output will once again re-start, however if the overcurrent condition persists it will latch of after the fifth unsuccessful attempt. To reset the latch, it will be necessary to toggle the PS_ON_L signal (B4) or recycle the incoming AC source. | I _o | 60 | | 70 | A _{DC} |
| Hot Swap Transients | V _o | -5 | | +5 | % |
| Active current share | V _o | -5 | | +5 | %of FL |

STANDBY OUTPUT

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|----------------|------|------|------------------|-------------------|
| Set point | | | 12.0 | | V _{DC} |
| Overall regulation (setpoint, line, load, temperature) | V _o | 11.7 | | 12.3 | V _{DC} |
| Ripple and noise (20MHz bandwidth, 0.1uF ceramic+10uF tantalum connected) | V _o | | | 120 ¹ | MV _{P-P} |
| Output current | | 0 | | 2 | A _{DC} |
| Transient response 50% step [10%-50%, 50% - 100%] (di/dt – 1A/μs, recovery 500μs) | I _o | -5 | | +5 | %V _o |
| Overvoltage protection, latched | | 13 | | 14.5 | V _{DC} |
| Overload protection - The output shall shutdown when an overcurrent is detected. It will auto restart after 2sec. However, if the overcurrent is re-detected the output will once again shutdown. This cycle will occur indefinitely while in the overcurrent condition | | | 3 | | A _{DC} |

Note: Output voltage allowed to dip to 10.0V temporarily during fault conditions on the main output (e.g., a short circuit on the main output pins)

¹ Can be over 120mV (300mV typical) at light load (around 1A each unit) in paralleled application

General Specifications

| Parameter | Device | Symbol | Typ | Unit |
|--|--------|--------|-----|------|
| Calculated Reliability Per Telcordia SR-332 M1C1 @40°C | | 576K | | Hrs |
| Weight | | 1.63 | | Lbs |

Technical Specifications

EMC Compliance

| Parameter | Criteria | Standard | Level | Test |
|-------------------------------|---------------------------------|--|-------------------------------------|---|
| AC input | Conducted emissions | EN55032, FCC Docket 20780 part 15, subpart J | A ¹ (With 6dB margin) | 0.15 – 30MHz |
| | Radiated emissions ² | EN55032 | A ² | 30 – 1000MHz |
| AC input immunity | Voltage dips | EN61000-4-11 | A | 230V _{in} , 80% load, Phase 45°, Dip 100% Duration 10ms |
| | | | V _{main} :B | 230V _{in} , 50% load, Phase 0°, Dip 100% Duration 20ms (V _{SB} : A, V ₁ :B) |
| | | | B | 230V _{in} , 100% load, Phase 45°, Dip 100% Duration > 20ms (V _{SB} /V ₁ :B) |
| | Voltage surge | EN61000-4-5 | 6kV | Common mode and differential mode, unit shall fail safely. |
| | | | 4kV | Common mode and differential mode, unit shall survive. The output may shut down and recover automatically (Criteria B) or require manual intervention (Criteria C) ³ |
| | | | 2kV | Common and differential mode, unit passes criteria A (normal performance) ⁴ |
| Fast transients | EN61000-4-4 | Level 3, criteria A | 5/50ns, 2kV (common mode) | |
| Input Current Harmonics | | IEC/EN 61000-3-2 | Comply | |
| Voltage Fluctuation & Flicker | | IEC/EN 61000-3-3 | Comply | |
| Enclosure immunity | Conducted RF fields | EN61000-4-6 | Level 3, criteria A | 140dB μ V, 0.15-80MHz, 80% AM |
| | Radiated RF fields | EN61000-4-3 | Level 3, criteria B | 10V/m, 80-1000MHz, 80% AM |
| | | ENV 50140 | A | |
| ESD | EN61000-4-2 | Level 4, criteria A | 8kV contact, 15kV air | |

¹ Contact the factory for a recommended external EMI filter to meet Class B emissions.

² Radiated emissions compliance is contingent upon the final system configuration.

³ Tests above ± 2 KV will be performed for information purposes to IEC/EN6100-4-5 with 12ohm impedance, differential & common mode.

⁴ Impedance is 2 ohms for ± 2 KV differential and common mode to comply with NEBS GR-1089 limits. Maximum load capacitance is required for these tests.

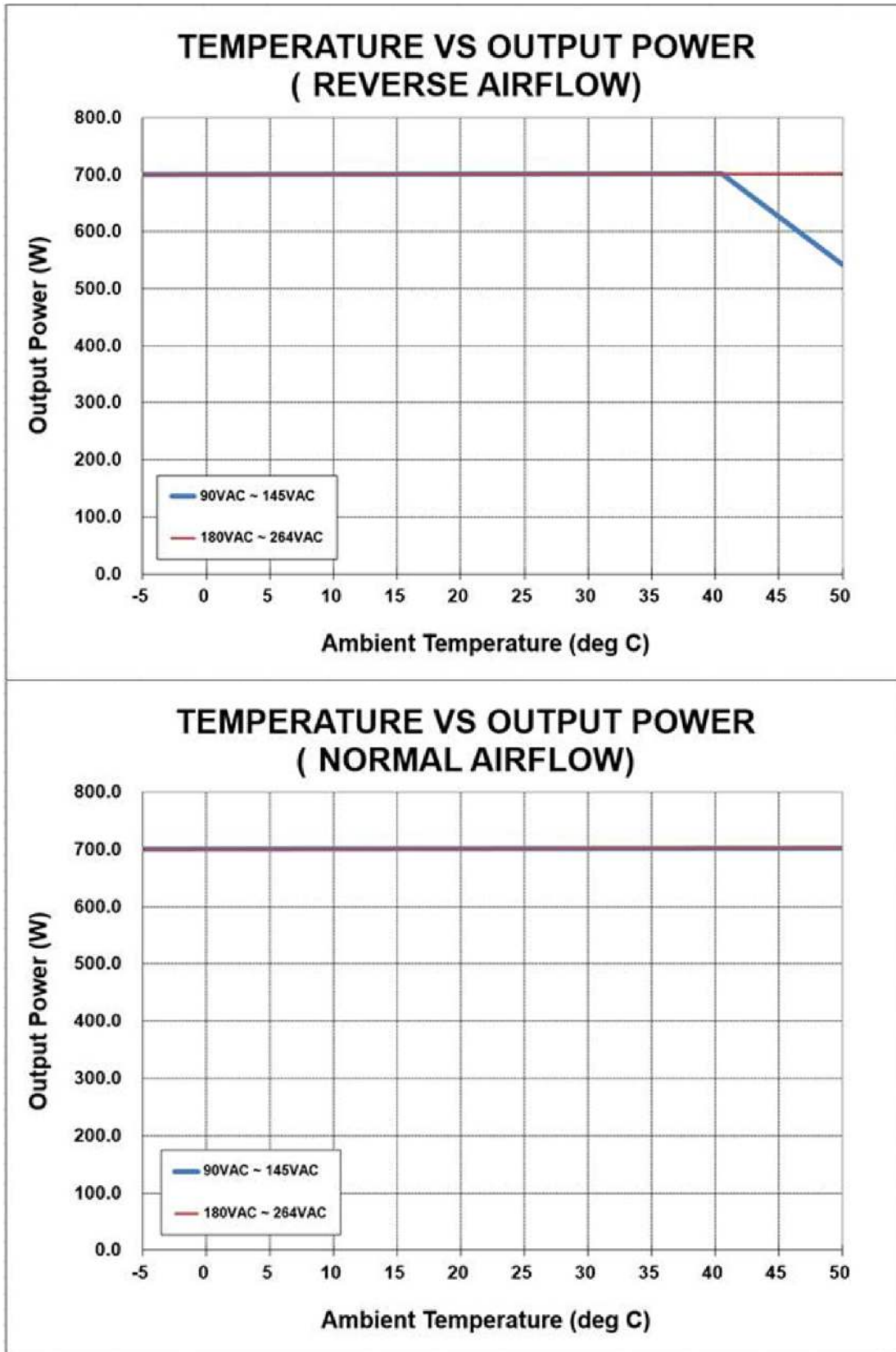
Environmental Specifications

| Parameter | Device | Min | Typ | Max | Unit |
|---|----------------|-----|-----|------|------|
| Ambient Inlet Temperature Rating Reverse airflow (air enters rear connector, exhausts at handle). 90-145Vac, 700W. De-rating above 40C (see following chart). | TA, Reverse/ST | -5 | | 50 | °C |
| Ambient Temperature Short Terms ≤ 96 hrs event, and ≤ 96 hrs total/year, which can exceed IPC9592 derating, but OTP and mfr's max temp specs must apply reverse airflow. De-rating above 40C allowed. | TA, Reverse/ST | -10 | | 55 | °C |
| Storage Temperature | | -40 | | 70 | °C |
| Operating Altitude Design Requirement without derating at 40°C inlet | | | | 3000 | m |
| Acoustic noise (full load) | | | 57 | | dba |
| Over Temperature Protection (inlet) Auto restart with 4°C hysteresis for recovery (warning issued at 70°C) | | | 70 | | °C |
| Humidity Relative humidity, non-condensing | | | | | % |
| Operating, +45C | | 5 | | 90 | |
| Storage | | 5 | | 95 | |
| Operational Vibration Sine sweep; 5-200Hz, 2G; random vibration, 5-500Hz, 1.11G | | | | | |
| Non-Operating Shock | | | | 30 | Grms |

Safety Specifications — Applicable Standards

- CAN/CSA C22.2 No 60950-1-07, Am.1:2011, Am 2:2014
- ANSI/UL 60950-1-2014
- IEC60950-1:2005 (2nd Ed.), Am 1:2009 + Am 2:2013
- CCC GB4943. 1-2011;GB9254-2008(Class A); GB17625.1-2012
- EN 60950-1:2006+A11:2009 +A1:2010 +A12:2011 +A2:2013
- BSMI CNS14336-1 (099/09/30); CNS13438 ((095/06/01)
- KC K 60950-1(2011-12)

Output Power Derating versus Ambient Inlet Temperature



Technical Specifications

Feature Specifications: Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions.

STATUS AND CONTROL SIGNALS

| Signal Name | I/O | Description | Interface Details |
|---|-----------------------------|--|--|
| INPUT_OK (AC Source) | Output | The signal output is driven high when input source is available and within acceptable limits. The output is driven low to indicate loss of input power. There is a minimum of 1ms pre-warning time before the signal is driven low prior to the PWR_OK signal going low. The power supply must ensure that this interface signal provides accurate status when AC power is lost. | Pulled up internally via 10K to 3.3Vdc. A logic high >3.0Vdc A logic low < 0.8Vdc Driven low by internal CMOS buffer. |
| PW_OK (Output OK) | Output | The signal is asserted, driven high, by the power supply to indicate that all outputs are valid. If any of the outputs fail then this output will be hi-Z or driven low. The output is driven low to indicate that the Main output is outside of lower limit of regulation (11.4Vdc). | Pulled up internally via 10K to 3.3Vdc. A logic high >3.0Vdc A logic low < 0.8Vdc Driven low by internal CMOS buffer. |
| SMB_ALERT (FAULT/WARNING) | Output | The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed. | Pulled up internally via 10K to 3.3Vdc. A logic high >3.0Vdc A logic low < 0.8Vdc Driven low by internal CMOS buffer. |
| PRESENT_L (Power Supply Absent) | Output | The signal is used to detect the presence (installed) of a PSU by the host system. The signal is connected to PSU logic SGND within the power module. | Passive connection to +VSB_Return. A logic low < 0.8Vdc |
| PS_ON (Power Supply Enable/Disable) | Input | This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +VSB_Return. In the low state the signal input shall not source more than 1mA of current. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions. | Pulled up internally via 10K to 3.3Vdc. A logic high >3.0Vdc A logic low < 0.8Vdc Input is via CMOS Schmitt trigger buffer. |
| PS_KILL | Input | This signal is used during hot swap to disable the main output during hot swap extraction. The input is pulled up internally to the internal housekeeping supply (within the power supply). The signal is provided on a short (lagging pin) and should be connected to +VSB_Return. | Pulled up internally via 10K to 3.3Vdc. A logic high >3.0Vdc A logic low < 0.8Vdc Input is via CMOS Schmitt trigger buffer. |
| ADDR (Address Select) | Input | An analogue input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications. Connection of a suitable resistor to +VSB_Return, in conjunction with an internal resistor divider chain, will configure the required address. | DC voltage between the limits of 0 and +3.3Vdc. |
| SCL (Serial Clock) | Both | A serial clock line compatible with PMBus® Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered. | V _{IL} is 0.8V maximum V _{OL} is 0.4V maximum when sinking 3mA V _{IH} is 2.1V minimum |
| SDA (Serial Data) | Both | A serial data line compatible with PMBus® Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. The signal is provided with a series isolator device to disconnect the internal power supply bus if the power module is unpowered. | V _{IL} is 0.8V maximum V _{OL} is 0.4V maximum when sinking 5mA V _{IH} is 2.1V minimum |
| V1_SENSE V1SENSE_RTN | Input | Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required then the voltage can be configured for local sense by: 1. V1_SENSE directly connected to power blades 6 to 10 (inclusive) 2. V1_SENSE_RTN directly connected to power blades 1 to 5 (inclusive) | Compensation for a up to 0.12Vdc total connection drop (output and return connections). |
| ISHARE | Bi-Directional Analogue Bus | The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analogue bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit). Analogue voltage: +8V maximum; 10K to +12V_RTN | |

Technical Specifications

Digital Interface Specifications

| PMBus® Signal Interface Characteristics | | | | | |
|---|----------------------|-----------------------|--------------------|------|------------------|
| Parameter | Conditions | Symbol | Min | Max | Unit |
| Input logic high voltage (CLK, DATA) | | V _{IH} | 0.7V _{DD} | 3.6 | V |
| Input logic low voltage (CLK, DATA) | | V _{IL} | 0 | 0.8 | V |
| Input high sourced current (CLK, DATA) | | I _{IH} | 0 | 10 | μA |
| Output low sink voltage (CLK, DATA, SMBALERT#) | I _o =5mA | V _{OL} | | 0.4 | V |
| Output low sink current (CLK, DATA, SMBALERT#) | | I _{OL} | 5 | | mA |
| Output high open drain leakage current (CLK, DATA, SMBALERT#) | V _o =3.6V | I _{oH} | 0 | 10 | μA |
| PMBus operating frequency range | Slave Mode | FPMB | 10 | 400 | kHz |
| Measurement System Characteristics | | | | | |
| Clock stretching | | tstretch | | 25 | ms |
| I _{OUT} measurement range | Linear | I _{RNG} | 0 | 74 | A |
| I _{OUT} measurement accuracy 25°C | | I _{OUT} | -3 | +3 | % of FL |
| V _{OUT} measurement range | Linear | V _{OUT(rng)} | 0 | 14 | V |
| V _{OUT} measurement accuracy | | V _{OUT(acc)} | -5 | +5 | % |
| Temp measurement range | Linear | Temp _(rng) | 0 | 125 | °C |
| Temp measurement accuracy ¹ | | Temp _(acc) | -5 | +5 | % |
| I _{IN} measurement range | Linear | I _{IN(rng)} | 0 | 16 | A _{RMS} |
| I _{IN} measurement accuracy | | I _{IN(acc)} | -5 | +5 | % of FL |
| V _{IN} measurement range | Linear | V _{IN(rng)} | 0 | 330 | V _{RMS} |
| V _{IN} measurement accuracy | | V _{IN(acc)} | -5 | +5 | % of FL |
| P _{IN} measurement range | Linear | P _{N(rng)} | 0 | 1023 | W |
| P _{IN} measurement accuracy | | P _{IN(acc)} | -5 | +5 | % of FL |
| Fan Speed measurement range | Linear | | 0 | 30k | RPM |
| Fan Speed measurement accuracy | | | -10 | 10 | % |
| Fan speed control range | number | | 0 | 100 | % |

Visual Indicators (LEDs)

Input (Green), Output (Bicolor Green/Amber)

| STATUS INDICATORS | | | |
|-------------------|---------------|---------------------|--|
| LED NAME | LED MODE | LED STATE/OPERATION | DESCRIPTION |
| Input | OK | Solid Green | Input voltage operating within normal specified range |
| Input | OV/UV Warning | Blinking Green | Input voltage operating in: 1) overvoltage warning; 2) under voltage warning range, or 3) above overvoltage range |
| Input | OFF or Fault | Off | Input voltage operating: 1) below under voltage range, or 2) not present |
| Output | Power Good | Solid Green | Main output & standby output enabled with no power supply warning or fault detected |
| Output | Standby | Blinking Green | Standby output enabled with no power supply warning or fault detected |
| Output | Warning | Blinking Amber | Power supply fault detected as per PMBus STATUS_X reporting bytes ² |
| Output | Fault | Solid Amber | Power supply fault detected as per PMBus STATUS_X reporting |

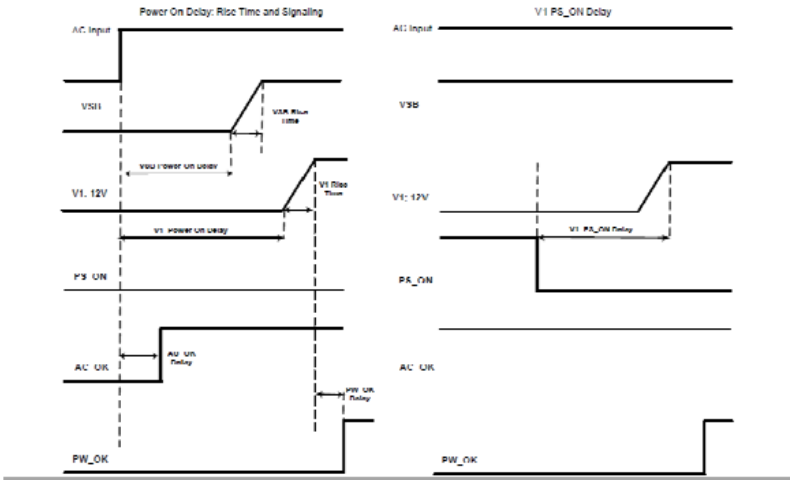
¹ Temperature accuracy reduces non-linearly with decreasing temperature

² LED fault/warning operation follows PMBus fault/warning reporting status flags but will not be "sticky" (i.e., if the fault stimulus is removed, even though the actual fault/warning is still showing [still "sticky" and not cleared], the relevant LED will revert to normal (non-fault) operation.

Technical Specifications

Timing Specifications

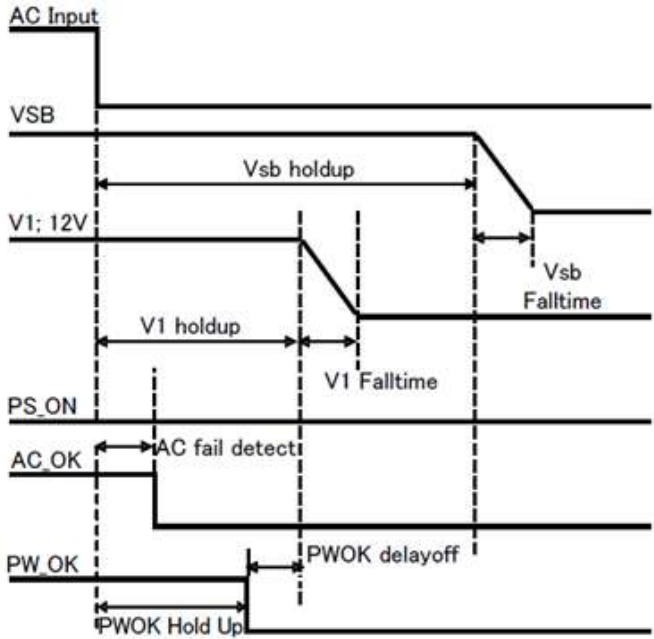
Turn-on delay & output rise time



| Time | Min (ms) | Max (ms) |
|--------------------|----------|----------|
| Vsb Rise Time | 10 | 200 |
| V1 Rise Time | 20 | 200 |
| Vsb Power-on Delay | - | 2700 |
| V1 Power-on Delay | - | 3000 |
| V1 PS_ON Delay | 100 | 150 |
| V1 PW_OK Delay | 100 | 300 |
| ACOK detect | 300 | 1000 |

The turn-on delay after apply of AC input (within the operating range) shall as defined in the following tables. The output rise times shall be measured from 10% of the nominal outputs to the lower limit of the regulation band as defined in the following tables.

Power removal holdup, fall time and signaling



| Power Removal Timing | Min | Max | Notes |
|-----------------------------|------|------|-----------|
| Vsb holdup | 40ms | - | |
| V1 holdup (effective Total) | 12ms | - | 650W |
| AC fail detect | - | 40ms | |
| PW_OK delay off | 1ms | - | Full load |
| PW_OK Hold up | 5ms | - | Full load |

Technical Specifications

Design Features

Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus.

All signals are referenced to 'SGND'.

Pull-up resistors: The clock, data, and SMBAlert lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I2C and SMBus standards.

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current complies to the I²C / SMBus specifications.

Serial Data (SDA): This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current complies to the I²C / SMBus specifications.

Digital Feature Descriptions

PMBus[®] compliance: The rectifier is fully compliant to the Power Management Bus (PMBus[®]) rev1.2 requirements. This Specification can be obtained from www.pmbus.org.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus[®] specification.

All communication over the PMBus[®] interface must support the Packet Error Checking (PEC) scheme. The PMBus[®] master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing a SMBAlert to the 'host' controller.

If a non-supported read is requested the rectifier will return 0x00h for data.

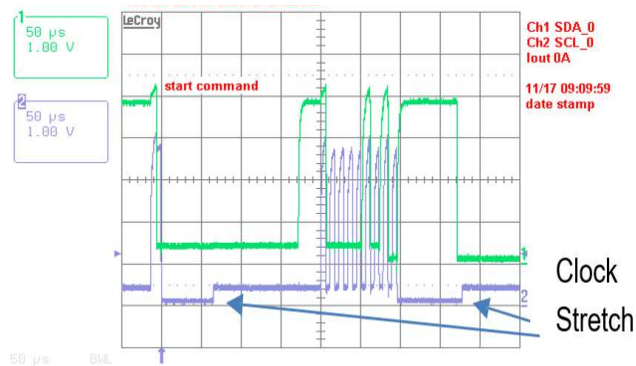
Data out-of-range: The rectifier validates data settings and sets the data out-of-range bit and SMBAlert if the data is not within acceptable range.

Master/Slave: The 'host controller' is always the MASTER. Rectifiers are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The 'slave' μ Controller inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller.

The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier. Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.



I²C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The rectifiers default to the 100kHz clock rate.

Packet Error Checking (PEC): The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the desired command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus[®] requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

SMBAlert: The μ C driven SMBAlert signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the rectifier has changed states and the signal will be latched LO until the rectifier receives a 'clear_faults' instruction.

The signal will be triggered for any state change, including the following conditions:

- VIN under or over voltage
- Vout under or over voltage
- OUT over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- SMBAlert is asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the SMBAlert signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled

The rectifier will re-assert the Alert line if the internal state of the rectifier has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the rectifier. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

Technical Specifications

Re-initialization: The I2C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Reinitialization is designed to guarantee that the I2C μ Controller does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few μ seconds required to accomplish reinitialization the I2C μ Controller may not recognize a command sent to it. (i.e. a start condition).

Read back delay: The rectifier issues the SMBAlert notification as soon as the first state change occurred. During an event a few different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive SMBAlert could be triggered by the transitioning state of the rectifier. In order to avoid successive SMBAlerts and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of a SMBAlert before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

Successive read backs: Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Global Broadcast: This is a powerful command because it instructs all rectifiers to respond simultaneously. A read instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

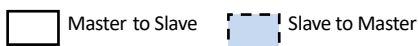
For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth acknowledge bit. To be certain that each rectifier responded to the global instruction, a READ instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

PMBus[®] Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

| | | | | | | | | |
|---|---------------|--|--|----|--------------|--|--|---|
| 1 | 8 | | | 1 | 8 | | | 1 |
| S | Slave address | | | Wr | Command Code | | | A |

| | | | | | | | | |
|---------------|--|---|----------------|--|---|-----|---|---|
| 8 | | 1 | 8 | | 1 | 8 | 1 | 1 |
| Low data byte | | A | High data byte | | A | PEC | A | P |



SMBUS annotations; S – Start, Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

| | | | | | | | | | |
|---|---------------|--|--|----|---|--------------|--|--|---|
| 1 | 7 | | | 1 | 1 | 8 | | | 1 |
| S | Slave address | | | Wr | A | Command Code | | | A |

| | | | | | | | | | |
|----|---------------|--|--|----|---|-----|--|--|---|
| 1 | 7 | | | 1 | 1 | 8 | | | 1 |
| Sr | Slave Address | | | Rd | A | LSB | | | A |

| | | | | | | |
|-----|--|---|-----|--|----|---|
| 8 | | 1 | 8 | | 1 | 1 |
| MSB | | A | PEC | | NA | P |

Block communications: When writing or reading more than two bytes of data at a time BLOCK instruction for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

| | | | | | | | | | |
|---|---------------|--|--|----|---|--------------|--|--|---|
| 1 | 7 | | | 1 | 1 | 8 | | | 1 |
| S | Slave address | | | Wr | A | Command Code | | | A |

| | | | | | | |
|----------------|--|---|--------|---|--------|---|
| 8 | | 1 | 8 | 1 | 8 | 1 |
| Byte count = N | | A | Data 1 | A | Data 2 | A |

| | | | | | | |
|-------|---|--------|---|-----|---|---|
| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
| | A | Data N | A | PEC | A | P |

Block read format:

| | | | | | | | | | |
|---|---------------|--|--|----|---|--------------|--|--|---|
| 1 | 7 | | | 1 | 1 | 8 | | | 1 |
| S | Slave address | | | Wr | A | Command Code | | | A |

| | | | | | |
|----|---------------|--|--|----|---|
| 1 | 7 | | | 1 | 1 |
| Sr | Slave Address | | | Rd | A |

| | | | | | | |
|----------------|--|---|--------|---|--------|---|
| 8 | | 1 | 8 | 1 | 8 | 1 |
| Byte count = N | | A | Data 1 | A | Data 2 | A |

| | | | | | | |
|-------|---|--------|---|-----|----|---|
| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
| | A | Data N | A | PEC | NA | P |

Linear Data Format: The definition is identical to Part II of the PMBus[®] Specification. All standard PMBus[®] values, except for output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16-bit mantissa. Output voltage has an E=–9 constant exponent.

The Linear Data Format is a two-byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

| Data Byte High | | | | | | | | Data Byte Low | | | | | | | | |
|----------------|--------------|---|---|---|---|---|---|---------------|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Exponent (E) | | | | | | | Mantissa (M) | | | | | | | | |

The relationship between the Mantissa, Exponent, and Actual. Value (V) is given by the following equation:

$$V = M * 2^E$$

Where: V is the value, M is the 11-bit, two's complement mantissa, E is the 5-bit, two's complement exponent.

Technical Specifications

Standard features

Supported features that are not readable: The commands below are supported at the described setting, but they cannot be read back through the command set.

Status and Alarm registers: The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear_fault command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault persists after the clear_faults is commanded, the register bit annunciating the fault is reset again.

| Command | Comments |
|-----------------------|---|
| ON_OFF_CONFIG (0x02) | Both the CNTL pin, and the OPERATION command, enabling or disabling the output, are supported. Other options are not supported. |
| Capability (0x19) | 400KHz, ALERT# |
| PMBus revision (0x98) | 1.2 |

PMBus® Addressing

Hardware setting: The signal pin, ADDR(A3) configure the address of the power supply. Note that the ground reference for addressing is Signal Ground (SGND). Internally each power supply has a 10kΩ pull up resistor between the ADDR pin and 3.3V. The resistance between the ADDR pin and SGND shall determine the values for A2-A0. The nominal resistor and corresponding voltage value for each position is tabulated below.

| ADDR PIN (A3) resistor to GND (K-ohm) | Nominal voltage(V) | Address | | |
|---------------------------------------|--------------------|---------|----|----|
| | | A2 | A1 | A0 |
| 0.82 | 0.25 | 0 | 0 | 0 |
| 2.7 | 0.70 | 0 | 0 | 1 |
| 5.6 | 1.18 | 0 | 1 | 0 |
| 8.2 | 1.48 | 0 | 1 | 1 |
| 15 | 1.98 | 1 | 0 | 0 |
| 27 | 2.41 | 1 | 0 | 1 |
| 56 | 2.80 | 1 | 1 | 0 |
| 180 | 3.12 | 1 | 1 | 1 |

Firmware setting:

| Device | Address | Address Bit Assignments (Most to Least Significant) | | | | | | | |
|-----------|---------|---|---|---|---|-----|----|----|-----|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| μP | B0 – BF | 1 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
| Broadcast | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EEprom | A0 – AF | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/W |
| | | MSB | | | | LSB | | | |

PMBus® Command set:

| Command | Hex Code | Data Field | Volatile Memory Storage ² / Default |
|------------------------|----------|------------|--|
| Operation | 0x01 | 1 | Yes |
| Clear_Faults | 0x03 | - | |
| Write_Protect | 0x10 | 1 | Yes/80 |
| Restore_default_all | 0x12 | - | |
| Restore_user_all | 0x16 | - | |
| Store_user_code | 0x17 | 1 | Yes |
| Restore_user_code | 0x18 | 1 | |
| Vout_mode | 0x20 | 1 | |
| Vin_ON | 0x35 | 2 | |
| Vin_OFF | 0x36 | 2 | |
| Fan_config_1_2 | 0x3A | 1 | Yes / 90 |
| Fan_command_1 | 0x3B | 2 | |
| Vout_OV_fault_limit | 0x40 | 2 | Yes / 14.0 |
| Vout_OV_fault_response | 0x41 | 1 | No / 80 |
| Vout_OV_warn_limit | 0x42 | 2 | Yes / 13.5 |
| Vout_UV_warn_limit | 0x43 | 2 | Yes / 10.8 |
| Vout_UV_fault_limit | 0x44 | 2 | Yes / 10.0 |
| Vout_UV_fault_response | 0x45 | 1 | No / C0 |
| Iout_OC_fault_limit | 0x46 | 2 | Yes / 66 |
| Iout_OC_fault_response | 0x47 | 1 | No / F8 |
| Iout_OC_LV_fault_limit | 0x48 | 2 | Yes / 7.0 |
| Iout_OC_warn_limit | 0x4A | 2 | Yes / 62.0 |
| OT_fault_limit | 0x4F | 2 | Yes / 130 |
| OT_fault_response | 0x50 | 1 | Yes / C0 |
| OT_warn_limit | 0x51 | 2 | Yes / 120 |
| Vin_OV_fault_limit | 0x55 | 2 | No / 275 |
| Vin_OV_fault_response | 0x56 | 1 | No / C0 |
| Vin_OV_warn_limit | 0x57 | 2 | Yes / 265 |
| Vin_UV_warn_limit | 0x58 | 2 | Yes / 85.5 |
| Vin_UV_fault_limit | 0x59 | 2 | No / 73 |
| Vin_UV_fault_response | 0x5A | 1 | No / C0 |
| Status_byte | 0x78 | 1 | |
| Status_word (+ byte) | 0x79 | 1 | |
| Status_Vout | 0x7A | 1 | |
| Status_Iout | 0x7B | 1 | |
| Status_Input | 0x7C | 1 | |
| Status_temperature | 0x7D | 1 | |
| Status_CML | 0x7E | 1 | |
| Status_fans_1_2 | 0x81 | 1 | |
| Read_Vin | 0x88 | 2 | |
| Read_Iin | 0x89 | 2 | |
| Read_Vout | 0x8B | 2 | |
| Read_Iout | 0x8C | 2 | |
| Read_temp_primary | 0x8D | 2 | |
| Read_temp_oring | 0x8E | 2 | |
| Read_temp_sr | 0x8F | 2 | |
| Read_fan_speed_1 | 0x90 | 2 | |
| Read_Pin | 0x97 | 2 | |
| Mfr_ID | 0x99 | 6 | |
| Mfr_model | 0x9A | 16 | |
| Mfr_revision | 0x9B | 7 | |
| Mfr_serial | 0x9E | 16 | |

Technical Specifications

| | | |
|--------------------------|------|---|
| Read_firmware_rev | 0xD5 | 7 |
| Read_run_timer | 0xD6 | 4 |
| Read_temp_inlet | 0xDB | 2 |
| Reserved for factory use | 0XDC | |
| Reserved for factory use | 0XDD | |
| Reserved for factory use | 0XDE | |

Command Descriptions

Operation (0x01): Turns the 12V output ON or OFF. The default state is ON at power up. Only the following data bytes are supported:

| FUNCTION | DATA BYTE |
|----------|-----------|
| Unit ON | 0x80 |
| Unit OFF | 0x00 |

To RESET the rectifier using this command, command the rectifier OFF, wait at least 2 seconds, and then command the rectifier back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (0x03): Clears all STATUS and FAULT registers and resets the Alert# line of the I2C side in control. The I2C side not in control cannot clear registers in the power supply. This command is always executable.

If a fault persists after the issuance of the clear_faults command, the specific registers indicating the fault first clears

have their parameters read, regardless of the write_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store_user_code may command. The but then get set again to indicate that the unit is still in the fault state.

WRITE_PROTECT register (0x10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands default setting of this register is enable_all_writes, write_protect 0x00h. The write_protect command must always be accepted.

| FUNCTION | DATA BYTE |
|---|-----------|
| Enable all writes | 00 |
| Disable all writes except write_protect | 80 |
| Disable all writes except write_protect and OPERATION | 40 |

Restore_Default_All (0x12): Restores all operating register values and responses to the factory default parameters set in the rectifier. The factory default cannot be changed.

Restore_default_code (0x14): Restore only a specific register parameter into the operating register section of the rectifier.

Store_user_code (0x17): Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

Restore_user_code (0x18): Restores the user default setting of a single register.

Vout_mode (0x20): This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits

specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout_command. These commands have a 16 bit mantissa. The exponent is fixed by the rectifier and is returned by this command.

Vin_ON (0x35): This is a 'read only' register that informs the controller at

| Mode | Bits [7:5] | Bits [4:0] (Parameter) |
|--------|------------|------------------------|
| Linear | 000b | xxxxxb |

what input voltage level the rectifier turns ON. The default value is tabulated in the data section.

Vin_OFF (0x36): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF. The default value is tabulated in the data section.

Fan_config_1_2 (0x3A): This command requires that the fan speed be commanded by duty cycle. Both fans must be commanded simultaneously. The tachometer pulses per revolution is not used. Default is duty cycle control.

Fan_command_1 (0x3B): This command instructs the rectifier to increase the speed of both fans. The transmitted data byte represents the hex equivalent of duty cycle in percentage, i.e. 100% = 0 x 64h. The command can only increase fan speed, it cannot instruct the rectifier to reduce the fan speed below what the rectifier requires for internal control. An incorrect value will result in a 'data error'.

Sending 00h tells the rectifier to revert back to its internal control.

Vout_OV_fault_limit (0x40): Sets the value at which the main output voltage will shut down. The default OV_fault value is set at 14.0Vdc. This level can be permanently changed and stored in non-volatile memory.

Vout_OV_fault_response (0x41): This is a 'read only' register. The only allowable state is a latched.

Vout_OV_warn_limit (0x42): Sets the value at which a warning will be issued that the output voltage is too high. The default OV_warn limit is set at 13.5Vdc. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_warn_limit (0x43): Sets the value at which a warning will be issued that the output voltage is too low. The default UV_warning limit is set at 10.8Vdc. Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_limit (0x44): Sets the value at which the rectifier will shut down if the output gets below this level. The default UV_fault limit is set at 10Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_response (0x45): This is a 'read only' register. The only allowable state is restart.

Iout_OC_fault_limit (0x46): Sets the value at which the rectifier will shut down at High/Low Line. This level can be permanently changed and stored in non-volatile memory.

Technical Specifications

Iout_OC_fault_response (0x47): This is a 'read only' register. The only allowable state is restart.

Iout_OC_warn_limit (0x4A): Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level at high/low line. This level can be permanently changed and stored in non-volatile memory.

OT_fault_limit (0x4F): Sets the value at which the rectifier responds to an OT event, sensed by the hottest sensor. The response is defined by the OT_fault_response register.

OT_fault_response (0x50): Sets the response if the output overtemperature exceeds the OT_fault_limit value. The default OT_fault_response is hiccup (0xc0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

OT_warn_limit (0x51): Sets the value at which the rectifier issues a warning when the hottest temperature sensor exceeds the warn limit.

Vin_OV_fault_limit (0x55): Sets the value at which the rectifier shuts down because the input voltage exceeds the allowable operational limit. The default Vin_OV_fault_limit is set at 76Vdc. This level can be permanently lowered and stored in non-volatile memory.

Vin_OV_fault_response (0x56): This is a 'read only' register. The only allowable state is restart.

Vin_OV_warn_limit (0x57): Sets the value at which a warning will be issued that the input voltage is too high. The default OV_warn_limit is 74Vdc. This level can be permanently changed and stored in non-volatile memory.

Vin_UV_warn_limit (0x58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV_fault_limit is 40Vdc. This level can be permanently raised, but not lowered, and stored in non-volatile memory.

Vin_UV_fault_limit (0x59): Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default Vin_UV_fault_limit is set at 38Vdc. This level can be permanently raised and stored in non-volatile memory.

Vin_UV_fault_response (0x5A): This is a 'read only' register. The only allowable state is restart.

STATUS_BYTE (0x78): Returns one byte of information with a summary of the most critical device faults.

| Bit Position | Flag | Default Value |
|--------------|------------------------------|---------------|
| 7 | Unit is busy | 0 |
| 6 | OUTPUT OFF | 0 |
| 5 | VOUT Overvoltage Fault | 0 |
| 4 | IOUT Overcurrent Fault | 0 |
| 3 | VIN Undervoltage Fault | 0 |
| 2 | Temperature Fault or Warning | 0 |
| 1 | CML (Comm. Memory Fault) | 0 |
| 0 | None of the above | 0 |

STATUS_WORD (0x79): Returns status_byte as the low byte and the following high_byte.

| Bit Position | Flag | Default Value |
|--------------|--------------------------|---------------|
| 7 | VOUT Fault or Warning | 0 |
| 6 | IOUT Fault or Warning | 0 |
| 5 | INPUT Fault or Warning | 0 |
| 4 | MFR SPECIFIC | 0 |
| 3 | POWER_GOOD# (is negated) | 0 |
| 2 | FAN Fault or Warning | 0 |
| 1 | OTHER | 0 |
| 0 | UNKNOWN Fault or Warning | 0 |

STATUS_VOUT (0x7A): Returns one byte of information of output voltage related faults.

| Bit Position | Flag | Default Value |
|--------------|-----------------|---------------|
| 7 | VOUT OV Fault | 0 |
| 6 | VOUT_OV_WARNING | 0 |
| 5 | VOUT_UV_WARNING | 0 |
| 4 | VOUT UV Fault | 0 |
| 3-0 | X | 0 |

STATUS_IOUT (0x7B): Returns one byte of information of output current related faults.

| Bit Position | Flag | Default Value |
|--------------|------------------------|---------------|
| 7 | IOUT OC Fault | 0 |
| 6 | IOUT OC LV Fault | 0 |
| 5 | IOUT OC Warning | 0 |
| 4 | X | 0 |
| 3 | CURRENT SHARE Fault | 0 |
| 2 | IN POWER LIMITING MODE | 0 |
| 1-0 | X | 0 |

The OC Fault limit sets where current limit is set. The rectifier shuts down below the LV fault limit setting.

STATUS_INPUT (0x7C): Returns one byte of information of input voltage related faults.

| Bit Position | Flag | Default Value |
|--------------|--------------------------------|---------------|
| 7 | VIN_OV_Fault | 0 |
| 6 | VIN_OV_Warning | 0 |
| 5 | VIN_UV_Warning | 0 |
| 4 | VIN_UV_Fault | 0 |
| 3 | Unit OFF for low input voltage | 0 |
| 2 | IIN_OC_Fault | 0 |
| 1-0 | X | 0 |

STATUS_TEMPERATURE (0x7D): Returns one byte of information of temperature related faults.

STATUS_CML (0x7E): Returns one byte of information of communication related faults.

| Bit Position | Flag | Default Value |
|--------------|------------|---------------|
| 7 | OT Fault | 0 |
| 6 | OT Warning | 0 |
| 5-0 | X | 0 |

STATUS_fans_1_2 (0x81): Returns one byte of information of fan status.

| Bit Position | Flag | Default Value |
|--------------|-----------------------------|---------------|
| 7 | Invalid/Unsupported Command | 0 |
| 6 | Invalid/Unsupported Data | 0 |
| 5 | Packet Error Check Failed | 0 |
| 4-2 | X | 0 |
| 1 | Other Communication Fault | 0 |
| 0 | X | 0 |

Technical Specifications

STATUS_fans_1_2 (0X81): Returns one byte of information of fan status.

| Bit Position | Flag | Default Value |
|--------------|-----------------------------|---------------|
| 7 | Fan 1 fault | 0 |
| 6 | X | 0 |
| 5-4 | X | 0 |
| 3-2 | Fan 1 & 2 speed overwritten | 0 |
| 1-0 | X | 0 |

Read back Descriptions

Single parameter read back: Functions can be read back one at a time using the read_word_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

| | | | | |
|---|---------------|----|---|--------------|
| 1 | 8 | 1 | 8 | 1 |
| S | Slave address | Wr | A | Command Code |
| | | | A | A |

| | | |
|----|---------------|----|
| 1 | 8 | 1 |
| Sr | Slave address | Rd |
| | | A |

| | | | | | | |
|-----|---|-----|---|-----|--------|---|
| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
| LSB | A | MSB | A | PEC | No-Ack | P |

Read back error: If the μ C does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read_fan_speed 1 (0x90): Reading the fan speed is in Linear Mode returning the RPM value of the fan.

Read_FRU_ID (0x99, 0x9A, 0x9B, 0x9E): Returns FRU information. Must be executed one register at a time.

| | | | | |
|---|---------------|----|---|--------------|
| 1 | 8 | 1 | 8 | 1 |
| S | Slave address | Wr | A | Command 0x9x |
| | | | A | A |

| | | | | |
|----|---------------|----|---|----------------|
| 1 | 8 | 1 | 8 | 1 |
| Sr | Slave address | Rd | A | Byte count = x |
| | | | A | A |

| | | | | | | | | |
|--------|---|------|---|--------|---|-----|--------|---|
| 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
| Byte_1 | A | Byte | A | Byte_x | A | PEC | No-Ack | P |

Mfr_ID (0x99): Manufacturer in ASCII – 6 characters maximum, General Electric – Critical Power represented as, GE-CP

Mfr_ID (0x9A): Manufacturer model-number in ASCII – 16 characters, for this unit: MPR0712TExxxxxx

Mfr_revision (0x9B): Total 7 bytes, provides the product series number when the product was manufactured.

Mfr_serial (0x9E): Product serial number includes the manufacturing date, KZ – manufacturing location, in this case Matamoros

51 – week of manufacture

018193xxx – serial #, mfr choice

Manufacturer-Specific PMBus® Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Read_firmware_rev [0xD5]: Reads back the firmware revision of all three μ C in the rectifier.

| | | | | | |
|---|---------------|----|---|-------------------|---|
| 1 | 7 | 1 | 1 | 8 | 1 |
| S | Slave address | Wr | A | Command Code 0xDD | A |

| | | | | | | |
|---|----|---------------|----|---|----------------|---|
| 1 | 1 | 7 | 1 | 1 | 8 | 1 |
| A | Sr | Slave Address | Rd | A | Byte Count = 6 | A |

| | | | |
|-------------------|---|-------------------|---|
| 8 | 1 | 8 | 1 |
| Primary major rev | A | Primary minor rev | A |

| | | | |
|---------------------|---|---------------------|---|
| 8 | 1 | 8 | 1 |
| Secondary major rev | A | Secondary minor rev | A |

| | | | | | | |
|---------------|---|--------------|---|-----|--------|---|
| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
| i2c major rev | A | i2c revision | A | PEC | No-ack | P |

Read_run_timer [0xD6]: This command reads back the recorded operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it

delivers main output power. Recorded capacity is approximately 10 years of operational state.

| | | | | | |
|---|---------------|----|---|-------------------|---|
| 1 | 7 | 1 | 1 | 8 | 1 |
| S | Slave address | Wr | A | Command Code 0xDE | A |

| | | | | | |
|----|---------------|----|---|----------------|---|
| 1 | 7 | 1 | 1 | 8 | 1 |
| Sr | Slave Address | Rd | A | Byte count = 3 | A |

| | | | | | |
|------------|---|------|---|------------|---|
| 8 | 1 | 8 | 1 | 8 | 1 |
| Time - LSB | A | Time | A | Time - MSB | A |

| | | |
|-----|--------|---|
| 8 | 1 | 1 |
| PEC | No-ack | P |

Technical Specifications

General performance descriptions

Default state: Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store_user_code).

Restart after a latching: PMBus™ fault_response commands can be configured to direct the rectifier to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin ON/OFF may be cycled OFF and then ON.
2. The unit may be commanded to restart via i2c through the Operation command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from latch off to restart.

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, except for changing to restart.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

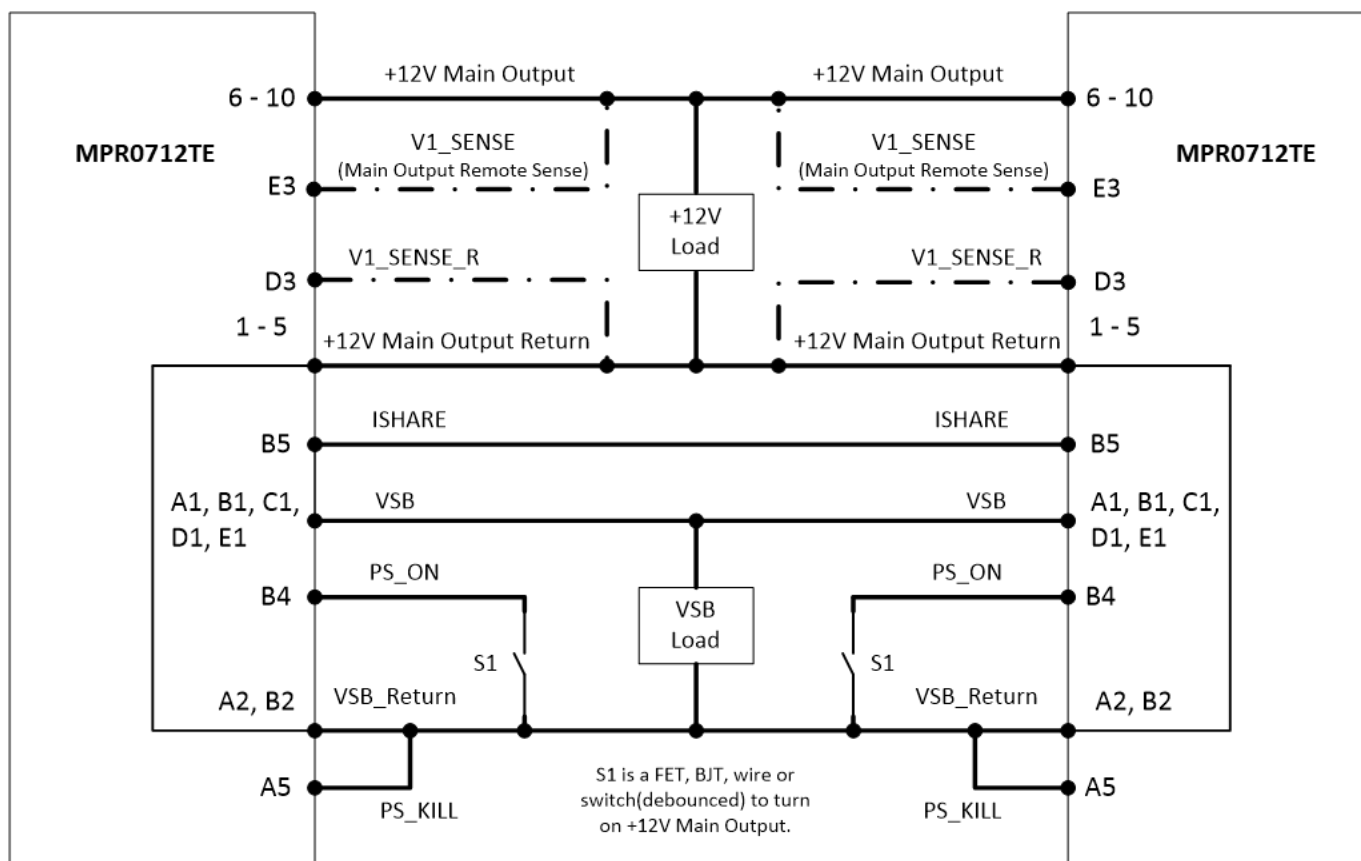
A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Auto_restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the

Wiring diagram for output

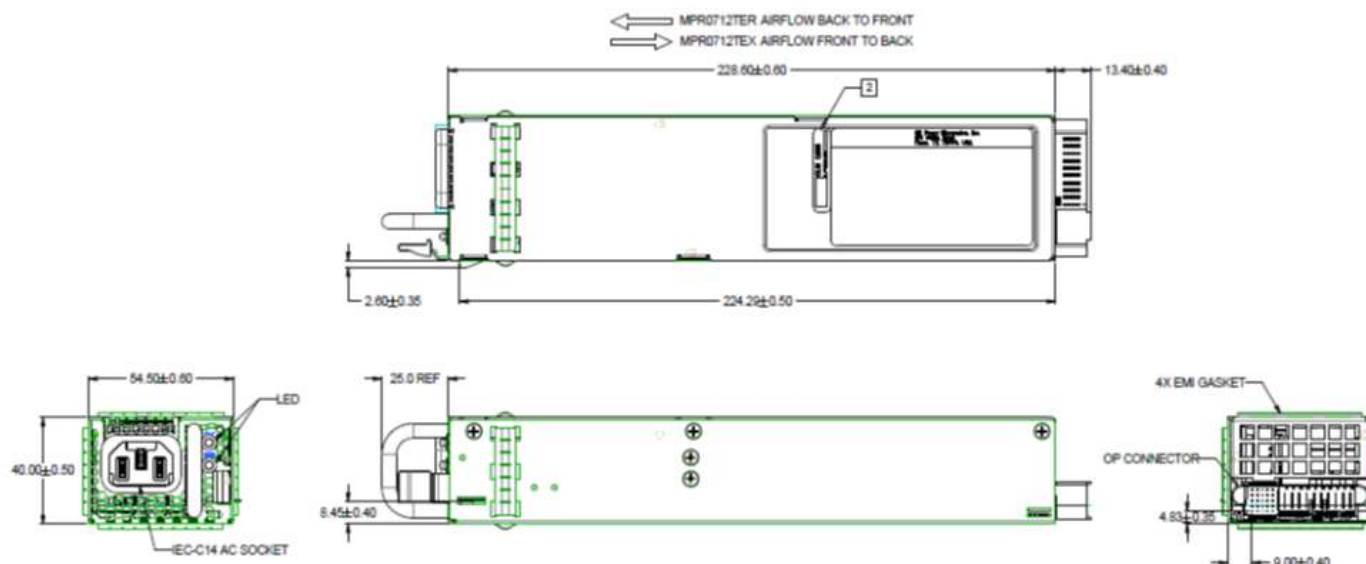


CURRENT SHARING NOTS

Main current sharing is achieved using active current share method details Current sharing can be achieved with or without the remote sense (V_SENSE) connected to the common load. +VSB outputs can be tied together for redundancy but total combined output power must not exceed the related standby power. The +VSB output has an internal ORING MOSFET for additional redundancy/internal short protection. The current sharing pin B5 is connected between sharing units (from an ISHARE bus). It is an input and/or an output (bi-directional analogue bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit, the voltage on the pin (and the common IHSARE bus would read 8VDC at 100% load. For two units sharing the same load this would read 4VDC for perfect current sharing (i.e. 50% load per unit). The load for both the main 12V and VSB rails at the initial startup shall not be allowed to exceed the capability of a single unit. The load can be increased after a delay of 3sec (minimum), to allow all sharing units to achieve steady regulation.

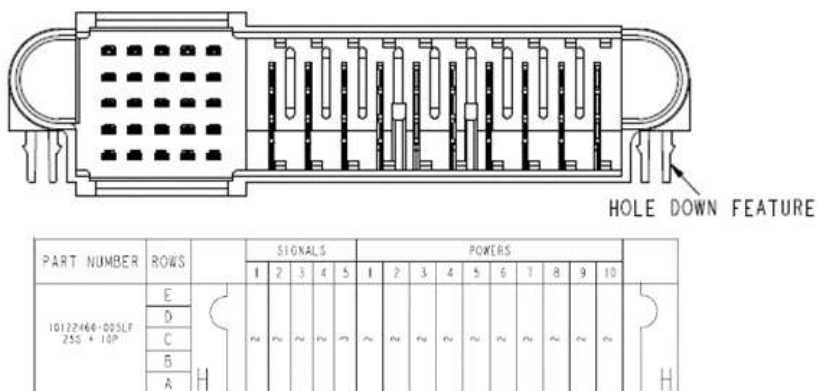
Technical Specifications

Mechanical Outline



Connector Pin Assignments

Input Connector: IEC320, C14; mating connector: IEC320, C13 type
Output Connector: MiniPAK HDL, 25s10p, RA Plug TE CONNECTIVITY 1926736-3
Mating connector: TE Connectivity 1926736-5



With respect to signals "3" in Columns 5, refers to the shortest level signal pin; the "shortest" pins are the "last to make, first to break" in the mating sequence

| Pin | Function | Description | Pin | Function | Description |
|------------|------------------|---------------------------------------|-----|------------|---------------------------------|
| 6,7,8,9,10 | +12V_OUT | +12V Main Output | C3 | SDA | I2C Serial Data Line |
| 1,2,3,4,5 | +12V_RTN | +12V Main Output Return | D3 | V1_SENSE_R | Remote Sense Return (-VE) |
| A1 | +VSB | Standby Output | E3 | V1_SENSE | Remote Sense (+VE) |
| B1 | +VSB | Standby Output | A4 | SCL | I2C Serial Clock Line |
| C1 | +VSB | Standby Output | B4 | PS_ON_L | Remote On/Off (Enable/Disable) |
| D1 | +VSB | Standby Output | C4 | SMB_ALERT | Alert signal to host system |
| E1 | +VSB | Standby Output | D4 | Unused | No End User Connection |
| A2 | +VSB_Return/SGND | Standby Output Return / Signal Ground | E4 | Input_OK | Input Source Present & "OK" |
| B2 | +VSB_Return/SGND | Standby Output Return / Signal Ground | A5 | PS_KILL | Power Supply "kill"; short pin |
| C2 | Unused | No End User Connection | B5 | ISHARE | Current Share bus; short pin |
| D2 | Unused | No End User Connection | C5 | PW_OK | Power "OK"; short pin |
| E2 | Unused | No End User Connection | D5 | Unused | No End User Connection |
| A3 | Address | Address | E5 | PRESENT_L | Power Module Present; short pin |
| B3 | Unused | No End User Connection | | | |

Technical Specifications

Ordering Information

Please contact your ABB Sales Representative for pricing, availability and optional features.

| PRODUCT | OUTPUT | STANDBY | AIRFLOW | ORDERING PART NUMBER |
|------------------|--|---------|-------------------------------|----------------------|
| MPR0712TEX12Z01A | 700W, +12Vout AC Input front-end with 12Vsbaux | 12V @2A | Standard (from ACin to DCout) | MPR0712TEX12Z01A |
| MPR0712TER12Z02A | 700W +12Vout AC Input front-end with 12Vsb aux; reverse air flow | 12V @2A | Reverse (from DCout to ACin) | MPR0712TER12Z02A |



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