3 W Power Amplifier
4.0 - 5.9 GHz

XP1044-QL
Rev. V7

Features

- P1dB = 34 dBm
- P_{OUT} 26 dBm @ EVM = 2.5% (PAR = 9.17 dB)
- OIP3 = 46 dBm
- Gain = 18.5 dB
- Voltage Supply = 8 V
- Input Internally Matched
- 7 mm Surface Mount Package
- RoHS* Compliant

Applications

- Wireless Networking & Communications
- ISM

Description

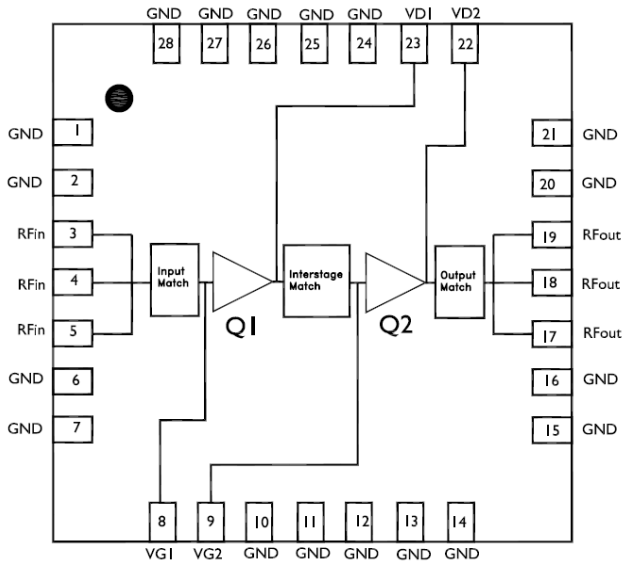
The XP1044 is a highly linear 2-stage power amplifier capable of 18.5 dB of gain, 34 dBm of power at 1 dB compression and is housed in an RoHS compliant 7 mm package. The XP1044 provides less than 2.5% EVM at 26 dBm output power with 802.16 OFDM signal and peak to average ratio 9.17 dB. The input and output of the device are internally pre-matched facilitating a simplified input and output match. This product operates off an 8 V voltage supply and requires negative voltage which is used for current control.

The XP1044-QL is specifically designed for WiMAX applications between 4.9 GHz and 5.9 GHz, and the performance can be shifted by adding external matching components to cover applications between 4 GHz and 5 GHz.

Ordering Information

Part Number	Package
XP1044-QL-0N00	bulk quantity
XP1044-QL-EV1	evaluation module for 4.9 GHz ~ 5.9 GHz
XP1044-QL-EV2	evaluation module for 4.0 GHz ~ 5.0 GHz

Functional Block Diagram



Pin Configuration

Pin #	Function
1,2,6,7,10,11,12,13,14,15, 16,20,21,24,25,26,27,28	Ground
3,4,5	RF Input
8	Gate Voltage1
9	Gate Voltage2
17,18,19	RF Output
23	Drain Voltage1
22	Drain Voltage2

Electrical Specifications: 4.9 - 5.9 GHz (5.8 GHz Typ.), T_A = 25°C[1]

Parameter	Units	Min.	Typ.	Max.
Power Gain	dB	16.5	18.5	—
Linear Power (@ EVM = 2.5%, OFDM, 802.16 PAR = 9.17 dB)	dBm	—	26	—
Input Return Loss (S11)	dB	—	-10	—
Output IP3 @ 22 dBm/Tone	dBm	44	46	—
Noise Figure	dB	—	5	—
Output P1dB	dBm	32.5	34.0	—
Supply Current Stage 1 ($I_{DD}1$) Stage 2 ($I_{DD}2$)	mA	—	 300 600	—
Gate Voltage Stage 1 (V_G1) Stage 2 (V_G2)	V	 -1.2 -1.2	 -0.85 -0.85	 -0.5 -0.5
Supply Voltage (V_D1 & V_D2)	V	—	8	—

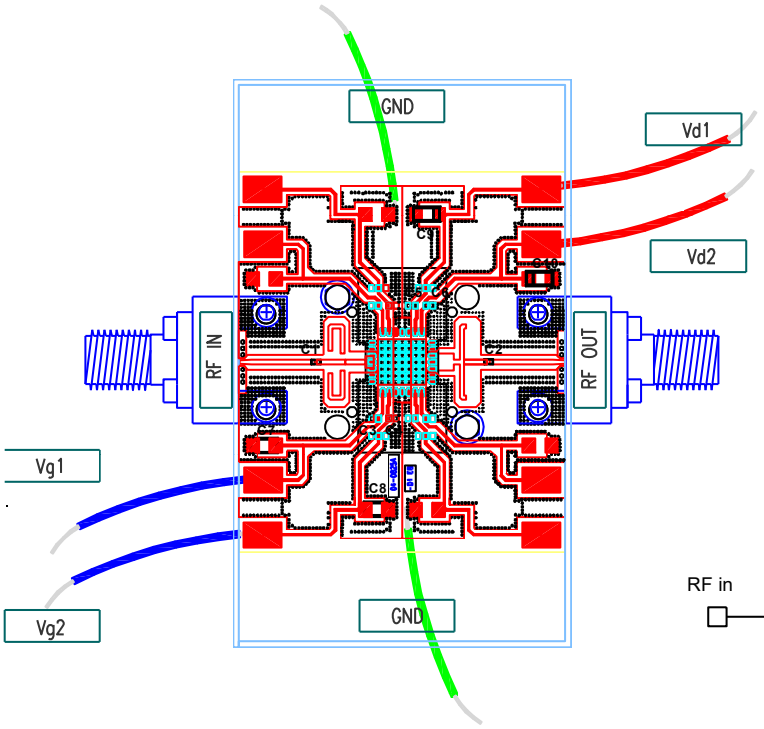
1. Unless otherwise specified, the following specifications are guaranteed at room temperature in a MACOM test fixture.

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Drain Supply Voltage (V_D)	+9 V
Gate Supply Voltage (V_G)	0 V ~ -5 V
RF Input Power (RF_{IN})	23 dBm
Stage 1 Current ($I_{DD}1$)	375 mA
Stage 2 Current ($I_{DD}2$)	750 mA
Power Dissipation (P_{DISS})	9 W
Storage Temperature	-55°C to +150°C
Junctions Temperature	+175°C
Operating Temperature[4] (T_A)	-40°C
ESD (HBM)	Class 1A
Moisture Sensitivity Level (MSL)	MSL3
Thermal Resistance[5] (R_{TH})	+15.6°C

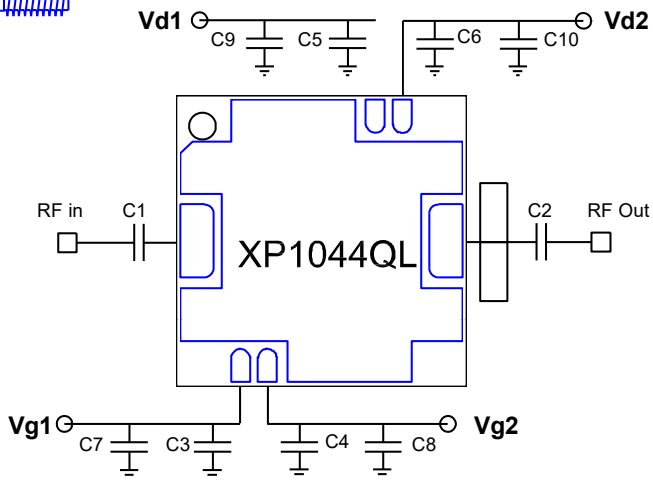
2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Calculate maximum operating backside temperature using: Tmax = 167°C – [V_D*$I_{DD}2$*R_{TH}]. Thermal resistance of the 1st stage is 2x R_{TH} of the output stage, and therefore $I_{DD}1$ must not exceed ½ $I_{DD}2$ for a specific maximum temperature.
5. Thermal resistance of stage 2 only.

Evaluation Board Layout (4.9 GHz ~ 5.9 GHz)

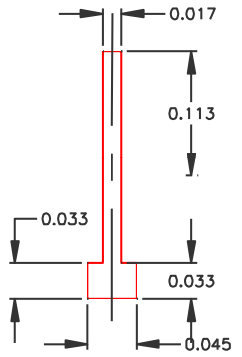


Ref Designator	Description	QTY
C1 , C2	10.0 pF 0402 Capacitor	1
C3, C4, C5, C6	1000 pF 0402 Capacitor	4
C7, C8, C9, C10	1 uF A-Case Capacitor	4

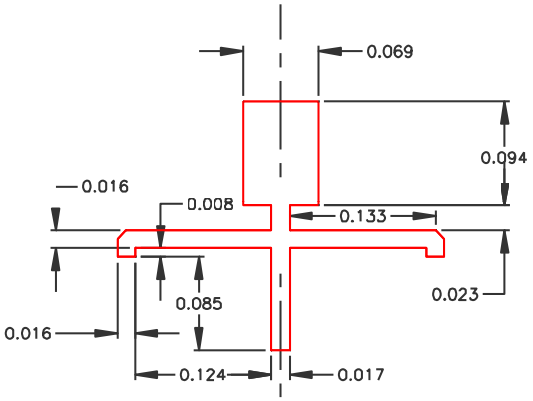
Material: Rogers 4003
Thickness: 8mil



Dimensions are in inches.



Input Match Details

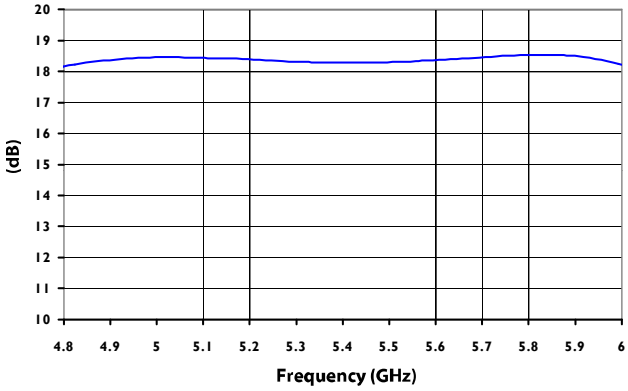


Output Match Details

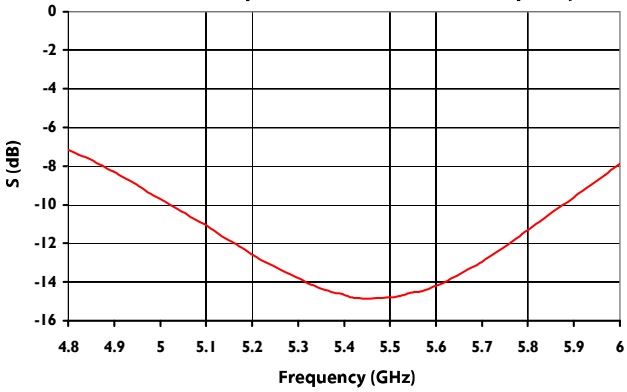
For improved performance at 6 GHz the thick transmission line (W = 0.069") on the output can be extended to touch the two open stubs.

Typical Performance Curves (EV1, $I_{DQ}1$ = 300 mA, $I_{DQ}2$ = 600 mA)

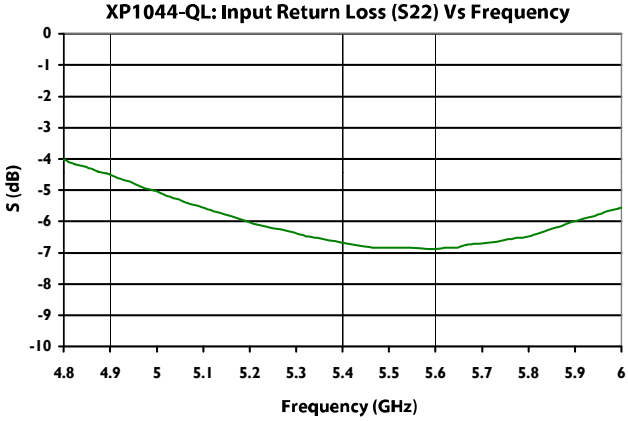
XP1044-QL: Gain Vs Frequency



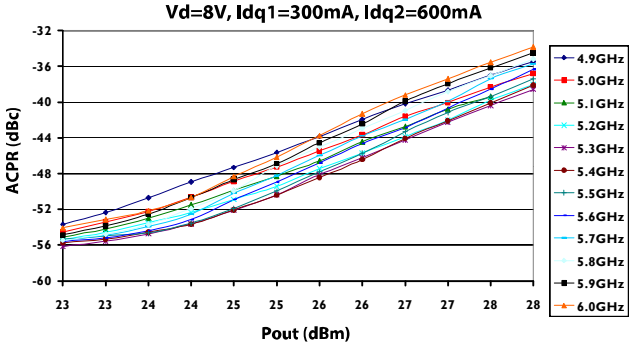
XP1044-QL: Input Return Loss (S11) Vs Frequency



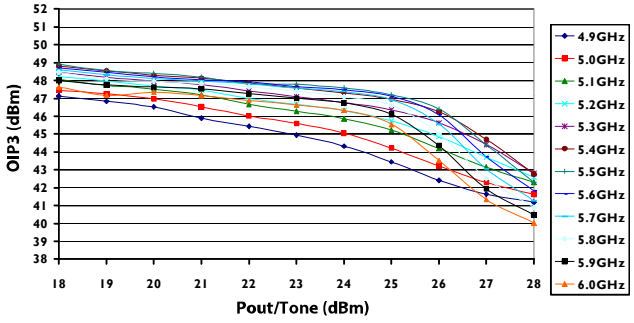
XP1044-QL: Input Return Loss (S22) Vs Frequency



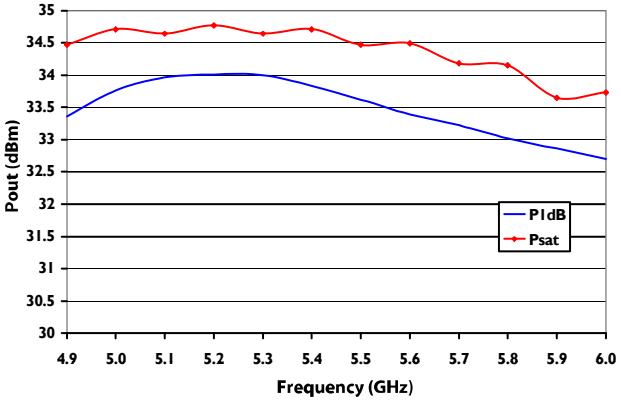
XP1044-QL: WCDMA 3GPP Downlink ACPR vs. Pout
Vd=8V, Idq1=300mA, Idq2=600mA



XP1044-QL: OIP3 vs. Pout
Vd=8V, Idq1=300mA, Idq2=600mA

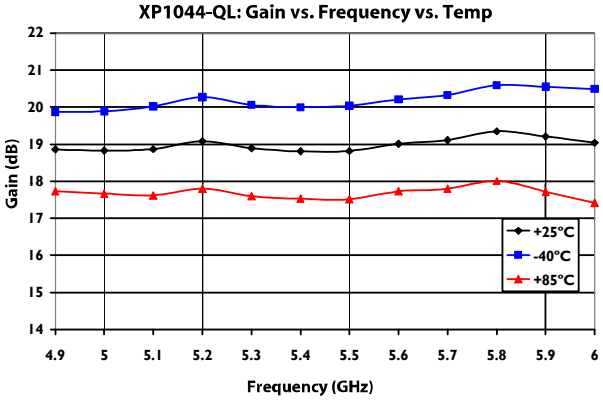


XP1044-QL: Power vs. Frequency
Vd=8V, Idq1 = 300mA, Idq2 = 600mA

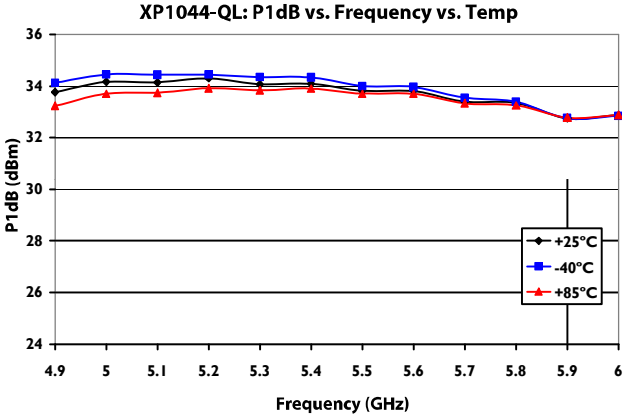


Typical Performance Curves (EV1, $I_{DQ}1$ = 300 mA, $I_{DQ}2$ = 600 mA, Over Temp)

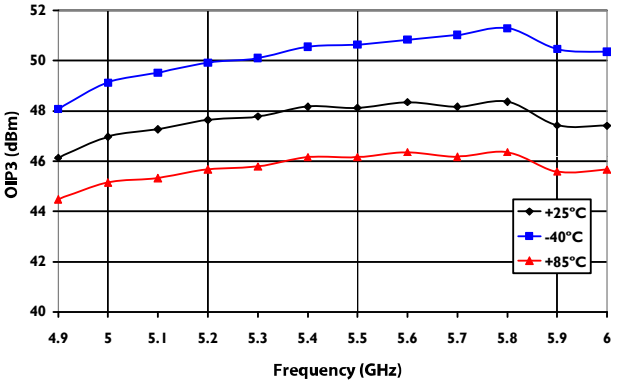
XP1044-QL: Gain vs. Frequency vs. Temp



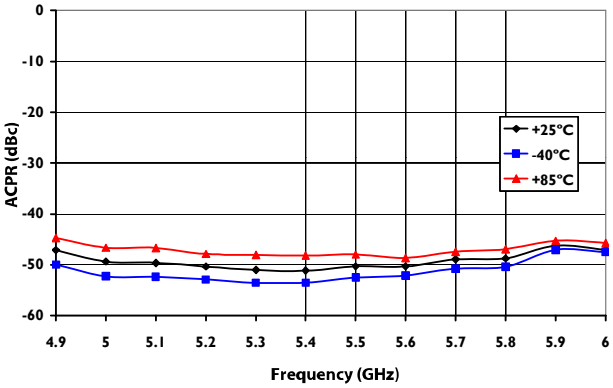
XP1044-QL: P1dB vs. Frequency vs. Temp



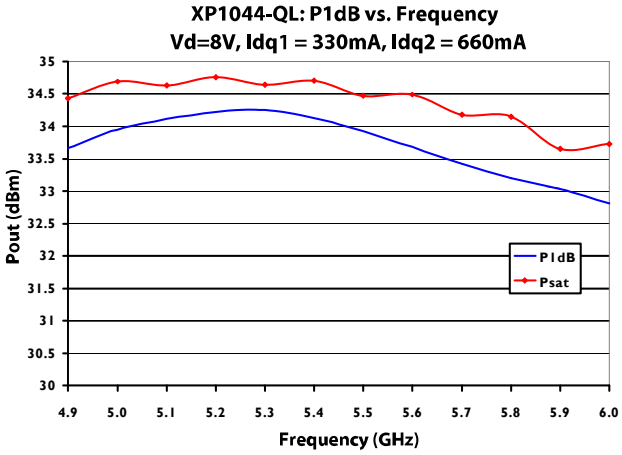
XP1044-QL: OIP3 vs. Frequency vs. Temp

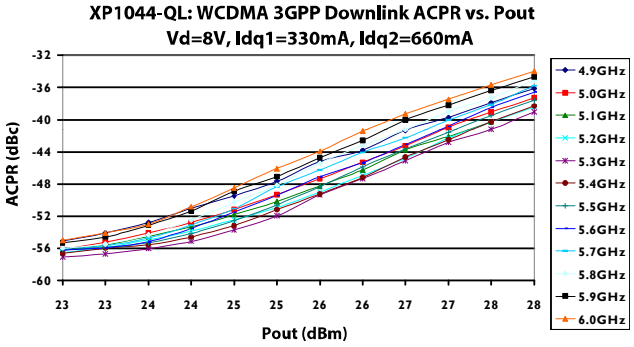


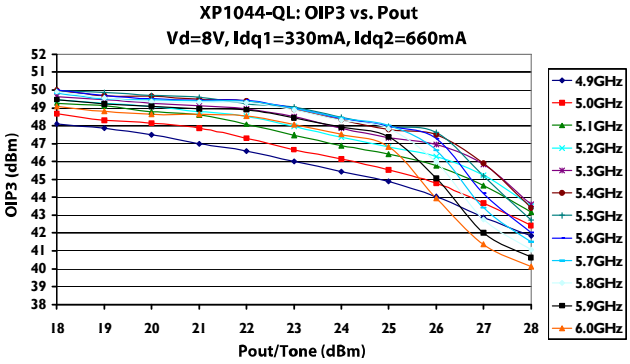
XP1044-QL: WCDMA ACPR vs. Frequency vs. Temp



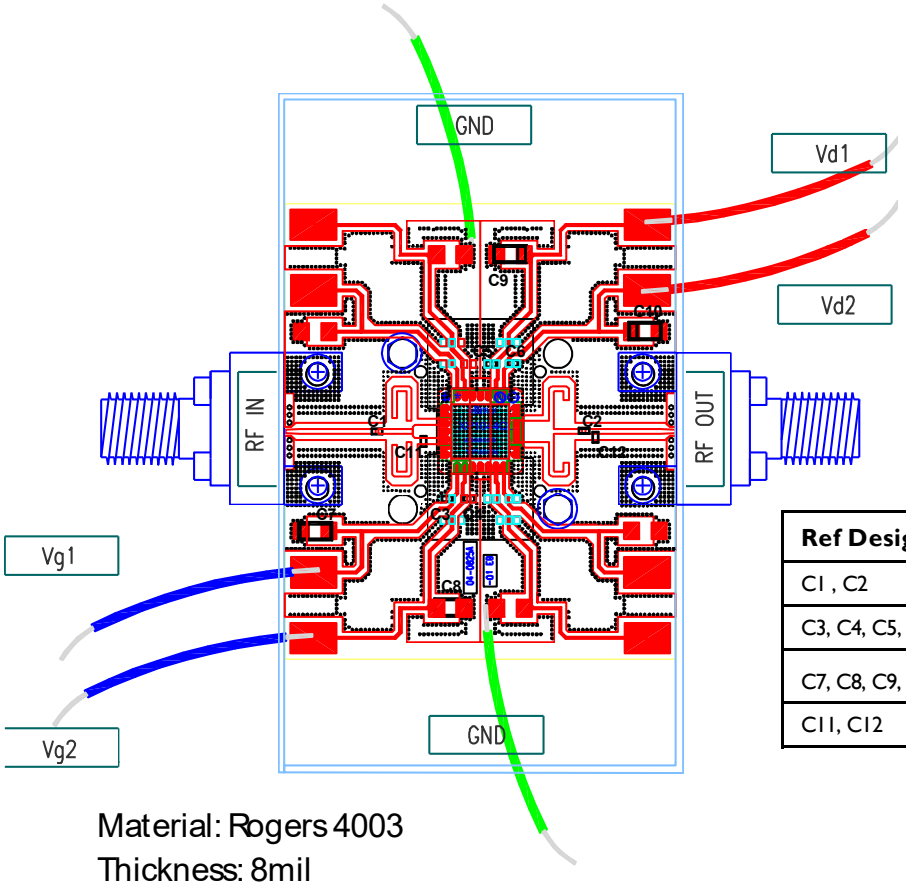
Typical Performance Curves (EV1, $I_{DQ}1$ = 330 mA, $I_{DQ}2$ = 660 mA)





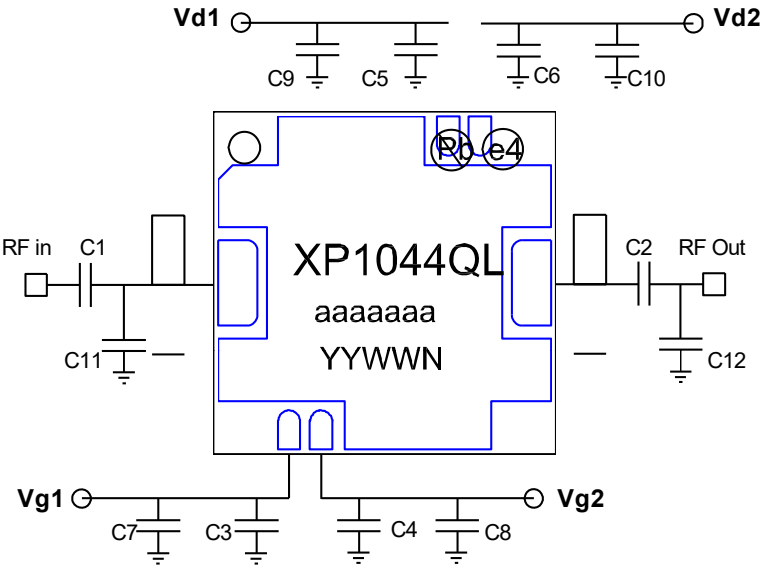


Evaluation Board Layout: EV2 (4.0 GHz ~ 5.0 GHz)



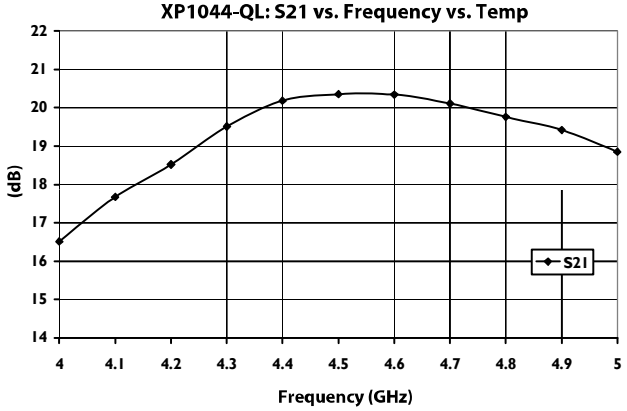
Ref Designator	Description	QTY
C1 , C2	10.0 pF 0402 Capacitor	1
C3, C4, C5, C6	1000 pF 0402 Capacitor	4
C7, C8, C9, C10	1 uF A-Case Capacitor	4
C11, C12	0.5 pF 0402 Capacitor	2

Material: Rogers 4003
Thickness: 8mil

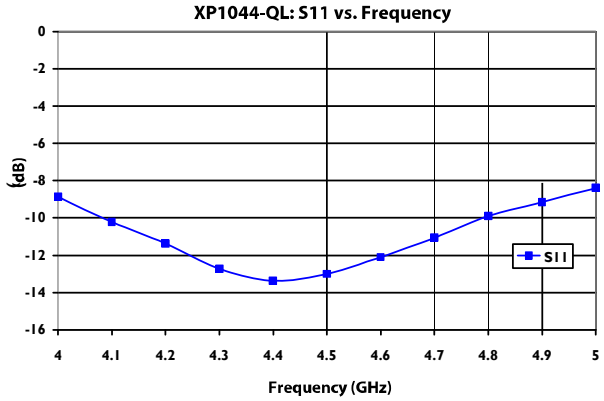


Typical Performance Curves (EV2, $I_{DQ}1$ = 300 mA, $I_{DQ}2$ = 600 mA)

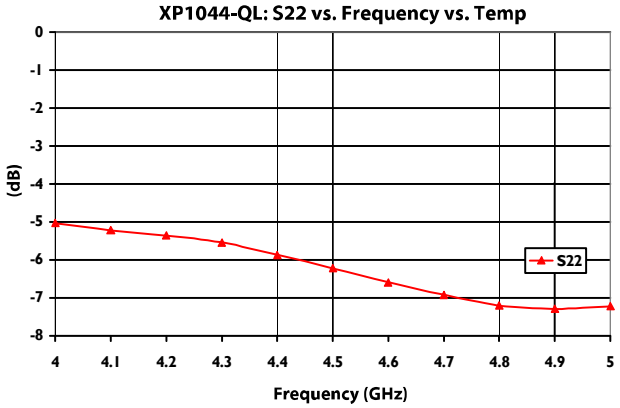
XP1044-QL: S21 vs. Frequency vs. Temp



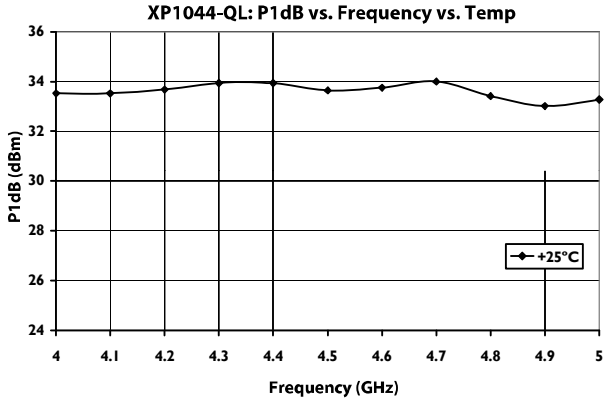
XP1044-QL: S11 vs. Frequency



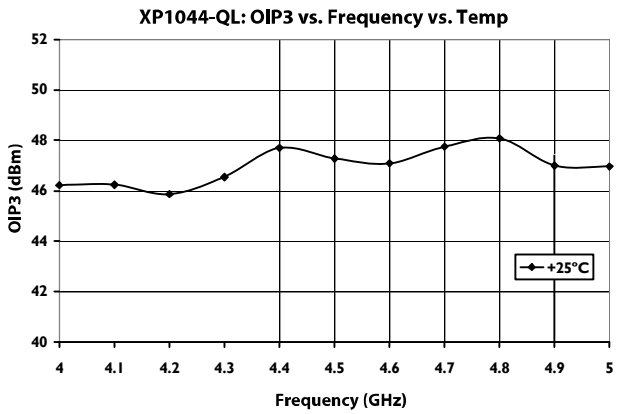
XP1044-QL: S22 vs. Frequency vs. Temp



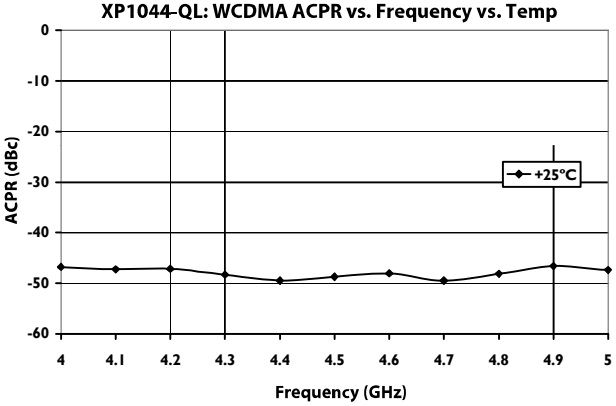
XP1044-QL: P1dB vs. Frequency vs. Temp



XP1044-QL: OIP3 vs. Frequency vs. Temp



XP1044-QL: WCDMA ACPR vs. Frequency vs. Temp



App Note [1] Biasing -

The XP1044-QL requires power supply sequencing. Negative voltage supply (V_G) needs to be turned on first and then positive voltage can be applied to the drain (V_D). When turning off the device, the positive supply (V_D) should be turned off first and then negative voltage (V_G) can be removed.

The gate voltage is adjusted in order to set the drain current to the desired level. The gate voltage required to achieve a certain current can vary over temperature and from one device to another due to pinch-off voltage variation. Constant drain current can be achieved by implementing an active bias circuit which allows for temperature compensation and eliminates the effect of pinch off voltage variation.

The input stage transistor periphery is half of the output stage transistor periphery and therefore the gate voltages needed to set the first stage current to 300 mA and the second stage current to 600 mA are the same. The gate voltages can be connected together and a single active bias circuit can be implemented adding a total of 6 components.

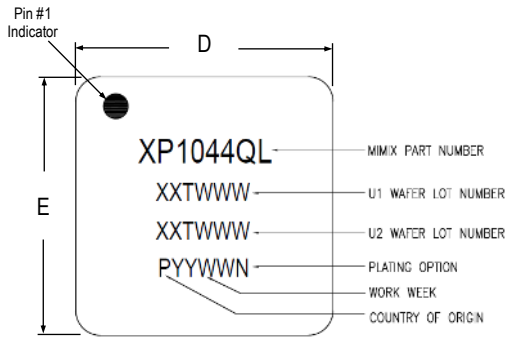
Handling Procedures

Please observe the following precautions to avoid damage:

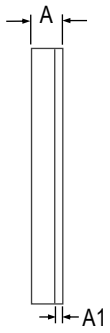
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

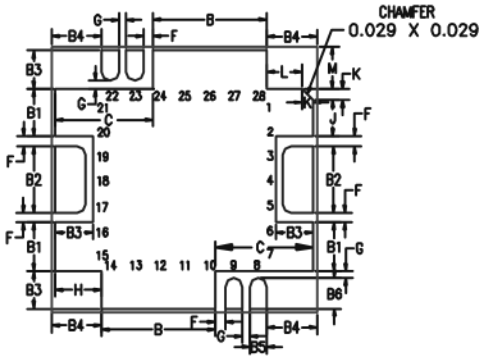
Lead-Free Package Dimensions/Layout



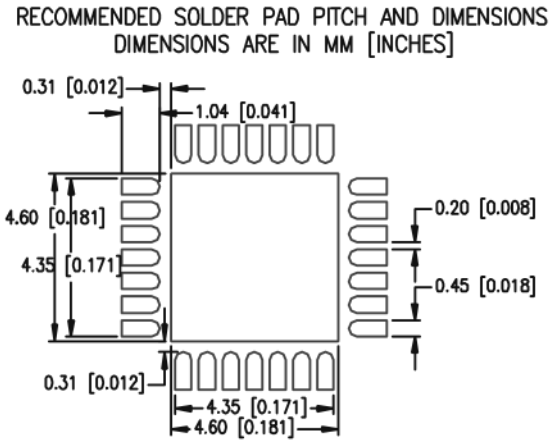
Top View



Side View



Bottom View



Designator	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.86	0.96	1.06	0.034	0.038	0.042
A1	—	0.20	—	—	0.008	—
B	0.40	3.00	0.50	0.113	0.118	0.023
B1	1.21	1.26	1.31	0.045	0.050	0.055
B2	1.70	1.75	1.80	0.064	0.069	0.074
B3	0.94	0.99	1.04	0.034	0.039	0.044
B4	1.27	1.32	1.37	0.047	0.052	0.057
B5	0.41	0.46	0.51	0.013	0.018	0.023
B6	0.75	0.80	0.85	0.026	0.031	0.036
C	2.47	2.52	2.57	0.094	0.099	0.104
D	7.00 BSC			0.276		
E	7.00 BSC			0.276		
F	0.20	0.25	0.30	0.005	0.010	0.015
G	0.14	0.19	0.24	0.002	0.007	0.012
H	1.17	1.22	1.27	0.043	0.048	0.053
J	0.92	O.97	1.02	0.033	0.038	0.043
K	0.24	0.29	0.34	0.006	0.011	0.016
L	0.88	0.93	0.97	0.031	0.036	0.041
M	1.05	1.10	1.15	0.038	0.043	0.048