

Ph. 480-503-4295 | NOPP@FocusLCD.com

TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

Graphic Display Module

Part Number

G126ADGFGN02WRC0XAL

Overview

128x64(56x39), FSTN, Gray background, No Backlight, Top view, Wide temp, Reflective (Positive), 3.0V LCD, Controller=ST7565R, RoHS Compliant

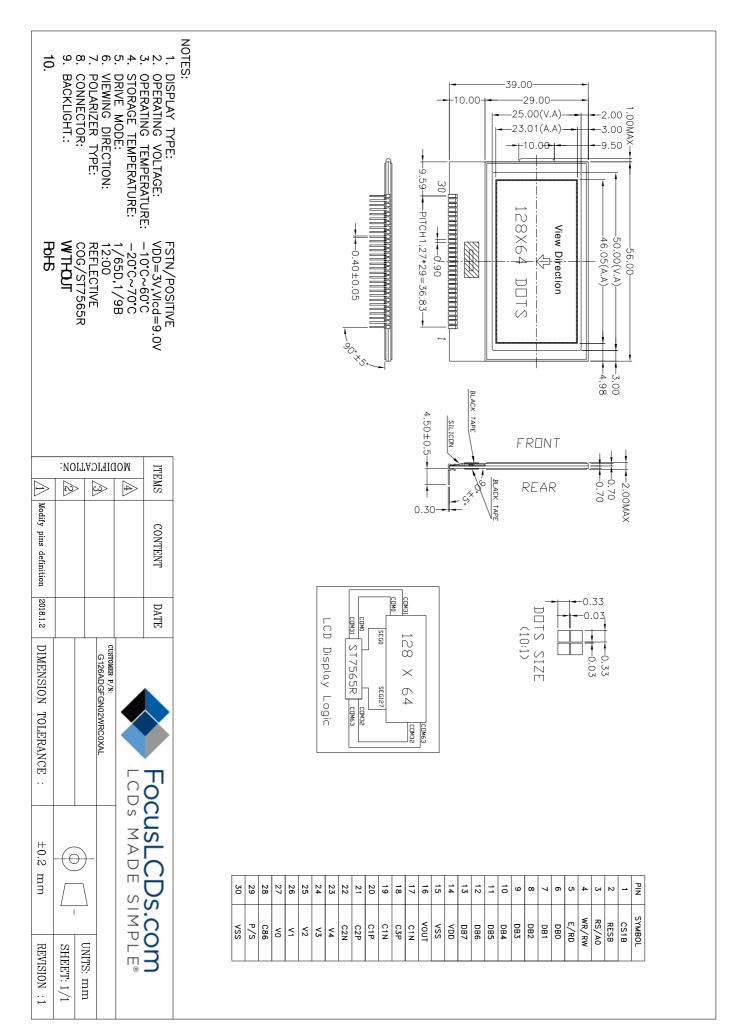


FEATURES

- 1. Support display capacity: 128 x 64 Pixels dots with FSTN mode.
- 2. On-chip Display Data RAM, Capacity: $128 \times 64 = 8'192$ bits.
- 3. Serial interfaces are supported.
- 4. Abundant command functions Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction selects, power saver, static indicator, common output status select, Vo voltage regulation internal resistor ratio set.
- 5. Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- 6. Low-power liquid crystal display power supply circuit equipped internally. Booster circuit (with Boost ratios of 4X/5X, where the step-up voltage reference power supply can be input externally).
- 7. High-accuracy voltage adjustment circuit (Thermal gradient –0.05%/°C) V0 voltage regulator resistors equipped internally, V1 to VSS voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- 8. CR oscillator circuit equipped internally.
- 9. Extremely low power consumption Operating power when the built-in power supply is used (an example) 60uA (VDD VSS = 3.0 V, Quad voltage, V0 VSS= 11.0 V). Conditions: When displays pattern OFF and the normal mode is selected.
- 10. Power supply operate on the low 1.8 voltage Logic power supply
 - -- VDD VSS = 1.8V to 3.3 V (+10% Range)
 - -- Boost reference voltage: VDD2 VSS = 2.4V to 3.3V
 - -- Booster maximum voltage limited
 - -- Liquid crystal drive power supply: V0 VSS = 4.0V to 13.0 V

GENERAL SPECIFICATIONS

ITEM	DESCRIPTION	UNIT
Outline Size	56.0(L)×39.0(W)×2.0(T)	mm
LCD Type	FSTN, Reflective, Positive, 1/65Duty, 1/9Bias	
Display type	128×64 dots	
View Area	50.0×25.0	mm
Display Area	46.05×23.01	mm
Dots size	0.33×0.0.33	mm
Dots pitch	0.36×0.36	mm
Controller & driver	ST7565R	
View Direction	12 O'Clock	
Interface mode	8bit-6800 & 8080, 4-SPI	
VDD&VOP(Type)	3.0 V & 9.0 V	V
Backlight(Type)	None	
Operation Temp.	-10~+60	$^{\circ}\!\mathbb{C}$
Storage Temp.	-20~+70	$^{\circ}\!$



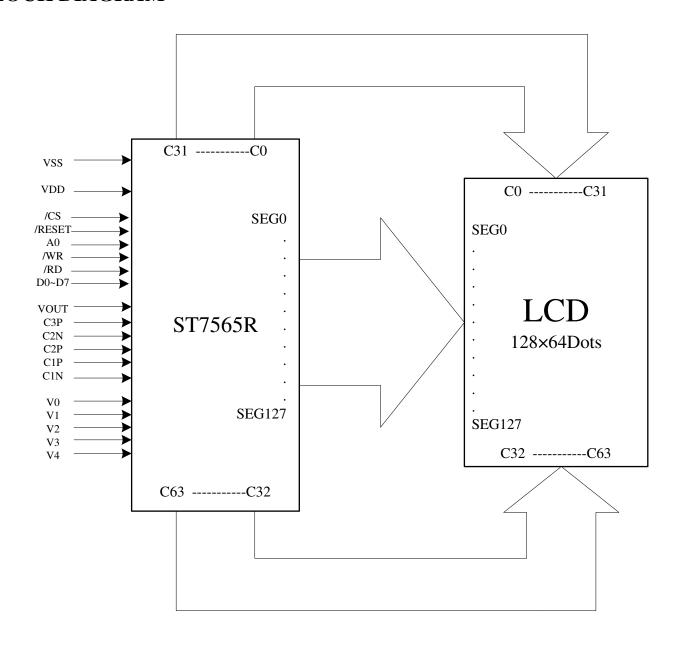


PIN CONNECTIONS

Pin No.	Pin Out	Description							
1	CS1B	Chip select input pin.							
2	RESB	Reset input pin; When /RES is set to "L".							
3	A0	0 = "H": Indicates that D0 to D7 are display data. 0 = "L": Indicates that D0 to D7 are control data.							
4	WR(R/W)	Read/Write execution control pin. When PSB is "H". RWR is not used in serial interface and should fix to "H" by VDD.							
5	RD(E)	Read/Write execution control pin. When PSB is "H". ERD is not used in serial interface and should fix to "H" by VDD.							
6	DB0	When using 8 hit parallel interfaces (6800 or 8080 mode)							
7	DB1	When using 8-bit parallel interface: (6800 or 8080 mode) 8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.							
8	DB2	When CS1B and CS2 are non-active (CS1B="H" & CS2="L"), D[7:0] pins are							
9	DB3	high impedance.							
10	DB4	When using serial interface: 4-LINE							
11	DB5	D7=SDA: Serial data input.							
12	DB6	D6=SCL: Serial clock input. D[5:0] are not used and should connect to "H" by VDD.							
13	DB7	D[3.0] are not used and should connect to H by VDD.							
14	VDD	Power supply for logic circuit.							
15	VSS	Ground.							
16	VOUT								
17	C1N								
18	C3P								
19	C1N	DC/DC voltage converter.							
20	C1P								
21	C2P								
22	C2N								
23	V4								
24	V3								
25	V2								
26	V1								
27	V0								
28	C86	C86 selects the microprocessor type in parallel interface mode. PSB C86 Selected Interface "H" "H" Parallel 6800 Series MPU Interface "H" "L" Parallel 8080 Series MPU Interface "L" - Serial 4-Line SPI Interface							
29	P/S	PSB selects the interface type: Serial or Parallel.							
30	VSS	Ground.							

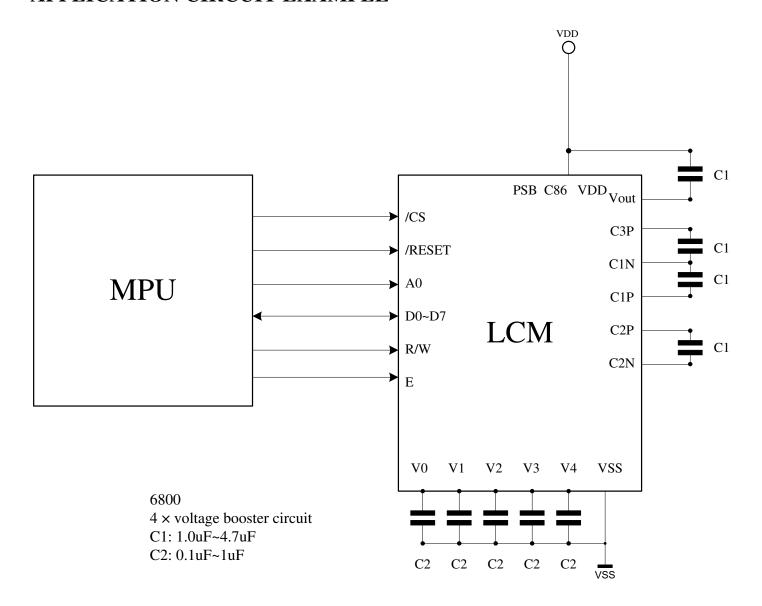


BLOCK DIAGRAM





APPLICATION CIRCUIT EXAMPLE





ABSOLUTE MAXIMUN RATING

ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT
POWER SUPPLY FOR LOGIC	VDD-VSS	-0.3	3.6	V
POWER SUPPLY FOR LCD DRIVE	V0-VSS	-0.3	16	V
INPUT VOLTAGE	VIN	-0.3	VDD+0.3	V
POWER SUPPLY FOR LED	VA-VK	-0.3		V

ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPER.	ATING	STO	RAGE	UNIT	COMMENT										
	MIN	MAX	MIN	MAX	UNII	COMMENT										
AMBIENT	-10	+60	-20	+70	$^{\circ}$											
TEMPERATURE	-10	+00	-20	+70												
HUMIDITY	1					WITHOUT										
HUMIDII I		/		/	1	CONDENSTION										
VIBRATION	1	,	,	,		SEE "ITEMS OF										
(M/S^2)	,	,	/	/	/	/	/	/	,	/	/	/	/	,	1	RELIABILITY"
TEMPERATURE	,	,	,	,		SEE "ITEMS OF										
CYCLING TEST	,	,	,	,		RELIABILITY"										
CORROSIVE GAS	NOT	·	NOT													
CORROSIVE GAS	ACCEP	TABLE	ACCEF	TABLE												

ELECTRICAL CHARACTERISTICS (Vss=0V)

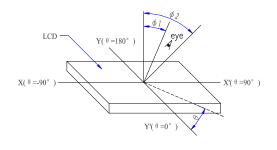
Item	Symbol	Condition	Min.	Тур	Max.	Unit	note
Power Supply for Logic	V_{DD} - V_{SS}		2.8	3.0	3.3	Volt	
Power Supply for Backlight	$V_{ m LED}$ + \sim $V_{ m LED}$ -	Ta=25℃				Volt	
T (\$7.14	V_{IL}	VIII 2VI-50	V_{SS}		0.3 V _{DD}	Volt	
Input Voltage	V_{IH}	Vdd=3V±5%	0.7 Vdd	-	V_{DD}	Volt	
Output	Vo _L	Vdd=3V±5%	V _{SS}	-	0.3 V _{DD}	Volt	
Voltage	Vo _H	v uu=3 v ±3%	0.7 Vdd	-	V_{DD}	Volt	
LCD		$T_a = 0^{\circ}C$					
driveVoltage(recommended	VSS -V0	$T_a=25$ °C	8.8	9.0	9.2	Volt	
Voltage)		$T_a = 50$ °C					
Power Supply	I_{DD}	$V_{DD} = 3.0 \text{V}$ $T_a = 25 ^{\circ}\text{C}$	-	150	300	uA	
Current for LCM	ILED	VLED=				mA	



ELECTRO-OPTICAL CHARACTERISTICS

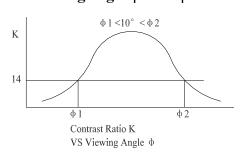
Item	Symbol	Condition	Min.	Тур	Max.	Unit	note
Viewing angle	Θ2-Θ1	T. 05°C	20	-	-	Dag	K=1.4
range	Φ	T _a =25℃	-	-	-	Deg	A,B
Disa Tima	Dica Tima T	T _a =25 °C	-	200	300		
Rise Time	$T_{\rm r}$	$T_a=0$ °C	-	-	-		Ф=10
Eall Times	J	$T_a=25$ $^{\circ}C$	-	214	300	ms	Θ=0 C
Fall Time T	$\mathrm{T_{f}}$	$T_a=0$ °C	-	-	-		
							Ф=10
Contrast	Cr	$T_a=25$ °C	-	8	-	-	$\Theta = 0$
							D

Definition of angle θ and ϕ



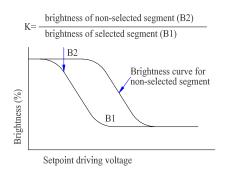
POSITIVE TYPE

Definition of viewing angle φ1 andφ2



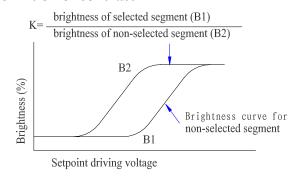
POSITIVE TYPE

Definition of contrast "K"

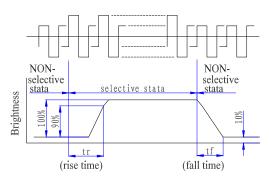


NEGATIVE TYPE

Definition of contrast "K"

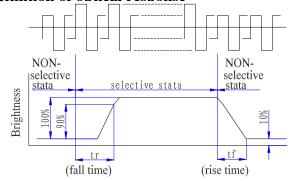


Definition of optical response



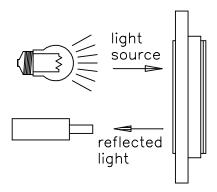
NEGATIVE TYPE

Definition of optical response

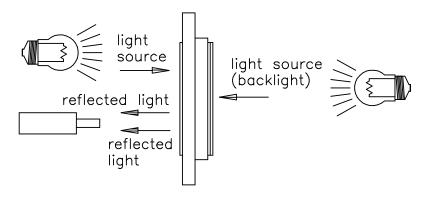




DESCRIPTION OF MEASURING EQUIPMENT



Reflective type



Transflective type



CONTROLLER ELECTRICAL CHARACTERISTICS

DC Characteristics

VSS=0V; Tamb = -30°C to +85°C; unless otherwise specified.

Itam	Cumahal	_	andition.		Rating		Unit	Applicable
Item	Symbol	C	ondition	Min.	Тур.	Max.	Unit	Pin
Operating Voltage (1)	VDD1			1.7	_	3.3	٧	VDD1
Operating Voltage (2)	VDD2			2.4	_	3.3	٧	VDD2
Operating Voltage (3)	VDD3			2.4	_	3.3	٧	VDD3
Input High-level Voltage	V _{IHC}			0.7 x VDD1	_	VDD1	٧	MPU
								Interface MPU
Input Low-level Voltage	V _{ILC}			VSS1	_	0.3 x VDD1	٧	Interface
Output High-level Voltage	Vohc	I _{OUT} =1mA, VDD1=1.8V		0.8 x VDD1	_	VDD1	٧	D[7:0]
Output Low-level Voltage	Volc	l _{oυτ} =-1m	I _{OUT} =-1mA, VDD1=1.8V		_	0.2 x VDD1	٧	D[7:0]
Input Lookago Current	1.			-1.0		1.0		MPU
Input Leakage Current	lu			-1.0	_	1.0	μΑ	Interface
Output Leakage Current	I _{LO}			-3.0	_	3.0	μΑ	MPU
Odiput Leakage Current	'LO			5.0		5.0	μΛ	Interface
Liquid Caretal Driver ON			Vop=8.5V,	_	0.6	0.8	ΚΩ	COMx
Liquid Crystal Driver ON Resistance	Ron	Ta=25°C	∆V=0.85V					
Resistance			VG=1.9V, ∆V=0.19V	_	1.3	1.5	ΚΩ	SEGx
		Dub-4						
Frame Frequency	FR		/65, Vop=8.5V a = 25℃	70	75	80	Hz	

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol Condition			Rating		Unit	Note
rest rattern	Symbol	Condition	Min.	Тур.	Max.	Unit	Note
		VDD1=VDD2=VDD3=3.0V,					
Display Pattern: SNOW	ISS	Booster X5	150	150	200	00 μΑ	
(Static)	155	V _{OP} = 8.5 V, Bias=1/9		130 300	300		
		Ta=25°C					
		VDD1=VDD2=VDD3=3.0V,					
Display OFF	ISS	Booster X5		95	190	uA	
Display OFF	133	V _{OP} = 8.5 V, Bias=1/9	_	30	190	uA	
		Ta=25°C					
Power Down	199	VDD1=VDD2=VDD3=3.0V,		8	16	шА	
Power Down	ISS	Ta=25°C	_	0	16	μA	

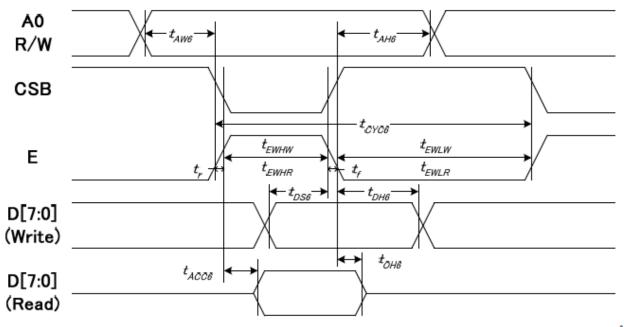
Note:

The Current Consumption is DC characteristics



TIMING CHARACTERISTICS

System Bus Timing for 6800 Series MPU



(VDD1 = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	_	
Address hold time	70	tAH6		10	_	
System cycle time		tCYC6		240	_	
Enable L pulse width (WRITE)		tEWLW		80	_	
Enable H pulse width (WRITE)	E	tEWHW		80	_]
Enable L pulse width (READ)		tEWLR		80	_	ns
Enable H pulse width (READ)		tEWHR		140		
Write data setup time		tDS6		40	_]
Write data hold time	DIZ:01	tDH6		10	_	
Read data access time	D[7:0]	tACC6	CL = 16 pF	_	70	
Read data output disable time		tOH6	CL = 16 pF	5	50	

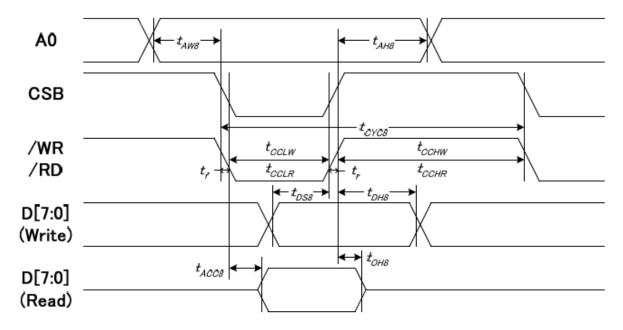
^{*1} The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr+tf) \le (tCYC6-tEWLW-tEWHW)$ for $(tr+tf) \le (tCYC6-tEWLR-tEWHR)$ are specified.

^{*2} All timing is specified using 20% and 80% of VDD1 as the reference.

^{*3} tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.



System Bus Timing for 8080 Series MPU



(VDD1 = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	40	tAW8		0	_	
Address hold time	A0	tAH8		10	_	1
System cycle time		tCYC8		240	_	
/WR L pulse width (WRITE)	WR	tCCLW		80	_	
/WR H pulse width (WRITE)	7	tCCHW		80	_	
/RD L pulse width (READ)	RD	tCCLR		140	_	ns
/RD H pulse width (READ)	_ KD	tCCHR		80		
WRITE Data setup time		tDS8		40	_	
WRITE Data hold time	DIZ:01	tDH8		20	_	
READ access time	D[7:0]	tACC8	CL = 16 pF	_	70	
READ Output disable time	7	tOH8	CL = 16 pF	5	50	

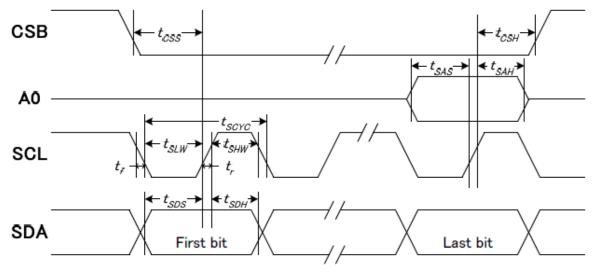
^{*1} The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr + tf) \le (tCYC8 - tCCLW - tCCHW)$ for $(tr + tf) \le (tCYC8 - tCCLR - tCCHR)$ are specified.

^{*2} All timing is specified using 20% and 80% of VDD1 as the reference.

^{*3} tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.



System Bus Timing for 4-Line Serial Interface

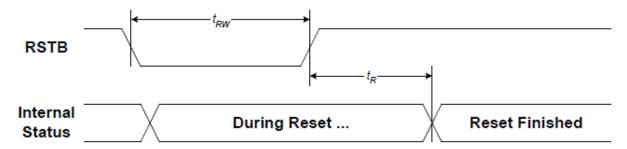


(VDD1 = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period		tSCYC		50	_	
SCLK "H" pulse width	SCLK	tSHW		25	_	
SCLK "L" pulse width]	tSLW		25	_	
Address setup time	40	tSAS		20	_	
Address hold time	A0	tsah		10	_	ns
Data setup time	SDA	tSDS		20	_	
Data hold time	SDA	tSDH		10	_	
CSB-SCLK time	CSB	tCSS		20	_	
CSB-SCLK time	CSD	tCSH		40	_	

^{*1} The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

Hardware Reset Timing



(VDD1 = 3.3V, Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		_	1.0	He
Reset "L" pulse width	tRW		1.0	1	us

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^{*2} All timing is specified using 20% and 80% of VDD1 as the standard.



DISPLAY COMMANDS

The display commands shown below control the internal state of the LCD driver ICs. Commands are sent from CPU to LCD module for the display control.(please to visit the web: http://www.sitronix.com.tw)

PU to LCD module for	r the	e disi	oiav c						V1S1t	the	web	: http://www.sitronix.com.tw/
Command	Α0	/RD	/WR		nma				D3 D2 D1 D0			Function
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	D	ispla	ay sta	art a	ddre		Sets the display RAM display star line address
(3) Page address set	0	1	0	1	0	1	1	Pa	ige a	ddre	ess	Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0	0	0	1	colu Lea	umn ast s	add ignif	cant ress icant ress	Sets the most significant 4 bits of the display RAM column address Sets the least significant 4 bits of the display RAM column address
(5) Status read	0	0	1		St	atus	;	0	0	0	0	Reads the status data
(6) Display data write	1	1	0			,	Writ	e da	ta			Writes to the display RAM
(7) Display data read	1	0	1				Read data					Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1		erat	ting	Select internal power supply operating mode
(17) Vo voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0		siste itio	or	Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1	0	0 Ele	0 ectro	0 nic v	0 olur	0 ne v	1 alue	Set the Vo output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator	0	1	0	1	0	1	0	1	1		0 1 Mode	0: OFF, 1: ON Set the flashing mode
register set				1	1	1	1	1	0	0	0	select booster ratio
(20) Booster ratio set	0	1	0	0	0	0	0	0	0		p-up lue	00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command



QUALITY LEVEL

Inspection conditions

Environmental conditions

The environmental conditions for inspection shall be as follows: Room temperature: $22\pm3^{\circ}$ C; Humidity: $50\pm10\%$ RH.

The external visual inspection

The inspection shall be performed by using a single 20W fluorescent lamp for illumination and the distance from LCD to eyes of the inspector should be 30cm or more.

Classification of defects

A major defect

A major defect refers to A defect which may substantially degrade usability for product applications.

Minor defect

A Minor defect refers to A defect which is not considered to substantially degrade product application or A defect which deviates from existing standards almost unrelated to the effective use of the product or its operation

Sampling procedures for each items acceptance level table

Defect type	Sampling procedures	AQL
Major defect	MIL-STD-105D Inspection level1	1.0
	normal inspection Single sample inspection	1.0
Minor defect	MIL-STD-105D Inspection level1	2.5
	normal inspection Single sample inspection	2.5

Life time

50,000Hrs(25° C in the room without ray of sun)

Items of reliability

ITEM	CONDITIONS	CRITERION	
High temperature operation test	+60°C \ 120 hours	1. It judged at room	
		temperature after 1 hours to be	
		good as appearance and	
		electrical test is normal after	
		the experiment.	
		2. Current consumption should	
		within the specification of Approval	
_		sheet Electro-optical characteristics	
Low temperature operation test	-10℃ \ 120 hours		
High temperature/humidity storage	+70℃,80%±10%RH \ 120		
test	hours		
High temperature storage test	+70°C \ 120 hours		
Low temperature storage test	-20°C \ 120 hours		
Temperature cycling test	-10°C (30 min)	5-10pcs	
	↓ ↑		
	25℃ (5 min)		
	↓ ↑		
	60°C (30 min)		
	, ,		
	CYCLES: 10		



Vibration	Random Wave: 10 ~ 50 Hz	
	Each Direction (x, y, z): 30	
	Min.	

Cosmetic criteria of LCD screen

DEFECT	JUDGEMENT CRITERION						
	Size d (mm)	Acceptable quantity in active area				
Spots	d≤0.	1	Disregard				
	0.1 <d<< td=""><td></td><td colspan="3">6</td></d<<>		6				
	0.2 <d≤< td=""><td></td><td colspan="3">2</td></d≤<>		2				
	d>0.		0				
	Note: $d = (Length + Width)/2$						
	Size d (mm)	Acceptable quantity in active area				
	d≤0.	3	Disregard				
Polarizer Bubbles	0.3 <d<< td=""><td>1.0</td><td colspan="3">3</td></d<<>	1.0	3				
1 Oldrizer Buooles	1.0≤d≤	1.5	1				
	d>1.	5	0				
	Note: $d = (Length + Length +$	- Width)/2					
	Width W	(mm)	A contable quantity in active area				
Lines	Length I	(mm)	Acceptable quantity in active area				
	$W \le 0$.02	Disregard				
	0.02 < W<0.05	L ≤ 5.0	6				
	0.02≤ W≤0.05	L > 5.0	0				
	0.05/W/0.1	L ≤ 2.0	6				
	0.05 <w≤0.1< td=""><td>L > 2.0</td><td>0</td></w≤0.1<>	L > 2.0	0				
	W > ().1	See criteria for spots				
Testing conditions: 20W	fluorescent lamp at	t 30 cm distar	ice at normal viewing angle				