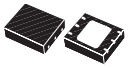
Automotive-grade, 1 A, low quiescent current, low-noise regulator with soft-start



DFN6 (3x3)
Wettable Flanks

Maturity status link
LD49100

Features

- AEC-Q100 qualified
- Temperature range: -40 °C to 125 °C
- Input voltage from 1.5 to 5.5 V
- Ultra low-dropout voltage (200 mV typ. at 1 A load)
- Very low quiescent current (20 µA typ. at no load, 200 µA typ. at 1 A load, 1 µA max. in off mode)
- Very low-noise with no bypass capacitor (30 μV_{RMS} at V_{OUT} = 0.8 V)
- Output voltage tolerance: ± 2.0% at 25 °C
- 1 A guaranteed output current
- Wide range of output voltages available on request: 0.8 V to 4.5 V with 100 mV step and adjustable from 0.8 V
- Logic-controlled electronic shutdown
- Power Good function
- Stable with ceramic capacitors C_{OUT} = 1 µF
- Internal current and thermal limit
- DFN6 (3x3 mm) package with wettable flanks

Applications

- Infotainment and cluster
- ADAS
- Telematics
- Body electronics

Description

The LD49100 provides 1 A maximum current with an input voltage range from 1.5 V to 5.5 V and a typical dropout voltage of 200 mV. The device is stable with ceramic capacitors on the input and output.

The ultra low-dropout voltage, low quiescent current and low-noise features make it suitable for a wide range of automotive applications. Power supply rejection is 70 dB at low frequency and starts to roll off at 10 kHz. Enable logic control function puts the LD49100 in shutdown mode, allowing a total current consumption lower than 1 µA.

The device features a precise Power Good indicator, useful to monitor and sequence functions. Internal 1 ms soft-start circuit allows the reduction of inrush current.

The device includes the short-circuit constant current limiting and thermal protection. The LD49100 is available in AEC-Q100 grade 1 qualified version, in a small 6-pin DFN6 (3x3 mm) with wettable flank package.

1 Circuit schematics

Figure 1. **LD49100 schematic diagram (adjustable version)**

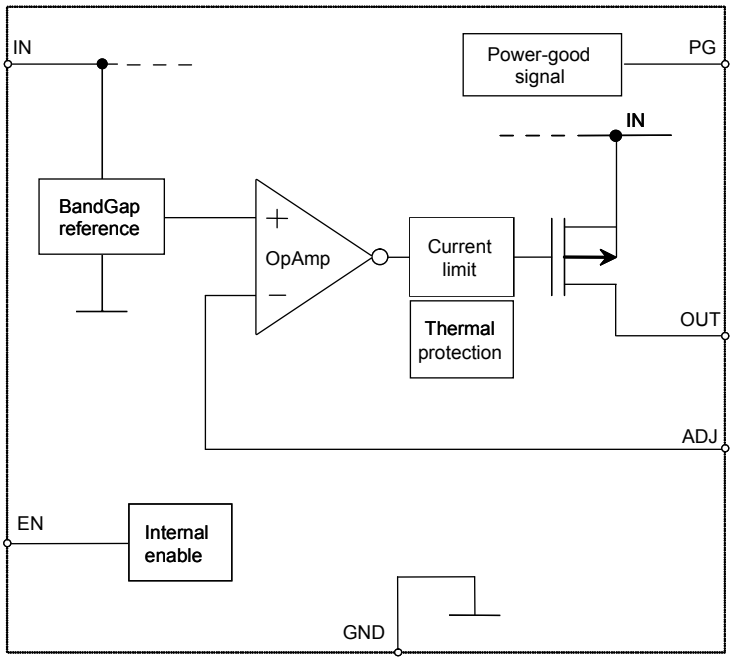
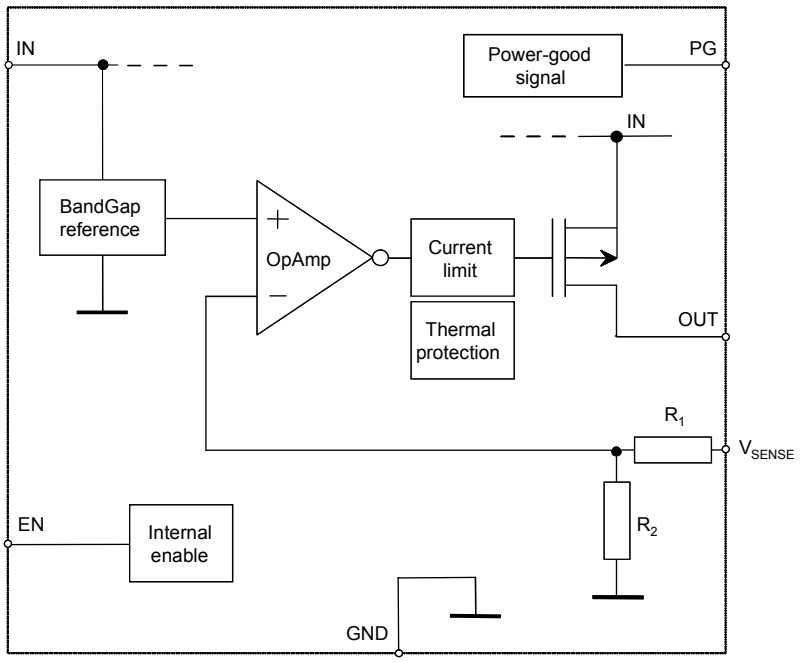
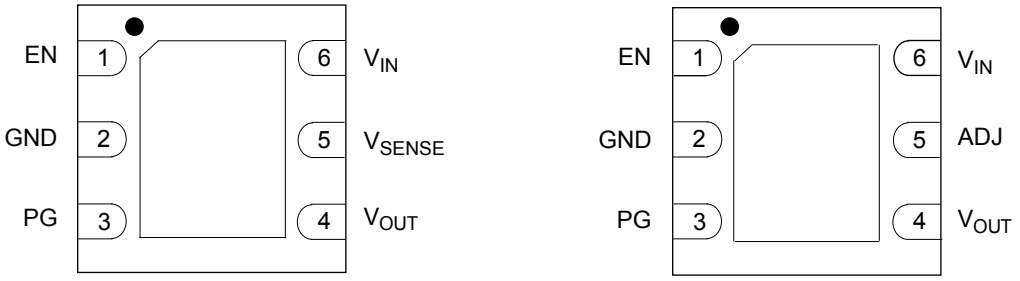


Figure 2. **LD49100 schematic diagram (fixed version)**



2 Pin configuration

Figure 3. **Pin connection (top view)**



LD49100 (fixed version)

LD49100 (adjustable version)

Table 1. **Pin description**

Symbol	Pin		Function
	LD49100 (adjustable version)	LD49100 (fixed version)	
EN	1	1	Enable input: set VEN = high to turn on the device VEN = low to turn off the device Don't leave this pin floating
GND	2	2	Common ground
PG	3	3	Power Good
V_{OUT}	4	4	Output voltage
ADJ/V_{SENSE}	5	5	ADJ: adjust pin on the adjustable version. Connect to resistor divider to set the output voltage. V_{SENSE}: output voltage sensing pin on fixed versions. Connect to V_{OUT}. Allows remote sensing
V_{IN}	6	6	LDO input voltage
GND	Exposed pad		Exposed pad has to be connected to GND

3 Absolute maximum ratings

Stressing the device above the rating listed in Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	-0.3 to 7	V
V_{OUT} /V_{SENSE}	DC output voltage, output voltage sense pin	-0.3 to V_{IN} + 0.3 (7 V max.)	V
EN	Enable pin	-0.3 to 7	V
PG	Power Good pin	-0.3 to 7	V
ADJ	Adjust pin	4	V
I_{OUT}	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C
T_{J-MAX}	Maximum junction temperature range	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W
R_{thJC}	Thermal resistance junction-case	10	°C/W

Note: R_{thJA} for DFN6 based on a 4-layer JEDEC PCB (2S2P) test board with 2 thermal vias.

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V
		CDM corner pins	750	

4 Electrical characteristics

Table 5. LD49100 electrical characteristics (adjustable version) T_J = 25 °C, V_{IN} = 1.8 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 100 mA, V_{EN} = V_{IN}, unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{ADJ}	V_{ADJ} accuracy	I_{OUT} = 10 mA, T_J = 25 °C	784	800	816	mV
		I_{OUT} = 10 mA -40 °C < T_J < 125 °C	776	800	824	
I_{ADJ}	Adjust pin current				1	µA
ΔV_{OUT}	Static line regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 100 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (1)	ΔV_{IN} = 500 mV I_{OUT} = 100 mA, t_R = 5 µs		10		mVpp
		ΔV_{IN} = 500 mV I_{OUT} = 100 mA, t_F = 5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 1 A		0.001		%/mA
ΔV_{OUT}	Transient load regulation (1)	I_{OUT} = 10 mA to 1 A t_R = 5 µs		40		mVpp
		I_{OUT} = 1 A to 10 mA, t_F = 5 µs		40		
V_{DROP}	Dropout voltage (2)	I_{OUT} = 1 A V_O fixed to 1.5 V -40 °C < T_J < 125 °C		200	400	mV
e_N	Output noise voltage	10 Hz to 100 kHz I_{OUT} = 100 mA V_{OUT} = 0.8 V		30		μV_{RMS}
SVR	Supply voltage rejection V_O = 0.8 V	V_{IN} = 1.8 V+/-V_{RIPPLE} V_{RIPPLE} = 0.25 V frequency = 1 kHz, I_{OUT} = 10 mA		70		dB
		V_{IN} = 1.8 V+/-V_{RIPPLE} V_{RIPPLE} = 0.25 V V_{RIPPLE} = 0.25 V frequency = 10 kHz, I_{OUT} = 100 mA		65		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA -40 °C < T_J < 125 °C			50	
		I_{OUT} = 0 to 1 A		200		
		I_{OUT} = 0 to 1 A -40 °C < T_J < 125 °C			300	
		V_{IN} input current in off mode: V_{EN} = GND (3)		0.001	1	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PG_ON} (4)	Power Good output threshold, rising	-40 °C < T_J < 125 °C	93		99	%V_{OUT}
V_{PG_OFF} (4)	Power Good output threshold, falling	-40 °C < T_J < 125 °C	91 (5)		95	
V_{PG_MIN}	Minimum Power Good threshold	-40 °C < T_J < 125 °C	91			%V_{OUT_NOM}
V_{PG_L}	Power Good output voltage low	I_{sink} = 6 mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L= 0		2.5		A
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V			0.4	V
	Enable input logic high	-40 °C < T_J< 125 °C	0.9			V
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
t_{SS}	Soft-start time (1)	From enable to 95% of $V_{OUT(NOM)}$	0.5	1	1.5	ms
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 5)	1			µF

1. *Guaranteed by design, not tested in production.*
2. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.5 V.*
3. *PG pin floating.*
4. *Power good is measured as a percentage of the real output voltage value - which includes temperature and process variation - not the nominal one.*
5. *91% or V_{PG_MIN} wichever is higher.*

Table 6. LD49100 electrical characteristics (fixed version) T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 100 mA, V_{EN} = V_{IN}, unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	I_{OUT} = 10 mA, T_J = 25 °C	-2.0		2.0	%
		I_{OUT} = 10 mA -40 °C < T_J < 125 °C	-3.0		3.0	
I_{SENSE}	I_{SENSE} sense pin current			2		µA
ΔV_{OUT}	Static line regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 100 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (1)	ΔV_{IN} = 500 mV I_{OUT} = 100 mA, t_R = 5 µs		10		mVpp
		ΔV_{IN} = 500 mV I_{OUT} = 100 mA, t_F = 5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 1 A		0.001		%/mA
ΔV_{OUT}	Transient load regulation (1)	I_{OUT} = 10 mA to 1 A, t_R = 5 µs		40		mVpp
		I_{OUT} = 1 A to 10 mA, t_F = 5 µs		40		
V_{DROP}	Dropout voltage (2)	I_{OUT} = 1 A, V_{OUT} > 1.5 V -40 °C < T_J < 125 °C		200	400	mV
e_N	Output noise voltage	10 Hz to 100 kHz I_{OUT} = 100 mA, V_{OUT} = 2.5 V		85		μV_{RMS}
SVR	Supply voltage rejection V_{OUT} = 1.5 V	V_{IN} = $V_{OUT(NOM)}$+0.5 V+/-V_{RIPPLE} V_{RIPPLE} = 0.1 V frequency = 1 kHz, I_{OUT} = 10 mA		65		dB
		V_{IN} = $V_{OUT(NOM)}$+0.5 V+/-V_{RIPPLE} V_{RIPPLE} = 0.1 V frequency = 10 kHz, I_{OUT} = 100 mA		62		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA, -40 °C < T_J < 125 °C			50	
		I_{OUT} = 0 to 1 A		200		
		I_{OUT} = 0 to 1 A -40 °C < T_J < 125 °C			300	
		V_{IN} input current in OFF mode: V_{EN} = GND(3)		0.001	1	
V_{PG_ON} (4)	Power Good output threshold, rising	-40 °C < T_J < 125 °C	93		99	%V_{OUT}
V_{PG_OFF} (4)	Power Good output threshold, falling	-40 °C < T_J < 125 °C	91 (5)		95	
V_{PG_MIN}	Minimum Power Good threshold	-40 °C < T_J < 125 °C	91			%V_{OUT_NOM}
V_{PG_L}	Power Good output voltage low	I_{sink} = 6 mA open drain output			0.4	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SC}	Short-circuit current	R_L = 0		2.5		A
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V			0.4	V
	Enable input logic high	-40 °C < T_J < 125 °C	0.9			V
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
t_{SS}	Soft-start time (1)	From enable to 95% of $V_{OUT(NOM)}$	0.5	1	1.5	ms
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 5)	1			µF

1. *Guaranteed by design, not tested in production.*
2. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.5 V.*
3. *PG pin floating.*
4. *Power good is measured as a percentage of the real output voltage value - which includes temperature and process variation - not the nominal one.*
5. *91% or V_{PG_MIN} wichever is higher.*

5 Typical performance characteristics

$C_{IN} = C_{OUT} = 1\ \mu F$

Figure 4. V_{ADJ} accuracy

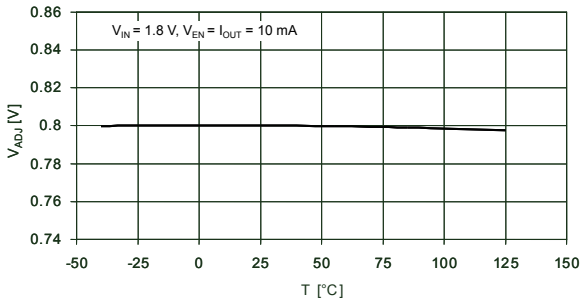


Figure 5. V_{OUT} accuracy

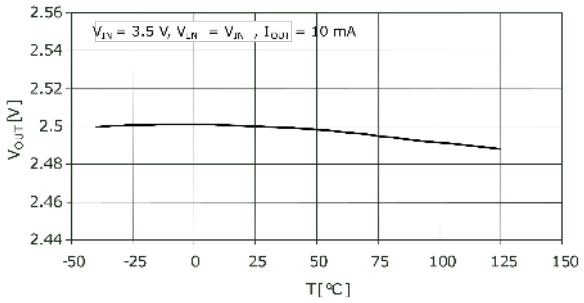


Figure 6. Dropout voltage vs. temperature (V_{OUT} = 2.5 V)

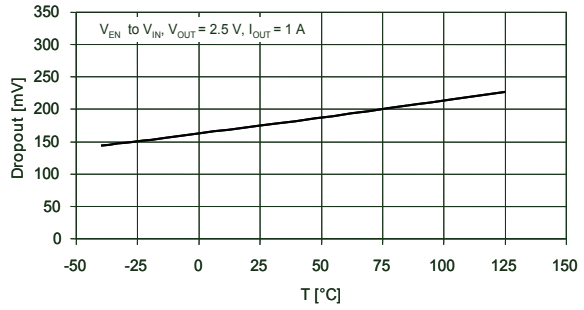


Figure 7. Dropout voltage vs. temperature (V_{OUT} = 1.5 V)

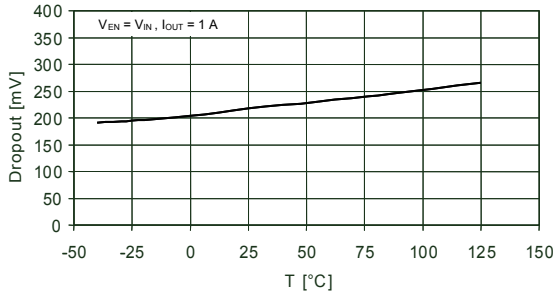


Figure 8. Dropout voltage vs. output current

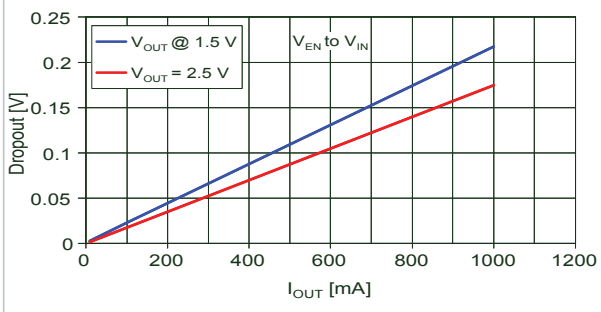


Figure 9. Short-circuit current vs. drop voltage

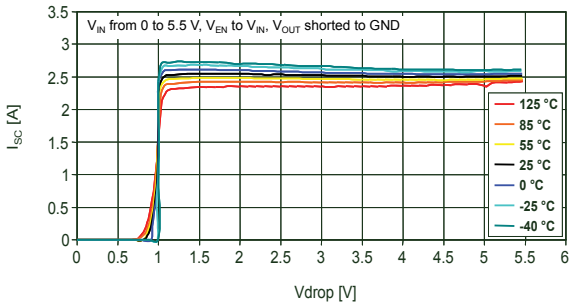


Figure 10. Output voltage vs. input voltage (V_{OUT} = 0.8 V)

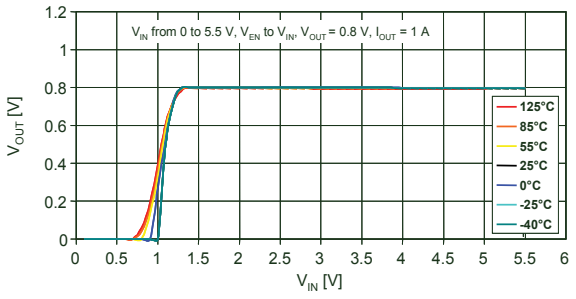


Figure 11. Output voltage vs. input voltage (V_{OUT} = 2.5 V)

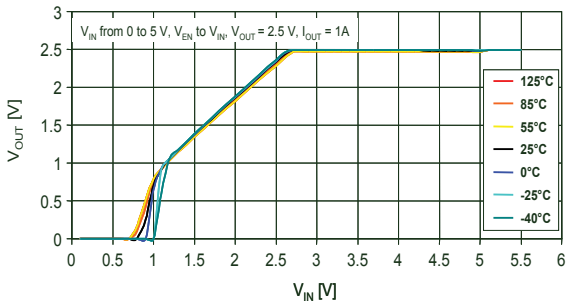


Figure 12. Quiescent current vs. temperature

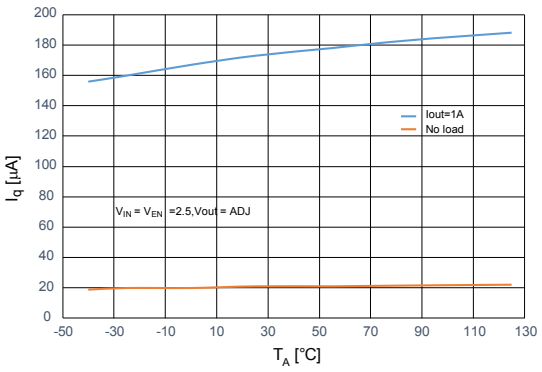


Figure 13. V_{IN} input current in off mode vs. temperature

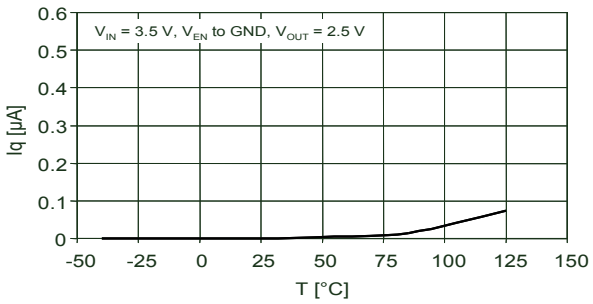


Figure 14. Load regulation

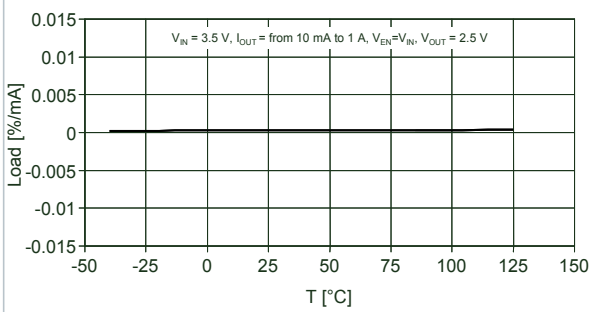


Figure 15. Line regulation V_{OUT} = 0.8 V

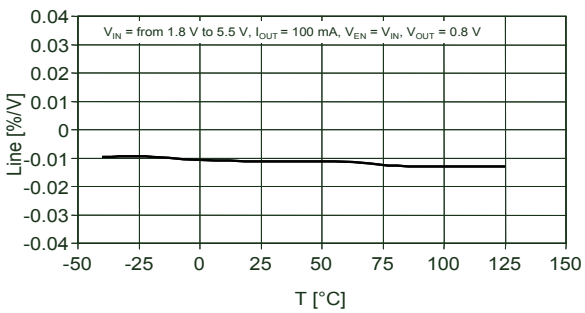


Figure 16. Line regulation V_{OUT} = 2.5 V

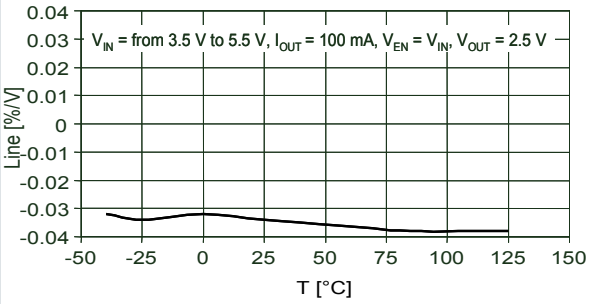


Figure 17. Supply voltage rejection vs. temperature (V_{OUT} = 0.8 V)

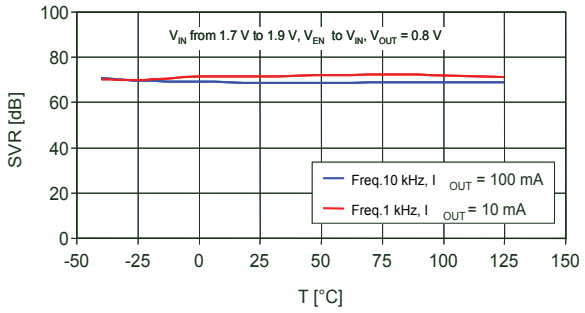


Figure 18. Supply voltage rejection vs. temperature (V_{OUT} = 2.5 V)

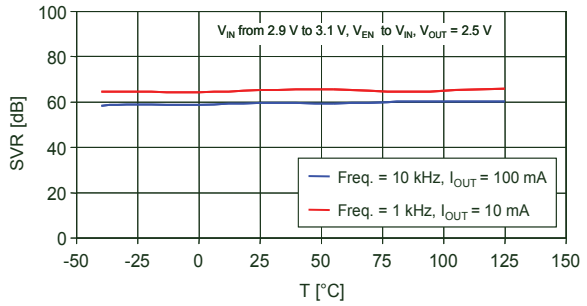


Figure 19. Supply voltage rejection vs. frequency (V_{OUT} = 0.8 V)

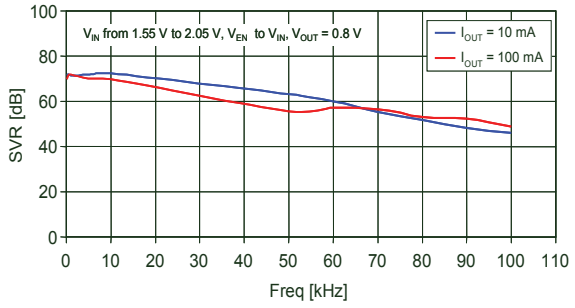


Figure 20. Supply voltage rejection vs. frequency (V_{OUT} = 2.5 V)

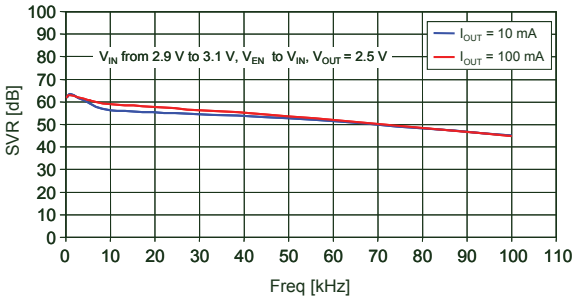
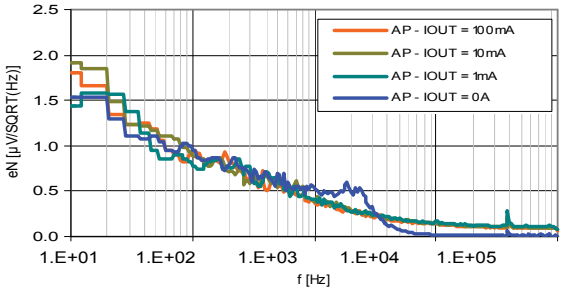


Figure 21. Output noise voltage vs. frequency



V_{IN} = 1.8 V, V_{OUT} = 0.8 V, V_{EN} = V_{IN}

Figure 22. Enable voltage vs. temperature

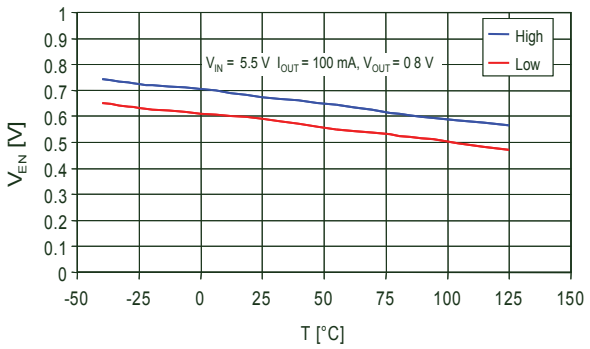
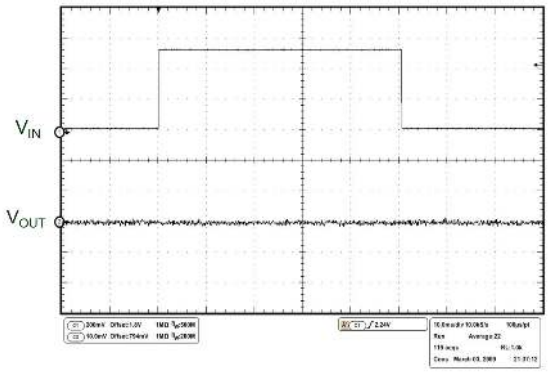
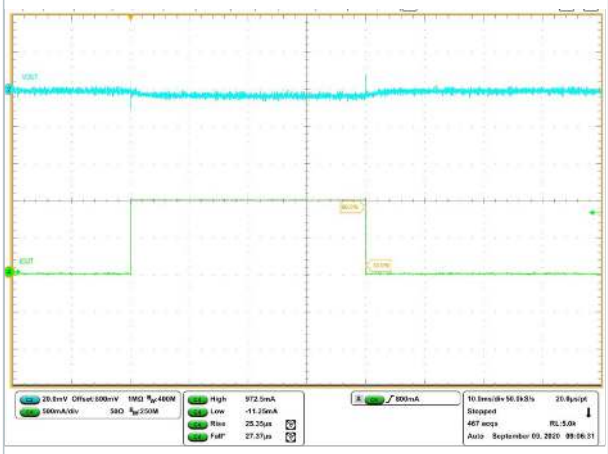


Figure 23. Line transient



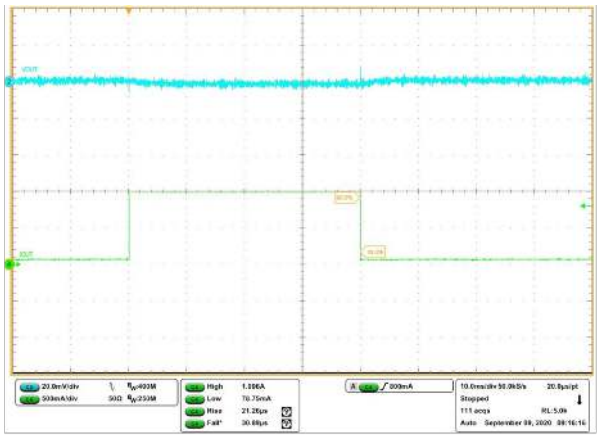
V_{IN} = 1.8 V to 2.3 V, V_{OUT} = 0.8 V, I_{OUT} = from 100 mA, $t_R = t_F$ = 5 µs

Figure 24. Load transient



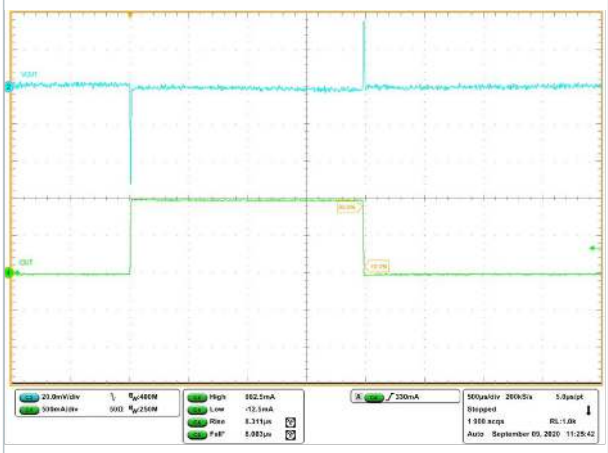
$V_{EN} = V_{IN}$ = 3.5 V, V_{OUT} = 0.8 V, I_{OUT} = from 10 mA to 1 A, $t_R = t_F$ = 5 µA

Figure 25. Load transient



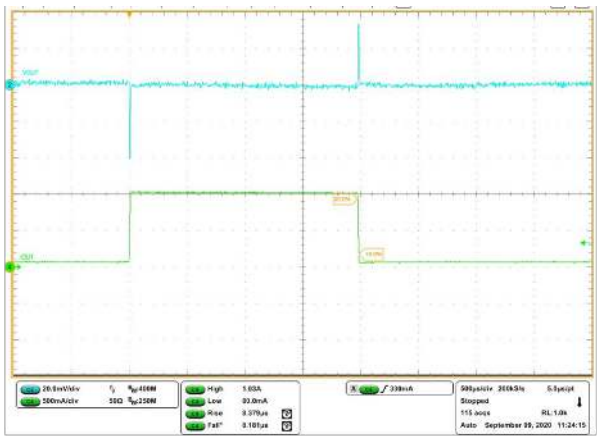
$V_{EN} = V_{IN}$ = 3.5 V, V_{OUT} = 0.8 V, I_{OUT} = from 100 mA to 1 A, $t_R = t_F$ = 5 µA

Figure 26. Load transient



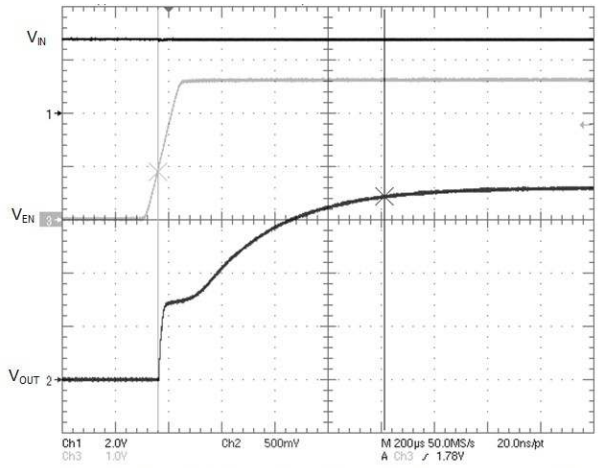
$V_{LN} = V_{IN}$ = 3.5 V, V_{OUT} = 2.5 V, I_{OUT} = from 10 mA to 1 A, $t_R = t_f$ = 5 µA

Figure 27. Load transient



$V_{EN} = V_{IN}$ = 3.5 V, V_{OUT} = 2.5 V, I_{OUT} = from 100 mA to 1 A, $t_R = t_F$ = 5 µA

Figure 28. Enable transient



V_{IN} = 2.8V, V_{OUT}=1.8V, V_{EN} from 0V to 2.8V, I_{OUT}=100mA, tr=tf=1us, C_{IN}=C_{OUT}=1µF

6 Application information

The LD49100 is an ultra low-dropout linear regulator. It provides up to 1 A with a low 200 mV dropout. The input voltage range is from 1.5 V to 5.5 V. The device is available both in fixed and adjustable output versions.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

Figure 29 and Figure 30 illustrate the typical application schematics:

Figure 29. Typical application circuit for fixed output version

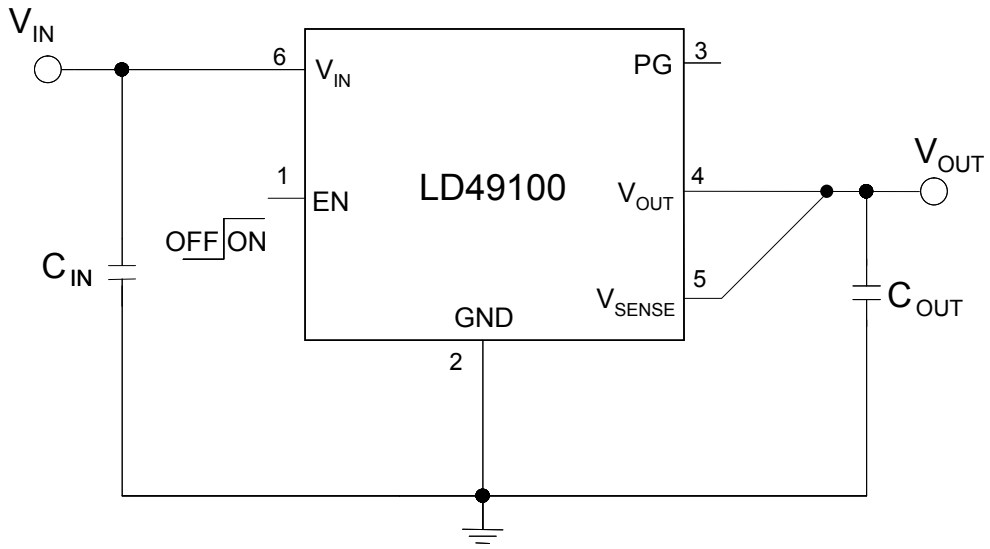
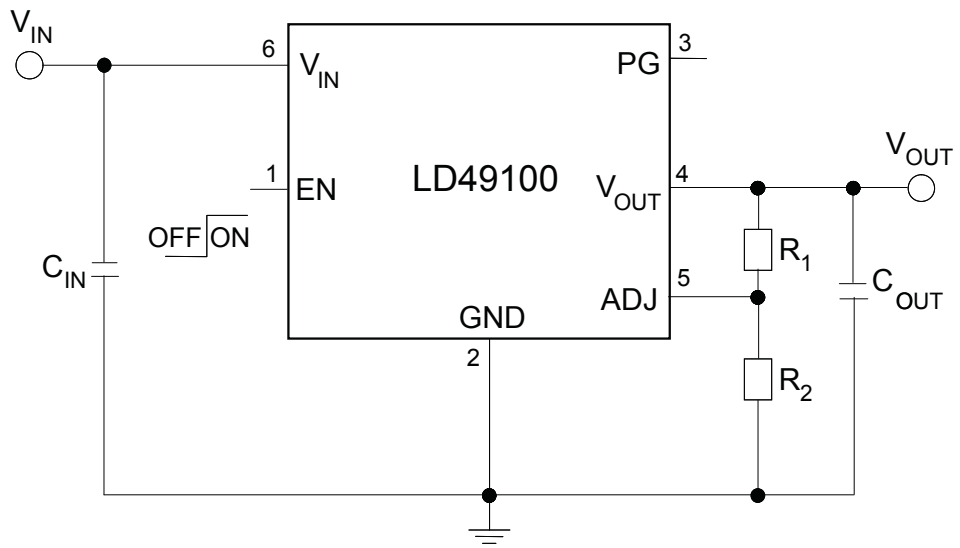


Figure 30. Typical application circuit for adjustable version



Regarding to the adjustable version, the output voltage can be fixed from 0.8 V up to the input voltage, minus the voltage drop across the pass element (dropout voltage), by connecting a resistor divider between ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider should be selected as follows:

$$V_{OUT} = V_{ADJ}\left(1 + R_1/R_2\right) \quad (1)$$

with

$$V_{ADJ} = 0.8V\left(typ.\right) \quad (2)$$

Resistors should be used with values in the range from 10 kΩ to 50 kΩ. Lower values can also be suitable, but they increase the current consumption.

6.1 External capacitors

The LD49100 voltage regulator requires external low ESR capacitors to assure control loop stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance defined in the following sections.

Input and output capacitors should be located as close as possible to the relevant pins.

6.1.1 Input capacitor

An input capacitor with a minimum value of 1 µF must be located as close as possible to the input pin of the device and returned to a clean analog ground. A good quality, low-ESR ceramic capacitor is suggested. It helps to ensure stability of the control loop, reduces the effects of inductive sources and improves ripple rejection.

A value above 1 µF may be chosen when the application involves fast load transients.

6.1.2 Output capacitor

The LD49100 requires a low-ESR capacitor connected on its output to keep the control loop stable and reduce the risk of ringing and oscillations. The control loop is designed to be stable with any good quality ceramic capacitor (such as X5R/X7R types) with a minimum value of 1 µF and equivalent series resistance in the 0 to 150 mΩ range.

It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region.

If the conditions above are met, there is no maximum limit to the output capacitance.

6.2 Output voltage sense pin

In the fixed output voltage version, on pin 5, a V_{SENSE} connection is available. This pin must not be left floating, since it is necessary for a correct sensing of the output voltage. It can be either connected to the load in a remote sensing configuration, or directly shorted to the V_{OUT} pin (pin 4, refer to Figure 29. Typical application circuit for fixed output version.

6.3 Power dissipation

An internal thermal feedback loop disables the output voltage if the die temperature rises to approximately 160 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without the risk of damaging the device.

A good PC layout should be used to maximize power dissipation. The thermal path for the heat generated by the device is from the die to the copper lead frame, through the package leads and exposed pad, to the PCB copper layer. The PCB copper layer works as a heatsink. The footprint copper pads should be as wide as possible to spread and dissipate the heat to the surrounding ambient. Feed-through vias to the inner or backside copper layers are also useful to improve the overall thermal performance of the device.

The device power dissipation depends on the input voltage, output voltage and output current, and is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} \quad (3)$$

Junction temperature of the device is:

$$T_{J\_MAX} = T_A + R_{thJA} \times P_D \quad (4)$$

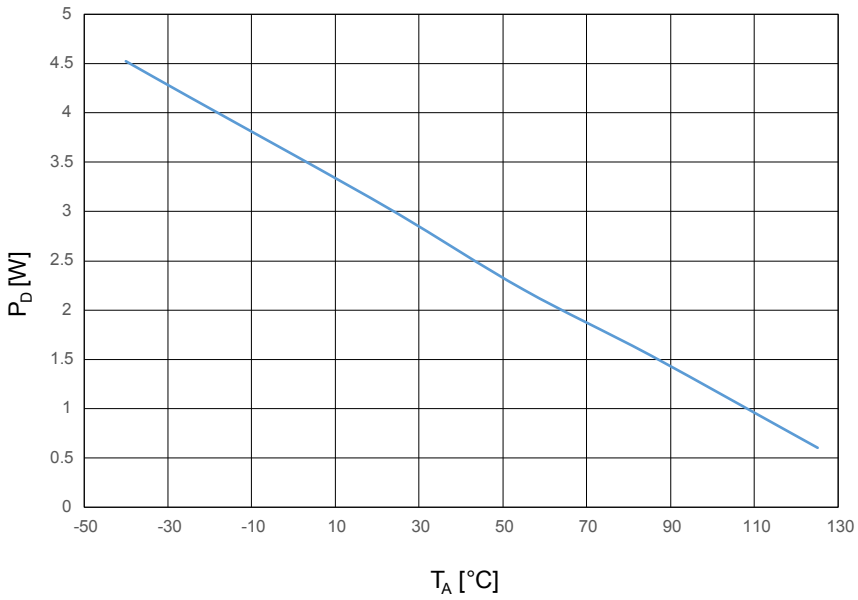
where:

T_{J_MAX} is the maximum junction of the die,125 °C

T_A is the ambient temperature

R_{thJA} is the thermal resistance junction-to-ambient

Figure 31. Power dissipation vs. ambient temperature



6.4 Enable function

The LD49100 features the enable function. When EN voltage is higher than 0.9 V, the device is ON, and if it is lower than 0.4 V, the device is OFF. In shutdown mode, consumption is lower than 1 µA.

An internal soft-startup circuit helps reducing the in-rush current at turn-on, by providing a typical output voltage rise-time of 1 ms.

EN pin has not an internal pull-up, so it cannot be left floating if it is not used.

6.5 Power Good function

Some applications require a flag showing that the output voltage is in the correct range.

Power Good threshold depends on the output voltage. When it is higher than $V_{PG\text{-}ON}$, Power Good (PG) pin goes to high impedance. If it is below $V_{PG\text{-}OFF}$ PG pin goes to low impedance. If the device works well, Power Good pin is at high impedance.

If the device is disabled (EN pin low) the PG signal is set to high impedance. This is done intentionally to avoid pull-down current by the PG pin in disabled mode.

Power Good function requires an external pull-up resistor, which has to be connected between PG pin and V_{IN} or V_{OUT}. PG pin typical current capability is up to 6 mA. A pull-up resistor for PG should be in the range from 100 kΩ to 1 MΩ. If Power Good function is not used, PG pin has to remain floating.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN6 (3x3 mm) automotive-grade package information

Figure 32. **DFN6 (3x3 mm) automotive-grade package outline**

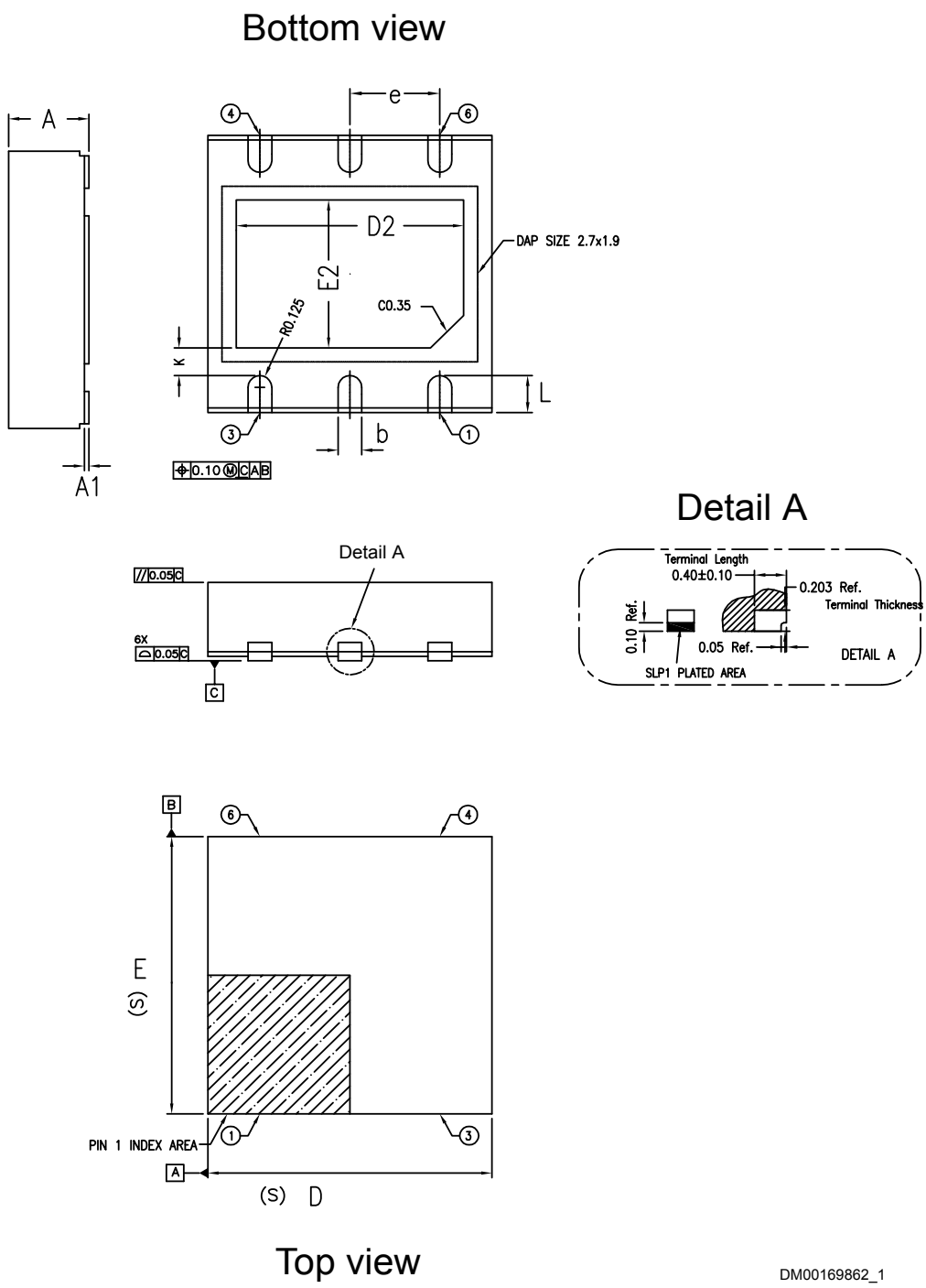
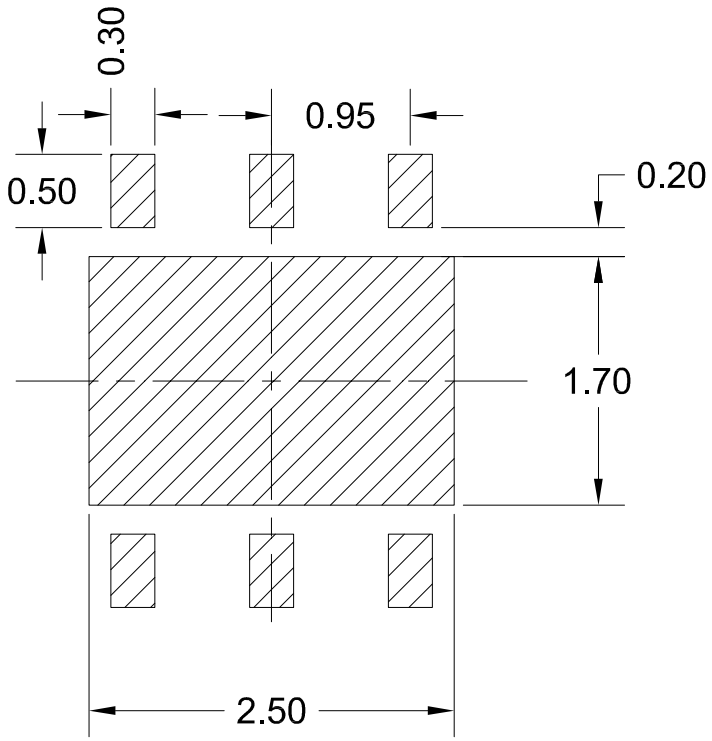


Table 7. **DFN6 (3x3 mm) automotive-grade mechanical data**

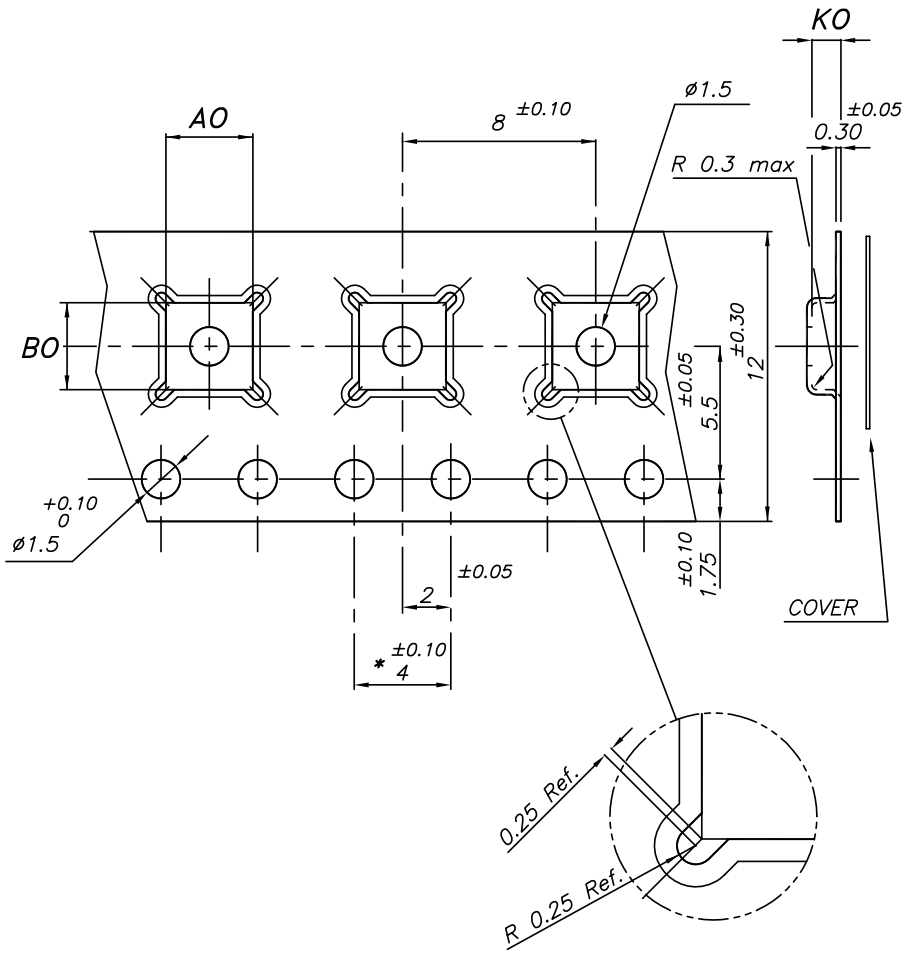
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.0		0.05
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
e		0.95	
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
L	0.30	0.40	0.50

Figure 33. **DFN6 (3x3 mm) automotive-grade recommended footprint**



7.2 DFN6 (3x3 mm) packing information

Figure 34. **DFN6 (3x3) tape outline**



– * 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20

7875978_N

Figure 35. **DFN6 (3x3 mm) tape oriented**

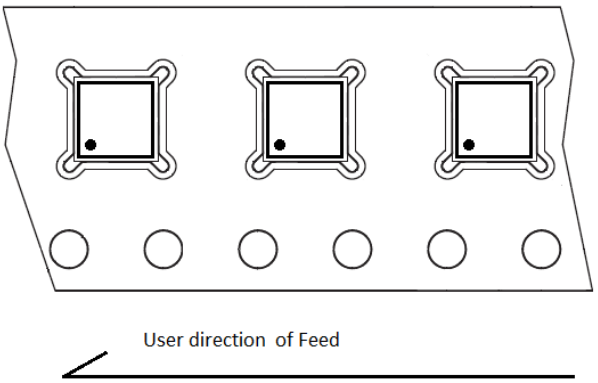


Figure 36. **DFN6 (3x3 mm) reel outline**

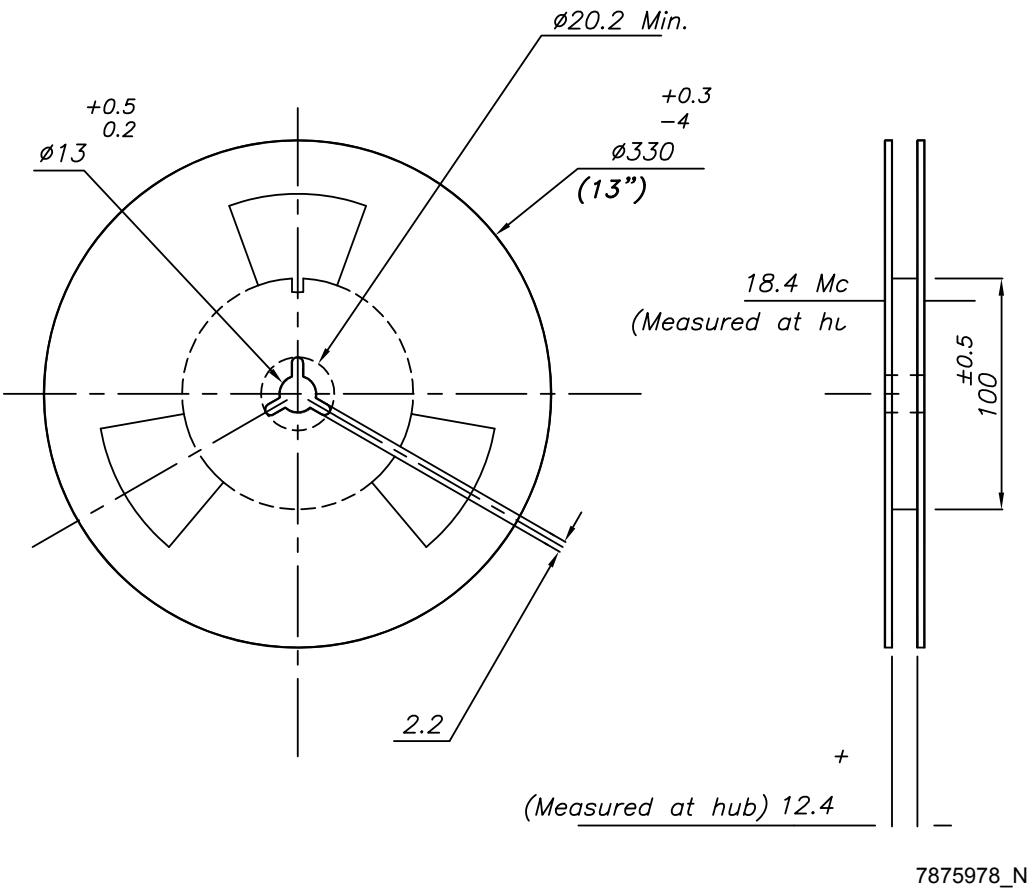


Table 8. **DFN6 (3x3) tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

8 Ordering information

Table 9. **Order code**

Order codes	Output voltages
LD49100PURY	Adjustable
LD49100PU10RY	1.0 V
LD49100PU12RY	1.2 V
LD49100PU15RY	1.5 V
LD49100PU18RY	1.8 V
LD49100PU25RY	2.5 V
LD49100PU30RY	3.0 V
LD49100PU33RY	3.3 V

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
26-Aug-2020	1	Initial release.
01-Sep-2020	2	Change maturity status.
11-Sep-2020	3	Load transient characteristics update in Section 5 Typical performance characteristics.
18-Feb-2021	4	Added new order codes LD49100PU10RY and LD49100PU15RY in Table 9. Order code.

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