

TPSM84x24 Power Module Evaluation Module User's Guide



ABSTRACT

The TPSM84824, TPSM84624, and TPSM84424 evaluation module (EVM) is designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the TPSM84x24 power module. This guide provides information on the correct usage of the EVM and an explanation of the numerous test points on the board.

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1 Description

This EVM features the TPSM84824/624/424 synchronous buck power module configured for operation with a 4.5-V to 17-V input voltage range. The output voltage can be set to one of six popular values by using a configuration jumper. Similarly, the switching frequency can be set to one of six values with a jumper. Additionally, the RTT resistor value, which selects the TurboTrans feature for improved transient response, is also selectable using a jumper. The full output current rating of the device can be supplied by the EVM. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Control test points and component footprints are provided for use of the ENABLE, PGOOD, and CLK features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The *VIN* Power terminal block (J1) is used for connection to the host input supply and the *VOUT* Power terminal block (J2) is used for connection to the load. These terminal blocks can accept up to 16-AWG wire.

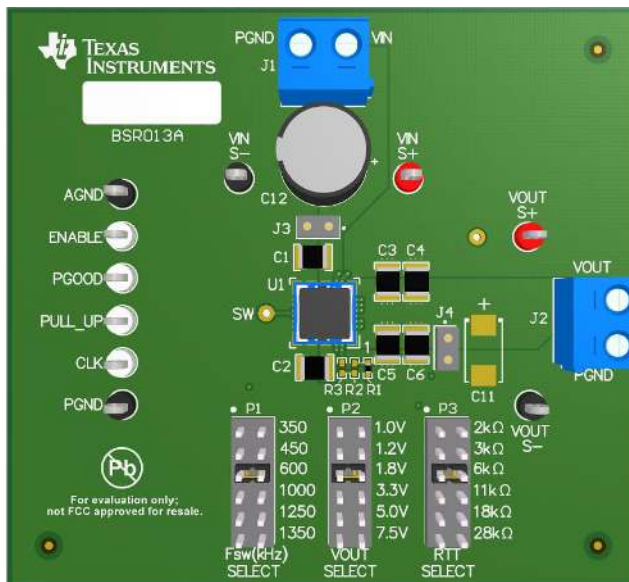


Figure 2-1. EVM User Interface

The S+ and S- test points for both VIN and VOUT, located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.

The VIN Scope (J3) and VOUT Scope (J4) test points can be used to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. The scope probe tip should be inserted into the socket marked with a white dot, and the scope ground lead should be inserted into the other socket.

The control test points located to the left of the device are made available to test the features of the device. The UVLO feature can be adjusted by changing resistors R24 and R25 on the bottom of the board. An external voltage can be applied to the PULL_UP test point for the PGOOD signal. Refer to the [Test Points Descriptions](#) section of this guide for more information on the individual control test points.

The Fsw SELECT jumper (P1), the VOUT SELECT jumper (P2) and the RTT SELECT jumper (P3) are provided for selecting the desired output voltage, the appropriate switching frequency and the appropriate TurboTrans resistor value. Before applying power to the EVM, ensure that the jumpers are present and properly positioned for the intended output voltage, switching frequency, and TurboTrans resistor value. Refer to [Table 2-1](#) for the recommended jumper settings. Always remove input power before changing the jumper settings.

Table 2-1. Output Voltage and Switching Frequency Jumper Settings

VOUT Select	Fsw Select	RTT Select
1 V	350 kHz	2 kΩ
1.2 V	450 kHz	3 kΩ
1.8 V	600 kHz	6 kΩ
3.3 V	1000 kHz	11 kΩ
5 V	1250 kHz	18 kΩ
7.5 V	1350 kHz	28 kΩ

3 Test Point Descriptions

Wire-loop test points and two scope probe test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point follows:

Table 3-1. Test Point Descriptions⁽¹⁾

VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
VIN S-	Input voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
VOUT S+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
VOUT S-	Output voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
AGND	Analog ground test point.
PGND	Power ground test point.
VIN Scope (J3)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT Scope (J4)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
ENABLE	Enable test point. Connect this test point to AGND to disable the device. Leave this test point open to enable the device. The UVLO resistor divider (R24 and R25) is connected at this point.
PGOOD	Monitors the power good signal of the device. This is an open drain signal.
PULL_UP	Test point provided for applying a pull-up voltage for the PGOOD signal. A 100-k Ω pull-up resistor (R26) is present on the EVM between this test point and the PGOOD signal.
CLK	Synchronization clock input test point. An AC coupling capacitor (C13) is present on the EVM between this test point and the SYNC pin of the device. Pads for a termination resistor (R27) are present between this test point and PGND. An external clock signal can be applied to this point to synchronize the device to an appropriate frequency.

(1) Refer to the product datasheet for absolute maximum ratings associated with above features.

4 Performance Data

Figure 4-1 through Figure 4-4 demonstrate the TPSM84824EVM performance. For more data regarding the TPSM84824, TPSM84624, or the TPSM84424, please see the product data sheet.

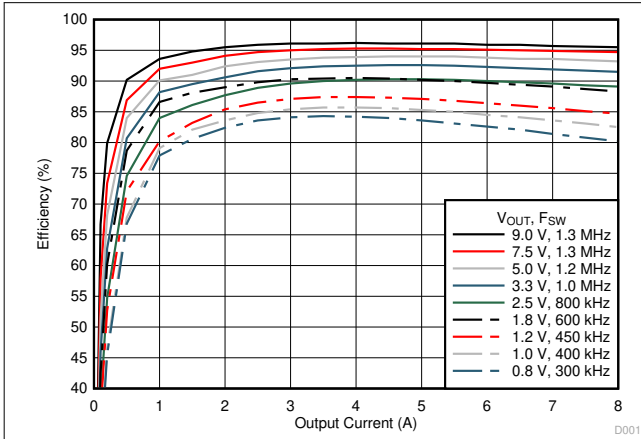


Figure 4-1. Efficiency ($V_{IN} = 12\text{ V}$)

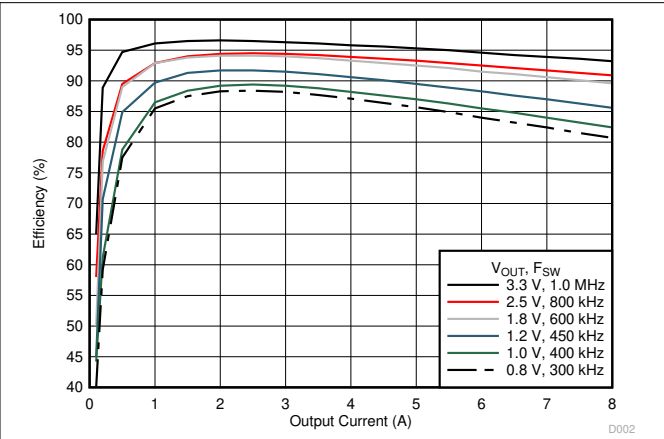


Figure 4-2. Efficiency ($V_{IN} = 5\text{ V}$)

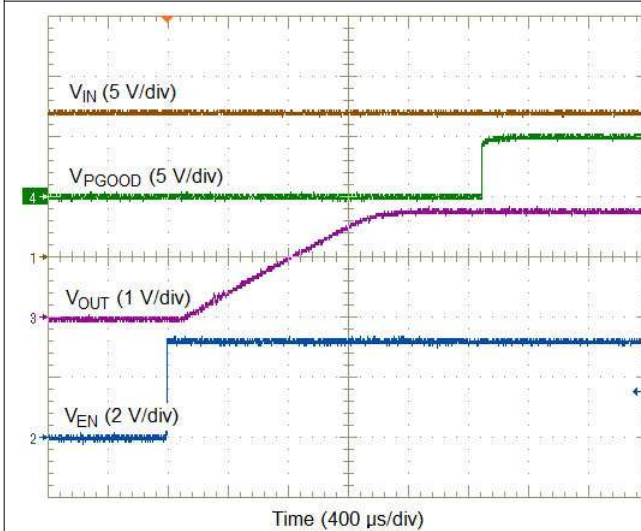


Figure 4-3. EN Start-up Waveforms

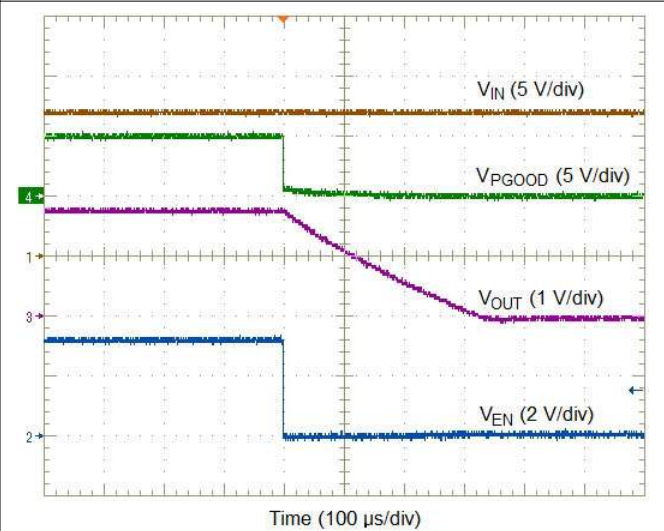


Figure 4-4. EN Shutdown Waveforms

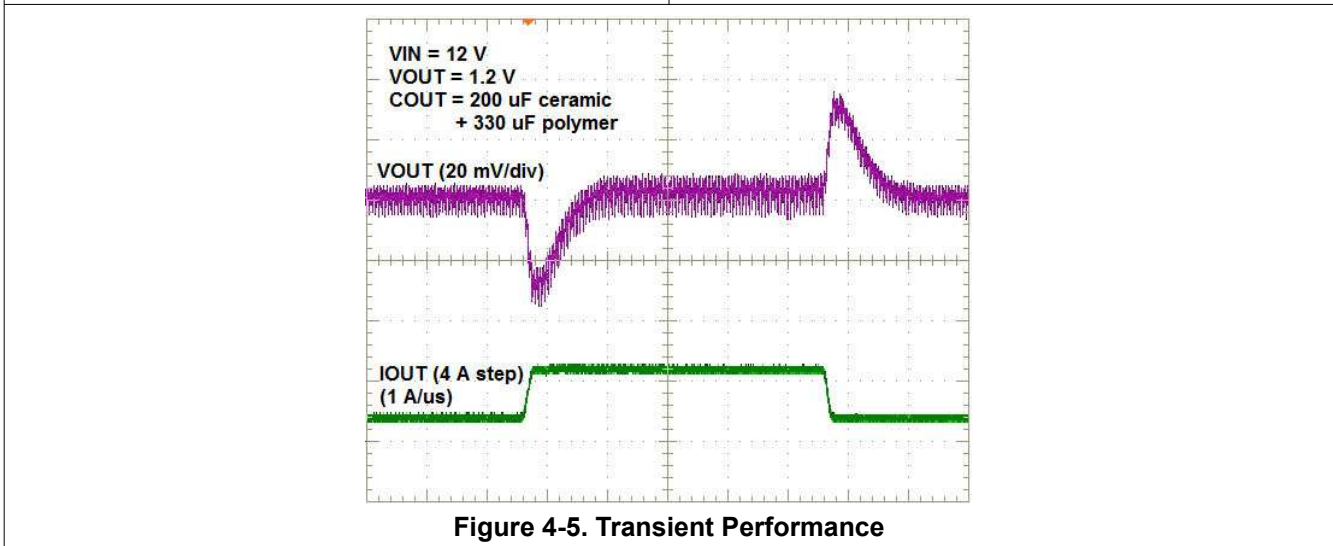


Figure 4-5. Transient Performance

5 Bill of Materials (BOM)

See [Table 5-1](#) for the TPSM84824EVM, TPSM84624EVM, or TPSM84424 bill of materials.

Table 5-1. EVM Bill of Materials

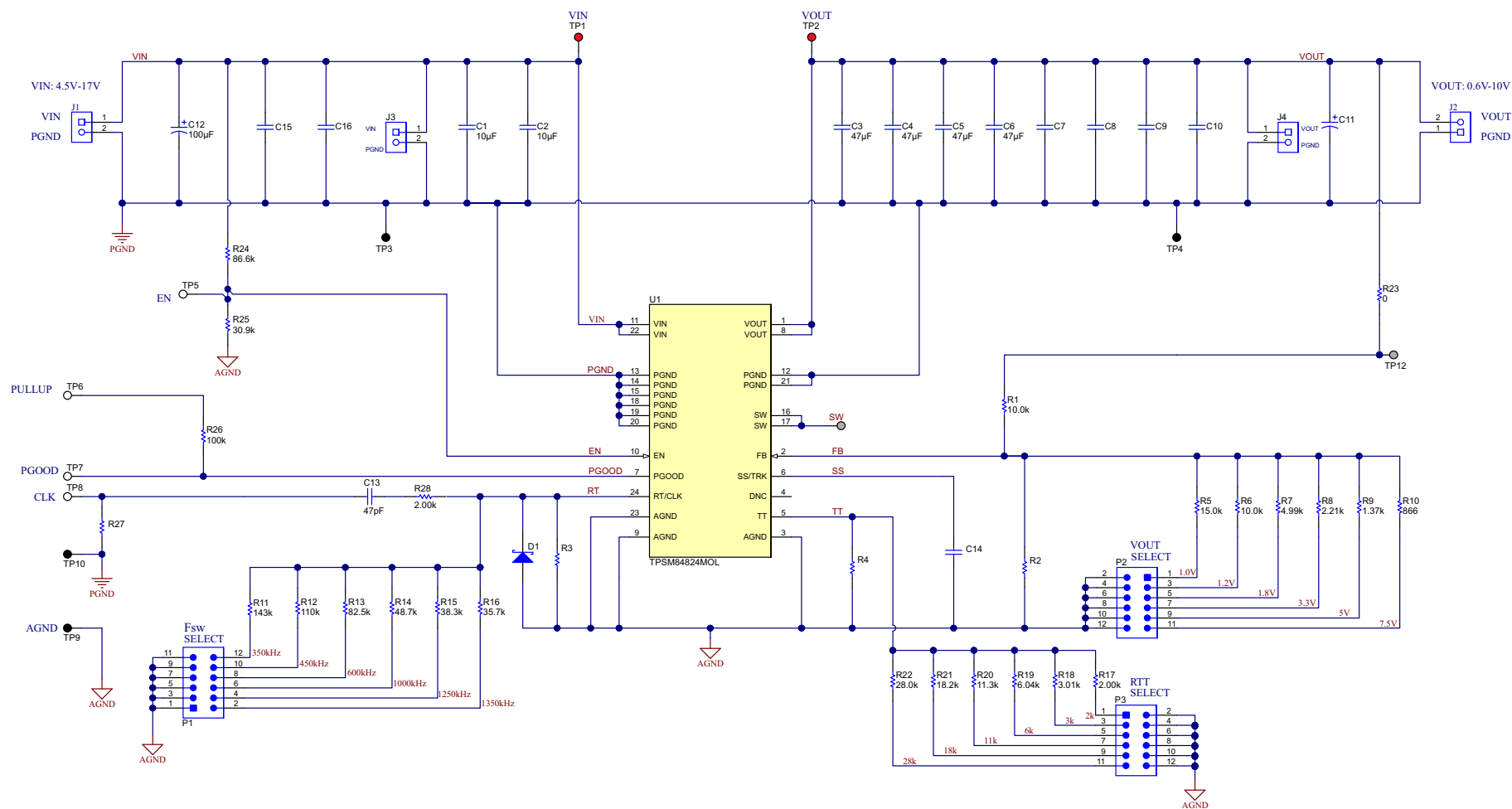
Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2	2	10 μ F	CAP, CERM, 10 μ F, 25 V,+/- 10%, X7R, 1210	1210	GRM32DR71E106KA12L	MuRata
C3, C4, C5, C6	4	47 μ F	CAP, CERM, 47 μ F, 10 V,+/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
C12	1	100 μ F	CAP, AL, 100 μ F, 50 V, +/- 20%, 0.162 ohm, TH		EEUFC1H101B	Panasonic
C13	1	47pF	CAP, CERM, 47 pF, 50 V,+/- 1%, C0G/NP0, 0603	0603	GRM1885C1H470FA01J	MuRata
J1, J2	2		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J3, J4	2		Socket Strip, 2x1, 100mil, Black, Tin, TH	Socket Strip, 100mil, 2pin	310-43-102-41-001000	Mill-Max
P1, P2, P3	3		Header, 100mil, 6x2, Tin, TH	Header, 6x2, 100mil, Tin	PEC06DAAN	Sullins Connector Solutions
R1	1	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R5	1	15.0k	RES, 15.0 k, 1%, 0.1 W, 0603	0603	CRCW060315K0FKEA	Vishay-Dale
R6	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R7	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	CRCW06034K99FKEA	Vishay-Dale
R8	1	2.21k	RES, 2.21 k, 1%, 0.1 W, 0603	0603	CRCW06032K21FKEA	Vishay-Dale
R9	1	1.37k	RES, 1.37 k, 1%, 0.1 W, 0603	0603	CRCW06031K37FKEA	Vishay-Dale
R10	1	866	RES, 866, 1%, 0.063 W, 0603	0603	CRCW0603866RFKEA	Vishay-Dale
R11	1	143k	RES, 143 k, 1%, 0.1 W, 0603	0603	CRCW0603143KFKEA	Vishay-Dale
R12	1	110k	RES, 110 k, 1%, 0.1 W, 0603	0603	CRCW0603110KFKEA	Vishay-Dale
R13	1	82.5k	RES, 82.5 k, 1%, 0.1 W, 0603	0603	CRCW060382K5FKEA	Vishay-Dale
R14	1	48.7k	RES, 48.7 k, 1%, 0.1 W, 0603	0603	CRCW060348K7FKEA	Vishay-Dale
R15	1	38.3k	RES, 38.3 k, 1%, 0.1 W, 0603	0603	CRCW060338K3FKEA	Vishay-Dale
R16	1	35.7k	RES, 35.7 k, 1%, 0.1 W, 0603	0603	CRCW060335K7FKEA	Vishay-Dale
R17, R28	2	2.00k	RES, 2.00 k, 1%, 0.1 W, 0603	0603	CRCW06032K00FKEA	Vishay-Dale
R18	1	3.01k	RES, 3.01 k, 1%, 0.1 W, 0603	0603	CRCW06033K01FKEA	Vishay-Dale
R19	1	6.04k	RES, 6.04 k, 1%, 0.1 W, 0603	0603	CRCW06036K04FKEA	Vishay-Dale
R20	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	CRCW060311K3FKEA	Vishay-Dale
R21	1	18.2k	RES, 18.2 k, 1%, 0.1 W, 0603	0603	CRCW060318K2FKEA	Vishay-Dale
R22	1	28.0k	RES, 28.0 k, 1%, 0.1 W, 0603	0603	CRCW060328K0FKEA	Vishay-Dale
R23	1	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Vishay-Dale
R24	1	86.6k	RES, 86.6 k, 1%, 0.1 W, 0603	0603	CRCW060386K6FKEA	Vishay-Dale

Table 5-1. EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R25	1	30.9k	RES, 30.9 k, 1%, 0.1 W, 0603	0603	CRCW060330K9FKEA	Vishay-Dale
R26	1	100k	RES, 100 k, 5%, 0.063 W, 0402	0402	CRCW0402100KJNED	Vishay-Dale
SH-P1, SH-P2 SH-P3	3	1x2	Shunt, 2mm, Gold plated, Black	2mm Shunt, Closed Top	2SN-BK-G	Samtec
TP1, TP2	2		Test Point, Multipurpose, Red, TH	Multipurpose Testpoint Red	5010	Keystone
TP3, TP4, TP9, TP10	4		Test Point, Multipurpose, Black, TH	Multipurpose Testpoint Black	5011	Keystone
TP5, TP16, TP7, TP8	4		Test Point, Multipurpose, White, TH	Multipurpose Testpoint White	5012	Keystone
U1	1		TPSM84824 MOL0024A (QFN-24)	MOL0024A	TPSM84824MOL	Texas Instruments
			TPSM84624 MOL0024A (QFN-24)		TPSM84624MOL	
			TPSM84424 MOL0024A (QFN-24)		TPSM8424MOL	
C7, C8, C9, C10	0		CAP, CERM, 1210	1210		
C11	0		CAP, Tantalum Polymer, 7343-40 SMD	7343-40		
C14	0		CAP, CERM, 0402	0402		
C15, C16	0		CAP, CERM, 1210	1210		
D1	0		Diode, Schottky, 30 V, 0.2 A, SOD-323	SOD-323	BAT54WS-7-F	Diodes Inc.
R2, R3	0		RES, 0.1 W, 0603	0603		
R4	0		RES, 0.063 W, 0402	0402		
R27	0		RES, 1W, 2512	2512		
TP11	0		Test Point. No entry in BOM.	N/A		

6 Schematic

Figure 6-1 is the schematic for the TPSM84824EVM. The schematic for the TPSM84624EVM and TPSM84424EVM is identical with the only difference is the U1 IC.



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Figure 6-1. TPSM84824EVM Schematic

7 PCB Layout

Figure 7-1 through Figure 7-6 show the PCB layers of the TPSM84824EVM, TPSM84624EVM and TPSM84424EVM.

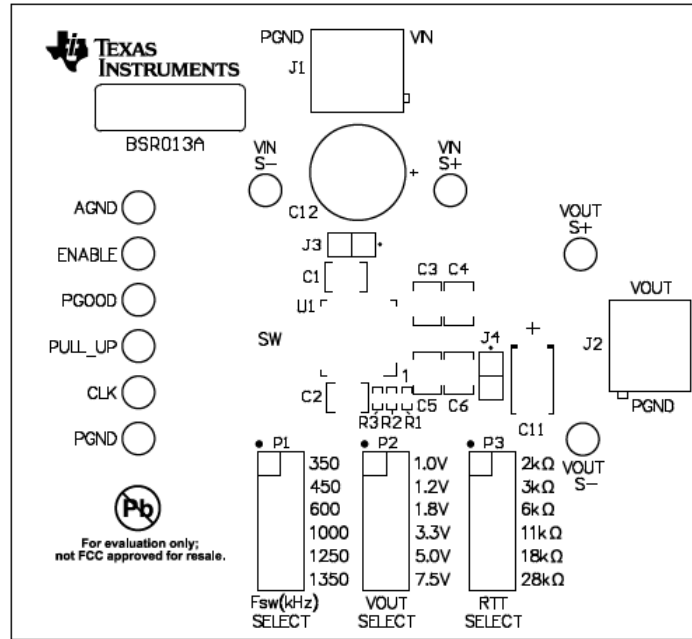


Figure 7-1. Topside Component Layout (Top View)

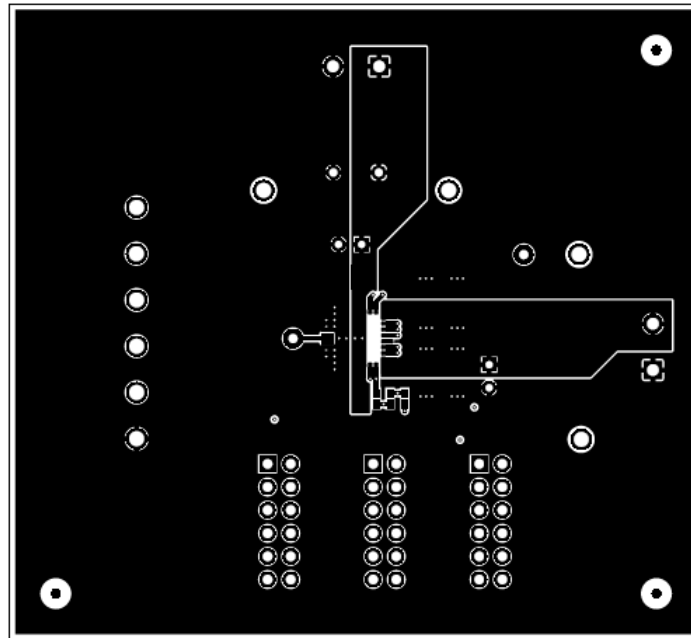


Figure 7-2. Topside Copper (Top View)

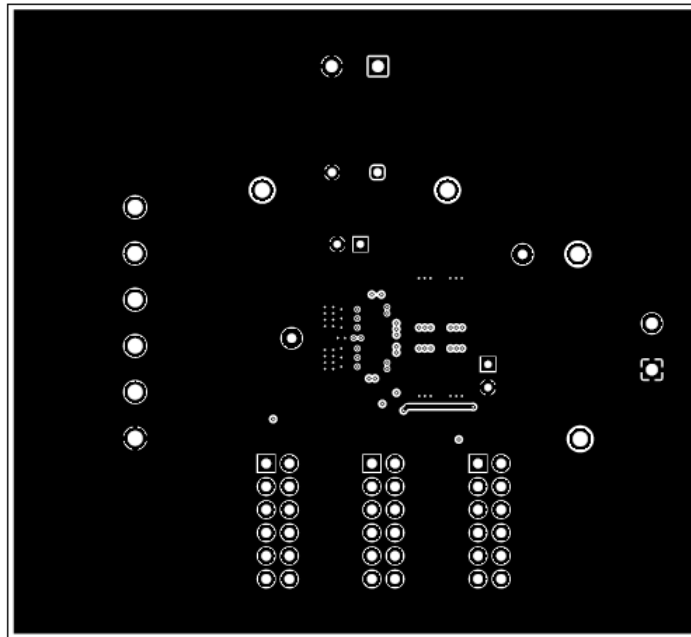


Figure 7-3. Layer 2 Copper (Top View)

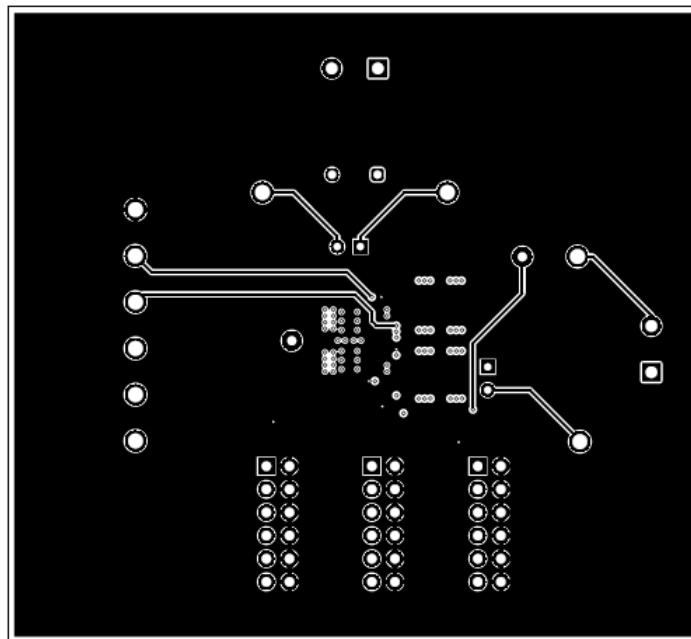


Figure 7-4. Layer 3 Copper (Top View)

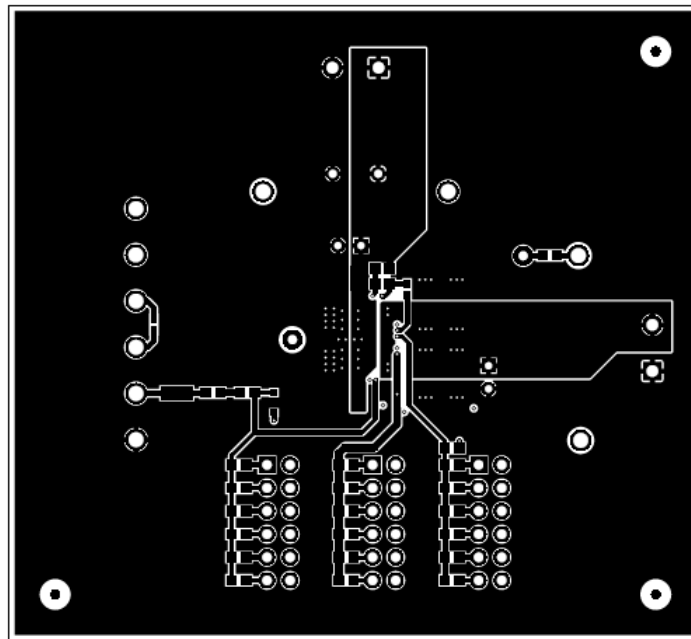


Figure 7-5. Bottom-Side Copper (Top View)

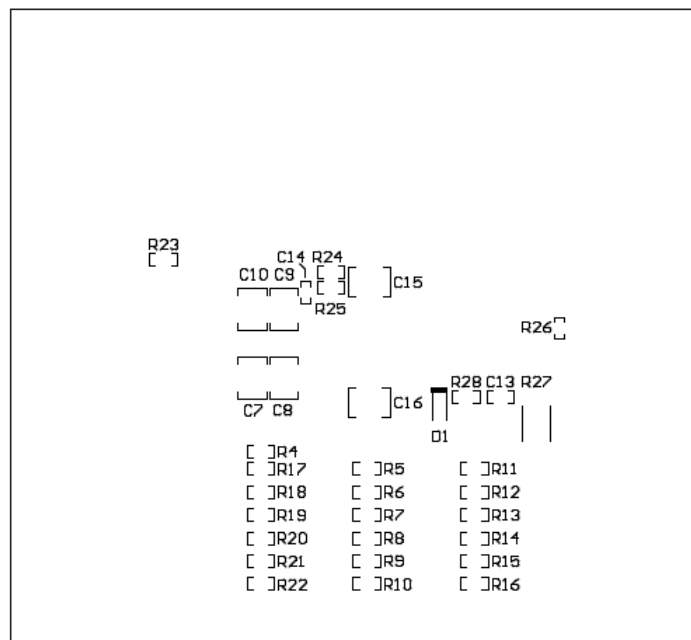


Figure 7-6. Bottom-Side Component Layout (Bottom View)

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2018) to Revision B (June 2021)	Page
• Updated user's guide title.....	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
Changes from Revision * (November 2017) to Revision A (March 2018)	Page
• Added TPSM84624EVM option to user guide.....	1

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