January 1998

Fast CMOS 20-Bit Buffers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16827T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162827T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162H827T
  - Bus Hold Retains Last Active Bus State During Three-State
  - Eliminates the Need for External Pull-Up Resistors

Description

These devices are 20-bit wide bus drivers designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the devices to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74FCT16827T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The CD74FCT162827T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H827T has "Bus Hold" which retains the input's last state whenever the input goes to high impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.
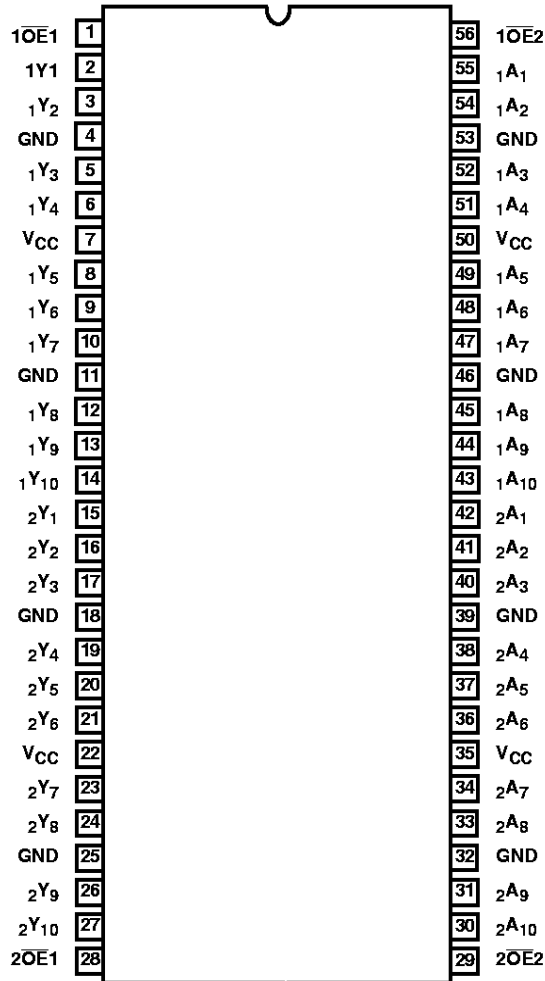
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827ETSM	-40 to 85	56 Ld SSOP	M56.300-P

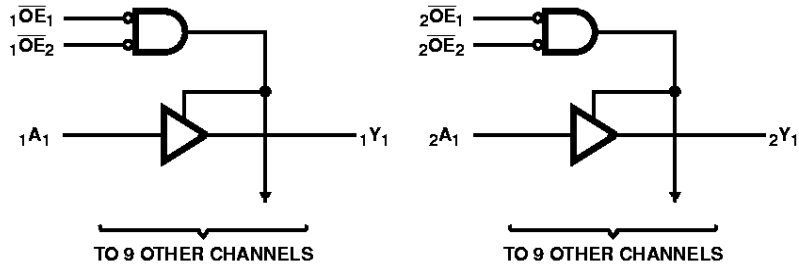NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

File Number **4190.2**

Pinout

CD74FCT16827T, CD74FCT162827T, CD74FCT162H827T
(SSOP, TSSOP)
TOP VIEW

Left	Pin		Pin	Right
$1\overline{OE}1$	1		56	$1\overline{OE}2$
1Y1	2		55	$_1A_1$
$_1Y_2$	3		54	$_1A_2$
GND	4		53	GND
$_1Y_3$	5		52	$_1A_3$
$_1Y_4$	6		51	$_1A_4$
V_{CC}	7		50	V_{CC}
$_1Y_5$	8		49	$_1A_5$
$_1Y_6$	9		48	$_1A_6$
$_1Y_7$	10		47	$_1A_7$
GND	11		46	GND
$_1Y_8$	12		45	$_1A_8$
$_1Y_9$	13		44	$_1A_9$
$_1Y_{10}$	14		43	$_1A_{10}$
$_2Y_1$	15		42	$_2A_1$
$_2Y_2$	16		41	$_2A_2$
$_2Y_3$	17		40	$_2A_3$
GND	18		39	GND
$_2Y_4$	19		38	$_2A_4$
$_2Y_5$	20		37	$_2A_5$
$_2Y_6$	21		36	$_2A_6$
V_{CC}	22		35	V_{CC}
$_2Y_7$	23		34	$_2A_7$
$_2Y_8$	24		33	$_2A_8$
GND	25		32	GND
$_2Y_9$	26		31	$_2A_9$
$_2Y_{10}$	27		30	$_2A_{10}$
$2\overline{OE}1$	28		29	$2\overline{OE}2$

Functional Block Diagram

TO 9 OTHER CHANNELS   TO 9 OTHER CHANNELS

TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$x\overline{OE}_1$	$x\overline{OE}_2$	xA_x	xY_x
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$x\overline{OE}_x$	Output Enable Inputs (Active LOW)
xA_x	Data Inputs (Note 2)
xY_x	Three-State Outputs

NOTE:

2. For the CD74FCT162H827T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage .... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range .... -40°C to 85°C
Supply Voltage to Ground Potential
 Inputs and V_{CC} Only .... -0.5V to 7.0V
Supply Voltage to Ground Potential
 Outputs and D/O Only .... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
 TSSOP Package 85
 SSOP Package 70
Maximum Junction Temperature .... 150°C
Maximum Storage Temperature Range .... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .... 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

| PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CD74FCT16827T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	μA
CD74FCT162827T, CD74FCT162H240T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}1$ = $\overline{OE}2$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	μA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}1$ = $\overline{OE}2$ = GND f_I = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}1$ = $\overline{OE}2$ = GND 8 Bits Toggling f_I = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	5.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.0	20.5 (Note 12)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	AT (NOTE 15) MIN	AT MAX	BT (NOTE 15) MIN	BT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
Propagation Delay $_XA_X$ to $_XY_X$	t_{PLH}, t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	8.0	1.5	5.0	1.5	4.4	1.5	3.8	1.5	3.2	ns
		$C_L = 300pF$ (Note 15) $R_L = 500\Omega$	1.5	15.0	1.5	13.0	1.5	10.0	1.5	7.5	1.5	7.0	ns
Output Enable Time $_X\overline{OE}_X$ to $_XY_X$	t_{PZH}, t_{PZL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	1.5	5.0	1.5	4.8	ns
		$C_L = 300pF$ (Note 16) $R_L = 500\Omega$	1.5	23.0	1.5	15.0	1.5	14.0	1.5	9.0	1.5	9.0	ns
Output Disable Time (Note 16) $\overline{OE}_N$ to Y_N	t_{PHZ}, t_{PLZ}	$C_L = 5pF$ $R_L = 500\Omega$	1.5	9.0	1.5	6.0	1.5	5.7	1.5	4.3	1.5	4.0	ns
		$C_L = 50pF$ $R_L = 500\Omega$	1.5	10.0	1.5	7.0	1.5	6.0	1.5	4.3	1.5	4.0	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.

5. Typical values are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.

6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

7. Pins with Bus Hold are identified in the pin description.

8. This specification does not apply to bidirectional functionalities with Bus Hold.

9. This parameter is determined by device characterization but is not production tested.

10. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.

14. See test circuit and wave forms.

15. Minimum limits are guaranteed but not tested on Propagation Delays.

16. This parameter is guaranteed but not production tested.

17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms
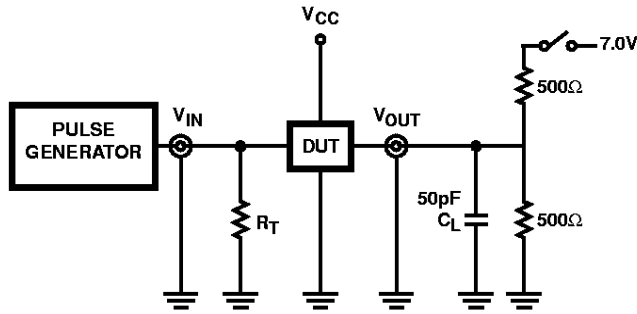
SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.
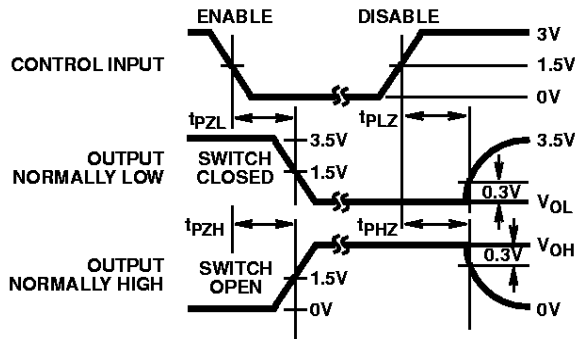
FIGURE 1. TEST CIRCUIT

FIGURE 2. ENABLE AND DISABLE TIMING
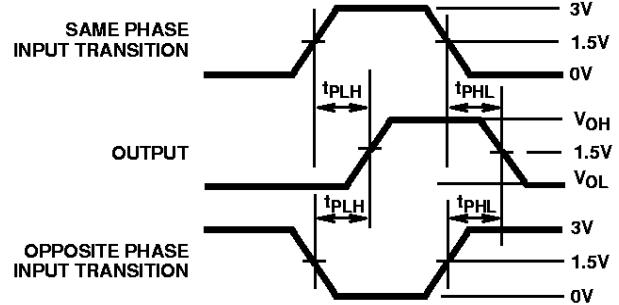
FIGURE 3. PROPAGATION DELAY

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