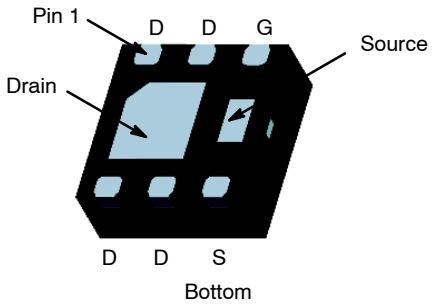
MOSFET – Single, P-Channel, POWERTRENCH®

-12 V, -12 A, 12.5 mΩ

FDMA908PZ

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
−12 V	12.5 mΩ @ −4.5 V	−12 A
	18 mΩ @ −2.5 V	
	28 mΩ @ −1.8 V	



DFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 506DT

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on−state resistance and zener diode protection against ESD. The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- Max $R_{DS(on)}$ = 12.5 mΩ at V_{GS} = −4.5 V, I_D = −12 A
- Max $R_{DS(on)}$ = 18 mΩ at V_{GS} = −2.5 V, I_D = −10 A
- Max $R_{DS(on)}$ = 28 mΩ at V_{GS} = −1.8 V, I_D = −8 A
- Low Profile − 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2.8 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

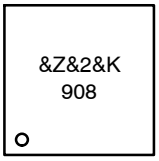
Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		−12	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	T_A = 25°C	 −12 −40	A
P_D	Power Dissipation – (Note 1a) – (Note 1b)	 T_A = 25°C T_A = 25°C	 2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

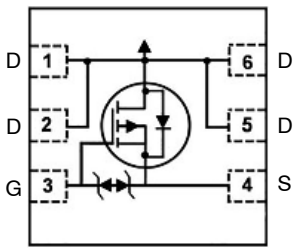
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
908 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDMA908PZ	DFN6 (Pb−Free, Halide Free)	3000 / Tape & Reel

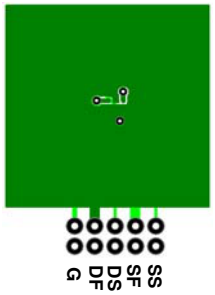
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	I_D = –250 μA, V_{GS} = 0 V	–12	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25°C	–	–10	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –9.6 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250 μA	–0.4	–0.6	–1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25°C	–	2.8	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = –4.5 V, I_D = –12 A	–	10	12.5	mΩ
		V_{GS} = –2.5 V, I_D = –10 A	–	13	18	
		V_{GS} = –1.8 V, I_D = –8 A	–	18	28	
		V_{GS} = –4.5 V, I_D = –12 A, T_J = 125°C	–	13	16	
g_{FS}	Forward Transconductance	V_{DD} = –5 V, I_D = –12 A	–	63	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –6 V, V_{GS} = 0 V, f = 1 MHz	–	2638	3957	pF
C_{oss}	Output Capacitance		–	649	974	pF
C_{rss}	Reverse Transfer Capacitance		–	602	903	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –6 V, I_D = –12 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω	–	11	21	ns
t_r	Rise Time		–	12	23	ns
$t_{d(off)}$	Turn–Off Delay Time		–	131	223	ns
t_f	Fall Time		–	71	121	ns
Q_g	Total Gate Charge	V_{DD} = –6 V, I_D = –12 A, V_{GS} = –4.5 V	–	24	34	nC
Q_{gs}	Gate to Source Charge		–	3.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	5.3	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = –2 A (Note 2)	–	–0.6	–1.2	V
		V_{GS} = 0 V, I_S = –12 A (Note 2)	–	–0.8	–1.2	
t_{rr}	Reverse Recovery Time	I_F = –12 A, di/dt = 100 A/μs	–	26	42	ns
Q_{rr}	Reverse Recovery Charge		–	8.5	17	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR–4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 52°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 145°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

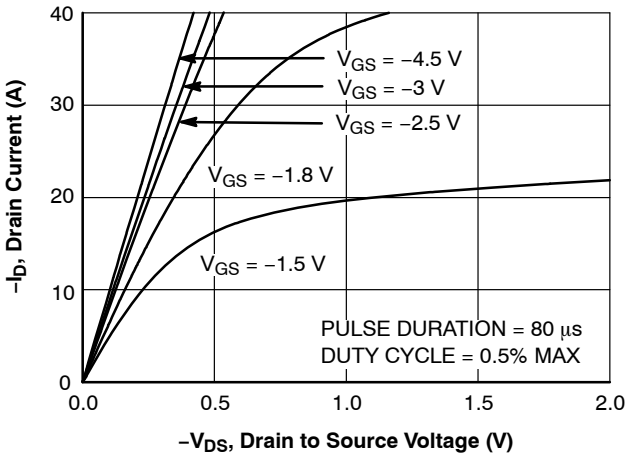


Figure 1. On−Region Characteristics

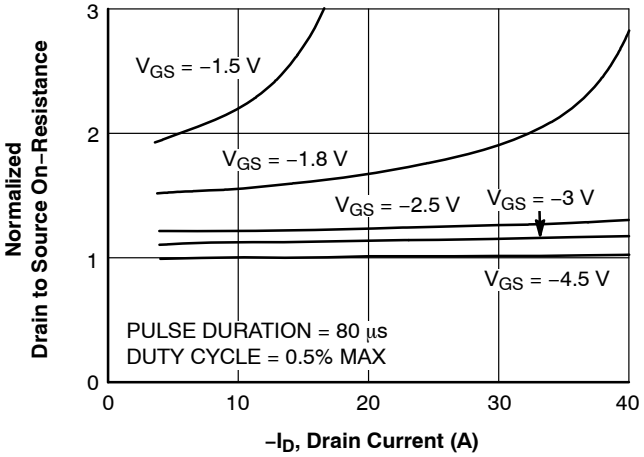


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

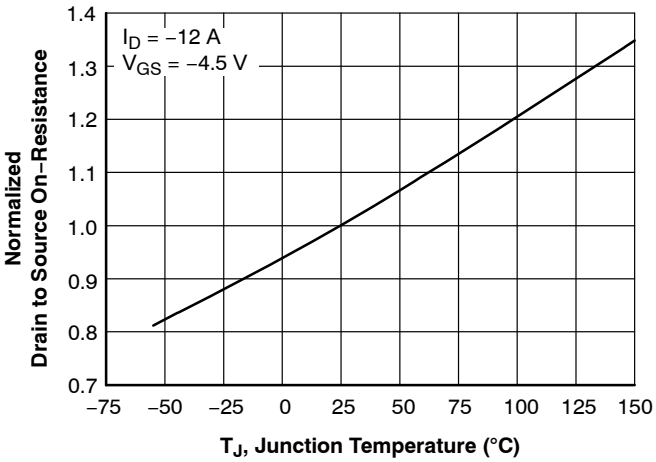


Figure 3. Normalized On−Resistance vs. Junction Temperature

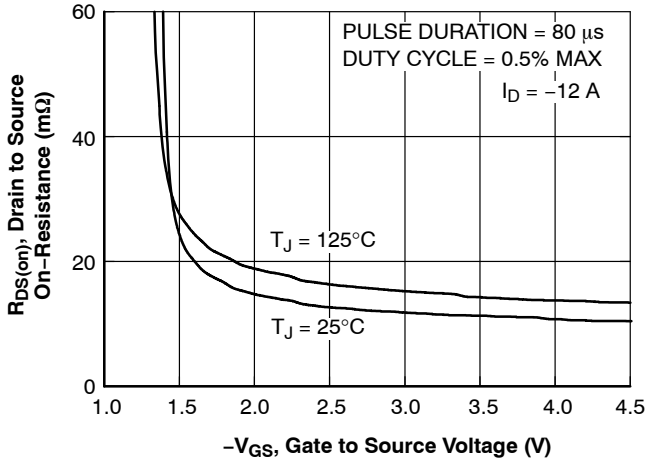


Figure 4. On−Resistance vs. Gate to Source Voltage

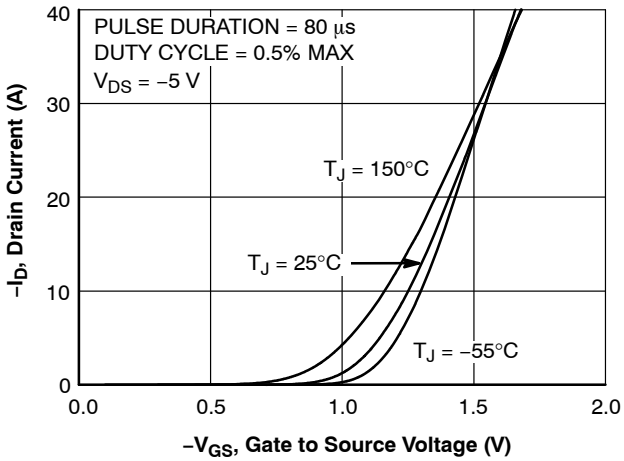


Figure 5. Transfer Characteristics

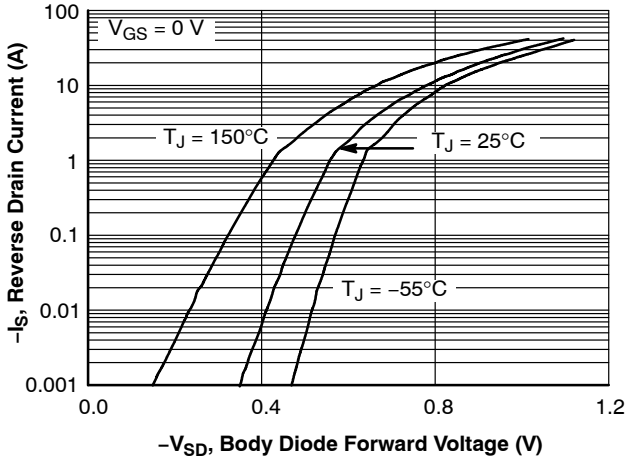


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

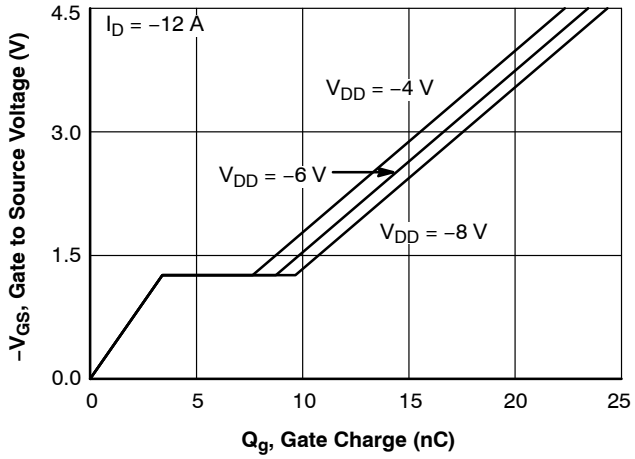


Figure 7. Gate Charge Characteristics

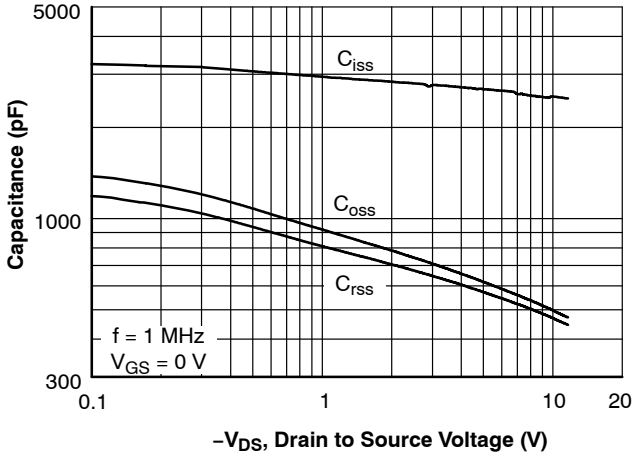


Figure 8. Capacitance vs. Drain to Source Voltage

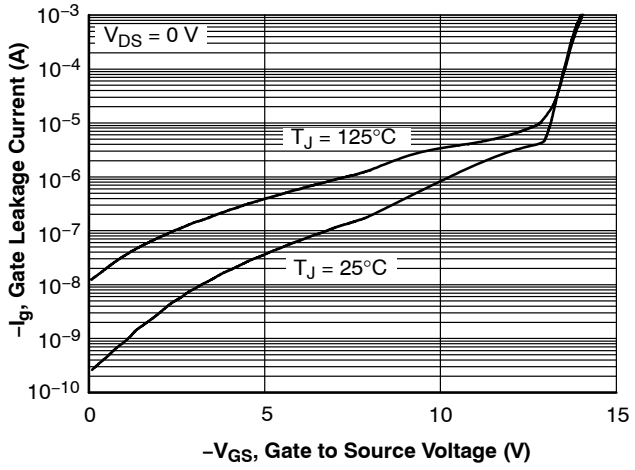


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

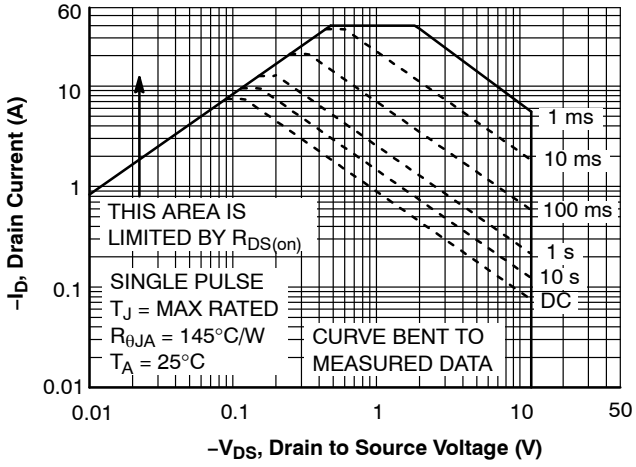


Figure 10. Forward Bias Safe Operating Area

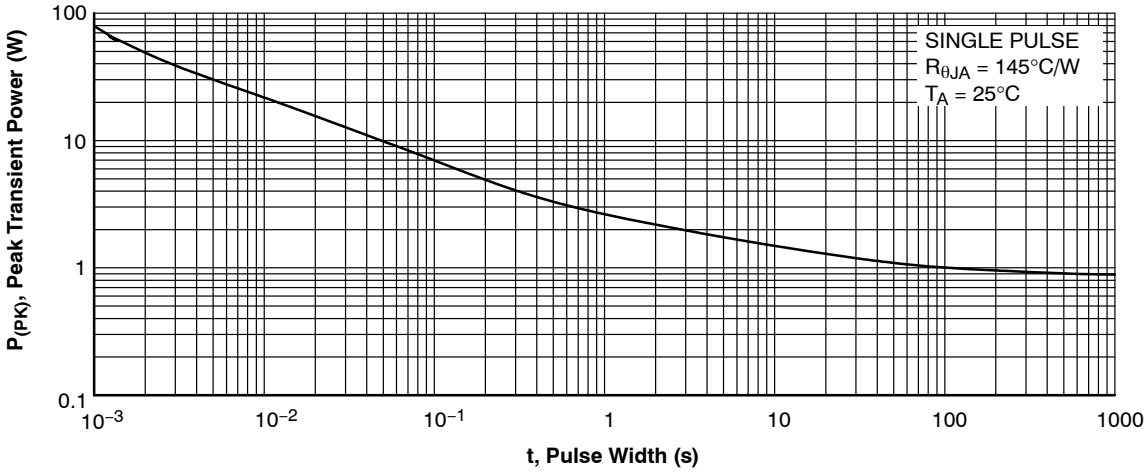


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

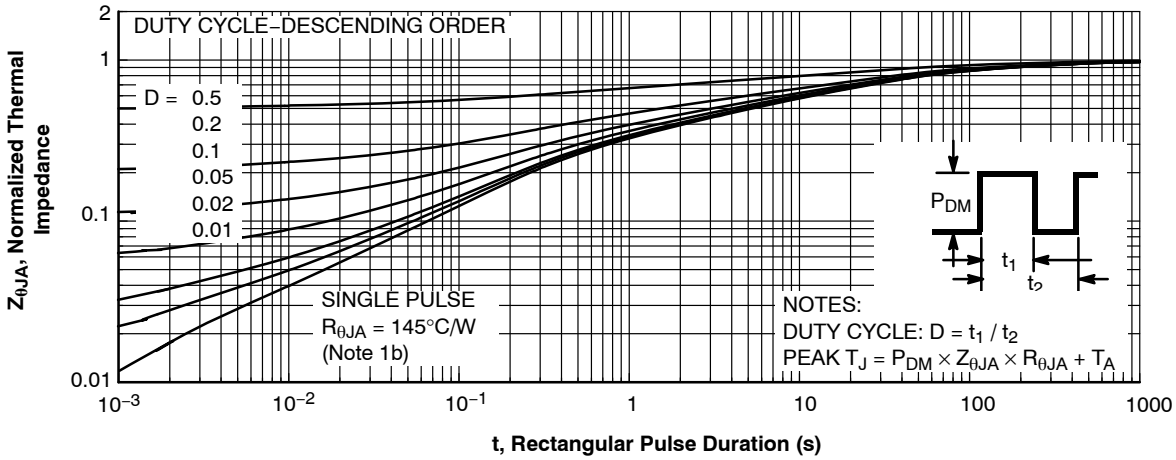


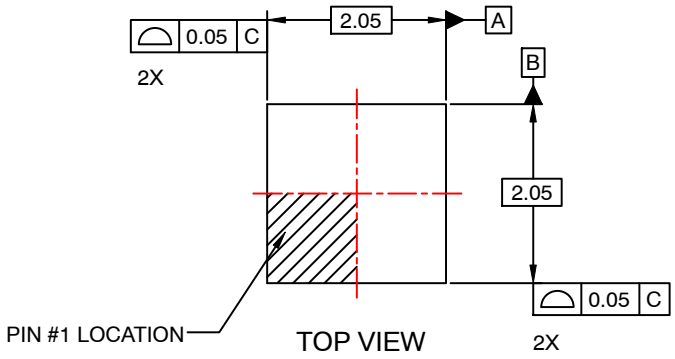
Figure 12. Junction−to−Ambient Transient Thermal Response Curve

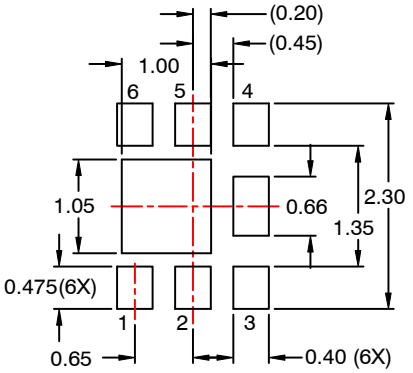
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

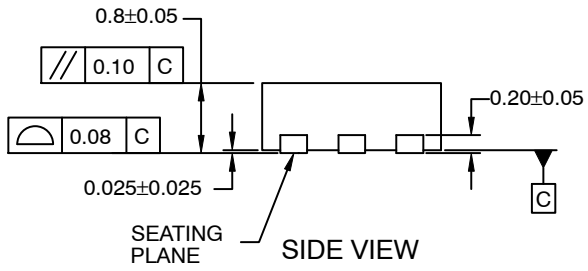
DFN6 2x2, 0.65P
CASE 506DT
ISSUE O

DATE 31 JUL 2016

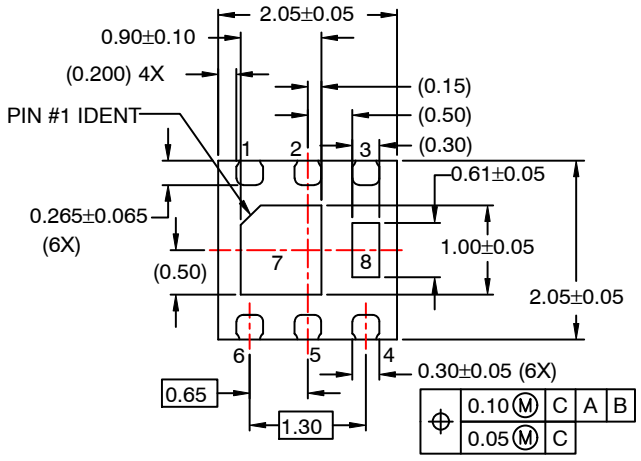




RECOMMENDED LAND PATTERN



Pin #	Function
1	Drain
2	Drain
3	Gate
4	Source
5	Drain
6	Drain
7	Drain
8	Source



NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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