

MOSFET – Single, P-Channel, POWERTRENCH®

-12 V, -12 A, 12.5 mΩ

FDMA908PZ

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- Max $R_{DS(on)}$ = 12.5 mΩ at $V_{GS} = -4.5$ V, $I_D = -12$ A
- Max $R_{DS(on)}$ = 18 mΩ at $V_{GS} = -2.5$ V, $I_D = -10$ A
- Max $R_{DS(on)}$ = 28 mΩ at $V_{GS} = -1.8$ V, $I_D = -8$ A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2.8 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

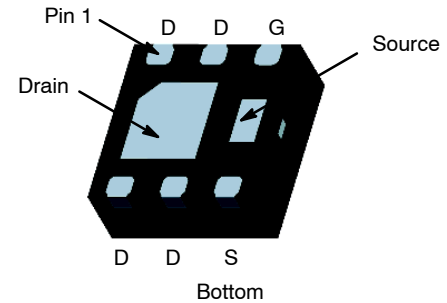
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-12	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	$T_A = 25^\circ\text{C}$ -12 -40	A
P_D	Power Dissipation – (Note 1a) – (Note 1b)	$T_A = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ 2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

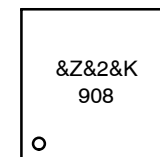
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
-12 V	12.5 mΩ @ -4.5 V	-12 A
	18 mΩ @ -2.5 V	
	28 mΩ @ -1.8 V	



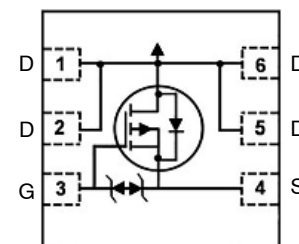
DFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 506DT

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- 908 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDMA908PZ	DFN6 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDMA908PZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-12	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-10	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -9.6 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V	-	-	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	2.8	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -4.5 V, I _D = -12 A	-	10	12.5	mΩ
		V _{GS} = -2.5 V, I _D = -10 A	-	13	18	
		V _{GS} = -1.8 V, I _D = -8 A	-	18	28	
		V _{GS} = -4.5 V, I _D = -12 A, T _J = 125°C	-	13	16	
g _{FS}	Forward Transconductance	V _{DD} = -5 V, I _D = -12 A	-	63	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -6 V, V _{GS} = 0 V, f = 1 MHz	-	2638	3957	pF
C _{oss}	Output Capacitance		-	649	974	pF
C _{rss}	Reverse Transfer Capacitance		-	602	903	pF

SWITCHING CHARACTERISTICS

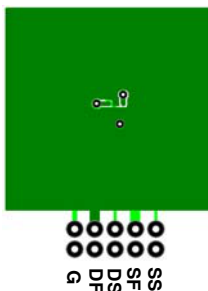
t _{d(on)}	Turn-On Delay Time	V _{DD} = -6 V, I _D = -12 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω	-	11	21	ns
t _r	Rise Time		-	12	23	ns
t _{d(off)}	Turn-Off Delay Time		-	131	223	ns
t _f	Fall Time		-	71	121	ns
Q _g	Total Gate Charge	V _{DD} = -6 V, I _D = -12 A, V _{GS} = -4.5 V	-	24	34	nC
Q _{gs}	Gate to Source Charge		-	3.4	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	5.3	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -2 A (Note 2)	-	-0.6	-1.2	V
		V _{GS} = 0 V, I _S = -12 A (Note 2)	-	-0.8	-1.2	
t _{rr}	Reverse Recovery Time	I _F = -12 A, di/dt = 100 A/μs	-	26	42	ns
Q _{rr}	Reverse Recovery Charge		-	8.5	17	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 52°C/W when mounted on a 1 in² pad of 2 oz copper



b. 145°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

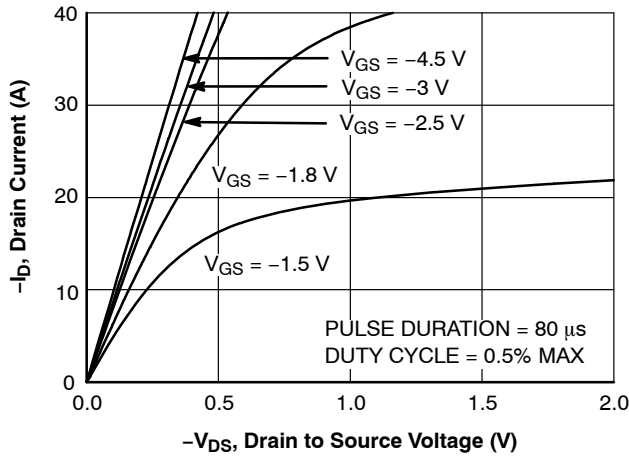


Figure 1. On-Region Characteristics

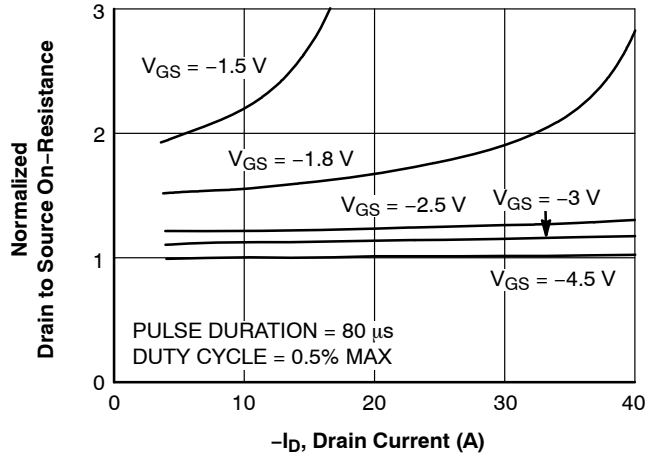


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

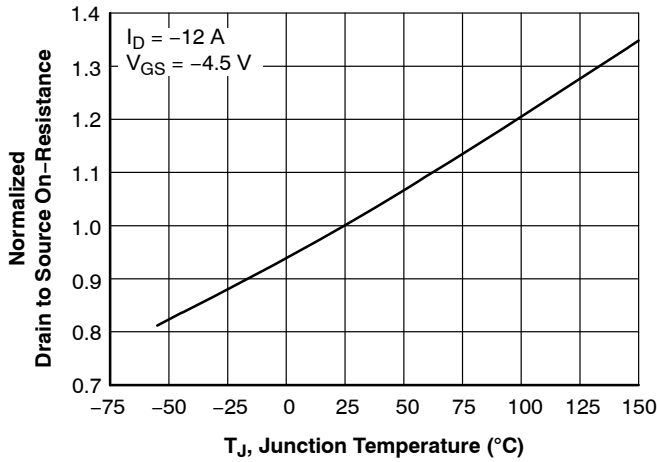


Figure 3. Normalized On-Resistance vs. Junction Temperature

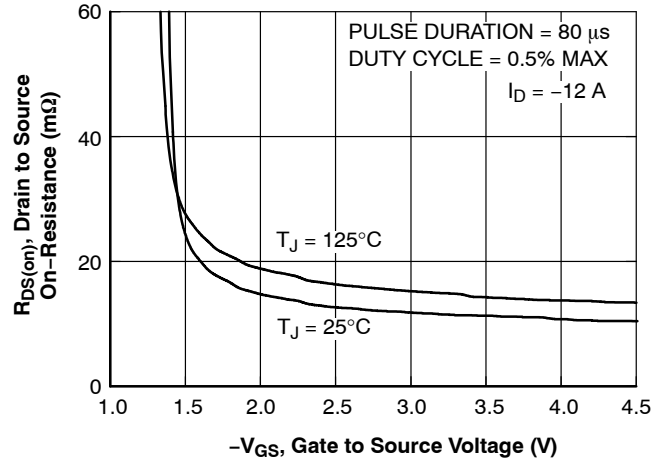


Figure 4. On-Resistance vs. Gate to Source Voltage

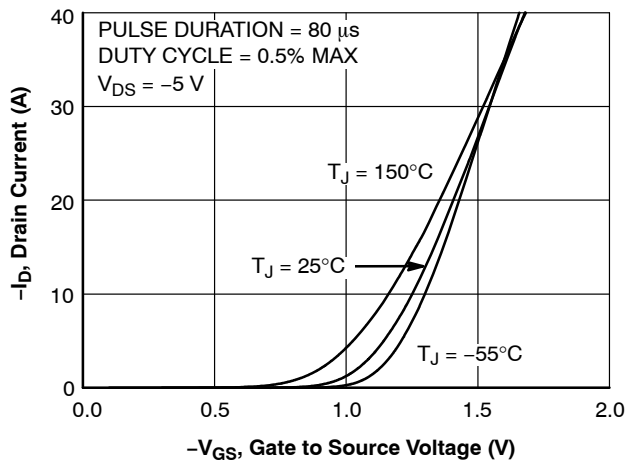


Figure 5. Transfer Characteristics

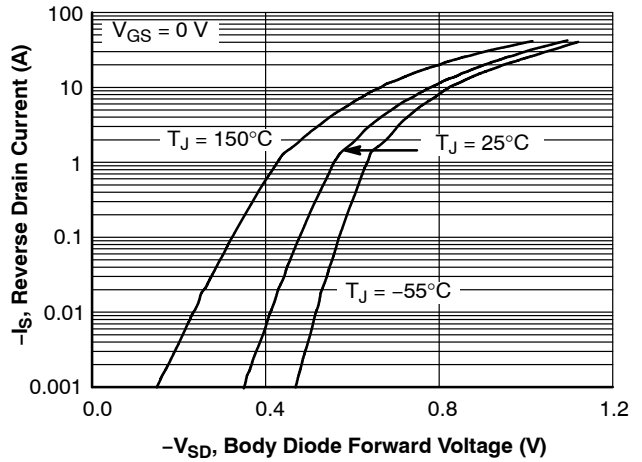


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

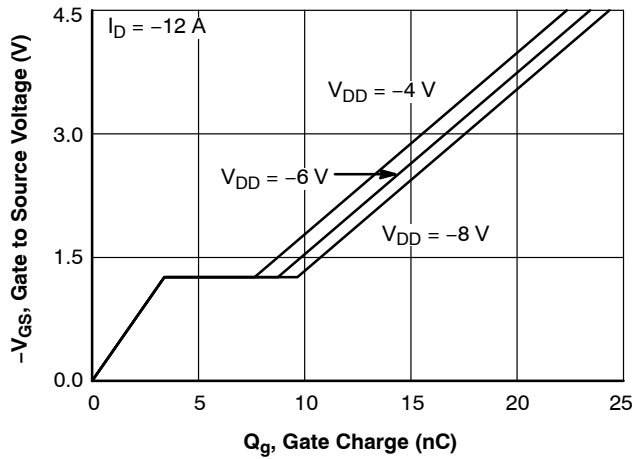


Figure 7. Gate Charge Characteristics

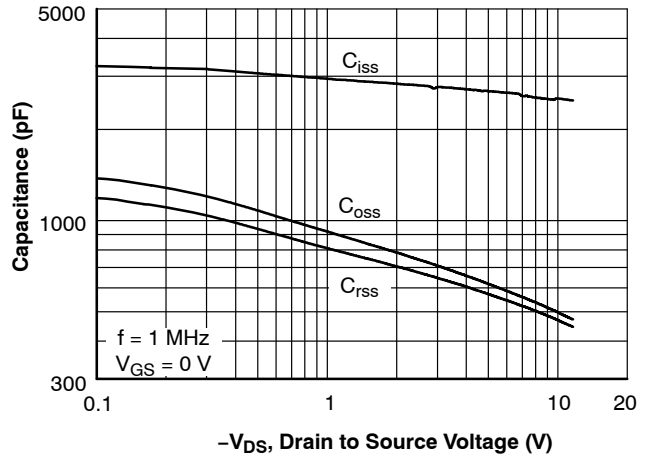


Figure 8. Capacitance vs. Drain to Source Voltage

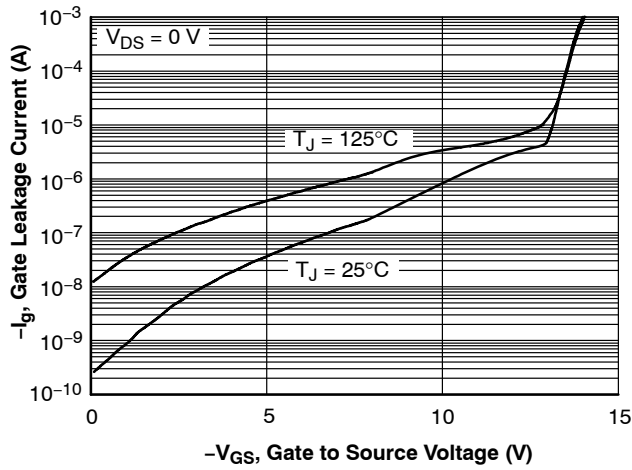


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

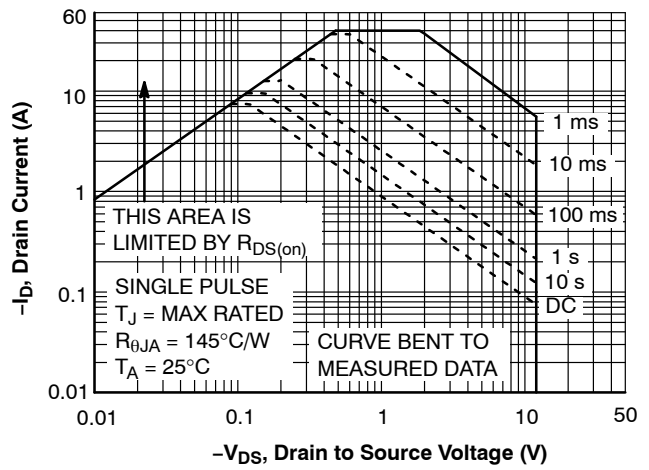


Figure 10. Forward Bias Safe Operating Area

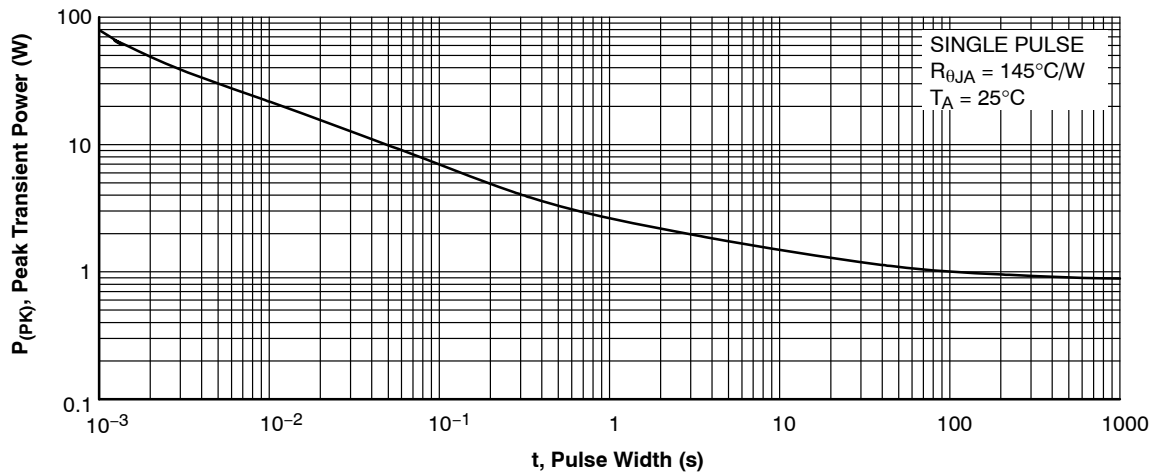


Figure 11. Single Pulse Maximum Power Dissipation

FDMA908PZ

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

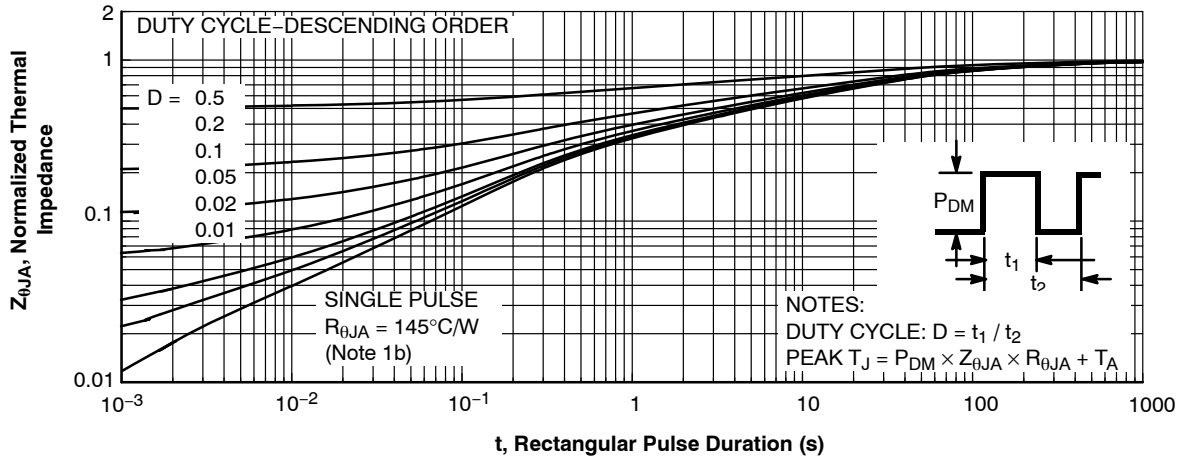


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

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MECHANICAL CASE OUTLINE

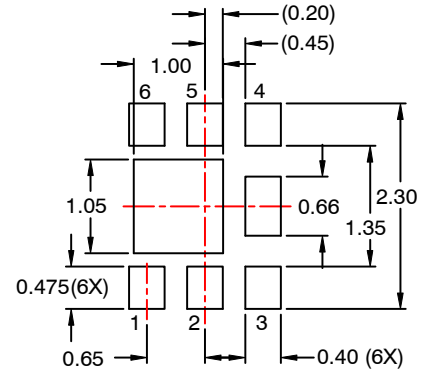
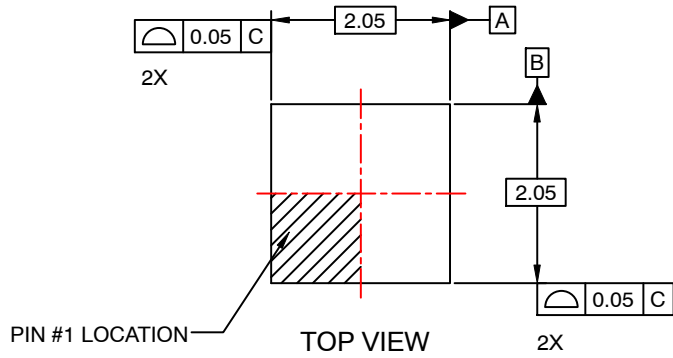
PACKAGE DIMENSIONS

ON Semiconductor®

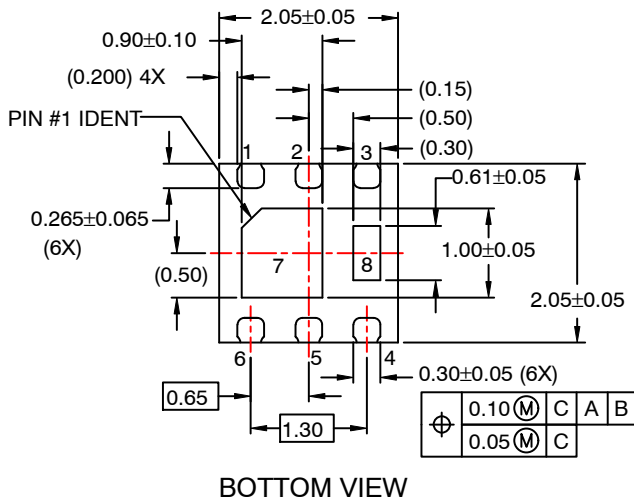
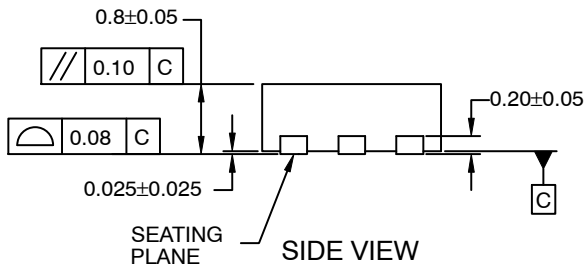


DFN6 2x2, 0.65P
CASE 506DT
ISSUE O

DATE 31 JUL 2016



RECOMMENDED LAND PATTERN



BOTTOM VIEW

Pin #	Function
1	Drain
2	Drain
3	Gate
4	Source
5	Drain
6	Drain
7	Drain
8	Source

NOTES:

- A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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