19-1309; Rev 0; 10/97

5-Tap Silicon Delay Line

General Description

The MXD1005 silicon delay line offers five equally spaced taps with delays ranging from 12ns to 250ns and a nominal accuracy of ±2ns or ±3%, whichever is greater. Relative to hybrid solutions, this device offers enhanced performance and higher reliability, and reduces overall cost. Each tap can drive up to ten 74LS loads.

The MXD1005 is available in multiple versions, each offering a different combination of delay times. It comes in the space-saving 8-pin µMAX package, as well as an 8-pin SO or DIP, allowing full compatibility with the DS1005 and other delay line products.

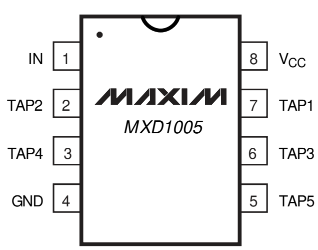
Applications

Clock Synchronization

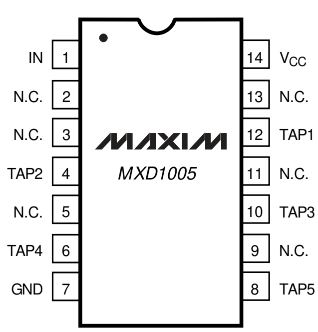
Digital Systems

Pin Configurations

TOP VIEW



DIP/SO/µMAX



DIP

Pin Configurations continued at end of data sheet.

Features

- ♦ **Improved Second Source to DS1005**
- ♦ **Available in Space-Saving 8-Pin µMAX Package**
- ♦ **17mA Supply Current vs. Dallas' 40mA**
- ♦ **Low Cost**
- ♦ **Delay Tolerance of ±2ns or ±3%, whichever is Greater**
- ♦ **TTL/CMOS-Compatible Logic**
- ♦ **Leading- and Trailing-Edge Accuracy**
- ♦ **Custom Delays Available**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXD1005C/D__	0°C to +70°C	Dice*
MXD1005PA__	-40°C to +85°C	8 Plastic DIP
MXD1005PD__	-40°C to +85°C	14 Plastic DIP
MXD1005SA__	-40°C to +85°C	8 SO
MXD1005SE__	-40°C to +85°C	16 Narrow SO
MXD1005UA__	-40°C to +85°C	8 µMAX

**Dice are tested at T_A = +25°C.*

Note: *To complete the ordering information, fill in the blank with the part number extension from the Part Number and Delay Times table to indicate the desired delay per output.*

Part Number and Delay Times

PART NUMBER EXTENSION (MXD1005_ _ _)	DELAY (t_{PHL}, t_{PLH}) PER OUTPUT (ns)				
	TAP1	TAP2	TAP3	TAP4	TAP5
60	12	24	36	48	60
75	15	30	45	60	75
100	20	40	60	80	100
125	25	50	75	100	125
150	30	60	90	120	150
175	35	70	105	140	175
200	40	80	120	160	200
250	50	100	150	200	250

Note: *Contact factory for characterization data.*

Functional Diagram appears at end of data sheet.

5-Tap Silicon Delay Line

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.5V to +6V
All Other Pins...-0.5V to (V_{CC} + 0.5V)
Short-Circuit Output Current (1sec)....................................50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.1mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.0mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.9mW/°C above +70°C)..................471mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) 696mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V ±5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 2)	4.75	5.00	5.25	V
Input Voltage High	V_{IH}	(Note 2)	2.2			V
Input Voltage Low	V_{IL}	(Note 2)			0.8	V
Input Leakage Current	I_L	0V ≤ V_{IN} ≤ V_{CC}	-1		1	µA
Active Current	I_{CC}	V_{CC} = 5.25V, period = minimum (Notes 3, 4)		17	70	mA
Output Current High	I_{OH}	V_{CC} = 4.75V, V_{OH} = 4.0V			-1	mA
Output Current Low	I_{OL}	V_{CC} = 4.75V, V_{OL} = 0.5V	12			mA
Input Capacitance	C_{IN}	T_A = +25°C (Note 5)		5	10	pF

TIMING CHARACTERISTICS

(V_{CC} = +5.0V ±5%, T_A = +25°C, unless otherwise noted.)

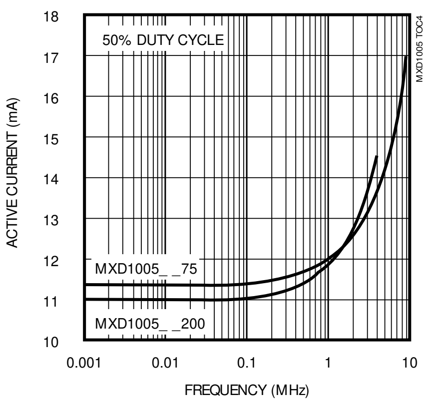
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	t_{WI}	(Note 6)	40% of TAP5 t_{PLH}			ns
Input-to-Tap Delay (leading edge)	t_{PLH}	(Notes 7–10)		See *Part Number and Delay Times* table		ns
Input-to-Tap Delay (trailing edge)	t_{PHL}	(Notes 7–10)		See *Part Number and Delay Times* table		ns
Power-Up Time	t_{PU}				100	ms
Period		(Note 6)	4(t_{WI})			ns

Note 1: Specifications to -40°C are guaranteed by design, not production tested.
Note 2: All voltages referenced to GND.
Note 3: Measured with outputs open.
Note 4: I_{CC} is a function of frequency and TAP5 delay. Only an MXD1005_ _60 operating with a 40ns period and V_{CC} = +5.25V will have a maximum I_{CC} of 70mA. For example, an MXD1005_ _100 will not exceed 30mA. See Supply Current vs. Input Frequency graph in *Typical Operating Characteristics.*
Note 5: Guaranteed by design.
Note 6: Pulse width and/or period specifications may be exceeded, but accuracy is application sensitive (i.e., layout, decoupling, etc.).
Note 7: V_{CC} = +5V at +25°C. Typical delays are accurate on both rising and falling edges within ±2ns or ±3%.
Note 8: See *Test Conditions* section.
Note 9: The combination of temperature variations from +25°C to 0°C or +25°C to +70°C and voltage variation from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional typical input-to-tap delay shift of ±1.5ns or ±4%, whichever is greater.
Note 10: All taps and outputs delays tend to vary unilaterally with temperature or supply variations. For example, if TAP1 slows down, all other taps will also slow down; TAP3 cannot be faster than TAP2.

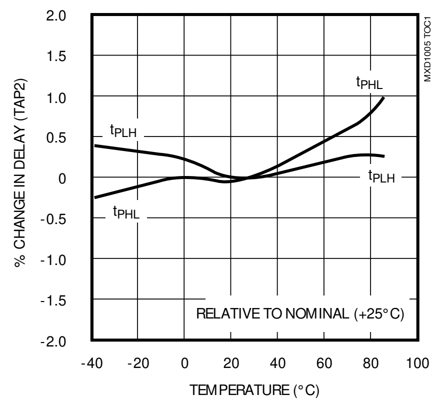
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

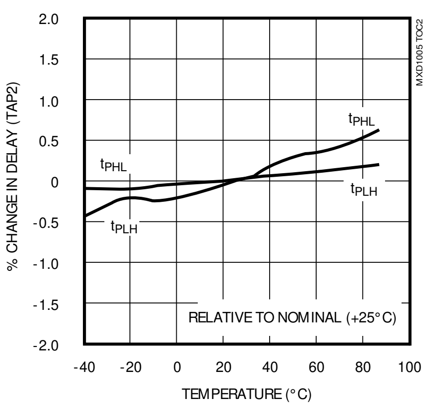
ACTIVE CURRENT vs. FREQUENCY



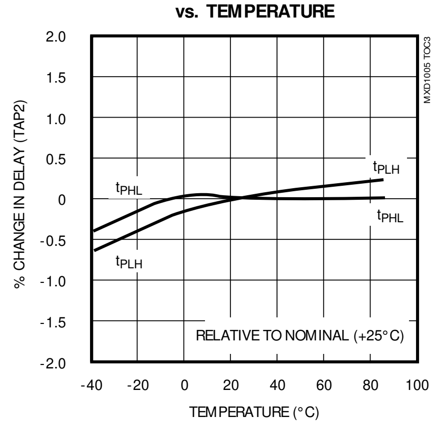
MXD1005_ _75 PERCENT CHANGE IN DELAY vs. TEMPERATURE



MXD1005_ _100 TO MXD1005_ _200 PERCENT CHANGE IN DELAY vs. TEMPERATURE



MXD1005_ _250 PERCENT CHANGE IN DELAY vs. TEMPERATURE



5-Tap Silicon Delay Line

Pin Description

PIN			NAME	FUNCTION
8-PIN DIP/SO/µMAX	14-PIN DIP	16-PIN SO		
1	1	1	IN	Signal Input
2	4	4	TAP2	40% of specified maximum delay
3	6	6	TAP4	80% of specified maximum delay
4	7	8	GND	Device Ground
5	8	9	TAP5	100% of maximum specified delay
6	10	11	TAP3	60% of specified maximum delay
7	12	13	TAP1	20% of specified maximum delay
8	14	16	V_{CC}	Power-Supply Input
—	2, 3, 5, 9, 11, 13	2, 3, 5, 7, 10, 12, 14, 15	N.C.	No Connection. Not internally connected.

Note: *Maximum delay is determined by the part number extension. See the Part Number and Delay Times table for more information.*

Definitions of Terms

Period: The time elapsed between the first pulse's leading edge and the following pulse's leading edge.

Pulse Width (t_{WI}): The time elapsed on the pulse between the 1.5V level on the leading edge and the 1.5V level on the trailing edge, or vice-versa.

Input Rise Time (t_{RISE}): The time elapsed between the 20% and 80% points on the input pulse's leading edge.

Input Fall Time (t_{FALL}): The time elapsed between the 80% and 20% points on the input pulse's trailing edge.

Time Delay, Rising (t_{PLH}): The time elapsed between the 1.5V level on the input pulse's leading edge and the corresponding output pulse's leading edge.

Time Delay, Falling (t_{PHL}): The time elapsed between the 1.5V level on the input pulse's trailing edge and the corresponding output pulse's trailing edge.

Test Conditions

Ambient Temperature:	+25°C ±3°C
Supply Voltage (V_{CC}):	+5V ±0.01V
Input Pulse:	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance:	50Ω max
Rise and Fall Times:	3.0ns max
Pulse Width:	500ns max
Period:	1µs

Each output is loaded with a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edges. The time delay due to the 74F04 is subtracted from the measured delay.

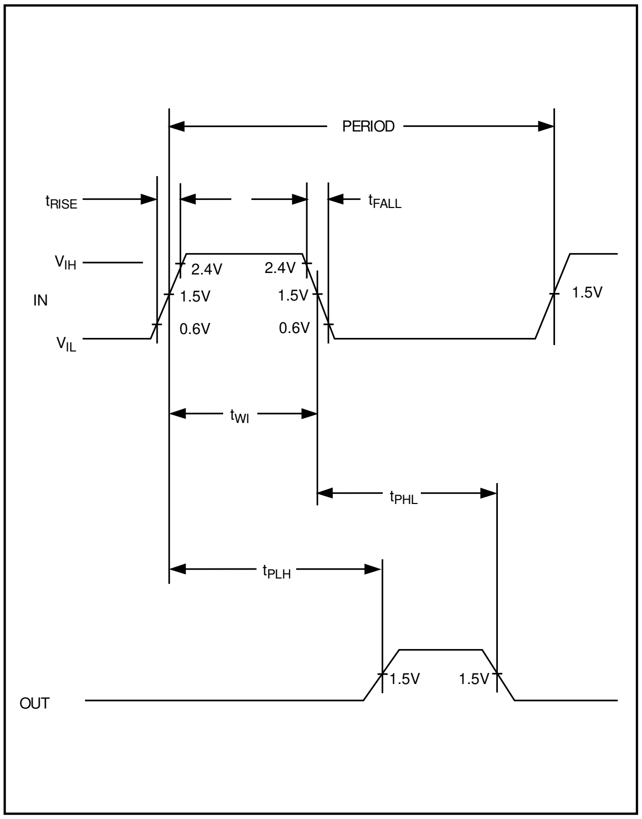


Figure 1. Timing Diagram

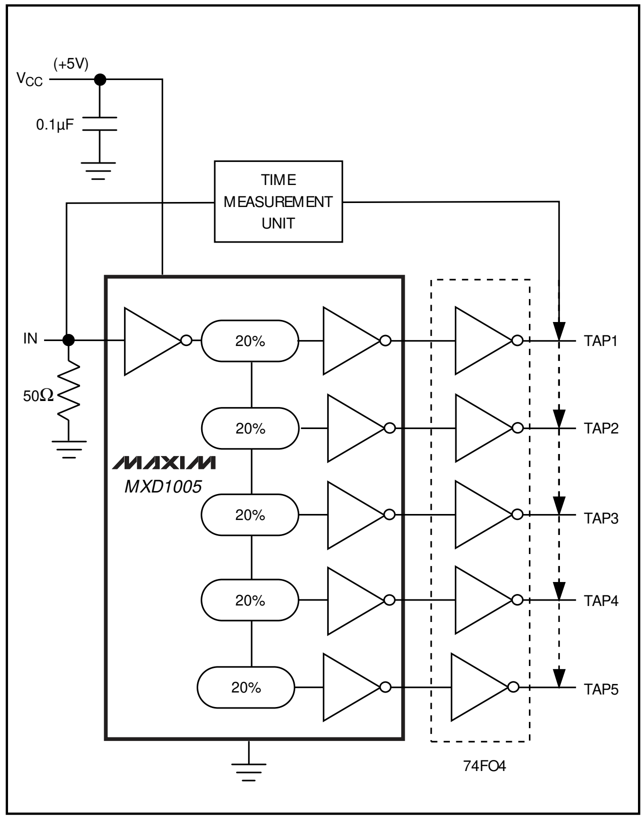


Figure 2. Test Circuit

Applications Information

Supply and Temperature Effects on Delay

Variations in supply voltage may affect the MXD1005's fixed tap delays. Supply voltages beyond the specified range may result with larger variations. The devices are internally compensated to reduce the effects of temperature variations. Although these devices might vary with supply and temperature, the delays vary unilaterally, which suggests that TAP3 can never be faster than TAP2.

Capacitance and Loading Effects on Delay

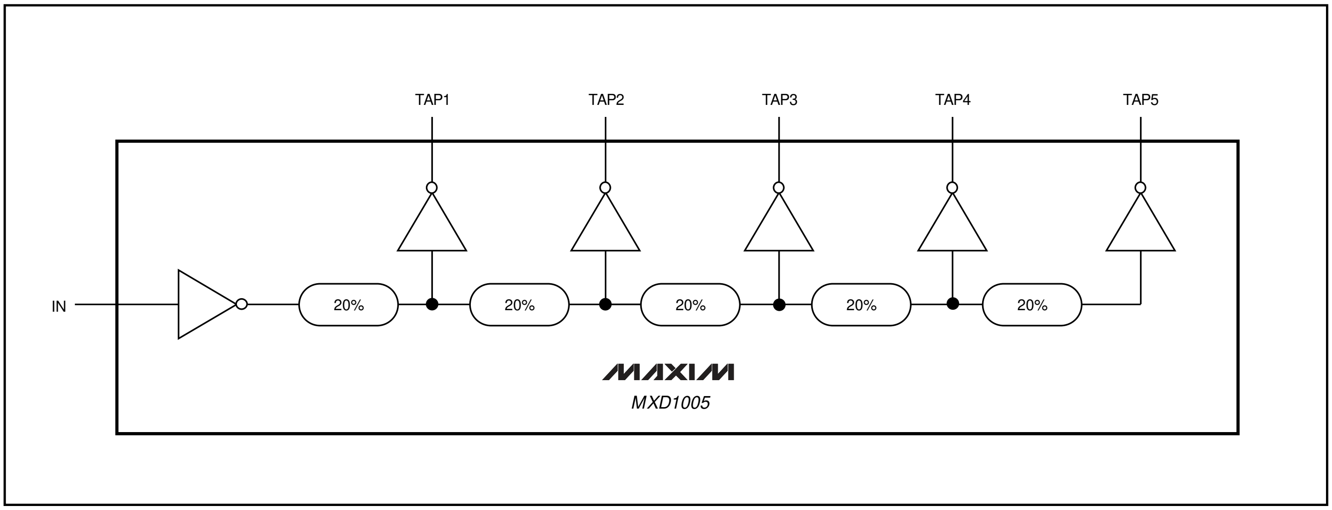
The output load can affect the tap delays. Larger capacitances tend to lengthen the rising and falling edges, thus increasing the tap delays. As the taps are loaded with other logic devices, the increased load will increase the tap delays.

Board Layout Considerations/Decoupling

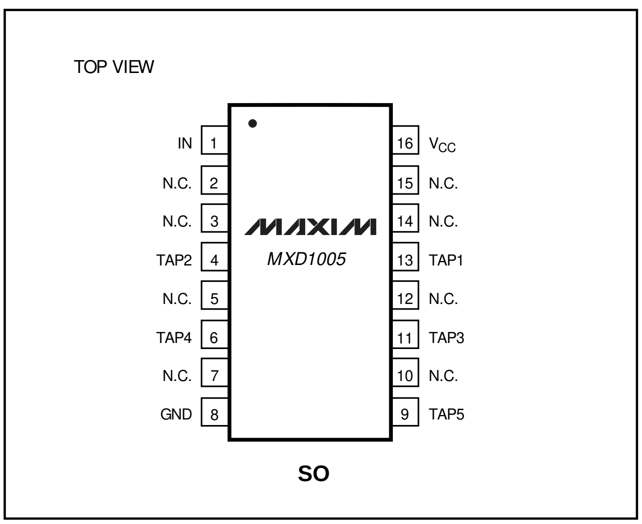
The device should be driven with a source that can deliver the required current for proper operation. A 0.1µF ceramic bypassing capacitor could be used. The board should be designed to reduce stray capacitance.

5-Tap Silicon Delay Line

Functional Diagram



Pin Configurations (continued)

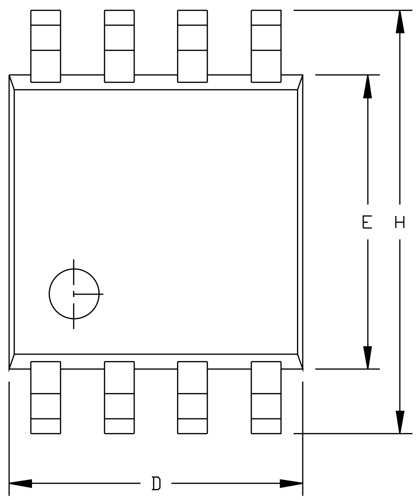


Chip Information

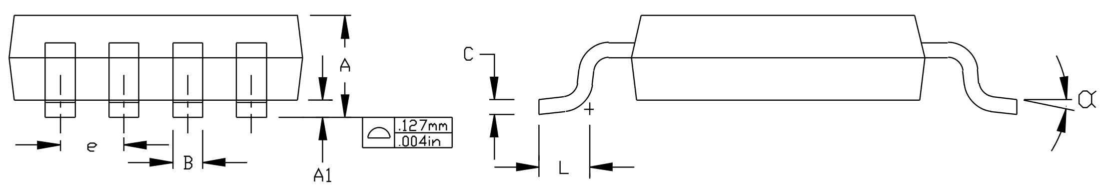
TRANSISTOR COUNT: 824

Package Information

8LUMAXD.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°



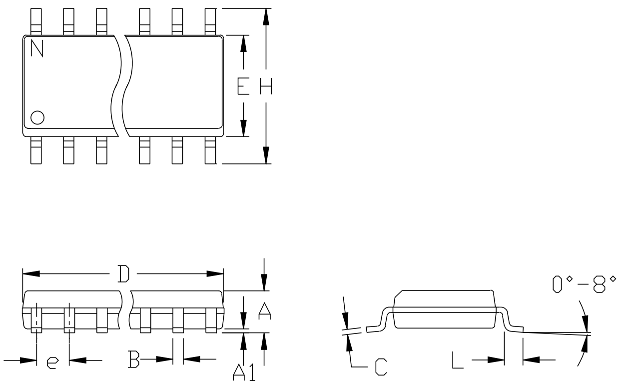
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
8LD uMAX PACKAGE OUTLINE DWG.

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	D	1/1

Package Information (continued)

SOICN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0041 REV: A