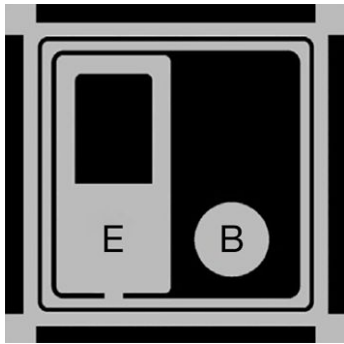


Silicon NPN Phototransistor



FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 0.52 x 0.52 x 0.185
- High photo sensitivity
- Radiant sensitive area: 0.14 mm²
- High radiant sensitivity
- Suitable for visible and near infrared radiation
- Fast response times
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

T1090P6 is a silicon NPN phototransistor chip with high radiant sensitivity, sensitive to visible and near infrared radiation.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY

COMPONENT	I _{ca} (μA)	φ (deg)	λ _{0.5} (nm)
T1090P6	65 to 750	± 60	620 to 1000

Note

- Test condition see table “Basic Characteristics”

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T1090P6-SD-F	wafer sawn on foil with disco frame	MOQ: 250 000 pcs	chip

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V _{CEO}	80	V
Emitter collector voltage		V _{ECO}	7.8	V
Collector current		I _C	50	mA
Junction temperature		T _j	125	°C
Operating temperature range		T _{amb}	-55 to +125	°C
Storage temperature range		T _{stg1}	-55 to +150	°C
Storage temperature range on foil		T _{stg2}	-40 to +50	°C

BASIC CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Collector emitter breakdown voltage	I _C = 10 μA, E = 0	V _{(BR)CEO}	80			V
Collector emitter dark current	V _{CE} = 50 V, E = 0	I _{CEO}		1	50	nA
Collector light current (Vishay selection type (1))	E _e = 1 mW/cm ² , λ = 950 nm, V _{CE} = 5 V	I _{ca}	65		750	μA
Wavelength of peak sensitivity		λ _p		840		nm
Range of spectral bandwidth		λ _{0.5}		620 to 1000		nm
Rise time	V _{CE} = 5 V, I _C = 2 mA, R _L = 100 Ω	t _r		4.3		μs
Fall time	V _{CE} = 5 V, I _C = 2 mA, R _L = 100 Ω	t _f		7.7		μs

Notes

- The measurements are based on samples of die which are mounted on a TO18-header without resin coating
- (1) Specific selection types possible

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

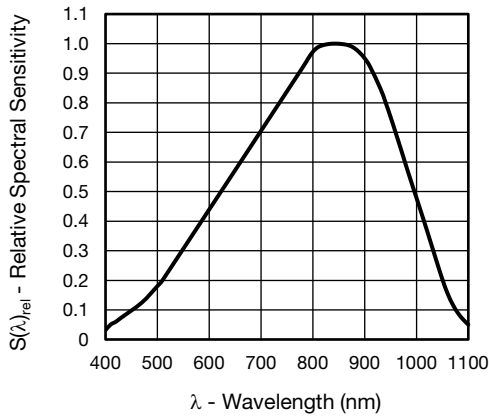


Fig. 1 - Relative Spectral Sensitivity vs. Wavelength

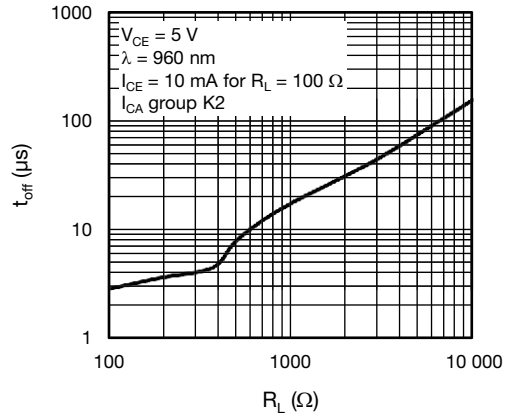


Fig. 3 - Turn-Off Time vs. Load Resistance

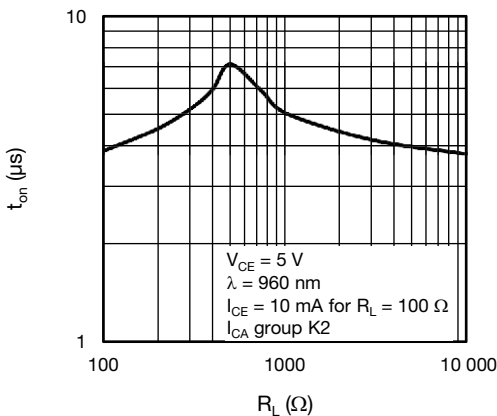


Fig. 2 - Turn-On Time vs. Load Resistance

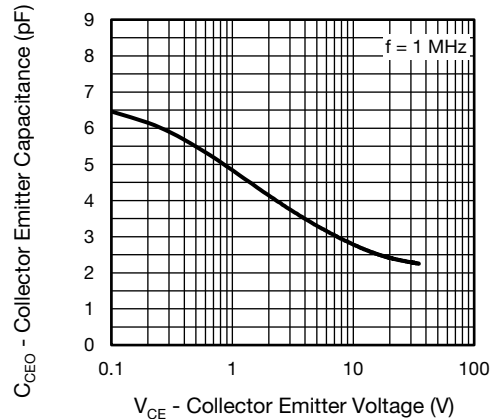
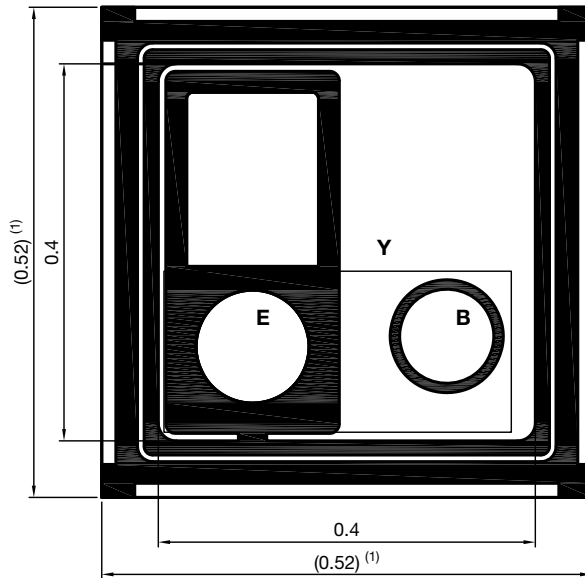


Fig. 4 - Collector Emitter Capacitance vs. Collector Emitter Voltage

DIMENSIONS in millimeters


Orientation of wafer flat



technical drawings according to DIN specifications

E: Emitter

B: Base

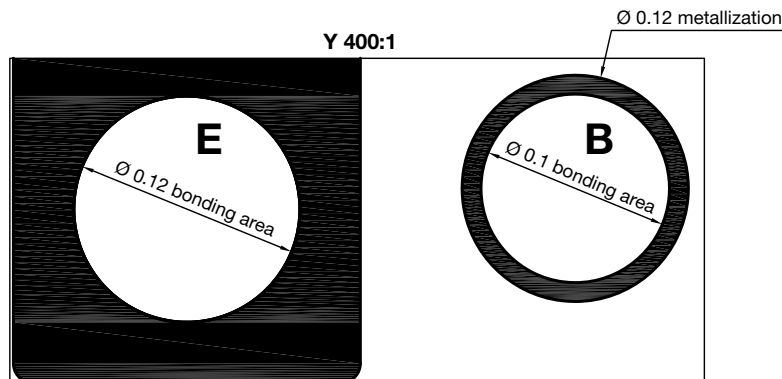
 Opt. active area: 0.135 mm²

Bonding area: E: Ø 120 µm

B: Ø 100 µm

Bonding restricted to this area in order to avoid damage of adjacent structures

Thickness: 185 µm ± 15 µm



Drawing-No.: 9.000-5078.3-4

Issue: 3; 03.05.2011

Notes

- Not indicated tolerances: ± 0.005

⁽¹⁾ Only for information: dimension of sawn die under consideration of 30 µm saw kerf

MECHANICAL DIMENSIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	L _x		0.52		mm
Length of chip edge (y-direction)	L _y		0.52		mm
Sensitive area	A _s		0.14		mm ²
Wafer diameter	D		150		mm
Die height	H	0.170	0.185	0.200	mm
Bond pad diameter emitter	d		0.120		mm
Bond pad diameter base	d		0.100		mm



ADDITIONAL INFORMATION	
Frontside metallization, base (B), emitter (E)	AlSi 1.2 μm
Backside metallization, collector	AuSb 1.2 μm
Dicing	Sawing
Die bonding technology	Epoxy bonding

Note

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870. The visual inspection shall be made in accordance with the “specification of visual inspection as referenced”. The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification. The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.



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