XS1-G04B-FB144 Datasheet

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1 Features

- **Quad-Tile Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  - Up to 1600 MIPS shared between up to 32 real-time logical cores
  - Each logical core has:
    - Guaranteed throughput of between 1/4 and 1/8 of tile MIPS
    - 16x32bit dedicated registers
  - 159 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- **Programmable I/O**
  - 88 general-purpose I/O pins, configurable as input or output
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 128 channel ends for communication with other cores, on or off-chip
- **Memory**
  - 256KB internal single-cycle SRAM (max 64KB per tile) for code and data storage
  - 32KB internal OTP (max 8KB per tile) for application boot code
- **JTAG Module for On-Chip Debug**
- **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- **Ambient Temperature Range**
  - Commercial qualification: 0 °C to 70 °C
  - Industrial qualification: -40 °C to 85 °C
- **Speed Grade**
  - 400 MHz part: 400 MIPS
- **144-pin FBGA package 0.8 mm pitch**

2 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12
A	IO VDD	X0D34	X0D35	X0D36	X0D37	X0D38	X0D39	X0D40	X0D41	X0D42	X0D43	VSS
B	X0D33	VSS	X0D18	X0D19	X0D20	IO VDD	VSS	X0D21	X0D22	X0D23	IO VDD	X2D24
C	X0D32	X0D17	VDD	X0D06	X0D07	X0D08	X0D09	X0D10	X0D11	VDD	X2D12	X2D25
D	X0D31	X0D16	X0D05	SS_PLL_BYPASS	SS_RESET	VDD	OTP_VPP	SS_XC0_BS[0]	SS_XC_CFG[0]	X2D00	X2D13	X2D26
E	X0D30	X0D15	X0D04	SS_CLK	VSS	VSS	VSS	VSS	SS_DEBUG	X2D01	X2D14	X2D27
F	X0D29	IO VDD	X0D03	SS_PLL_AGND	VSS	VSS	VSS	VSS	VDD	X2D02	VSS	X2D28
G	X0D28	VSS	X0D02	VDD	VSS	VSS	VSS	VSS	SS_TEST_ENA	X2D03	IO VDD	X2D29
H	X0D27	X0D14	X0D01	SS_PLL_AVDD	VSS	VSS	VSS	VSS	SS_TCK	X2D04	X2D15	X2D30
J	X0D26	X0D13	X0D00	SS_PLL_LOCK	SS_TMS	SS_TDO	VDD	SS_TDI	SS_TRST	X2D05	X2D16	X2D31
K	X0D25	X0D12	VDD	X2D11	X2D10	X2D09	X2D08	X2D07	X2D06	VDD	X2D17	X2D32
L	X0D24	IO VDD	X2D23	X2D22	X2D21	VSS	IO VDD	X2D20	X2D19	X2D18	VSS	X2D33
M	VSS	X2D43	X2D42	X2D41	X2D40	X2D39	X2D38	X2D37	X2D36	X2D35	X2D34	IO VDD

3 Signal Description

Module	Signal	Function	Type	Active	Properties
	PU=Pull Up, PD=Pull Down, ST=Schmitt Trigger Input, OT=Output Tristate, S=Switchable R_S=Required for SPI boot (§5.6), R_U=Required for USB-enabled devices (§10)				
Power	VDD	Digital tile power	PWR	—	
	VSS	Digital ground	GND	—	
	IO VDD	Digital I/O power	PWR	—	
	SS_PLL_AGND	Analog ground for PLL	GND	—	
	SS_PLL_AVDD	Analog PLL power	PWR	—	
	OTP_VPP	OTP programming voltage	PWR	—	
	SS_RESET	Global reset input	Input	—	PU, ST
PLL	SS_CLK	PLL reference clock	Input	—	PD, ST
	SS_PLL_BYPASS	PLL bypass	Input	—	PD
	SS_XC0_BS[0:0]	Boot status (tile 0)	I/O	—	PU
JTAG	SS_TDI	Test data input	Input	—	PU, ST
	SS_TDO	Test data output	Output	—	PD
	SS_TMS	Test mode select	Input	—	PU, ST
	SS_TRST	Test reset input	Input	—	PU, ST
	SS_TCK	Test clock	Input	—	PU, ST
	SS_DEBUG	Multi-chip debug	I/O	—	PU
Tile 0 I/O	X0D00	$P1A^0$	I/O	—	R_S
	X0D01	$X0LA^{4i}_{5b}$ $P1B^0$	I/O	—	R_S
	X0D02	$X0LA^{3i}_{5b}$ $P4A^0$ $P8A^0$ $P16A^0$ $P32A^{20}$	I/O	—	R_U
	X0D03	$X0LA^{2i}_{5b}$ $P4A^1$ $P8A^1$ $P16A^1$ $P32A^{21}$	I/O	—	R_U
	X0D04	$X0LA^{1i}_{2b/5b}$ $P4B^0$ $P8A^2$ $P16A^2$ $P32A^{22}$	I/O	—	R_U
	X0D05	$X0LA^{0i}_{2b/5b}$ $P4B^1$ $P8A^3$ $P16A^3$ $P32A^{23}$	I/O	—	R_U
	X0D06	$X0LA^{0o}_{2b/5b}$ $P4B^2$ $P8A^4$ $P16A^4$ $P32A^{24}$	I/O	—	R_U
	X0D07	$X0LA^{1o}_{2b/5b}$ $P4B^3$ $P8A^5$ $P16A^5$ $P32A^{25}$	I/O	—	R_U
	X0D08	$X0LA^{2o}_{5b}$ $P4A^2$ $P8A^6$ $P16A^6$ $P32A^{26}$	I/O	—	R_U
	X0D09	$X0LA^{3o}_{5b}$ $P4A^3$ $P8A^7$ $P16A^7$ $P32A^{27}$	I/O	—	R_U
	X0D10	$X0LA^{4o}_{5b}$ $P1C^0$	I/O	—	R_S
	X0D11	$P1D^0$	I/O	—	R_S
	X0D12	$P1E^0$	I/O	—	R_U
	X0D13	$X0LB^{4i}_{5b}$ $P1F^0$	I/O	—	R_U
	X0D14	$X0LB^{3i}_{5b}$ $P4C^0$ $P8B^0$ $P16A^8$ $P32A^{28}$	I/O	—	R_U
	X0D15	$X0LB^{2i}_{5b}$ $P4C^1$ $P8B^1$ $P16A^9$ $P32A^{29}$	I/O	—	R_U
	X0D16	$X0LB^{1i}_{2b/5b}$ $P4D^0$ $P8B^2$ $P16A^{10}$	I/O	—	R_U
	X0D17	$X0LB^{0i}_{2b/5b}$ $P4D^1$ $P8B^3$ $P16A^{11}$	I/O	—	R_U
	X0D18	$X0LB^{0o}_{2b/5b}$ $P4D^2$ $P8B^4$ $P16A^{12}$	I/O	—	R_U
	X0D19	$X0LB^{1o}_{2b/5b}$ $P4D^3$ $P8B^5$ $P16A^{13}$	I/O	—	R_U
	X0D20	$X0LB^{2o}_{5b}$ $P4C^2$ $P8B^6$ $P16A^{14}$ $P32A^{30}$	I/O	—	R_U
	X0D21	$X0LB^{3o}_{5b}$ $P4C^3$ $P8B^7$ $P16A^{15}$ $P32A^{31}$	I/O	—	R_U

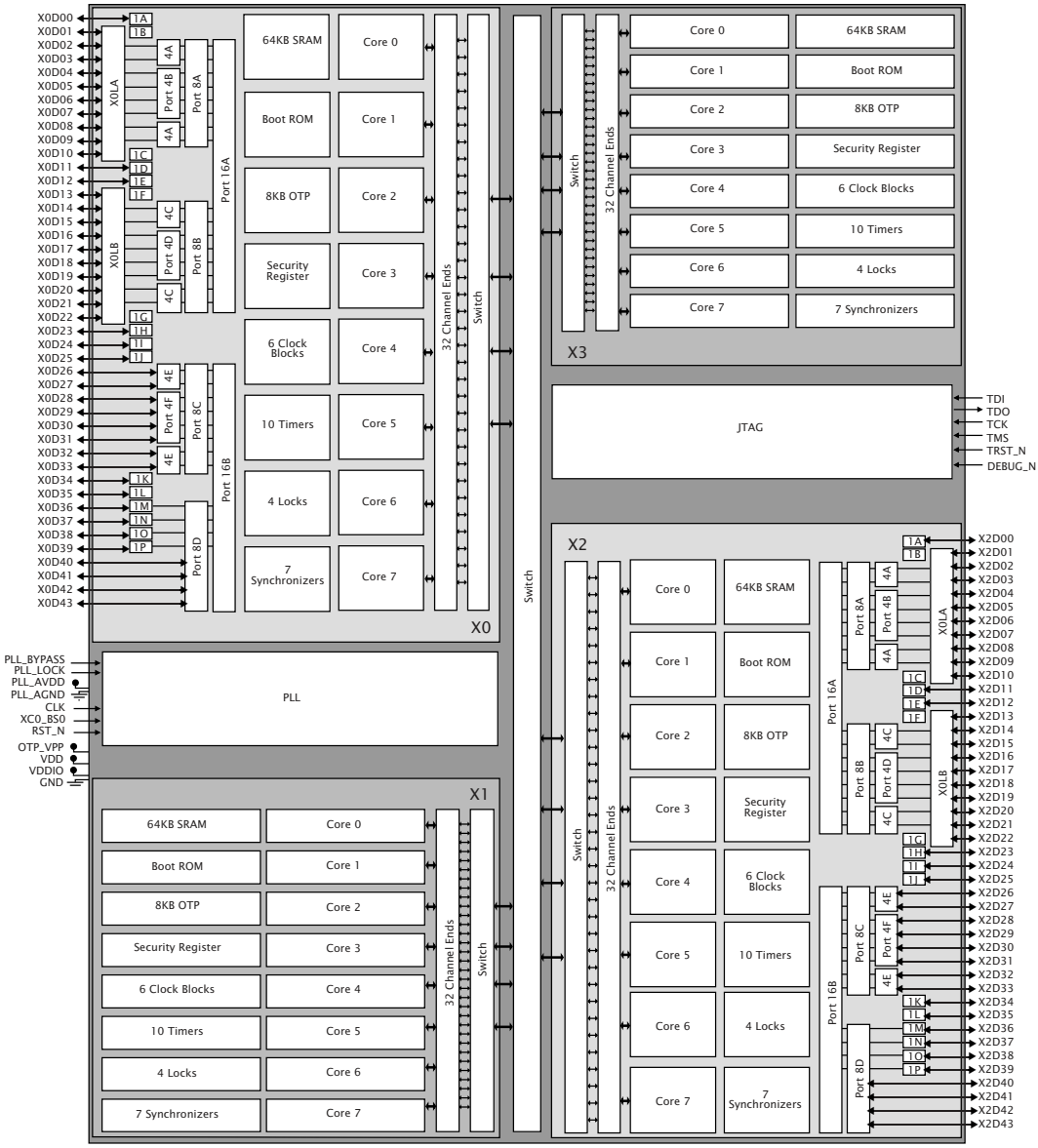
(continued)

Module	Name	Function	Type	Active	Properties
Tile 0 I/O	X0D22	X0LB$^{4o}_{5b}$ P1G^{0}	I/O	—	R_U
	X0D23	P1H^{0}	I/O	—	R_U
	X0D24	P1I^{0}	I/O	—	
	X0D25	P1J^{0}	I/O	—	
	X0D26	P4E^{0} P8C^{0} P16B^{0}	I/O	—	R_U
	X0D27	P4E^{1} P8C^{1} P16B^{1}	I/O	—	R_U
	X0D28	P4F^{0} P8C^{2} P16B^{2}	I/O	—	R_U
	X0D29	P4F^{1} P8C^{3} P16B^{3}	I/O	—	R_U
	X0D30	P4F^{2} P8C^{4} P16B^{4}	I/O	—	R_U
	X0D31	P4F^{3} P8C^{5} P16B^{5}	I/O	—	R_U
	X0D32	P4E^{2} P8C^{6} P16B^{6}	I/O	—	R_U
	X0D33	P4E^{3} P8C^{7} P16B^{7}	I/O	—	R_U
	X0D34	P1K^{0}	I/O	—	
	X0D35	P1L^{0}	I/O	—	
	X0D36	P1M^{0} P8D^{0} P16B^{8}	I/O	—	
	X0D37	P1N^{0} P8D^{1} P16B^{9}	I/O	—	R_U
	X0D38	P1O^{0} P8D^{2} P16B^{10}	I/O	—	R_U
	X0D39	P1P^{0} P8D^{3} P16B^{11}	I/O	—	R_U
	X0D40	P8D^{4} P16B^{12}	I/O	—	R_U
	X0D41	P8D^{5} P16B^{13}	I/O	—	R_U
	X0D42	P8D^{6} P16B^{14}	I/O	—	R_U
	X0D43	P8D^{7} P16B^{15}	I/O	—	R_U
Tile 2 I/O	X2D00	P1A^{0}	I/O	—	
	X2D01	X2LA$^{4i}_{5b}$ P1B^{0}	I/O	—	
	X2D02	X2LA$^{3i}_{5b}$ P4A^{0} P8A^{0} P16A^{0} P32A^{20}	I/O	—	R_U
	X2D03	X2LA$^{2i}_{5b}$ P4A^{1} P8A^{1} P16A^{1} P32A^{21}	I/O	—	R_U
	X2D04	X2LA$^{1i}_{2b/5b}$ P4B^{0} P8A^{2} P16A^{2} P32A^{22}	I/O	—	R_U
	X2D05	X2LA$^{0i}_{2b/5b}$ P4B^{1} P8A^{3} P16A^{3} P32A^{23}	I/O	—	R_U
	X2D06	X2LA$^{0o}_{2b/5b}$ P4B^{2} P8A^{4} P16A^{4} P32A^{24}	I/O	—	R_U
	X2D07	X2LA$^{1o}_{2b/5b}$ P4B^{3} P8A^{5} P16A^{5} P32A^{25}	I/O	—	R_U
	X2D08	X2LA$^{2o}_{5b}$ P4A^{2} P8A^{6} P16A^{6} P32A^{26}	I/O	—	R_U
	X2D09	X2LA$^{3o}_{5b}$ P4A^{3} P8A^{7} P16A^{7} P32A^{27}	I/O	—	R_U
	X2D10	X2LA$^{4o}_{5b}$ P1C^{0}	I/O	—	
	X2D11	P1D^{0}	I/O	—	
	X2D12	P1E^{0}	I/O	—	R_U
	X2D13	X2LB$^{4i}_{5b}$ P1F^{0}	I/O	—	R_U
	X2D14	X2LB$^{3i}_{5b}$ P4C^{0} P8B^{0} P16A^{8} P32A^{28}	I/O	—	R_U
	X2D15	X2LB$^{2i}_{5b}$ P4C^{1} P8B^{1} P16A^{9} P32A^{29}	I/O	—	R_U
	X2D16	X2LB$^{1i}_{2b/5b}$ P4D^{0} P8B^{2} P16A^{10}	I/O	—	R_U
	X2D17	X2LB$^{0i}_{2b/5b}$ P4D^{1} P8B^{3} P16A^{11}	I/O	—	R_U
	X2D18	X2LB$^{0o}_{2b/5b}$ P4D^{2} P8B^{4} P16A^{12}	I/O	—	R_U
	X2D19	X2LB$^{1o}_{2b/5b}$ P4D^{3} P8B^{5} P16A^{13}	I/O	—	R_U
	X2D20	X2LB$^{2o}_{5b}$ P4C^{2} P8B^{6} P16A^{14} P32A^{30}	I/O	—	R_U

(continued)

Module	Name	Function	Type	Active	Properties
Tile 2 I/O	X2D21	$X2LB^{3o}_{5b}$ $P4C^{3}$ $P8B^{7}$ $P16A^{15}$ $P32A^{31}$	I/O	—	R_U
	X2D22	$X2LB^{4o}_{5b}$ $P1G^{0}$	I/O	—	R_U
	X2D23	$P1H^{0}$	I/O	—	R_U
	X2D24	$P1I^{0}$	I/O	—	
	X2D25	$P1J^{0}$	I/O	—	
	X2D26	$P4E^{0}$ $P8C^{0}$ $P16B^{0}$	I/O	—	R_U
	X2D27	$P4E^{1}$ $P8C^{1}$ $P16B^{1}$	I/O	—	R_U
	X2D28	$P4F^{0}$ $P8C^{2}$ $P16B^{2}$	I/O	—	R_U
	X2D29	$P4F^{1}$ $P8C^{3}$ $P16B^{3}$	I/O	—	R_U
	X2D30	$P4F^{2}$ $P8C^{4}$ $P16B^{4}$	I/O	—	R_U
	X2D31	$P4F^{3}$ $P8C^{5}$ $P16B^{5}$	I/O	—	R_U
	X2D32	$P4E^{2}$ $P8C^{6}$ $P16B^{6}$	I/O	—	R_U
	X2D33	$P4E^{3}$ $P8C^{7}$ $P16B^{7}$	I/O	—	R_U
	X2D34	$P1K^{0}$	I/O	—	
	X2D35	$P1L^{0}$	I/O	—	
	X2D36	$P1M^{0}$ $P8D^{0}$ $P16B^{8}$	I/O	—	
	X2D37	$P1N^{0}$ $P8D^{1}$ $P16B^{9}$	I/O	—	R_U
	X2D38	$P1O^{0}$ $P8D^{2}$ $P16B^{10}$	I/O	—	R_U
	X2D39	$P1P^{0}$ $P8D^{3}$ $P16B^{11}$	I/O	—	R_U
	X2D40	$P8D^{4}$ $P16B^{12}$	I/O	—	R_U
	X2D41	$P8D^{5}$ $P16B^{13}$	I/O	—	R_U
	X2D42	$P8D^{6}$ $P16B^{14}$	I/O	—	R_U
	X2D43	$P8D^{7}$ $P16B^{15}$	I/O	—	R_U
Reserved	SS_PLL_LOCK	Reserved (do not connect)	Output	—	PD
	SS_TEST_ENA	Reserved (tie to VSS)	Input	—	PD
	SS_XC_CFG[0:0]	Reserved (tie to VSS)	Input	—	PD

4 Block Diagram



5 Product Overview

The XMOS XS1-G04B-FB144 is a powerful device that provides a simple design process and highly-flexible solution to many applications. The device consists of four xCORE Tiles, each comprising a flexible multicore microcontroller with tightly integrated I/O and on-chip memory. The processors run mutiple tasks simultaneously using logical cores, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. Logical cores use channels to exchange data within a tile or across tiles. The tiles are connected via an integrated switch network, which uses a proprietary physical layer protocol, and which can also be used to add additional resources to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

The device can be configured using a set of software components that are rapidly customized and composed. XMOS provides source code libraries for many standard components. The device can be programmed using high-level languages such as C/C++ and XMOS-originated extensions to C, called XC, that simplify the control over concurrency, I/O and time.

The XMOS toolchain includes compilers, a simulator, debugger and static timing analyzer. The combination of real-time software, a compiler and timing analyzer enables the programmer to close timings on components of the design without a detailed understanding of the hardware characteristics.

5.1 Logical cores, Synchronizers and Locks

Each xCORE Tile has up to eight active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for n cores). Figure 1 shows the guaranteed core performance depending on the number of cores used.

Figure 1: Core performance

Speed Grade	Minimum MIPS per core (for *n* cores)							
	1	2	3	4	5	6	7	8
400 MHz	100	100	100	100	80	67	57	50

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum.

5.2 Channel Ends, Links and Switch

Logical cores communicate using point-to-point connections formed between two channel ends. Between tiles, channel communications are implemented over

xConnect Links and routed through switches. The links operate in either 2bit/direction or 5bit/direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link. A total of eight 5bit links are available between every pair of cores.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-G Link Performance and Design Guide, X7561.

5.3 Ports and Clock Blocks

Ports provide an interface between the logical cores and I/O pins. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The operation of each port is synchronized to a clock block. A clock block can be connected to an external clock input, or it can be run from the divided reference clock. A clock block can also output its signal to a pin. On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

The ports and links are multiplexed, allowing the pins to be configured for use by ports of different widths or links. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

5.4 Timers

Timers are 32-bit counters that are relative to the xCORE Tile reference clock. A timer is defined to tick every 10 ns. This value is derived from the reference clock, which is configured to tick at 100 MHz by default.

5.5 PLL

The PLL is used to generate all on-chip clocks. SS_CLK is the reference clock input. It should be supplied with a clock with monotonic rising edges and should be stable before SS_RESET is taken high.

Many standard clock frequencies can be used with appropriate settings configured into the PLL. At boot time, before the PLL can be reconfigured, the PLL multiplier is set using the pins specified in the table in Figure 2. The PLL increases the clock frequency to the tile frequency used to run the processor data path and the switch.

Further details on configuring the clock can be found in the XS1-G Clock Frequency Control document, X3221.

Figure 2: PLL boot modes

SS_PLL_BYPASS	PLL Multiplier	SS_CLK Input (MHz)	Boot Frequency (MHz)
0	20	12.5–20	250–400
1	0.5	<100	<50

5.6 Boot ROM

The boot procedure is illustrated in Figure 3. If bit 5 of the security register is set (*see* §5.7.1), the device boots from OTP. Otherwise, SS_XC0_BS[0] controls the boot source.

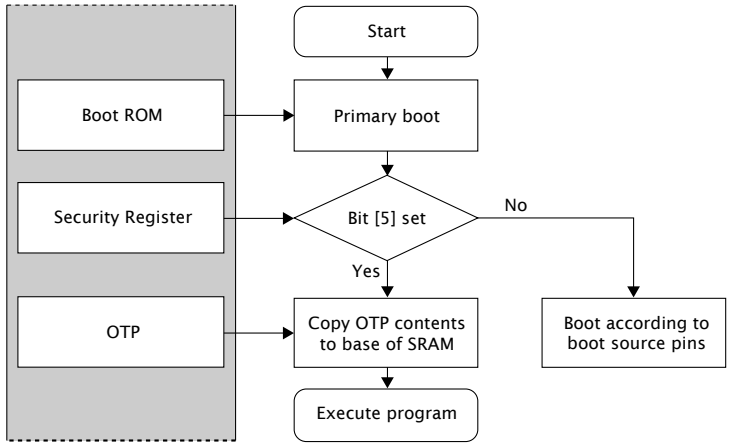


Figure 3: Boot procedure

SS_XC0_BS[0] operates as an input prior to the de-assertion of SS_RESET. The device latches the value driven onto these pins on the rising edge (de-assertion) of SS_RESET. The value driven should be static and configured using a pullup or pulldown resistor, as the device drives the boot status on this pin after reset. The value configured on this pin defines the boot mode, as described in Figure 4.

SS_XC0_BS[0]	Boot Mode		
0	Boot from SPI		
	Pin[A]	Signal	Description
	X0D00	MISO	Master In Slave Out
	X0D01	SS	Slave Select
	X0D10	SCLK	Clock
	X0D11	MOSI	Master Out Slave In
1	None: Device waits to be booted from JTAG		

Figure 4: Boot source pins

A The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. An SPI boot program can be burned into OTP and used at any time.

After reset is complete, SS_XC0_BS[0] becomes an output and indicates the boot mode, as described in Figure 5.

Figure 5: Boot mode indication pins

SS_XC0_BS[0]	Boot Confirmation
0	Booted from SPI
1	Booted from OTP or JTAG

5.7 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in 2k rows x 32-bit configuration which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

5.7.1 Security Register

The security register enables the following security features:

- **Secure Boot**: The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (*see* §5.6). This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.
- **Disable JTAG**: The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
- **Disable Link access**: Other tiles are forbidden access to the processor state via the system switch.

  Disabling both JTAG and Link access transforms an xCORE Tile into a “secure island” with other tiles free for non-secure user application code.
- **Disable Global Debug access**: Disables access to the SS_DEBUG pin.
- **OTP Master and Sector Lock**: Further access to the OTP is prevented by setting the master lock. Locks can also be applied to each of the four OTP sectors individually.

These security features provide a strong level of protection and are sufficient for providing strong IP security.

5.8 SRAM

Each xCORE Tile integrates a single 64 KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or

32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

5.9 JTAG

The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory.

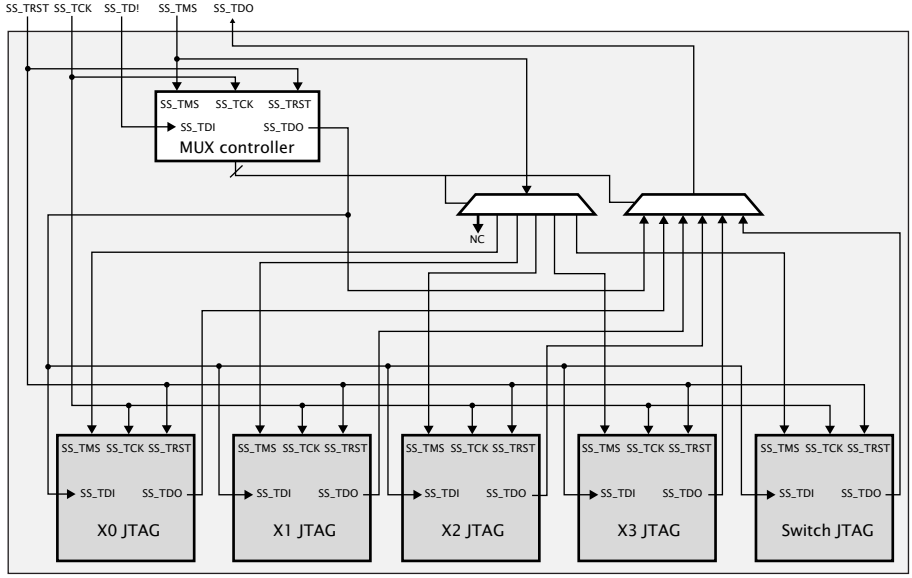


Figure 6: JTAG chain structure

The JTAG chain structure is illustrated in Figure 6. Directly after reset, two TAP controllers are present in the JTAG chain for each xCORE Tile: the boundary scan TAP and the chip TAP. The boundary scan TAP is a standard 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. The chip TAP provides access into the xCORE Tile, switch and OTP for loading code and debugging.

The SS_TRST pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the SS_TRST pin can be tied to ground to hold the JTAG module in reset.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 7.

Figure 7: IDCODE return value

Bit31				Device Identification Register																								Bit0
Version				Part Number																Manufacturer Identity								1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	1	1
0				0				1				0				4				6				3				3

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 8. The OTP User ID field is read from bits [22:31] of the security register on xCORE Tile 0 (all zero on unprogrammed devices).

Figure 8: USERCODE return value

Bit31										Usercode Register																				Bit0
OTP User ID										Unused				Silicon Revision																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8				0				0						

5.10 Power Supplies

The device has the following types of power supply pins:

- VDD pins for the xCORE Tile tile
- IO VDD pins for the I/O lines
- SS_PLL_AVDD pins for the PLL
- OTP_VPP pins for faster programming the OTP (optional)

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The IO VDD supply must ramp to its final value before VDD reaches 0.4 V.

The SS_PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 Ω resistor and 1 µF multi-layer ceramic capacitor) is recommended on this pin.

The SS_OTP_VPP supply can be optionally provided for faster OTP programming times, otherwise an internal charge pump is used.

The following ground pins are provided:

- PLL_AGND for PLL_AVDD
- GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and IO VDD supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

SS_RESET is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §5.6). SS_RESET and must be asserted low during and after power up for 100 ns.

6 DC and Switching Characteristics

6.1 Operating Conditions

Figure 9: Operating conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIO	I/O supply voltage	3.00	3.30	3.60	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	
OTP_VPP	OTP external programming voltage (optional program only)	6.18	6.50	6.83	V	
Cl	xCORE Tile I/O load capacitance			25	pF	
Ta	Ambient operating temperature (Commercial)	0		70	°C	
	Ambient operating temperature (Industrial)	-40		85	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

6.2 DC Characteristics

Figure 10: DC characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2.00		5.50	V	A, B
V(IL)	Input low voltage	-0.30		0.80	V	A, B
V(OH)	Output high voltage	2.40			V	A, B
V(OL)	Output low voltage			0.40	V	A, B
R(PU)	Pull-up resistance		100K		Ω	A, C

A All pins except power supply pins.

B Internal pull-up resistors are fitter to general-purpose I/O pins.

C Use for unused I/O only. The internal pull-up resistor is not recommended as a substitute for an external pull-up resistor.

6.3 ESD Stress Voltage

Figure 11: ESD stress voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model	-2.00		2.00	KV	
MM	Machine model	-200		200	V	

6.4 Reset Timing

Figure 12: Reset timing

Symbol	Parameters	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	100			ns	
T(PLLLOCK)	PLL lock			1	ms	
T(INIT)	Initialization time			<100	µs	A

A Shows the time taken to start booting after SS_RESET has gone high.

6.5 Quiescent Current

Figure 13: Quiescent current

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		120		mA	
I(PLLQ)	Quiescent PLL current		4		mA	

6.6 Power Consumption

Figure 14: xCORE Tile currents

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
PD	Tile power dissipation		1.6		Watts	A, B, C, D

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages operating at 400 MHz with nominal activity on all tiles.

C PD(TYP) value is the usage power consumption under typical operating conditions.

D PD(TYP) value includes quiescent current.

The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.

More detailed power analysis can be found in the XS1-G Power Consumption document, X7561.

6.7 Clock

Figure 15: Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	12.5	20	20	MHz	
SR	Slew rate	1		2	ns	
f(MAX)	Processor clock frequency			400	MHz	

Further details can be found in the XS1-G Clock Frequency Control document, X3221.

The OTP may be programmed using its internal charge pump or by supplying a 6.5V VPP programming voltage on the SS_OTP_VPP pin. Unless a programming cycle is underway the SS_OTP_VPP pins should be left undriven.

6.8 xCORE Tile I/O AC Characteristics

Figure 16: I/O AC characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

6.9 xConnect Link Performance

Figure 17: Link performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	A, B
B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	B
B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	B

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of SS_CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

6.10 JTAG Timing

Figure 18: JTAG timing

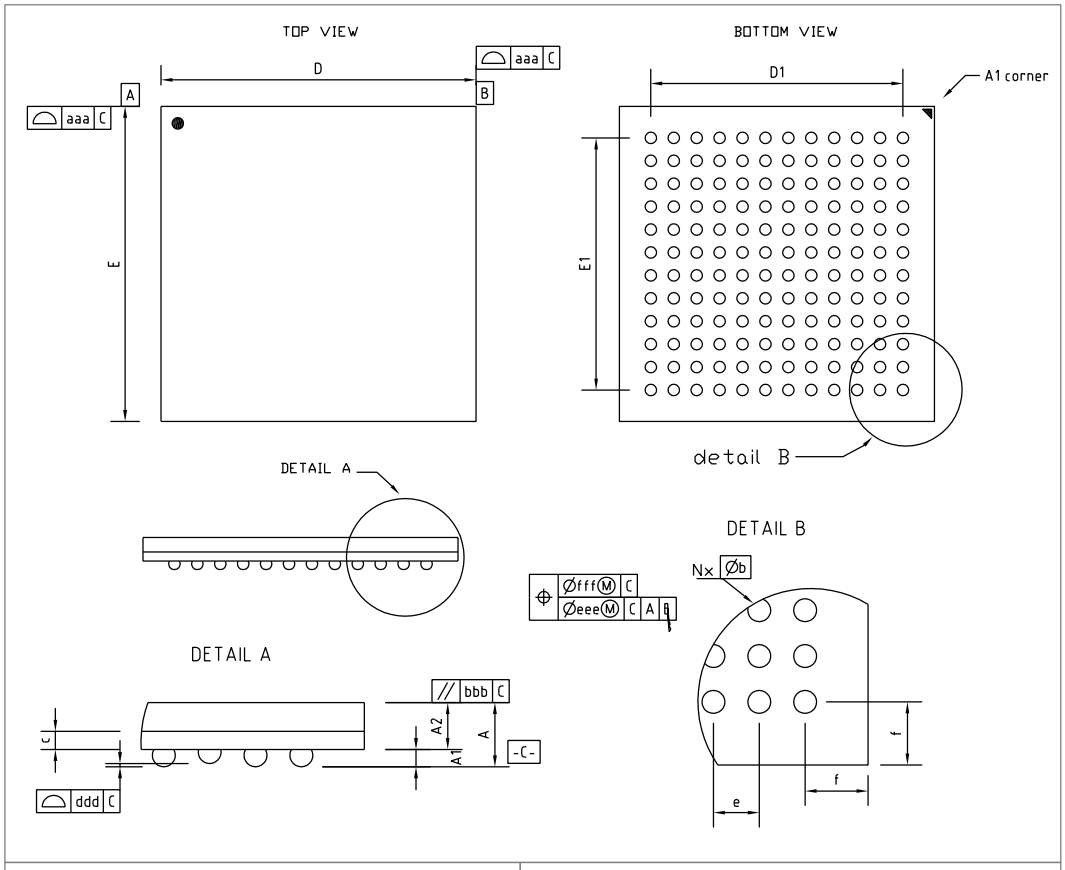
Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(TCK)	TCK period	30			ns	
T(SETUP)	TDO to TCK setup time	5			ns	A
T(HOLD)	TDO to TCK hold time			10	ns	A
T(DELAY)	TCK to output delay			15	ns	B

A Timing applies to SS_TMS, SS_TRST and SS_TDI inputs.

B Timing applies to SS_TDO output.

All JTAG operations are synchronous to SS_TCK apart from the global asynchronous reset SS_TRST.

7 Package Information



Dimensional Ref.			
REF	Min.	Nom	Max.
A			1.7
A1	0.21		
A2		1.06	
D		11.0	
D1		8.8	
E		11.0	
E1		8.8	
b		0.4	
c	0.32	0.36	0.40
e		0.8	
f		1.1	
m		12	
n		144	

Dimensional Tol.	
aaa	0.15
bbb	0.20
ddd	0.10
eee	0.15
fff	0.08

Notes
1. All dimensions in MM
2. 'e' represents the basic solder ball pitch
3. 'm' represents the basic solder ball matrix size. And 'n' is the number of attached solder balls
4. 'b' is measurable at the maximum solder ball diameter parallel the the primary datum -C-
5. Dimension 'aaa' is measured parallel to primary datum -C-
6. Primary datum -C- and the seating plane are defined by the spherical crowns of the solder balls
7. The package surface shall be matte finish charmilles 24 to 27
8. The over package thickness 'A' already considers collapse balls
11. Reference Jedec Design Guide 4.5 and MO-275

7.1 Part Marking

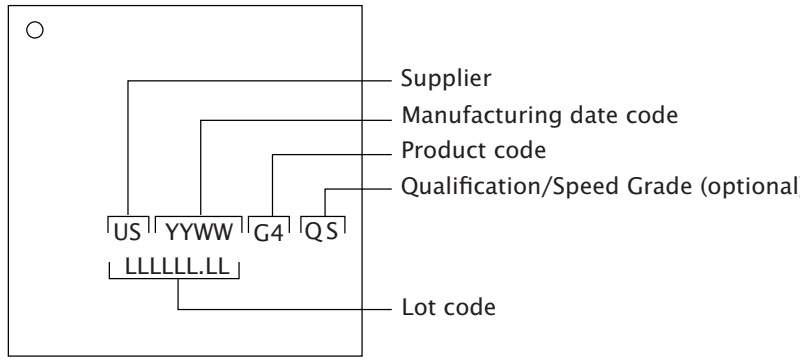


Figure 19: Part marking scheme

8 Ordering Information

Figure 20: Orderable part numbers

Product Code	Qualification	Speed Grade
XS1-G04B-FB144-C4	Commercial	400 MHz
XS1-G04B-FB144-I4	Industrial	400 MHz

9 Development Tools

XMOS provides a comprehensive suite of development tools. Source files, timing scripts and a board design file are input to the compiler toolchain which produces a binary executable. This executable file can be simulated, loaded onto the device and debugged over JTAG, programmed into flash memory on the board or written to OTP memory on the device. The tools can also encrypt the flash image and write the decrpytion key securely to OTP memory.

The tools can be driven from either a graphical development environment or the command line and are supported on Windows, Linux and MacOS X. The tools are available at no cost from xmos.com/downloads. Information on using the tools is provided in a separate user guide, X1013.

10 Addendum: XMOS USB Interface

XMOS provides a low-level USB interface for connecting the device to a USB transceiver using the UTMI+ Low Pin Interface (ULPI). The ULPI signals must be connected to the pins named in Figure 21. Note also that some ports on the same tile are used internally and are not available for use when the USB driver is active (they are available otherwise).

Pin	Signal
X*n*D02	Unavailable when USB active
X*n*D03	
X*n*D04	
X*n*D05	
X*n*D06	
X*n*D07	
X*n*D08	
X*n*D09	

Pin	Signal
X*n*D12	ULPI_STP
X*n*D13	ULPI_NXT
X*n*D14	ULPI_DATA[0]
X*n*D15	ULPI_DATA[1]
X*n*D16	ULPI_DATA[2]
X*n*D17	ULPI_DATA[3]
X*n*D18	ULPI_DATA[4]
X*n*D19	ULPI_DATA[5]
X*n*D20	ULPI_DATA[6]
X*n*D21	ULPI_DATA[7]
X*n*D22	ULPI_DIR
X*n*D23	ULPI_CLK

Pin	Signal
X*n*D26	Unavailable when USB active
X*n*D27	
X*n*D28	
X*n*D29	
X*n*D30	
X*n*D31	
X*n*D32	
X*n*D33	

X*n*D37	Unavailable when USB active
X*n*D38	
X*n*D39	
X*n*D40	
X*n*D41	
X*n*D42	
X*n*D43	

Figure 21: ULPI signals provided by the XMOS USB driver

11 Associated Design Documentation

Document Title	Information	Document Number
Device Package User Guide	Land pattern, solder paste, ground recommendations	X4979
Estimating Power Consumption For XS1-G Devices	Power consumption	X6037
Programming XC on XMOS Devices	Timers, ports, clocks, cores and channels	X9577
XMOS Tools User Guide	Compilers, assembler and linker/mapper Timing analyzer and debugger Flash and OTP programming utilities	X1013

- Example schematic diagrams detailing minimal system configurations are available from http://www.xmos.com/support/silicon.

12 Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	X7879
XS1 Port I/O Timing	Port timings	X5821
XS1-G System Specification	Link, switch and system information	X2725
XS1-G Link Performance and Design Guidelines	Link timings	X7561
XS1-G Clock Frequency Control	Advanced clock control	X3221

13 Revision History

The page numbers in this section refer to this document.

Rev. X1087H-10/12

1. Renamed XCore to xCORE Tile, and Thread to Core.
2. Instruction description updated - page 2.

Rev. X1087G-05/12-B

1. Block diagram updated: pins listed sequentially, 4-bit ports updated - page 7.

Rev. X1087F-05/12

1. SS_XC0_CFG and SS_PLL_BYPASS tied to VSS on page 4.
2. OTP section updated and moved before SRAM on page 11.

Rev. X1087E-03/12

1. Removed “Volatile” from Memory description on page 2.

Rev. X1087D-10/11

1. Updated “Part Marking” on page 19.

Rev. X1087C-05/11-B

1. Revised format.
2. Standard XMOS Link format XnLn on page 4.

Rev. X1087B-01/11

1. Replaced “Port Pin Table” with “Signal Description” on page 4.
2. Updated “ULPI” on page 19 with set of disabled signals.
3. Removed “Device Configuration”.
4. Added “Associated Design Documentation” on page 20.
5. Clock frequencies of betweeen 20 MHz and 25 MHz are **not** supported.
6. Removed documentation of numerous JTAG commands, which were incorrect.
7. Updated Figure 10 in “DC Characteristics” on page 15 by removing rows for I(OH) and I(OL).
8. Updated Figure 17 in “xConnect Link Performance’ on page 17 by removing rows for B(2link) and B(5link), and adding rows for B(2linkP), B(5linkP), B(2linkS) and B(5linkS).
9. Renamed IO VSS signals to VSS.

Rev. X1087A-06/10

1. Revised format.
2. Updated “Power Consumption” on page 16.