19-5172; Rev 0; 2/10

Microsemi

MAX3625B Evaluation Kit

Evaluates: MAX3625B

General Description

The MAX3625B evaluation kit (EV kit) is an assembled demonstration board that provides convenient evaluation of the MAX3625B low-jitter, precision clock generator. The EV kit includes an on-board 25MHz crystal to allow immediate testing.

The EV kit includes switches to allow easy selection of different modes of operation. The reference input and clock outputs use SMA connectors and are AC-coupled to simplify connection to test equipment.

Features

- **AC-Coupled I/Os for Ease of Testing**
- **Fully Assembled and Tested**
- **+3.3V Power-Supply Operation**
- **On-Board 25MHz Crystal**

Ordering Information

PART	TYPE
MAX3625BEVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C3, C4, C5, C7, C8, C11–C16, C18, C19	14	0.1µF ±10% ceramic capacitors (0402)
C2	1	10µF ±10% ceramic capacitor (0603)
C6, C17, C20	3	0.01µF ±10% ceramic capacitors (0402)
C9	1	33pF ±10% ceramic capacitor (0402)
C10	1	27pF ±10% ceramic capacitor (0402)
J1, J3, J5	0	Not installed
J2, J48	2	Test points
J4	1	2-pin header, 0.1in centers
J13–J16, J18, J19, J36	7	SMA connectors
L1	1	2.7µH inductor
R1–R4, R12, R13	6	150Ω ±5% resistors (0402)
R5, R6	0	Not installed
R7–R10, R14, R15, R16	7	49.9Ω ±1% resistors (0402)
R11	1	10.5Ω ±1% resistor (0402)
SW1, SW2, SW3, SW11	4	SP3T switches
SW6, SW8, SW9, SW12, SW13	5	SPDT switches
TP6, TP7	2	Test points
U1	1	Low-jitter, precision clock generator (24 TSSOP-EP*) Microsemi MAX3625BEUG+
Y1	1	25MHz crystal NDK EXS00A-AT00429
—	1	Shunt
—	1	PCB: MAX3625B EVALUATION BOARD+, REV A

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Component Supplier

SUPPLIER	PHONE	WEBSITE
NDK America	815-544-7900	www.ndk.com/en

Note: *Indicate that you are using the MAX3625B when contacting this component supplier.*

MAX3625B Evaluation Kit

Quick Start

To evaluate the MAX3625B, configure the EV kit as follows:

1) Determine which output is going to be evaluated and remove the 49.9Ω termination resistors located near the connectors. Then connect that output to the test equipment using SMA cables.
2) Connect a +3.3V power supply to J48 (VCC) and J2 (GND). Set the current limit to 200mA.
3) If the on-board crystal is used (IN_SEL set HIGH), the PLL divider should be set to divide by 25 (FB_SEL set LOW) to achieve the standard output rates shown in Table 3.
4) Use Table 3 to set the output divider switches to achieve the output frequency desired.
5) Enable the output under test by setting the related output-enable switch (Qx_OE) HIGH.

Table 1. Adjustment and Control Descriptions (see *Quick Start* first)

COMPONENT	NAME	FUNCTION
J4	INDUCTOR SHUNT	J4 shunts the power-supply inductor. Normal operation is J4 shunted.
SW1	SELB1	SW1 and SW2 set the output divider for the QB outputs. See Table 3 for more information.
SW2	SELB0	SW1 and SW2 set the output divider for the QB outputs. See Table 3 for more information.
SW3	SELA1	SW3 and SW11 set the output divider for the QA outputs. See Table 3 for more information.
SW6	$\overline{\text{BYPASS}}$	Set LOW to bypass the PLL. Set HIGH to engage the PLL. Note that when the PLL is bypassed the output dividers are automatically set to divide by 1.
SW8	FB_SEL	Sets the PLL divider. See Table 2 for more information.
SW9	QA_OE	Set HIGH to enable LVPECL output QA. Set LOW to force a logic zero at QA.
SW11	SELA0	SW3 and SW11 set the output divider for the QA outputs. See Table 3 for more information.
SW12	QB_OE	Set HIGH to enable the QB LVPECL outputs. Set LOW to force a logic zero at the QB outputs. See Table 3 for more information.
SW13	IN_SEL	Set HIGH to select the crystal as the frequency source. Set LOW to select the REF_IN as the frequency source.

Table 2. PLL Divider Settings

FB_SEL INPUT	PLL DIVIDER
HIGH	÷24
LOW	÷25

Table 3. Output Divider Settings

INPUT		NA/NB DIVIDER	OUTPUT FREQUENCY (MHz)
SELA1/ SELB1	SELA0/ SELB0		M = 25 AND XTAL = 25MHz
LOW	HIGH	÷2	312.5
HIGH	LOW	÷4	156.25
HIGH	HIGH	÷5	125
LOW	LOW	÷10	62.5

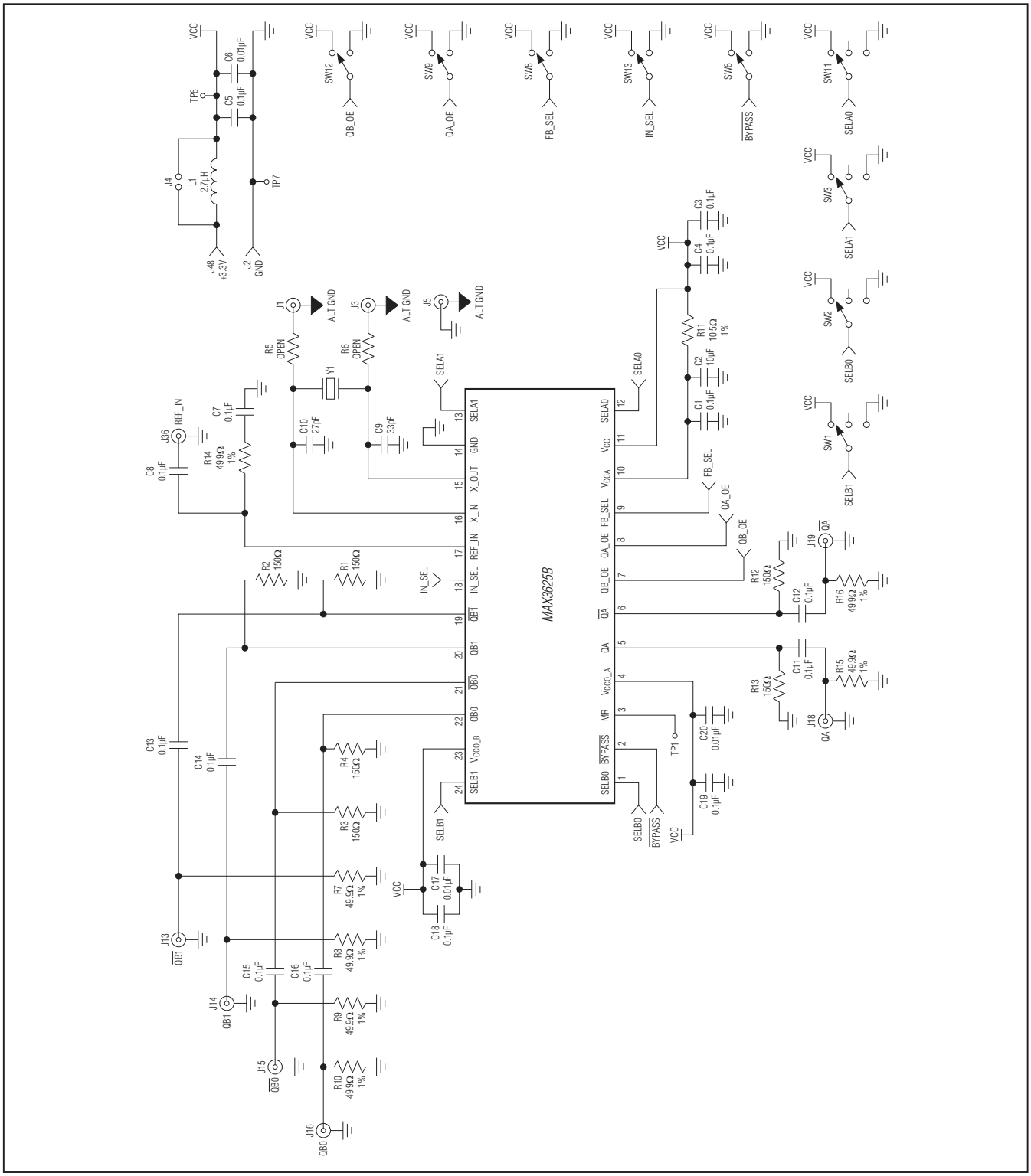


Figure 1. MAX3625B EV Kit Schematic

MAX3625B Evaluation Kit

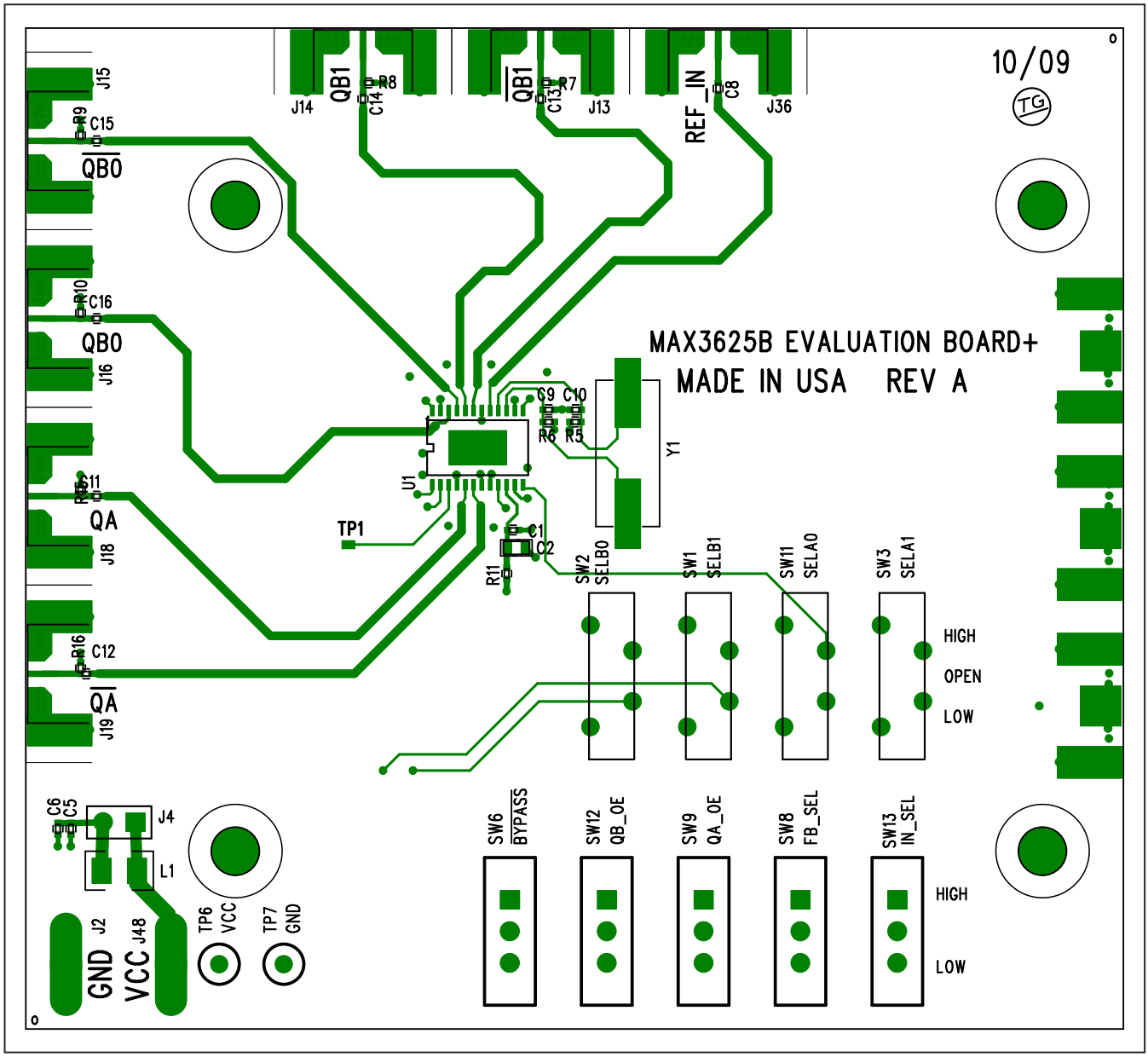


Figure 2. MAX3625B EV Kit Assembly Drawing—Top Side

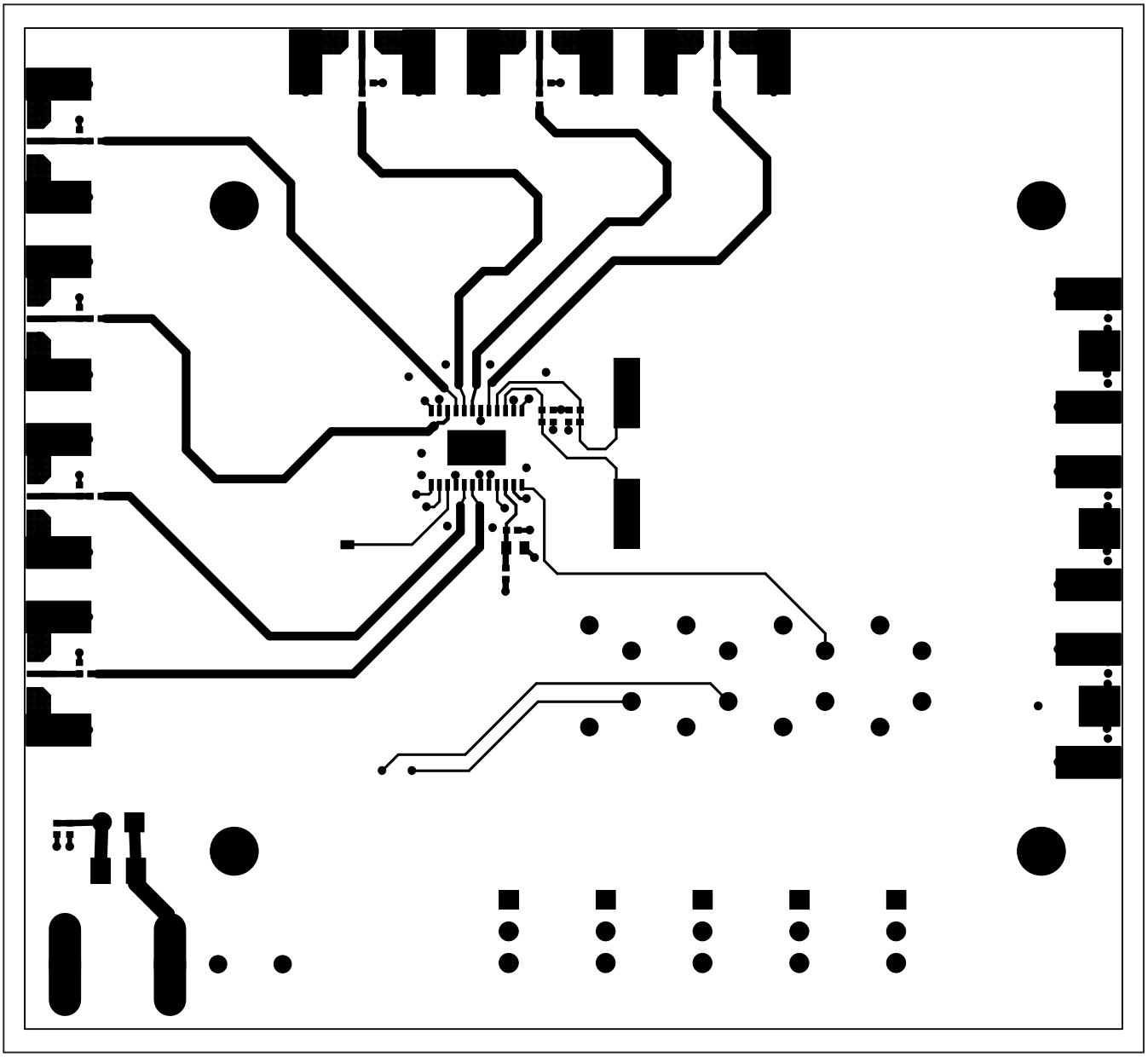


Figure 3. MAX3625B EV Kit Layout—Component Side

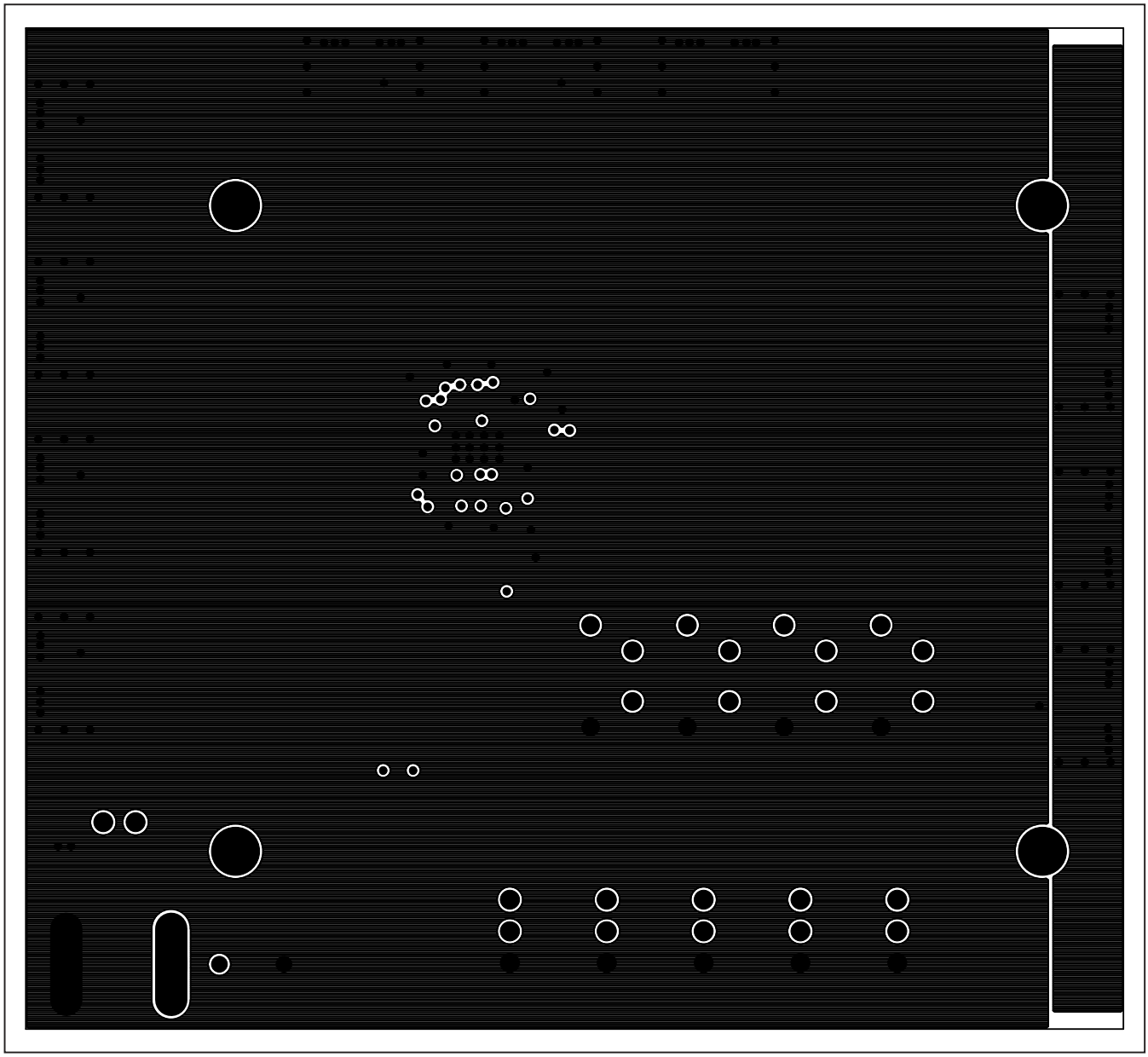


Figure 4. MAX3625B EV Kit Layout—Ground Plane

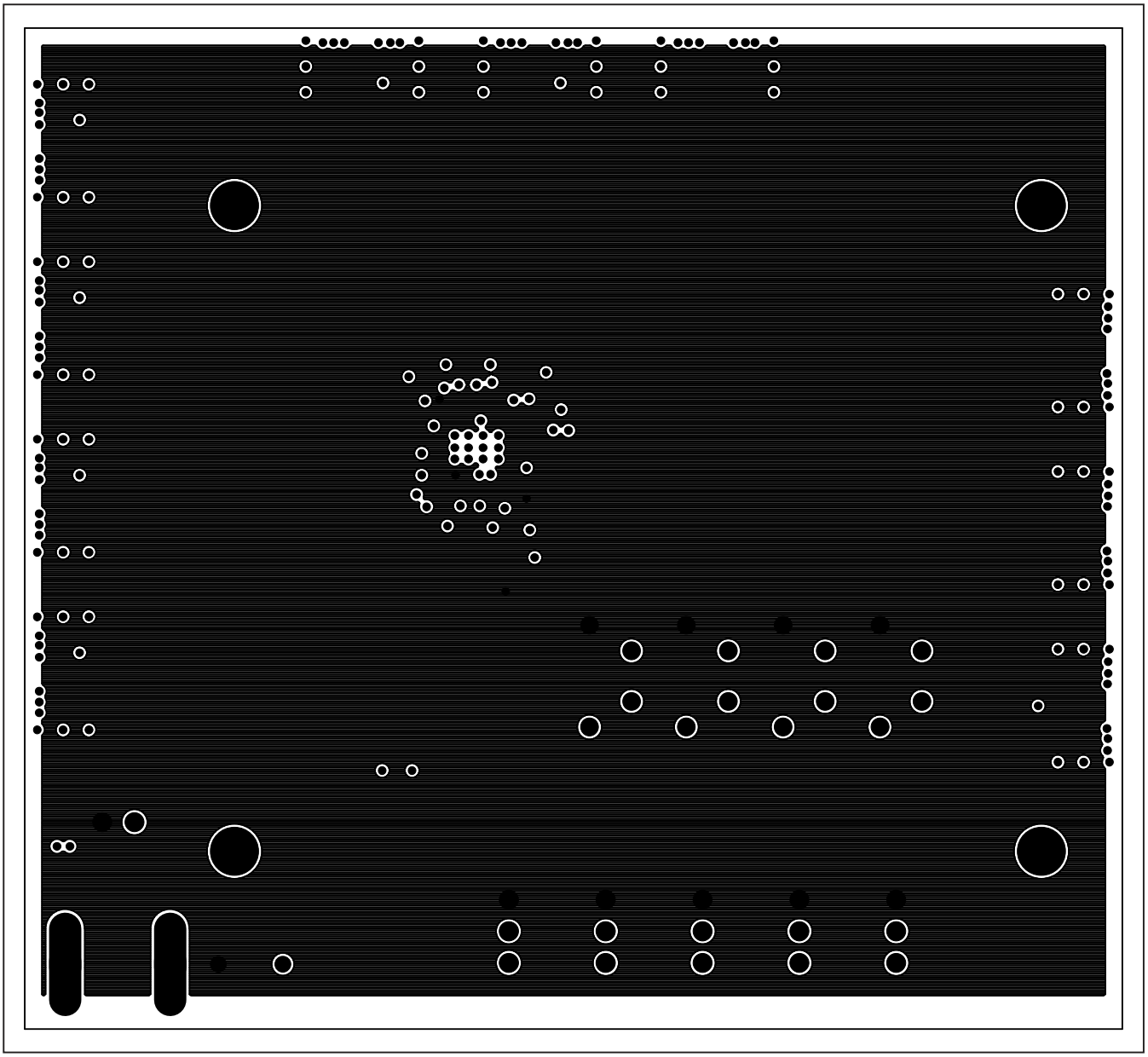


Figure 5. MAX3625B EV Kit Layout—Power Plane

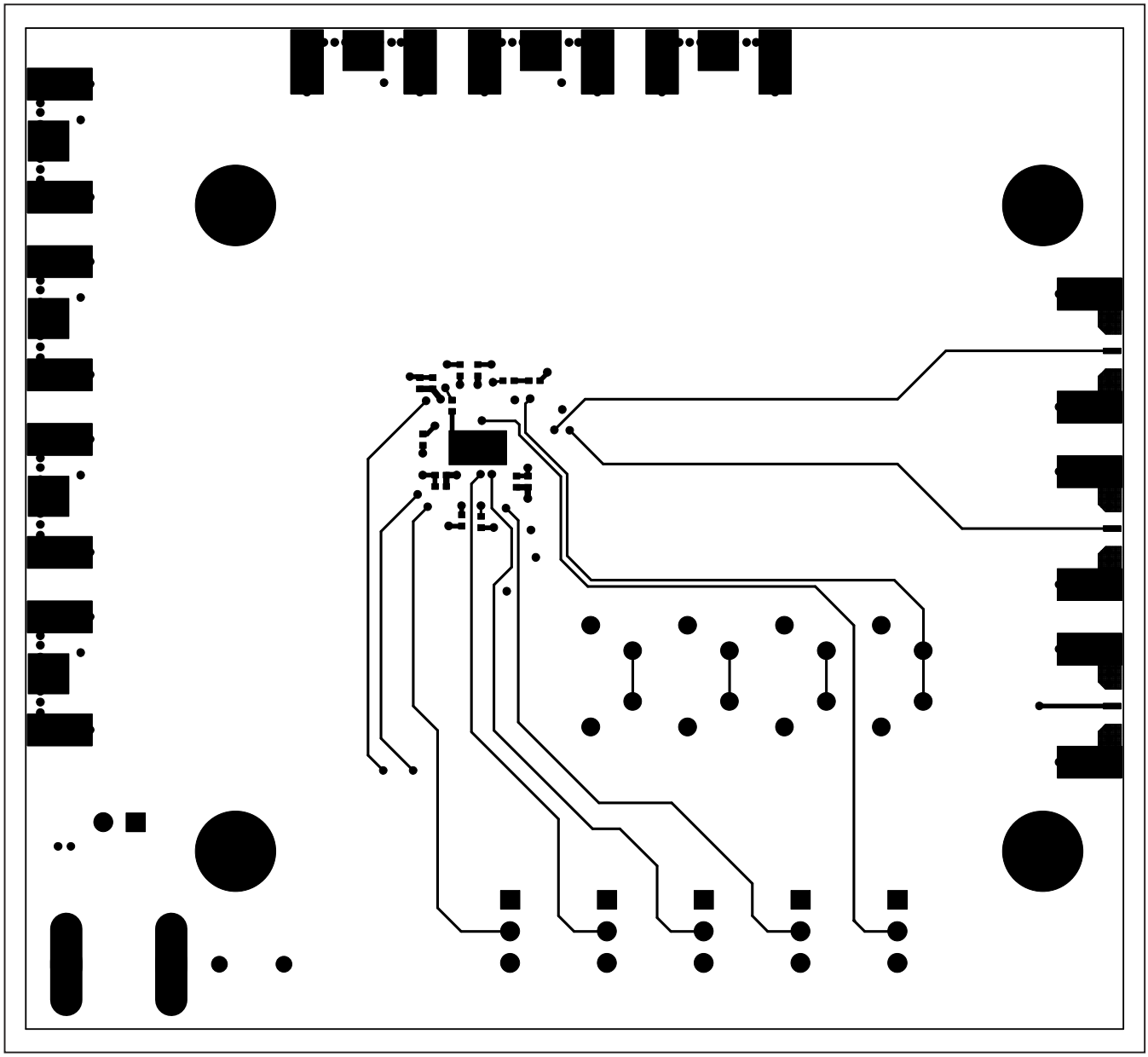


Figure 6. MAX3625B EV Kit Layout—Solder Side

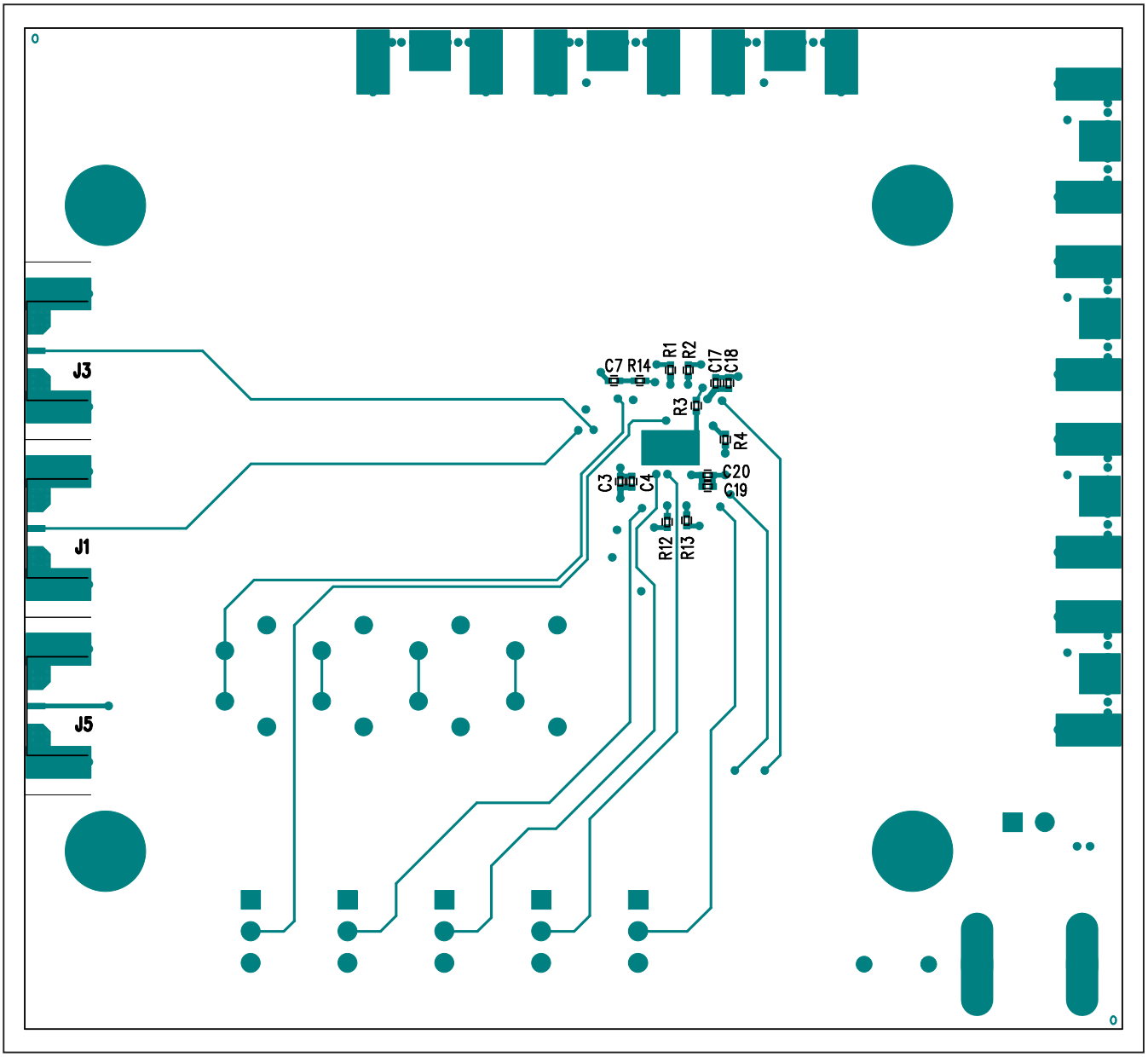
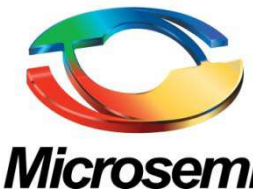


Figure 7. MAX3625B EV Kit Assembly Drawing—Bottom Side



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.