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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

## TFT Display Module

Part Number

E24RA-FW420-N

### Overview:

- 2.4-inch TFT (42.72x60.4 I I)
- 240x320 iXr1
- 3SPI & 3.5VDC. Lit | Lit
- ° 0T at Iix
- All View
- Transmissive
- No Touch Panel
- 420 NITS
- TFT IC: ST7789
- RoHS Compliant

## Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, and a backlight unit. The resolution of the 2.4" TFT-LCD contains 240(RGB)x320 pixels and can display up to 65k/262k colors.

## TFT Features

Low Input Voltage: 3.3V

Display Colors: 65k/262k

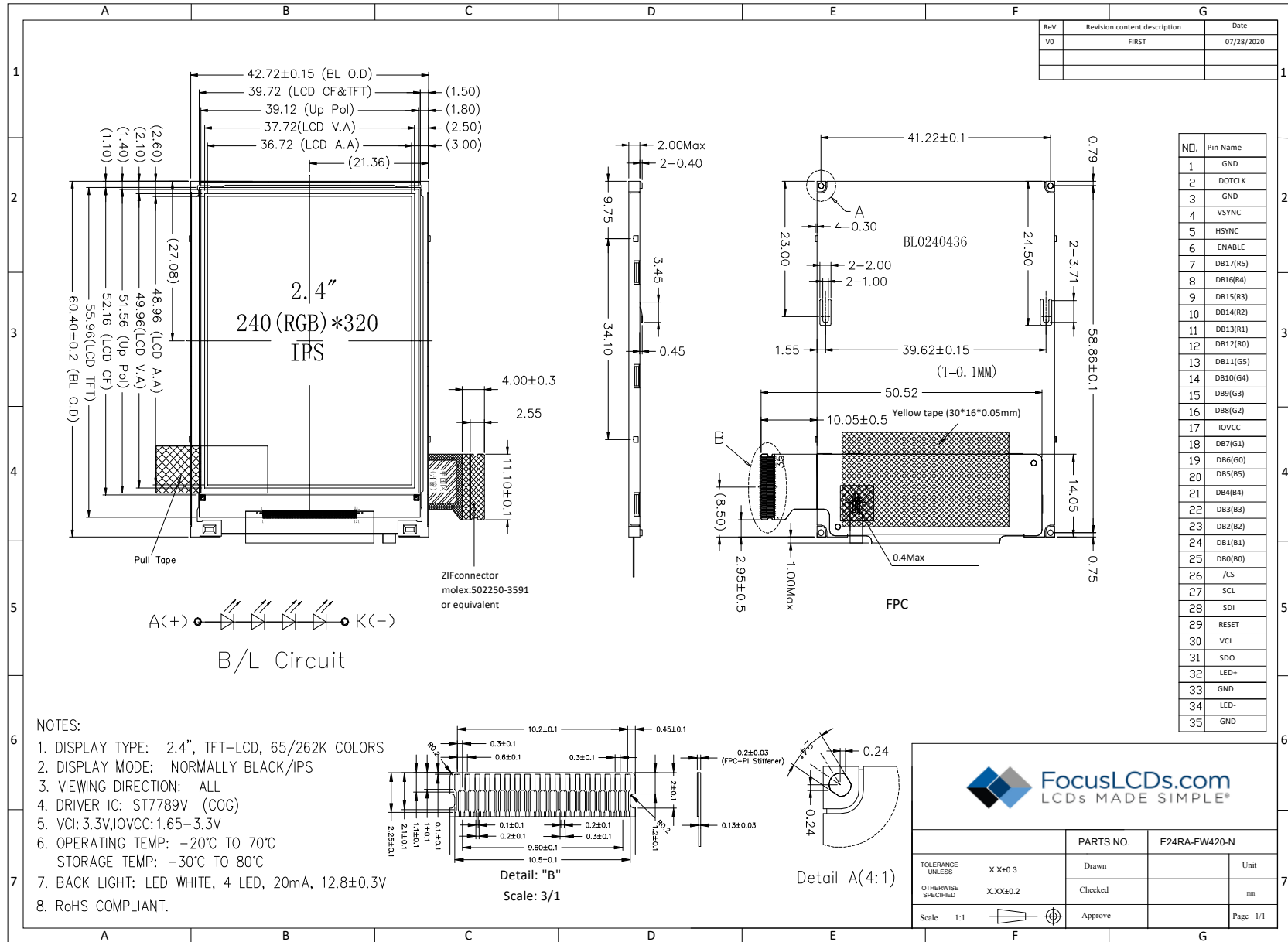
Interface: 3SPI+16/18-bit RGB

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	36.72 (H) x 48.96(V) (2.4 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	65k/262k	colors	-
Number of pixels	240(RGB)x320	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153 (H) x 0.153 (V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7789V	-	-
Interface	3 SPI + 16/18-bit RGB	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

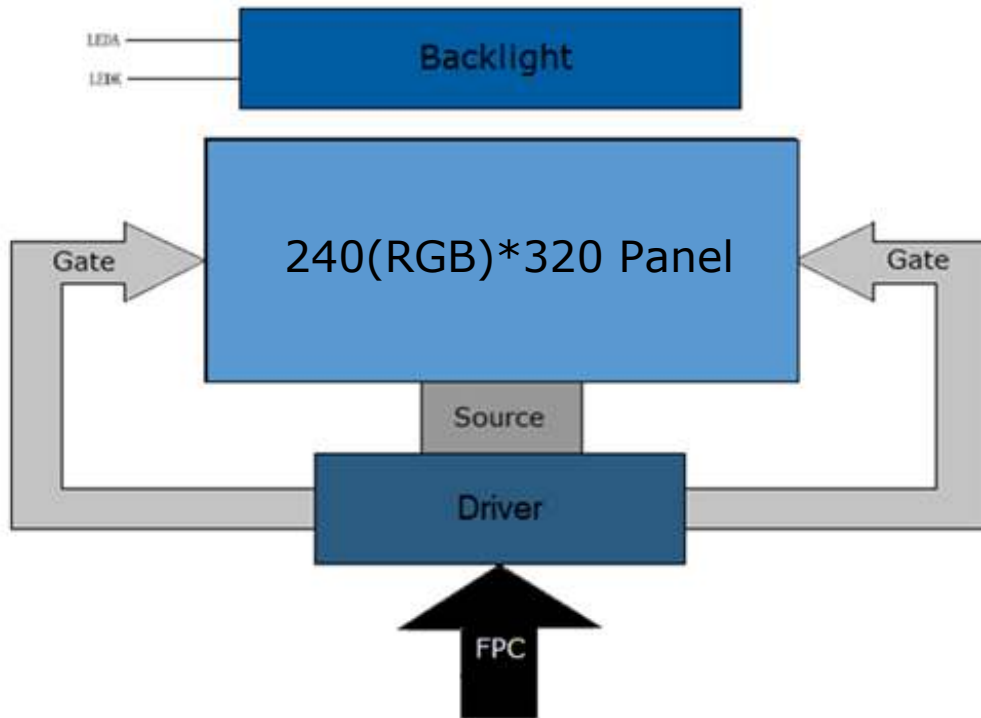
## Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Height (H)		42.72		mm	-
	Vertical (V)		60.40		mm	-
	Depth (D)		2.00		mm	-
	Weight		--		g	

# 1. Outline Dimensions



## 2. Block Diagram



### 3. Input Terminal Pin Assignment

Recommended Connector: FH26W-35S-0.3SHW(60)

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	DOTCLK	Dot clock signal for RGB interface. If not used, pin to IOVCC or GND.	I
3	GND	Ground	P
4	VSYNC	Vertical frame synchronizing signal for RGB interface. If not used, pin to IOVCC or GND.	I
5	HSYNC	Horizontal line synchronizing signal for RGB interface. If not used, pin to IOVCC or GND.	I
6	ENABLE	Data enable signal for RGB interface. If not used, pin to IOVCC or GND.	I
7-16	DB17-DB8	RGB interface data pins. For 16-bit interface, use DB17-DB13, DB11-DB1. For the 18-bit interface use pins DB17-DB0. If not used, pin to IOVCC or GND.	I/O
17	IOVCC	Supply voltage for IO. (1.65V-3.3V)	P
18-25	DB7-DB0	RGB interface data pins. If not used, pin to GND.	I/O
26	CS	Chip select pin for SPI interface. Low enabled.	I
27	SCL	Clock signal for SPI interface. If not used, pin to VCI or GND.	I
28	SDI	SPI interface data input pin. The data is latched on the rising edge of the SCL signal. If not used, pin to IOVCC or GND.	I
29	RESET	Reset signal of the device. Setting pin low initializes the chip. Must be reset after power is supplied.	I
30	VCI	Supply voltage (3.3V)	P
31	SDO	SPI interface data output pin. The data is output on the falling edge of the SCL signal. If not used, leave this pin open.	O
32	LEDA	Anode pin of the backlight	P
33	GND	Ground	P
34	LEDK	Cathode pin of the backlight	P
35	GND	Ground	P

*I: Input, O: Output, P: Power*

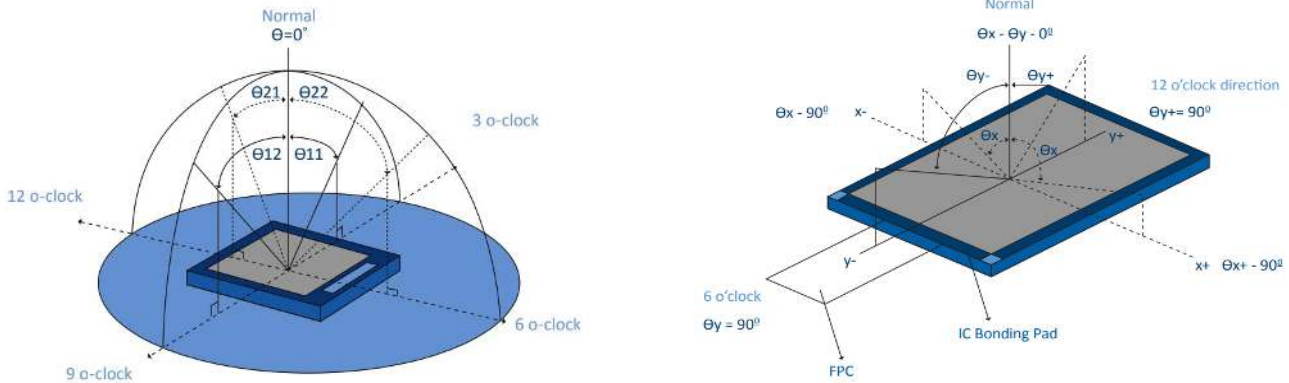
## 4. LCD Optical Characteristics

### 4.1 Optical Specifications

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note	
Color Gamut	S%		--	70	--	%	(3)	
Contrast Ratio	CR		640	800	--	%	(2)	
Response Time	Rising		TR+TF	--	35	45	ms	(4)
	Falling							
Color Filter Chromaticity	White	$W_x$	0.270	0.310	0.350		(5)(6)	
		$W_y$	0.291	0.331	0.371			
	Red	$R_x$	0.593	0.633	0.673			
		$R_y$	0.296	0.336	0.376			
	Green	$G_x$	0.282	0.322	0.362			
		$G_y$	0.565	0.605	0.645			
	Blue	$B_x$	0.106	0.146	0.186			
		$B_y$	0.008	0.048	0.088			
Viewing Angle	Hor.	$\Theta_L$	--	80	--	degree	(1)(6)	
		$\Theta_R$	--	80	--			
	Ver.	$\Theta_T$	--	80	--			
		$\Theta_B$	--	80	--			
Option View Direction	ALL						(1)	

**Optical Specification Reference Notes:**

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

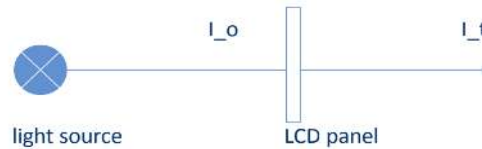


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

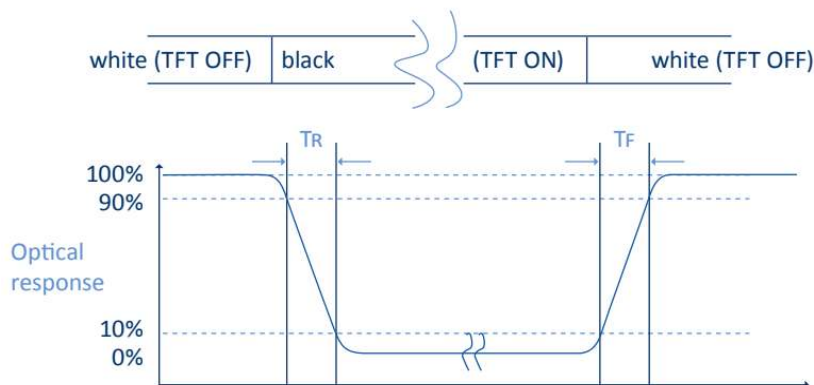
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} \times 100\%$$



Io = the brightness of the light source.  
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:

Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y), G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

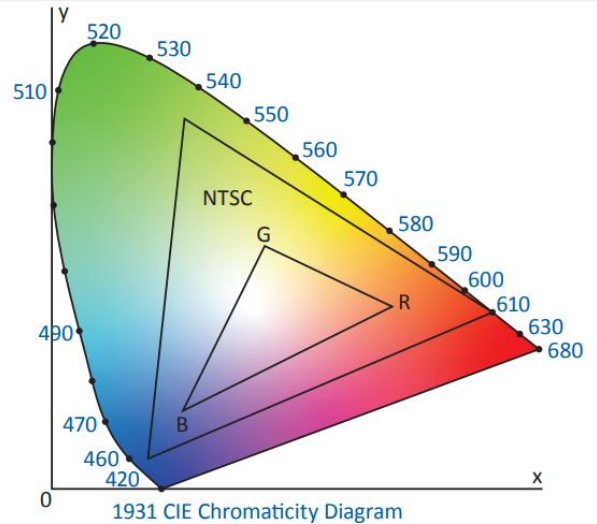
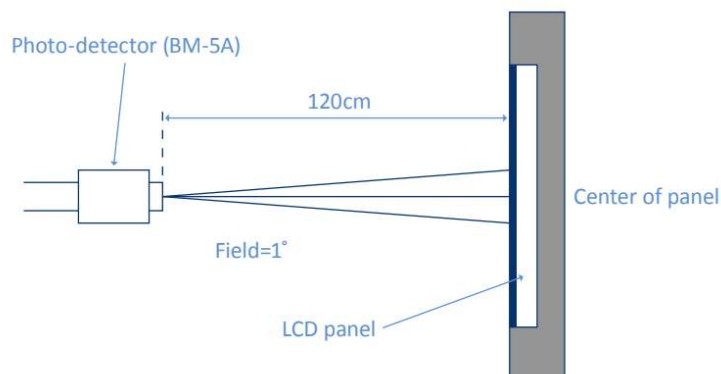
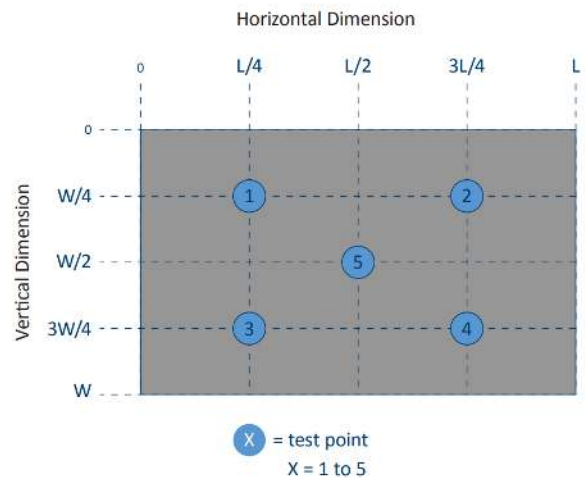
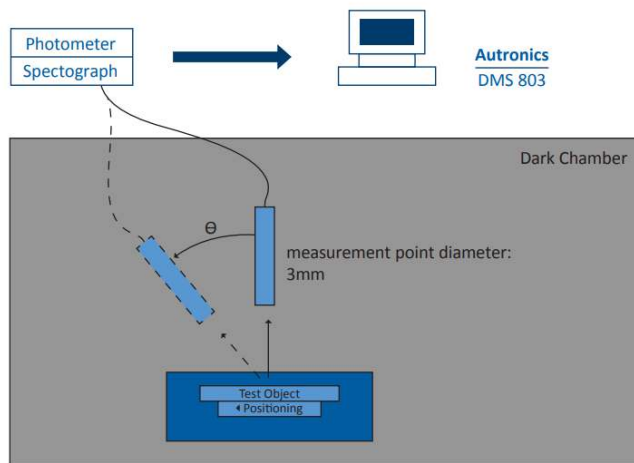


Fig. 1931 CIE chromacity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





## 5. TFT Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 °C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

*NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.*

### 5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.4	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current Consumption	IDD	--	8.5	--	mA	
Level Input Voltage	VIH	0.7IOVCC	--	IOVCC	V	
	VIL	GND	--	0.3IOVCC	V	
Level Output Voltage	VOH	0.8IOVCC	--	IOVCC	V	
	VOL	GND	--	0.2IOVCC	V	

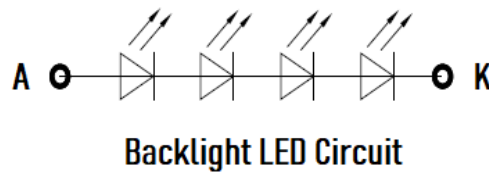
### 5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	15	20	--	mA	
Forward Voltage	VF	--	12.8	--	V	
LCM Luminance	LV	370	420	--	cd/m <sup>2</sup>	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

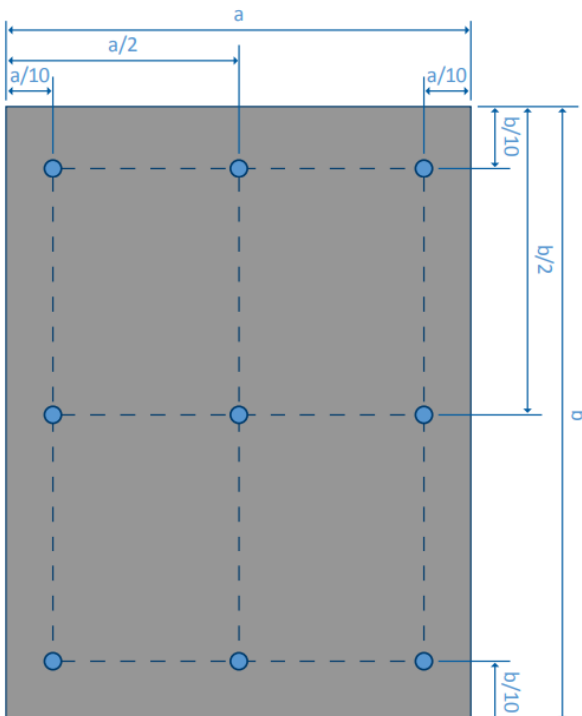
The back-light system is edge-lighting type with 4 white LEDs.

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a=25\pm 3^\circ\text{C}$ , typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at  $T_a=25^\circ\text{C}$  and  $I_L=20\text{mA}$ . The LED lifetime could be decreased if operating  $I_L$  is larger than 20mA. The constant current driving method is suggested.



Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

## 6. AC Characteristic

### 6.1 Parallel RGB Interface Characteristics

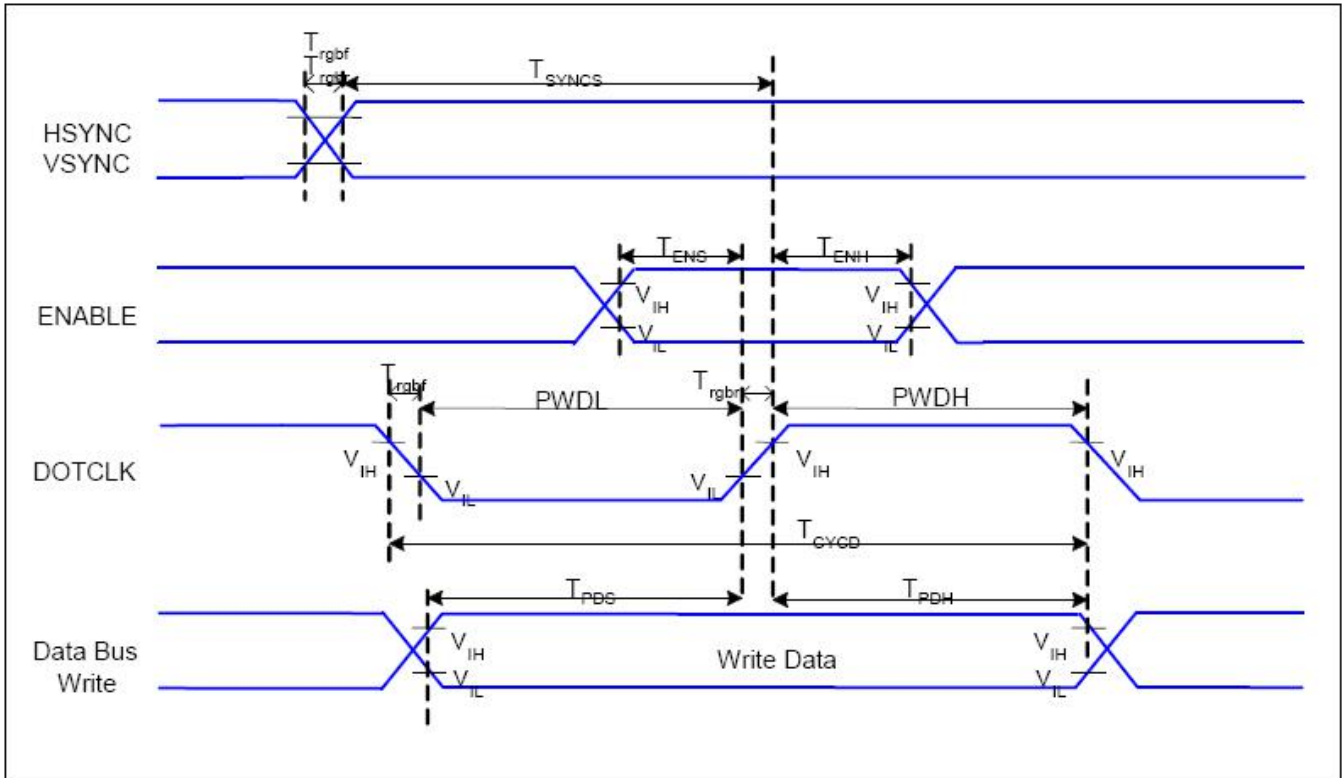


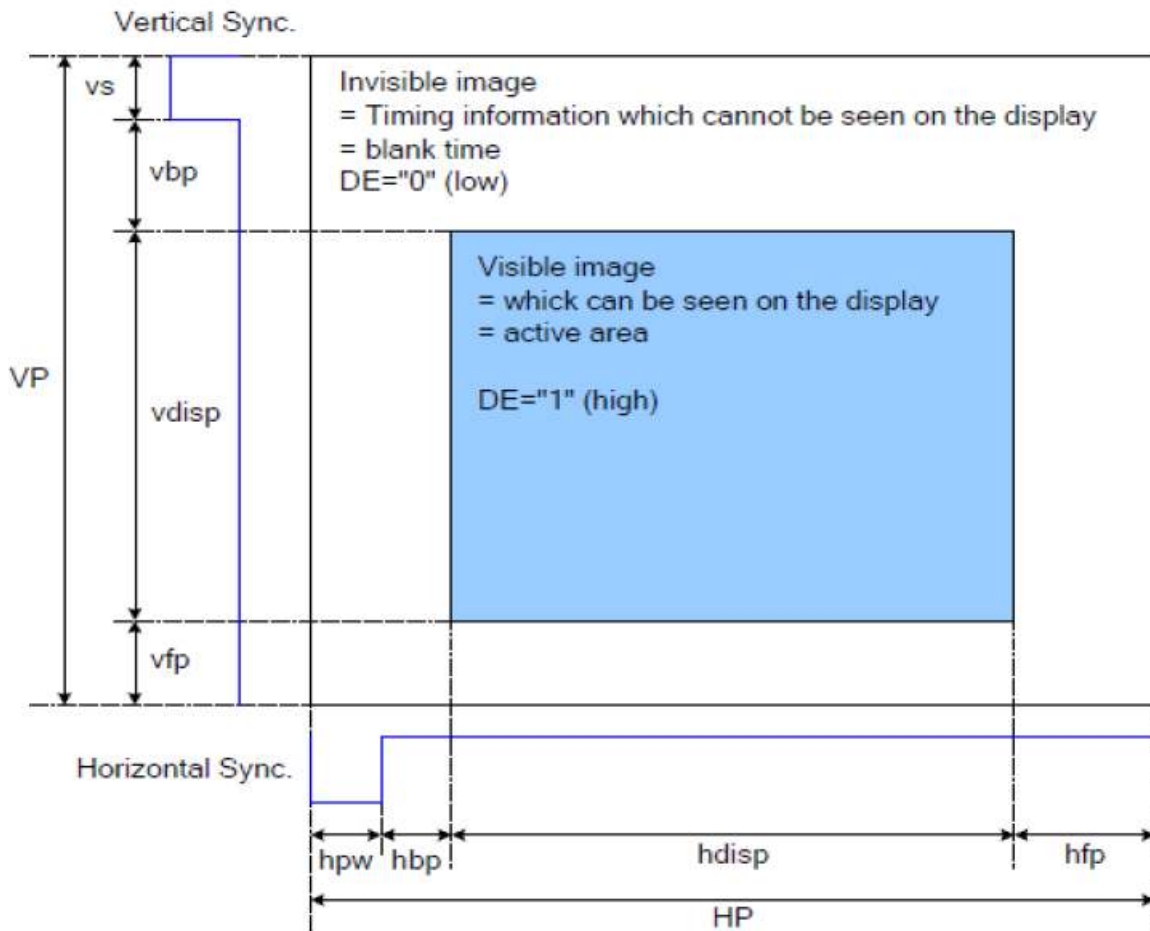
Figure 6.1: Parallel RGB Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	$T_{SYNCS}$	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	$T_{ENS}$	Enable Setup Time	25	-	ns	
	$T_{ENH}$	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	$T_{CYCD}$	DOTCLK Cycle Time	120	-	ns	
	$T_{RGHR}, T_{RGHF}$	DOTCLK Rise/Fall Time	-	20	ns	
DB	$T_{PDS}$	PD Data Setup Time	50	-	ns	
	$T_{PDH}$	PD Data Hold Time	50	-	ns	

Table 6.1: Parallel RGB Interface Timing Characteristics

## 6.2 Timing Tables

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC and DOTCLK signals. The data can be written only within the specified area with low power consumption by using the window address function. The back porch and front porch are used to set the RGB interface timing signals.



Parameter	Symbol	Min	Typ	Max	Unit
DCLK frequency	dclk	--	7	--	MHz
Horizontal sync width	hpw	2	10	hpw+hbp=31	Clock
Horizontal back porch	hbp	4	10		Clock
Horizontal front porch	hfp	2	38	--	Clock
Vertical sync width	vs	1	4	vs+vbp=127	Line
Vertical back porch	vbp	1	4		Line
Vertical front porch	vfp	1	8	--	Line

Table 6.2: RGB Interface Timing Table

## 6.2 Display Serial Interface Characteristics (3-line SPI system)

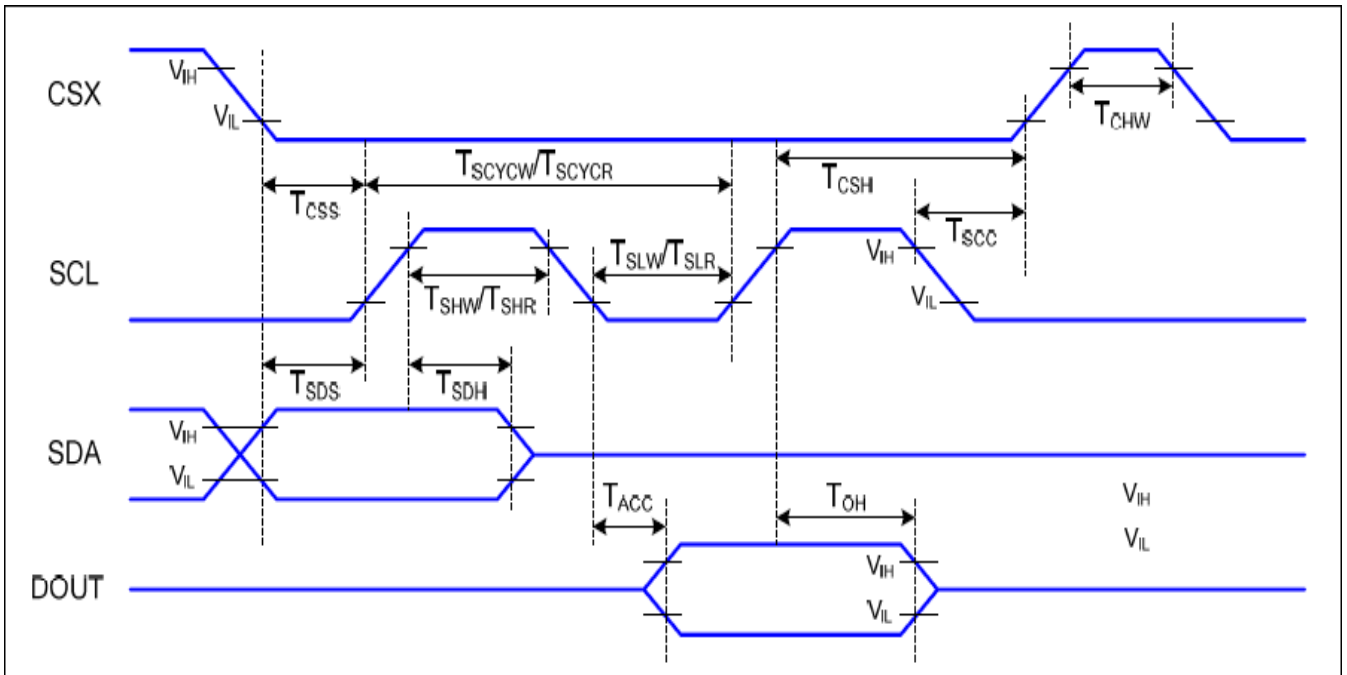


Figure 6.3: Serial Interface 3-SPI Timing Diagram

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C°

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	$T_{CSS}$	Chip select setup time (write)	15		ns	
	$T_{CSH}$	Chip select hold time (write)	15		ns	
	$T_{CSS}$	Chip select setup time (read)	60		ns	
	$T_{SCC}$	Chip select hold time (read)	65		ns	
	$T_{CHW}$	Chip select "H" pulse width	40		ns	
SCL	$T_{SCYCW}$	Serial clock cycle (write)	66		ns	
	$T_{SHW}$	SCL "H" pulse width (write)	15		ns	
	$T_{SLW}$	SCL "L" width (write)	15		ns	
	$T_{SCYCR}$	Serial clock cycle (read)	150		ns	
	$T_{SHR}$	SCL "H" pulse width (read)	60		ns	
	$T_{SLR}$	SCL "L" pulse width (read)	60		ns	
SDA (DIN)	$T_{SDS}$	Data setup time	10		ns	
	$T_{SDH}$	Data hold time	10		ns	
DOUT	$T_{ACC}$	Access time	10	50	ns	For max CL=30pF For min CL=8pF
	$T_{OH}$	Output disable time	15	50		

Table 6.3: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

### 6.3 Reset Timing

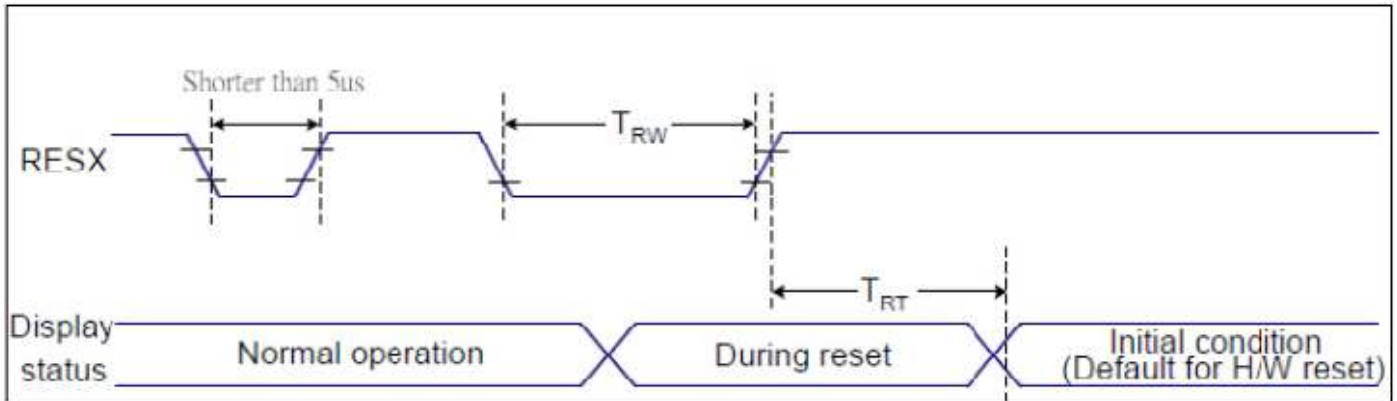


Figure 6.3: Reset Timing Diagram

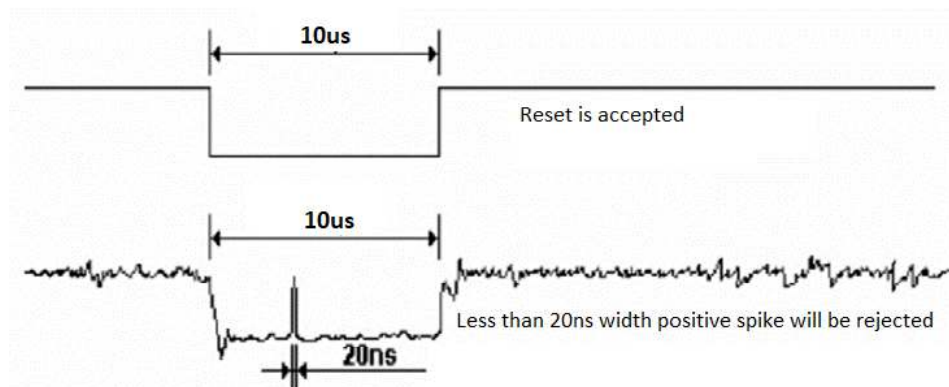
Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

## 7. Cautions and Handling Precautions

### 7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

### 7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.