LUMISSIL MICROSYSTEMS

A Division of ISSI

# T31ZX Smart Video Application Processor

## DATA SHEET

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# History

| Version | Date | Author | Description |
|---|---|---|---|
| Rev 1.0 | | | Initial |
| Rev 1.1 | 2022-03-14 | eleven | Modify diagram RISC-V  frequency and add Table3-5 |
| Rev 1.2 | 2022-04-13 | eleven | Modify cpu frequency from 1.5G to 1.4G and modify the memory capacity of block diagram |
| Rev 1.2 | 2022-04-15 | eleven | Modify resolution to 2592x2048 |
| Rev 1.3 | 2022-05-19 | eleven | Modify 3.4.1 Power-On Sequence |
| Rev 1.4 | 2022-06-09 | eleven | Modify 3.4.1 Power-On Sequence |

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(see page 7 for further instructions on how to automate populating list)

# Introduction

T31ZX is a smart video application processor targeting for video devices like mobile camera, security survey, video talking, video analysis and so on. This SoC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements addressed by video devices. T31ZX provides high-speed CPU computing power, excellent image signal process, fluent 2592x2048 resolution video recording.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data L1 cache, and 128kB L2 cache, operating at 1.4GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is a video encoder engine designed to process video streams using the HEVC(ISO/IEC 23008-2 High Efficiency Video Coding) and AVC(ISO/IEC 14496-10 Advanced Video Coding) standards. It also supports still picture encoding using the JPEG standard(ITU T.81). Together with the on chip video accelerating engine and post image processing unit, T31ZX delivers high video performance. The maximum resolution of 2592x2048 in the format of AVC are supported in encoding. up to 40Mbit/s, 2592x2048@25fps.

The ISP (Image signal processor) core supports excellent image process with the image from raw sensors. It supports DVP,BT and MIPI interface. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading, it can supply maximum resolution 2592x2048 resolution image for view or encoding to store or transfer.

For more quickly and easily to use T31ZX, 1G bit DDR2 is integrated on chip.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG, MAC, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

# 1 Overview

## 1.1 Block Diagram

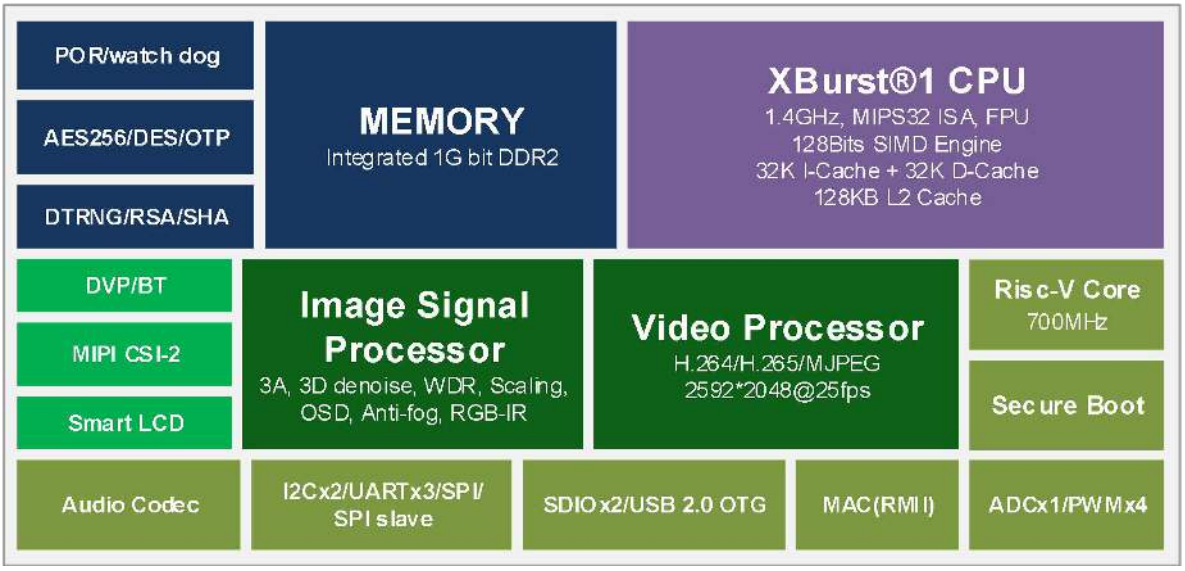


**Figure 1-1 T31ZX Diagram**

## 1.2 Features

### 1.2.1 CPU

- XBurst®-1 core
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.4GHz
- MMU
  - 32-entry joint-TLB
  - 8 entry instruction TLB
  - 8 entry data TLB
- L1 Cache
  - 32kB instruction cache
  - 32kB data cache
- Hardware debug support
- 16kB tight coupled memory
- L2 Cache
  - 128kB unify cache

### 1.2.2 Video Processor Unit

- Support DVT HEVC/AVC/JPEG Encoder

- Support HEVC up to 20Mbit/s and AVC up to 40Mbit/s, maximum frame rate is 2592x2048@25fps
- maximum size up to 2592x2048 resolution

### 1.2.3 Image Signal Processor

- Dynamic/Static Defect Pixel Correction
- Green Equalization
- Black Level Correction
- Lens Shading Correction
- 3A(Auto Exposure/Auto White Balance/Auto Focus)
- Support Statistical Information Output(3A)
- Adaptive Dynamic Range Compression
- Demosaic
- Sharpen
- Bayer Denoise
- 2D/3D Denosie
- Color Noise Suppression
- Lens Distortion Correction
- 2D Color Correction
- 3D Color Correction
- Gamma Correction
- Defog, WDR
- 3 Independent Image Scaler and Output
- Crop, Mirror and Flip
- Support Maximum Resolution:2592x2048

### 1.2.4 Smart LCD Controller

- Basic Features
  - Display size up to 800x600@60Hz,24BPP
  - Smart LCD interface 6800(type A) and 8080(type B)
- Colors Supports
  - Support up to 16,777,216 (16M) colors
- Panel Supports
  - transmit 565 by two cycle via SLCD 8bit data interface
  - transmit 888 by three cycle via SLCD 8bit data interface
  - Supports different size of display panel
  - Supports internal DMA operation and direct write register operation

### 1.2.5 Video input

- Support 8/10/12 bit RGB Bayer input
- Support DVP, BT1120(serial mode)/BT656/BT601 and MIPI CSI(2 lane, up to 1.5Gbps)

- Support maximum: 2592x2048@25fps
- Support single-sensor input

### 1.2.6 Audio System

- Integrated Audio codec
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K
- Low power DMIC Controller
  - 16bit data interface and 20bit precision internal controller
  - SNR:90dB,THD:-90dB@FS -20dB
  - Linear high pass filter include. Attenuation:-2.9dB@100Hz,22dB@27Hz,-36dB@10Hz
  - Low power voice trigger when waiting to start talking
  - 1/2/3/4 channel digital MIC support
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation
  - Sample frequency supported:8k,16k
- I2S Interface
  - Support standard interface protocol

### 1.2.7 Memory Interface

- Integrated 1G bit DDR2 on chip
- Static memory interface
  - Support 6 external chip selection CS6~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

### 1.2.8 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit

  - One three-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for P0, ISP, VPU, IPU
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflow
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer controller
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ $2^{24}$ - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 1 Channels
  - Resolution: 10-bit

- Integral nonlinearity: ±1 LSB
- Differential nonlinearity: ±0.5 LSB
- Resolution/speed: up to 2MSPS
- Max Frequency: 24MHz
- Low power dissipation: 1.5mW(worst)
- Support multi-touch detect
- Support write control command by software
- Single-end and Differential Conversion Mode
- Support external touch screen controller
- Pin Description

- OTP Slave Interface
  - Total 1024 bits. Lower 192bits are read only, other higher bits are read-able and write-able

### 1.2.9 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 3 interrupts, each interrupt corresponds to the group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 2 independent SMB channels (SMB0, SMB1)
- One High Speed Synchronous serial interfaces (SFC)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - transmit-only or receive-only operation
  - MSB first for command and data transfer, and LSB first for address transfer
  - 64 entries x 32 bits wide data FIFO
  - one device select

  - Configurable sampling point for reception
  - Configurable timing parameters: $t_{SLCH}$, $t_{CHSH}$ and $t_{SHSL}$
  - Configurable flash address wide are supported
  - transfer formats: Standard SPI only
  - two data transfer mode: slave mode and DMA mode
  - Configurable 6 phases for software flow
- Normal Speed Synchronous serial interfaces (SSI1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- Three UARTs (UART0, UART1, UART2)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands

  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
- Ethernet Media Access controller and interface
  - 10, 100Mbps data transfer rates with the following PHY interfaces:
    - RMII interface to communicate with an external Fast Ethernet PHY
  - Full-duplex operation:
    - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
    - forwarding of received Pause frames to the user application
  - Half-duplex operation:
  - CSMA/CD Protocol support
  - Frame bursting and frame extension in 100 Mbps half-duplex operation
  - Preamble and start of frame data (SFD) insertion in Transmit path
  - Preamble and SFD deletion in the Receive path
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Automatic Pad and CRC Stripping options for receive frames
  - Flexible address filtering modes, such as:
    - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
    - 64-bit Hash filter for multicast and unicast (DA) addresses
    - Option to pass all multicast addressed frames
    - Promiscuous mode to pass all frames without any filtering for network monitoring
    - Pass all incoming packets (as per filter) with a status report
  - Support Standard or Jumbo Ethernet frames with up to 2 KB of size
  - IEEE 802.1Q VLAN tag detection for reception frames
  - MDIO master interface for PHY device configuration and management
  - CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
  - Programmable watchdog timeout limit in the receive path
  - Detect remote wake-up frames and AMD magic packets

- Digital True Random Number Generator（DTRNG）
  - Pure digital logic circuits
  - True random number
  - Interrupt mode and no interrupt mode

- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
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  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
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  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
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        - Option to pass all multicast addressed frames
        - Promiscuous mode to pass all frames without any filtering for network monitoring
        - Pass all incoming packets (as per filter) with a status report
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    - MDIO master interface for PHY device configuration and management
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    - Programmable watchdog timeout limit in the receive path
    - Detect remote wake-up frames and AMD magic packets
- Digital True Random Number Generator（DTRNG）
    - Pure digital logic circuits
    - True random number
    - Interrupt mode and no interrupt mode

### 1.2.10 Bootrom

16kB Boot ROM memory

## 1.3 Characteristic

| Item | Characteristic |
|---|---|
| Process Technology | 22nm CMOS low power |
| Power supply voltage | General purpose I/O: 1.5~3.6V<br>DDR I/O: 1.5V(DDR2)<br>EFUSE programming: 1.8V ± 10%<br>Analog power supply 1: 1.8V ± 10%<br>Analog power supply 2: 3.3V ± 10%<br>Core: 0.8V ± 0.1V |
| Package | QFN 88 |
| Operating frequency | 1.4GHz |

# 2 Packaging and Pinout Information

## 2.1 Overview

T31ZX processor is offered in QFN88, show in Figure 2- 1. The T31ZX pin to ball assignment is show in Figure2-2. The detailed pin description is listed in Table 2- 1 ~ Table 2-14.

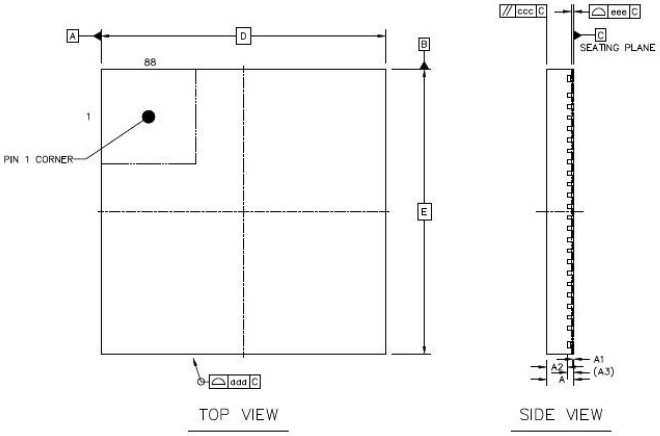
## 2.2 Solder Process

T31ZX package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

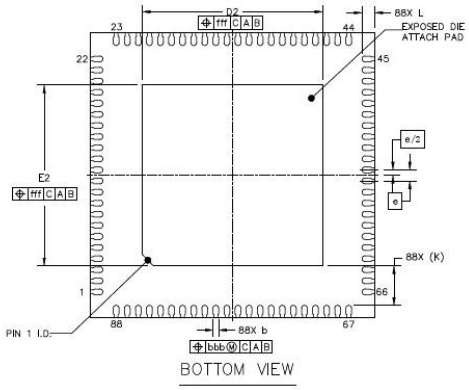
## 2.3 Moisture Sensitivity Level

T31ZX package moisture sensitivity is level 3.

## 2.4 T31ZX Package




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.13 | 0.18 | 0.23 |
| BODY SIZE | X | D | | 9 BSC | |
| | Y | E | | 9 BSC | |
| LEAD PITCH | | e | | 0.35 BSC | |
| EP SIZE | X | D2 | 5.6 | 5.7 | 5.8 |
| | Y | E2 | 5.6 | 5.7 | 5.8 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 1.25 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.07 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |




NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP •Sn8~20u

**Figure 2-1 T31ZX package outline drawing**

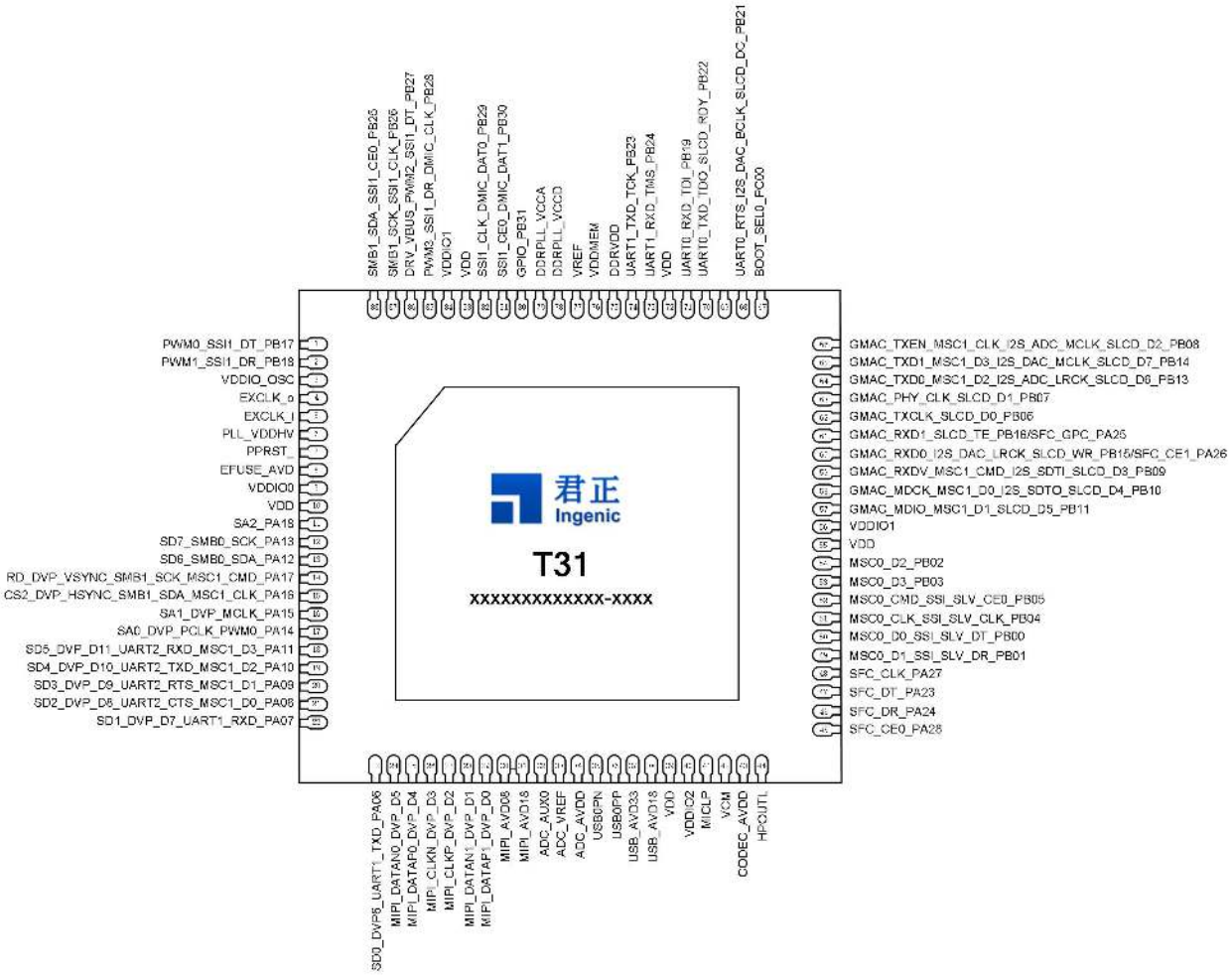



**Figure 2- 2 T31ZX pin to ball assignment**

## 2.5 Pin Description

### 2.5.1 Static Memory/DVP/I2Cx/UARTx/PWM/MSC1

**Table2- 1Static Memory/DVP/I2Cx/UARTx/PWM/MSC1 Pins(13)**

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 11 | SA02<br>PA18 | 2mA | SA2: Static memory address bus bit 2<br>PA18: GPIO group A bit 18 | VDDIO0 |
| 12 | SD7<br>SMB0_SCK<br>PA13 | 2mA<br>PU-rst | SD7: Static memory data bus bit 7<br>SMB0_SCK: I2C 0 serial clock<br>PA13: GPIO group A bit 13 | VDDIO0 |

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 13 | SD6<br>SMB0_SDA<br>PA12 | 2mA<br>PU-rst | SD6: Static memory data bus bit 6<br>SMB0_SDA: I2C 0 serial data<br>PA12: GPIO group A bit 12 | VDDIO0 |
| 14 | RD<br>DVP_VSYNC<br>SMB1_SCK<br>MSC1_CMD<br>PA17 | 2mA<br>PU-rst | RD: Static memory read signal<br>DVP_VSYNC: DVP vertical sync<br>SMB1_SCK: I2C 1 serial clock<br>MSC1_CMD: MSC (MMC/SD) 1 command<br>PA17: GPIO group A bit 17 | VDDIO0 |
| 15 | CS2<br>DVP_HSYNC<br>SMB1_SDA<br>MSC1_CLK<br>PA16 | 2mA<br>PU-rst | CS2: Static memory chip 2 select<br>DVP_HSYNC: DVP horizontal sync<br>SMB1_SDA: I2C 1 serial data<br>MSC1_CLK: MSC (MMC/SD) 1 clock output<br>PA16: GPIO group A bit 16 | VDDIO0 |
| 16 | SA1<br>DVP_MCLK<br>PA15 | 2mA<br>SR-<br>rst* | SA1: Static memory address bus bit 1<br>DVP_MCLK: DVP main clock output<br>PA15: GPIO group A bit 15 | VDDIO0 |
| 17 | SA0<br>DVP_PCLK<br>PWM0<br>PA14 | 2mA | SA0: Static memory address bus bit 0<br>DVP_PCLK: camera sensor pixel clock input<br>PWM0: PWM channel 0 output<br>PA14: GPIO group A bit 14 | VDDIO0 |
| 18 | SD5<br>DVP_D11<br>UART2_RXD<br>MSC1_D3<br>PA11 | 2mA<br>PU-<br>rst* | SD5: Static memory data bus bit 5<br>DVP_D11:DVP data in bit 11<br>UART2_RXD: UART2 data receive<br>MSC1_D3: MSC (MMC/SD) 1 data bit 3<br>PA11: GPIO group A bit 11 | VDDIO0 |
| 19 | SD4<br>DVP_D10<br>UART2_TXD<br>MSC1_D2<br>PA10 | 2mA | SD4: Static memory data bus bit 4<br>DVP_D10:DVP data in bit 10<br>UART2_TXD: UART2 data transmit<br>MSC1_D2: MSC (MMC/SD) 1 data bit 2<br>PA10: GPIO group A bit 10 | VDDIO0 |
| 20 | SD3<br>DVP_D9<br>UART2_RTS<br>MSC1_D1<br>PA09 | 2mA | SD3: Static memory data bus bit 3<br>DVP_D9:DVP data in bit 9<br>UART2_RTS: UART2 request-to-send handshaking<br>MSC1_D1: MSC (MMC/SD) 1 data bit 1<br>PA09: GPIO group A bit 09 | VDDIO0 |

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 21 | SD2<br>DVP_D8<br>UART2_CTS<br>MSC1_D0<br>PA08 | 2mA | SD2: Static memory data bus bit 2<br>DVP_D8:DVP data in bit 8<br>UART2_CTS: UART2 clear-to-send handshaking<br>MSC1_D0: MSC (MMC/SD) 1 data bit 0<br>PA08: GPIO group A bit 08 | VDDIO0 |
| 22 | SD1<br>DVP_D7<br>UART1_RXD<br>PA07 | 2mA | SD1: Static memory data bus bit 1<br>DVP_D7:DVP data in bit 7<br>UART1_RXD: UART 1 receive data<br>PA07: GPIO group A bit 07 | VDDIO0 |
| 23 | SD0<br>DVP_D6<br>UART1_TXD<br>PA06 | 2mA | SD0: Static memory data bus bit 0<br>DVP_D6:DVP data in bit 6<br>UART1_TXD: UART1 data transmit<br>PA06: GPIO group A bit 06 | VDDIO0 |

### 2.5.2 SFC

**Table2- 2SFC Pins(4)**

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 45 | SFC_CE0<br>PA28 | 8mA<br>PU-rst | SFC_CE0: high speed ssi chip 0 select<br>PA28: GPIO group A bit 28 | VDDIO1 |
| 46 | SFC_DR<br>PA24 | 8mA<br>PU-rst | SFC_DR: high speed ssi receive data<br>PA24: GPIO group A bit 24 | VDDIO1 |
| 47 | SFC_DT<br>PA23 | 8mA<br>PU-rst<br>SMT-rst | SFC_DT: high speed ssi transmit data<br>PA23: GPIO group A bit 23 | VDDIO1 |
| 48 | SFC_CLK<br>PA27 | 8mA<br>PU-rst | SFC_CLK: high speed ssi clock<br>PA27: GPIO group A bit 27 | VDDIO1 |
| 60* | SFC_CE1<br>PA26 | 8mA<br>PU-rst | SFC_CE1: high speed ssi chip 1 select<br>PA26: GPIO group A bit 26 | VDDIO1 |
| 61* | SFC_GPC<br>PA25 | 8mA<br>PU-rst | SFC_GPC: high speed ssi general-purpose control<br>PA25: GPIO group A bit 25 | VDDIO1 |

NOTES:

Pin 60 and 61 share IO with PB15 and PB16, If need configure as this function, please fixed the another IO to GPIO input model.

### 2.5.3 MSC0/GMAC/PWMx/UARTx/I2C1/SSI1/SSI_SLV/JTAG/SLCD/DMIC/I2S

**Table2- 3 MSC0/GMAC/PWMx/UARTx/I2C1/SSI1/SSI_SLV//JTAG/SLCD/DMIC/I2S Pins (30)**

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 1 | PWM0<br>SSI1_DT<br>PB17 | 2mA<br>PD-rst | PWM0: PWM channel 0 output<br>SSI1_DT: normal speed ssi 1 transmit data<br>PB17: GPIO group B bit 17. | VDDIO1 |
| 2 | PWM1<br>SSI1_DR<br>PB18 | 2mA<br>PD-rst | PWM1: PWM channel 1 output<br>SSI1_DR: normal speed ssi 1 receive data<br>PB18: GPIO group B bit 18. | VDDIO1 |
| 49 | MSC0_D1<br>SSI_SLV_DR<br>PB01 | 2mA | MSC0_D1: MSC (MMC/SD) 0 data bit 1<br>SSI_SLV_DR: ssi slave receive data<br>PB01: GPIO group B bit 01 | VDDIO1 |
| 50 | MSC0_D0<br>SSI_SLV_DT<br>PB00 | 2mA | MSC0_D0: MSC (MMC/SD) 0 data bit 0<br>SSI_SLV_DT: ssi slave transmit data<br>PB00: GPIO group B bit 00 | VDDIO1 |
| 51 | MSC0_CLK<br>SSI_SLV_CLK<br>PB04 | 2mA | MSC0_CLK: MSC (MMC/SD) 0 clock output<br>SSI_SLV_CLK: ssi slave clock<br>PB04: GPIO group B bit 04 | VDDIO1 |
| 52 | MSC0_CMD<br>SSI_SLV_CE0<br>PB05 | 2mA<br>PU-rst | MSC0_CMD: MSC (MMC/SD) 0 command<br>SSI_SLV_CE0: ssi slave chip 0 select<br>PB05: GPIO group B bit 05 | VDDIO1 |
| 53 | MSC0_D3<br>PB03 | 2mA | MSC0_D3: MSC (MMC/SD) 0 data bit 3<br>PB03: GPIO group B bit 03 | VDDIO1 |
| 54 | MSC0_D2<br>PB02 | 2mA | MSC0_D2: MSC (MMC/SD) 0 data bit 2<br>PB02: GPIO group B bit 02 | VDDIO1 |
| 57 | GMAC_MDIO<br>MSC1_D1<br>SLCD_D5<br>PB11 | 2mA<br>PU-rst | GMAC_MDIO: gmac MDIO which is clocked by MDC<br>MSC1_D1: MSC (MMC/SD) 1 data bit 1<br>SLCD_D5: smart lcd data output bit 5<br>PB11: GPIO group B bit 11. | VDDIO1 |
| 58 | GMAC_MDCK<br>MSC1_D0<br>I2S_SDTO<br>SLCD_D4<br>PB10 | 2mA<br>PD-rst | GMAC_MDCK: gmac manage data clock<br>MSC1_D0: MSC (MMC/SD) 1 data bit 0<br>I2S_SDTO: I2S serial data output signal<br>SLCD_D4: smart lcd data output bit 4<br>PB10: GPIO group B bit 10. | VDDIO1 |
| 59 | GMAC_RXDV<br>MSC1_CMD<br>I2S_SDTI<br>SLCD_D3 | 2mA | GMAC_RXDV: gmac receive data valid<br>MSC1_CMD: MSC (MMC/SD) 1 command<br>I2S_SDTI:I2S serial data input signal<br>SLCD_D3: smart lcd data output bit 3 | VDDIO1 |

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| | PB09 | | PB09: GPIO group B bit 09. | |
| 60* | GMAC_RXD0<br>I2S_DAC_LRCK<br>SLCD_WR<br>PB15 | 2mA | GMAC_RXD0: gmac receive data bit 0<br>I2S_DAC_LRCK: I2S DAC left/right clock<br>SLCD_WR: smart lcd write data control<br>PB15: GPIO group B bit 15. | VDDIO1 |
| 61* | GMAC_RXD1<br>SLCD_TE<br>PB16 | 2mA<br>PU-rst | GMAC_RXD1: gmac receive data bit 1<br>SLCD_TE: smart lcd crack control<br>PB16: GPIO group B bit 16. | VDDIO1 |
| 62 | GMAC_TXCLK<br>SLCD_D0<br>PB06 | 2mA | GMAC_TXCLK: gmac transmitting clock<br>SLCD_D0: smart lcd data output bit 0<br>PB06: GPIO group B bit 06 | VDDIO1 |
| 63 | GMAC_PHY_CLK<br>SLCD_D1<br>PB07 | 2mA | GMAC_PHY_CLK: gmac phy clock<br>SLCD_D1: smart lcd data output bit 1<br>PB07: GPIO group B bit 07 | VDDIO1 |
| 64 | GMAC_TXD0<br>MSC1_D2<br>I2S_ADC_LRCK<br>SLCD_D6<br>PB13 | 2mA | GMAC_TXD0: gmac transmit data bit 0<br>MSC1_D2: MSC (MMC/SD) 1 data bit 2<br>I2S_ADC_LRCK: I2S ADC left/right clock<br>SLCD_D6: smart lcd data output bit 6<br>PB13: GPIO group B bit 13. | VDDIO1 |
| 65 | GMAC_TXD1<br>MSC1_D3<br>I2S_DAC_MCLK<br>SLCD_D7<br>PB14 | 2mA<br>PU-rst | GMAC_TXD1: gmac transmit data bit 1<br>MSC1_D3: MSC (MMC/SD) 1 data bit 3<br>I2S_DAC_MCLK: I2S DAC system clock<br>SLCD_D7: smart lcd data output bit 7<br>PB14: GPIO group B bit 14. | VDDIO1 |
| 66 | GMAC_TXEN<br>MSC1_CLK<br>I2S_ADC_MCLK<br>SLCD_D2<br>PB08 | 2mA | GMAC_TXEN: gmac transmitting enable<br>MSC1_CLK: MSC (MMC/SD) 1 clock output<br>I2S_ADC_MCLK: I2S system clock<br>SLCD_D2: smart lcd data output bit 2<br>PB08: GPIO group B bit 08 | VDDIO1 |
| 67 | (BOOT_SEL0)<br>PC00 | 2mA<br>PU-rst | It is taken as BOOT select bit 0 by Boot ROM code<br>PC00: GPIO group C bit 00 | VDDIO1 |
| 68 | UART0_RTS<br><br>I2S_DAC_BCLK<br>SLCD_DC<br>PB21 | 2mA | UART0_RTS: UART 0 request-to-send handshaking<br>I2S_DAC_BCLK: I2S DAC bit clock<br>SLCD_DC: smart lcd cmd/data identify<br>PB21: GPIO group B bit 21 | VDDIO1 |
| 69 | UART0_CTS<br>I2S_ADC_BCLK | 2mA | UART0_CTS: UART 0 clear-to-send handshaking<br>I2S_ADC_BCLK: I2S ADC bit clock | VDDIO1 |

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| | SLCD_CS<br>PB20 | | SLCD_CS: smart lcd chip select<br>PB20: GPIO group B bit 20 | |
| 70 | UART0_TXD<br>TDO<br>SLCD_RDY<br>PB22 | 2mA | UART0_TXD: UART 0 data transmit<br>TDO: JTAG data output<br>SLCD_RDY: smart lcd work status<br>PB22: GPIO group B bit 22 | VDDIO1 |
| 71 | UART0_RXD<br>TDI<br>PB19 | 2mA<br>PU-rst | UART0_RXD: UART 0 data receive<br>TDI: JTAG data input<br>PB19: GPIO group B bit 19 | VDDIO1 |
| 73 | UART1_RXD<br>TMS<br>PB24 | 2mA<br>PU-rst | UART1_RXD: UART 1 receive data<br>TMS: JTAG mode select<br>PB24: GPIO group B bit 24 | VDDIO1 |
| 74 | UART1_TXD<br>TCK<br>PB23 | 2mA | UART1_TXD: UART 1 transmit data<br>TCK: JTAG clock input<br>PB23: GPIO group B bit 23 | VDDIO1 |
| 80 | GPIO_PB31 | 2mA<br>PD-rst | PB31: GPIO group B bit 31 | VDDIO1 |
| 81 | SSI1_CE0<br>DMIC_DAT1<br>PB30 | 2mA<br>PU-rst | SSI1_CE0: normal speed ssi 1 chip 0 select<br>DMIC_DAT1: digital microphone data bit 1<br>PB30: GPIO group B bit 30 | VDDIO1 |
| 82 | SSI1_CLK<br>DMIC_DAT0<br>PB29 | 2mA<br>PU-rst | SSI1_CLK: normal speed ssi 1 clock<br>DMIC_DAT0: digital microphone data bit 0<br>PB29: GPIO group B bit 29 | VDDIO1 |
| 85 | PWM3<br>SSI1_DR<br>DMIC_CLK<br>PB28 | 2mA<br>PD-rst | PWM3: PWM channel 3 output<br>SSI1_DR: normal speed ssi 1 data receive<br>DMIC_CLK: digital microphone clock output<br>PB28: GPIO group B bit 28 | VDDIO1 |
| 86 | PWM2<br>DRV_VBUS<br>SSI1_DT<br>PB27 | 2mA<br>PD-rst | PWM2: PWM channel 2 output<br>DRV_VBUS:USB-5V control signal<br>SSI1_DT: normal speed ssi 1 transmit data<br>PB27: GPIO group B bit 27 | VDDIO1 |
| 87 | SMB1_SCK<br>SSI1_CLK<br>PB26 | 2mA<br>PU-rst | SMB1_SCK: I2C 1 serial clock<br>SSI1_CLK: normal speed ssi 1 clock<br>PB26: GPIO group B bit 26 | VDDIO1 |
| 88 | SMB1_SDA<br>SSI1_CE0_<br>PB25 | 2mA<br>PU-rst | SMB1_SDA: I2C 1 serial data<br>SSI1_CE0: normal speed ssi 1 chip 0 select<br>PB25: GPIO group B bit 25 | VDDIO1 |

NOTES:
Pin 60 and 61 share IO with PA25 and PA26, If need configure as this function, please fixed the another IO to GPIO input model.

### 2.5.4 System Control

**Table2- 4System Control Pins(1)**

| QFN Pin Location | Pin Function Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 7 | PPRST_ | 2mA SMT | PPRST_: RTC power on reset and RESET-KEY reset input | VDDIO0 |

### 2.5.5 Digital IO/core power/ground

**Table2- 5IO/Core power supplies Pins (10)**

| QFN Pin Location | Pin Names | Pin Function Description |
|---|---|---|
| 9 | VDDIO0 | VDDIO0: IO digital power for DVP power domain, 1.8V |
| 56,84 | VDDIO1 | VDDIO1: IO digital power for normal function Pad power domain, 1.8V/3.3V |
| 40 | VDDIO2 | VDDIO2: IO digital power for normal function Pad power domain, 1.8V/3.3V |
| 10,39,55, 72,83 | VDD | VDD: CORE digital power, 0.8V |
| Epad | VSS | VSS: IO digital ground for none DRAM and CORE digital ground, 0V |

### 2.5.6 DDR power/ground

**Table2- 6DDR power/ground supplies Pins (5)**

| QFN Pin Location | Pin Names | Pin Function Description |
|---|---|---|
| 77 | VREF | VREF: DDR reference voltage, (VREF = VDDMEM/2) |
| 76 | VDDMEM | VDDMEM: DDR IO supply(1.5V for DDR2) |
| 75 | DDRVDD | DDRVDD: DDR PHY 1.5V supply |
| 78 | DDR_PLLVCCD | DDR_PLLVCCD: DDR PLL power supply for digital |
| 79 | DDR_PLLVCCA | DDR_PLLVCCA: DDR PLL power supply for analog |

### 2.5.7 Analog - USB

**Table2- 7USB 2.0 OTG (4)**

| QFN Pin Location | Pin Names | Pin Function Description | IO Power |
|---|---|---|---|
| 36 | USB0PP | USB0PP: USB data-positive | USB_AVD33 |
| 35 | USB0PN | USB0PN: USB data-negative | USB_AVD33 |
| 37 | USB_AVD33 | USB_AVD33: This is the analog supply that is used to support 3.3V signaling. This supply has both integrated IO pads and associated ESD. The expectation is that this supply is unique to the USB PHY. The PHY provides two pins for this power supply, but they can often be bonded out to a single package pin if the parasitic are low enough to support the current draw. | - |
| 38 | USB_AVD18 | USB_AVD18: This is the analog supply that is used to support 1.8V signaling. This supply has both integrated IO pads. | - |

### 2.5.8 Analog - MIPI and DVP

**Table2- 8MIPI CSI and DVP(8)**

| QFN Pin Location | Pin Names | Pin Function Description | IO Power |
|---|---|---|---|
| 24 | DATAN0<br>DVP_D5 | DATAN0: In MIPI model is data lane 0 serial signal<br>DVP_D5: In TTL model is DVP input data bit 5 | MIPI_AVD18 |
| 25 | DATAP0<br>DVP_D4 | DATAP0: In MIPI model is data lane 0 serial signal<br>DVP_D4: In TTL model is DVP input data bit 4 | MIPI_AVD18 |
| 26 | CLKN<br>DVP_D3 | CLKN: In MIPI model is clock lane serial signal<br>DVP_D3: In TTL model is DVP input data bit 3 | MIPI_AVD18 |
| 27 | CLKP<br>DVP_D2 | CLKP: In MIPI model is clock lane serial signal<br>DVP_D2: In TTL model is DVP input data bit 2 | MIPI_AVD18 |
| 28 | DATAN1<br>DVP_D1 | DATAN1: In MIPI model is data lane 1 serial signal<br>DVP_D1:In TTL model is DVP input data bit 1 | MIPI_AVD18 |
| 29 | DATAP1<br>DVP_D0 | DATAP1: In MIPI model is data lane 1 serial signal<br>DVP_D0： In TTL model is DVP input data bit 0 | MIPI_AVD18 |
| 30 | MIPI_AVD08 | MIPI_AVD08: PHY analog power, 0.8V | - |
| 31 | MIPI_AVD18 | MIPI_AVD18: PHY analog power, 1.8V | - |

**NOTES:**

1. DVP_Dx signals can input form this Pad when configure the MIPI PHY to TTL model

### 2.5.9 Analog - SARADC

**Table 2-1 SARADC Pins (3)**

| QFN Pin Location | Pin Names | Pin Function Description | IO Power |
|---|---|---|---|
| 32 | ADC_AUX0 | ADC_AUX0: SARADC channel 0 input | ADC_AVDD |
| 33 | ADC_VREF | SADC_VREF: Voltage reference input, 0.5* ADC_AVDD ~ 0.99* ADC_AVDD | - |
| 34 | ADC_AVDD | ADC_AVDD: SARADC analog power, 1.8 V | - |

### 2.5.10 Analog - CODEC

**Table2- 9CODEC Pins (4)**

| QFN Pin Location | Pin Names | Pin Function Description | IO Power |
|---|---|---|---|
| 41 | MICP | MICP: differential microphone input | CODEC_AVDD |
| 42 | VCM | VCM: Reference voltage output | CODEC_AVDD |
| 44 | HPOUT | HPOUT: headphone output | CODEC_AVDD |
| 43 | CODEC_AVDD | CODEC_AVDD:1.8V analog supply | - |

### 2.5.11 Analog - EFUSE

**Table2- 10EFUSE Pins (1)**

| QFN Pin Location | Pin Names | Pin Function Description |
|---|---|---|
| 8 | EFUSE_AVD | EFUSE_AVD: EFUSE programming power, 0V/1.8V |

### 2.5.12 Analog - CLOCK/PLL

**Table2- 11 CLOCK/PLL Pins (4)**

| QFN Pin Location | Pin Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 5 | EXCLK_XI | 2~30 MHz Oscillator, OSC on/off | EXCLK_XI: external oscillator clock input or external 24MHz clock input | VDDIO_OSC |
| 4 | EXCLK_XO | | EXCLK_XO: external oscillator clock output | VDDIO_OSC |
| 3 | VDDIO_OSC | - | VDDIO_OSC: Oscillator power supply, 1.8V | - |

| QFN Pin Location | Pin Names | IO Cell Char. | Pin Function Description | IO Power |
|---|---|---|---|---|
| 6 | PLL_VDDHV | - | PLL_VDDHV:PLL analog supply power 1.8V | - |

**NOTES:**

1 All GPIO are programmable with multi-voltage (1.8V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

2 The meaning of phases in IO cell characteristics are:

- 8/16mA out: The IO cell's output driving strength is about 8/16mA.
- PU: The IO cell contains a pull-up resistor and fixed pull up.
- PD: The IO cell contains a pull-down resistor and fixed pull down.
- PU-rst: The IO cell during reset and after the pull up function is enabled.
- PD-rst: The IO cell during reset and after the pull down function is enabled.
- SMT: The IO cell is Schmitt trigger input and fixed.
- SMT-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.
- SR-rst: The IO cell during reset and after the slew-rate function select fast mode.

# 3 Electrical Specifications

## 3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3- 1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

**Table3- 1 Absolute Maximum Ratings**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Storage Temperature | -65 | 150 | °C |
| Operation Temperature | -40 | 125 | °C |
| VDDMEM power supplies voltage | -0.1 | 1.98 | V |
| DDRVDD power supplies voltage | -0.1 | 1.98 | V |
| DDR_PLLVCCA power supplies voltage | -0.1 | 1.98 | V |
| DDR_PLLVCCD power supplies voltage | -0.1 | 0.88 | V |
| VDDIO0 power supplies voltage | -0.5 | 1.98 | V |
| VDDIO1 power supplies voltage | -0.5 | 3.63 | V |
| VDDIO2 power supplies voltage | -0.5 | 3.63 | V |
| VDD power supplies voltage | -0.1 | 0.88 | V |
| PLL_VDDHV power supplies voltage | -0.1 | 1.98 | V |
| EFUSE_AVD power supplies voltage | -0.1 | 1.98 | V |
| USB_AVD33 power supplies voltage | -0.1 | 3.63 | V |
| USB_AVD18 power supplies voltage | -0.1 | 1.98 | V |
| ADC_AVDD power supplies voltage | -0.1 | 1.98 | V |
| CODEC_AVDD power supplies voltage | -0.1 | 1.98 | V |
| Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins | - | 2000 | V |

| Parameter | Min | Max | Unit |
|---|---|---|---|
| together, either polarity. Three stresses maximum. | | | |

## 3.2 Recommended operating conditions

**Table3- 2Recommended operating conditions for power supplies**

| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| VDDMEM | VDDMEM voltage for SSTL18 (DDR2) | 1.62 | 1.8 | 1.98 | V |
| DDRVDD | DDR KGD power supplies voltage | 1.62 | 1.8 | 1.98 | V |
| DDR_PLLVCCA | DDR PLL power supplies voltage | 1.62 | 1.8 | 1.98 | V |
| DDR_PLLVCCD | DDR PLL power supplies voltage | 0.72 | 0.8 | 0.88 | V |
| VDDIO0 | GPIO power domain 0 supplies voltage | 1.62 | 1.8 | 1.98 | V |
| VDDIO1 | GPIO power domain 1 supplies voltage | 1.5 | 3.3 | 3.63 | V |
| VDDIO2 | GPIO power domain 2 supplies voltage | 1.5 | 3.3 | 3.63 | V |
| VDD | VDD core supplies voltage | 0.72 | 0.8 | 0.88 | V |
| PLL_VDDHV | APLL, MPLL and VPLL analog voltage | 1.62 | 1.8 | 1.98 | V |
| EFUSE_AVD | EFUSE program supplies voltage | 1.62 | 1.8 | 1.98 | V |
| USB_AVD33 | USB PHY VCCA3P3 analog voltage | 3.0 | 3.3 | 3.6 | V |
| USB_AVD18 | USB PHY VCC18 analog voltage | 1.62 | 1.8 | 1.98 | V |
| ADC_AVDD | SAR-ADC analog voltage | 1.62 | 1.8 | 1.98 | V |
| CODEC_AVDD | CODEC analog voltage | 1.62 | 1.8 | 1.98 | V |
| MIPI_AVD08 | MIPI analog voltage | 0.72 | 0.8 | 0.98 | V |
| MIPI_AVD18 | MIPI analog voltage | 1.62 | 1.8 | 1.98 | V |

**Table3- 3Recommended operating conditions for VDDIO0/VDDIO1/VDDIO2 supplied pins**

| Symbol | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH18}$ | Input high voltage for 1.8V I/O application | *0.65 | - | +0.3 | V |
| $V_{IL18}$ | Input low voltage for 1.8V I/O application | -0.3 | - | *0.35 | V |
| $V_{IH25}$ | Input high voltage for 2.5V I/O application | 1.7 | - | +0.3 | V |
| $V_{IL25}$ | Input low voltage for 2.5V I/O application | -0.3 | - | 0.7 | V |
| $V_{IH33}$ | Input high voltage for 3.3V I/O application | 2 | - | +0.3 | V |
| $V_{IL33}$ | Input low voltage for 3.3V I/O application | -0.3 | - | 0.8 | V |

**Table3- 4 Recommended operating conditions for others**

| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | -20 | 25 | +85 | °C |

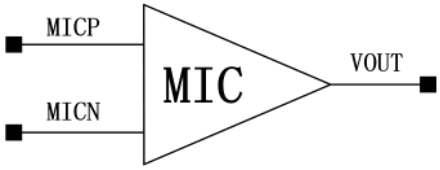
| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | -40 | 25 | +125 | °C |

**Table3- 5Thermal Resistance parameter**

| Ambient Temperature | 25°C | | |
|---|---|---|---|
| Thermal Resistance | θ ja（℃/W） | θ jb（℃/W） | θ jc（℃/W） |
| JEDEC 2S2P | 37.5 | 16.8 | 4.2 |

## 3.3 Audio codec

### 3.3.1 Microphone input

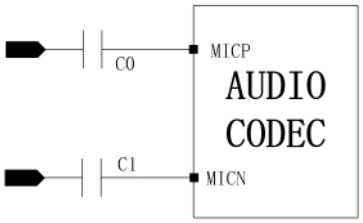



There are two inputs channels named left ADC channel and right ADC channel. In the each channel, there are one inputs which are configured as differential input by the microphone PGA(MICL).

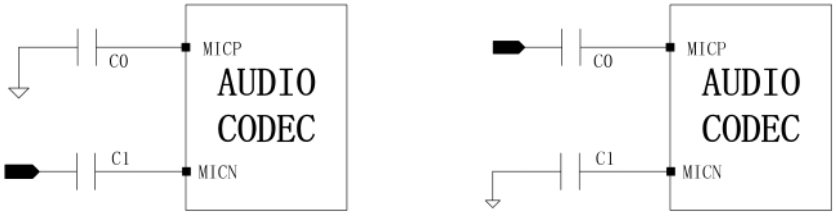
The signal of microphone output should be input to AUDIO CODEC through DC-blocking capacitor, as shown in following figure. The capacitance and input resistance form a high pass filter. For example, when the gain of the MIC module is 20dB, the input resistance is 45KΩ and 0.1uF DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 45 \times 10^{3} \times 0.1 \times 10^{-6}} = 35.4Hz$$

The capacitance of the DC-blocking capacitor should be determined by the minimum input impedance and application requirements.




If the output of microphone is single-ended, the AUDIO ADC input should be connected as following figure.




Microphone PGA has four gains to amplify the input signal, that is, 0dB, 20dB, 30dB and 40dB.

### 3.3.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC_L and ALC_R) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

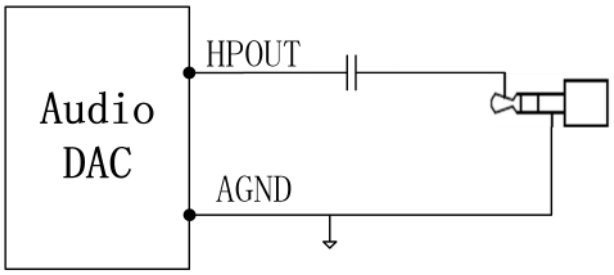
### 3.3.3 Headphone output

Audio codec DAC output can drive 16Ω or 32Ω headphone load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16Ωheadphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.




The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB.

### 3.3.4 Microphone bias

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.8*CODEC_AVDD to 0.975* CODEC_AVDD with a step of 0.025* CODEC_AVDD.

## 3.4 Power On, Reset and BOOT

### 3.4.1 Power-On Sequence

The external voltage regulator and other power-on devices must provide the T31ZX processor with a specific sequence of power and resets to ensure proper operation. Figure 3- 1 shows this sequence and Table 3-6 gives the timing parameters. Following are the name of the power.

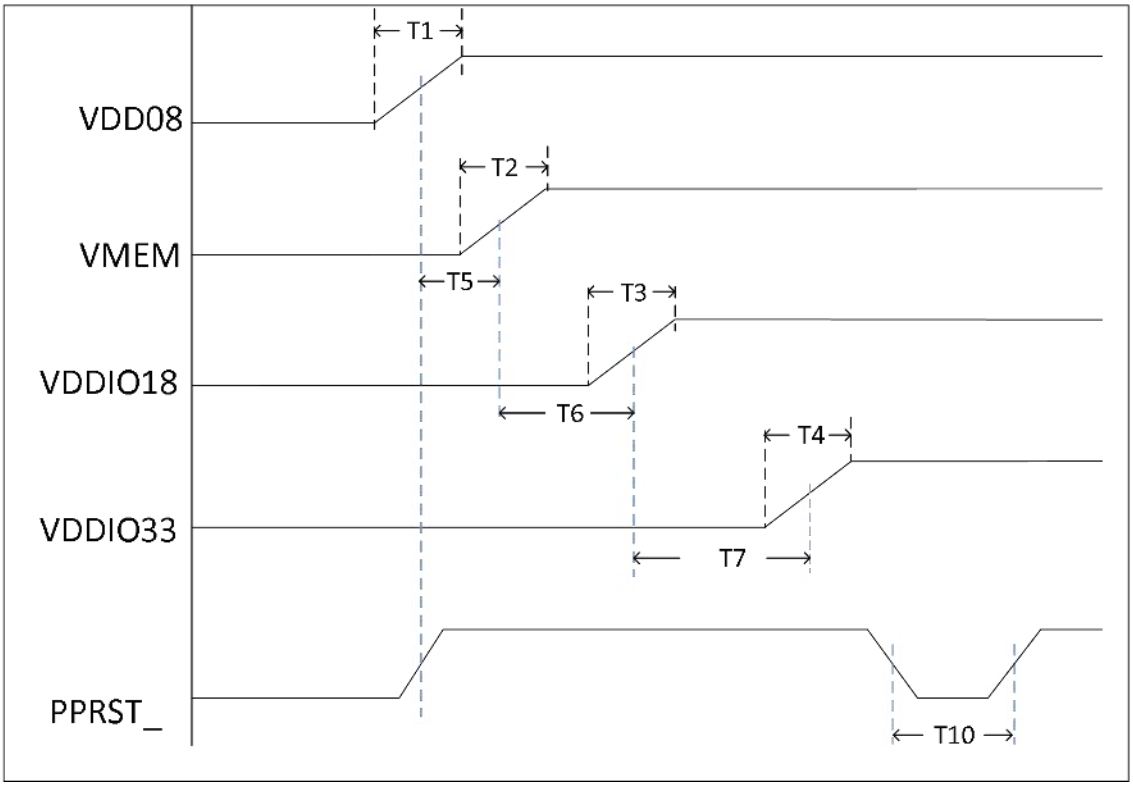
- VDD08: all 0.8V power supplies, VDD, DDR_PLLVCCD, MIPI_AVD08, USB_AVD08, PLL_VDD, USB_AVD08
- VMEM: VDDMEM,DDRVDD
- VDD18: VDDIO0,DDR_PLLVCCA,PLL_VDDHV, USB_AVD18, MIPI_AVD18, ADC_AVDD, CODEC_AVDD
- VDD33: VDDIO1,VDDIO2,USB_AVD33

**Table3- 6 Power-On Sequence Parameters**

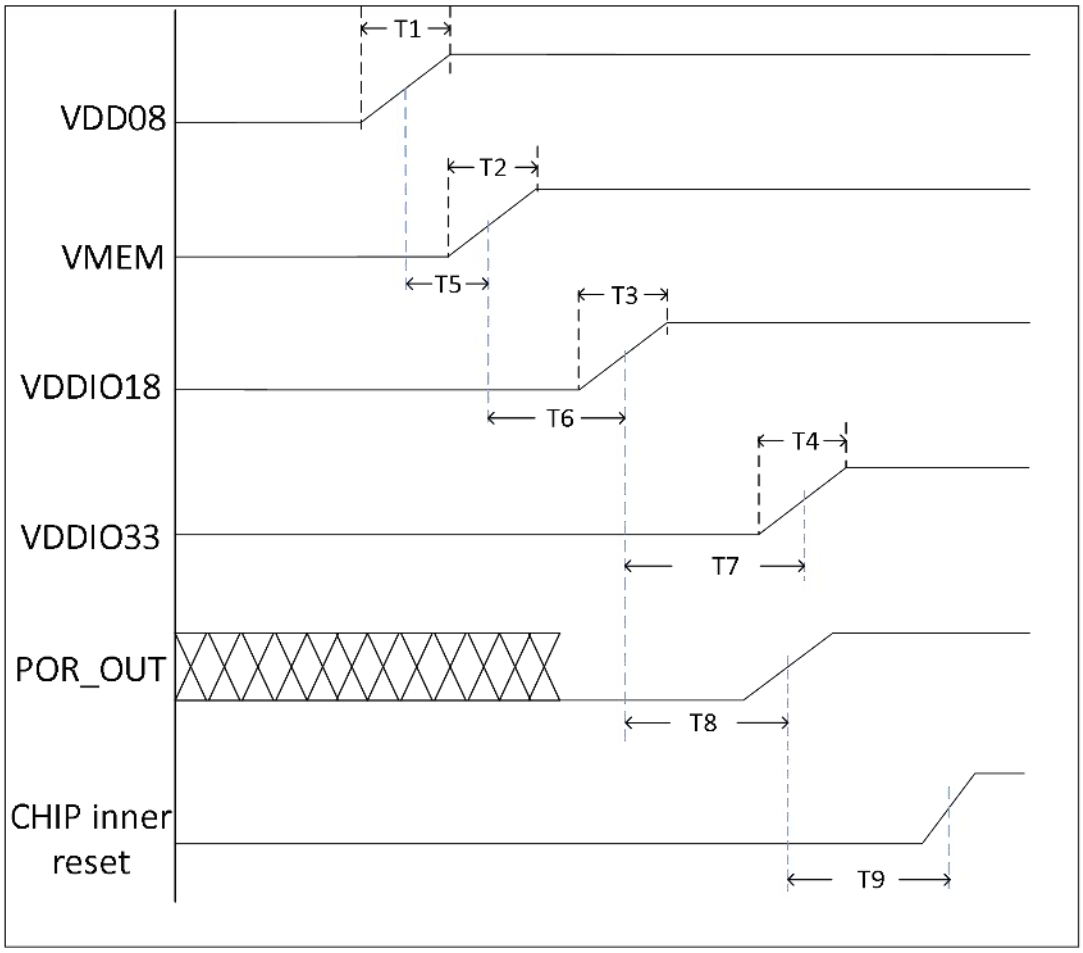
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| T1 | VDD08 rise time[1] | - | - | 400 | us |
| T2 | VMEM rise time | - | - | 400 | us |
| T3 | VDDIO18 rise time | - | - | 400 | us |
| T4 | VDDIO33 rise time | - | - | 400 | us |
| T5 | Delay between VDD08 arriving 50% to VMEM arriving 50% | T1*0.5 | - | - | us |
| T6 | Delay between VMEM arriving 50% to VDDIO18 arriving 50% | 0 | - | - | us |
| T7 | Delay between VDDIO18 arriving 50% to VDDIO33 arriving 50% | T3 | - | - | us |
| T8 | Delay between VDDIO18 arriving 50% to POR_OUT arriving 50% | - | 240 | - | us |
| T9 | Delay between POR_OUT arriving 50% to chip inner reset arriving 50% | | 10 | | ms |
| T10 | PPRST_ kept time[2] | | 100 | | us |

**NOTES:**

- [1]: The power rise time is defined as 10% to 90%.
- [2]: The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.
- In addition, when the CPU is used in a low-power solution, it is recommended that each power supply use a high-efficiency DCDC power supply, and the conversion efficiency should be above 90%.




PPRST_ reset mode




POR reset mode

**Figure3- 1 Power-On Sequence Diagram**

### 3.4.2 Reset procedure

There are 4 reset sources: 1. PPRST_ pin reset; 2. POR hardware reset;3.WDT timeout reset; 4. Hibernating reset when exiting hibernating mode. After reset, program start from boot.

- PPRST_ pin reset.

  This reset is triggered when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

- POR(Power-On-Reset) hardware reset.

  The chip POR circuit provides reliable reset function for general applications. Powered by 1.8V analog supply and monitors 0.8V digital and 1.8V analog supply. It generates reset signal to digital logic. Set low if analog supply or digital supply is below the threshold voltage(typical 1.35V threshold for 1.8V supply and 0.6V threshold for 0.8V supply), and will be set high if both of analog supply and digital supply exceed the threshold voltage.

- WDT reset.

  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

- Hibernating reset.

  This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description” for details. The oscillators are on. The USB 2.0 OTG PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

### 3.4.3 BOOT

The boot sequence of the T31X is controlled by boot_sel0. The configuration is shown as follow:

**Table3- 7 Boot Configuration of T31X**

| boot_sel0 | Boot method |
|---|---|
| 0 | MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B.<br>MSC1 use GPIO Port C) |
| 1 | SFC boot @ CS4 (SPI boot) |

**Note:**

1. When SFC boot start failure, the program in bootrom will go into MSC0 boot, If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.

2. When MSC0 boot start failure, the program in bootrom will go into MSC1 boot， If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used. If MSC1 boot start failure, jump to USB boot.

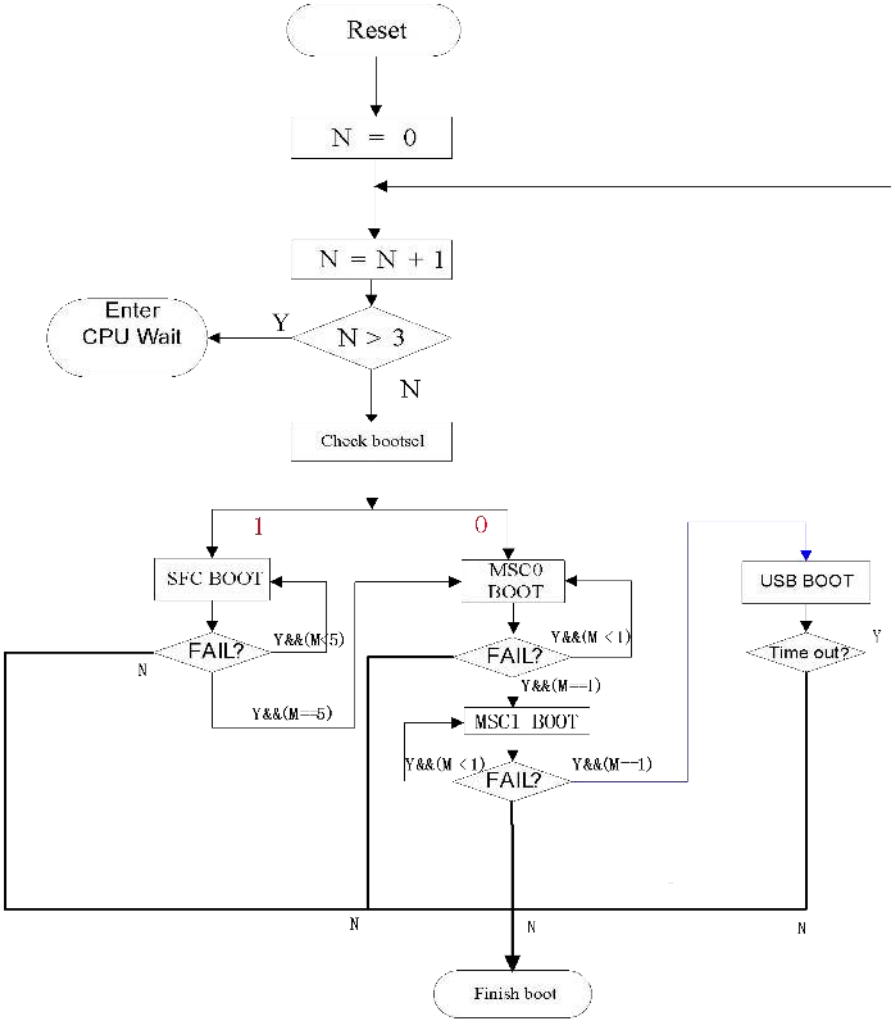



**Figure3- 2 Boot sequence diagram of T31ZX**

As shown in boot sequence Block Diagram， After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[0] to determine the boot method.

2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , …, and finally 1024th page will be tried in consecutive order.

3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.

4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the maximum 100KB code from SPI NAND/NOR flash to cache and jump to it.