Using the TPS51206EVM-745, 2-A Peak Sink/Source DDR Termination Regulator With VTTREF Buffered Reference for DDR2, DDR3, DDR3L, and DDR4

The TPS51206EVM-745 evaluation module (EVM) uses the TPS51206. The TPS51206 is a sink/source double data rate (DDR) termination regulator with VTTREF buffered reference output. It is specifically designed for low-input voltage, low cost, low external component count systems where space is a key consideration.

Contents

1 Description 3
1.1 Typical Applications 3
1.2 Features 3
2 Electrical Performance Specifications 3
3 Schematics 5
4 Test Setup 7
4.1 Test Equipment 7
4.2 Recommended Wire Gauge 7
4.3 Recommended Test Setup 7
5 Configurations 8
5.1 Transient Load Selection 8
5.2 Source Transient Load Selection 9
5.3 Sink Transient Load Selection 9
5.4 S1, S2 Enable Selection 9
6 Test Procedure 9
6.1 DDR2 (0.9VTT)/DDR3 (0.75VTT)/DDR3L (0.675VTT)/DDR4 (0.6VTT) Source Load Regulation 9
6.2 DDR2 (0.9VTT)/DDR3 (0.75VTT)/DDR3L (0.675VTT)/DDR4 (0.6VTT) Sink/Source Current Transient 10
6.3 DDR2 (0.9VTT)/DDR3 (0.75VTT)/DDR3L (0.675VTT)/DDR4 (0.6VTT) Loop Stability Measurement 10
6.4 List of Test Points 10
6.5 Equipment Shutdown 11
7 Performance Data and Typical Characteristic Curves 11
7.1 VTT Load Regulation 11
7.2 VTTREF Load Regulation 13
7.3 VTT Dropout Voltage 15
7.4 VTT Sink/Source Load Transient 17
7.5 DDR3(0.75VTT) S5 Enable Turnon/Turnoff 19
7.6 DDR3 (0.75VTT) S3 Enable Turnon/Turnoff 20
7.7 DDR3 (0.75VTT) Bode Plot 21
8 EVM Assembly Drawing and PCB Layout 21
9 Bill of Materials 25

List of Figures

1 TPS51206EVM-745, Schematic 1 5
2 TPS51206EVM-745, Schematic 2 6

3 TPS51206EVM-745 Recommended Test Setup 8
4 DDR2(0.9VTT) Load Regulation 11
5 DDR3 (0.75VTT) Load Regulation 11
6 DDR3L (0.675VTT) Load Regulation 12
7 DDR4 (0.6VTT) Load Regulation 12
8 DDR2 (0.9VTTREF) Load Regulation 13
9 DDR3 (0.75VTTREF) Load Regulation 13
10 DDR3L (0.675VTTREF) Load Regulation 14
11 DDR4 (0.6VTTREF) Load Regulation 14
12 DDR2 (0.9VTT) Dropout Voltage 15
13 DDR3 (0.75VTT) Dropout Voltage 15
14 DDR3L (0.675VTT) Dropout Voltage 16
15 DDR4 (0.6VTT) Dropout Voltage 16
16 DDR2 (0.9VTT) 1.8-A Sink/Source 17
17 DDR3 (0.75VTT) 1.5-A Sink/Source 17
18 DDR3L (0.75VTT) 1.35-A Sink/Source 18
19 DDR4 (0.6VTT) 1.2-A Sink/Source 18
20 DDR3 (0.75VTT) S5 Enable Turnon 19
21 DDR3 (0.75VTT) S5 Enable Turnoff 19
22 DDR3 (0.75VTT) S3 Enable Turnon 20
23 DDR3 (0.75VTT) S3 Enable Turnoff 20
24 DDR3 Bode plot 21
25 TPS51206EVM-745 Top Layer Assembly Drawing 22
26 TPS51206EVM-745 Top Layer 22
27 TPS51206EVM-745 Internal Layer 1 23
28 TPS51206EVM-745 Internal Layer 2 23
29 TPS51206EVM-745 Bottom Layer 24
30 TPS51206EVM-745 Bottom Layer Assembly 24

List of Tables

1 TPS51206EVM-745 Electrical Performance Specifications 3
2 Transient Load Selection 8
3 Source Transient Load Selection 9
4 Sink Transient Load Selection 9
5 S3, S5 Enable Selection 9
6 Functions of Each Test Point 10
7 Bill of Materials 25

1 Description

The TPS51206EVM-745 is designed to provide proper termination voltage and a 10-mA buffered reference voltage for DDR memory which covers DDR2 (0.9VTT), DDR3 (0.75VTT), DDR3L (0.675VTT) and DDR4 (0.6VTT) specifications with minimal external components.

1.1 Typical Applications

- DDR2/DDR3/DDR3L/DDR4 memory power supplies
- SSTL_18, SSTL_15, SSTL_135, and HSTL termination

1.2 Features

- VDD voltage: support 5-V rail and 3.3-V rail
- VLDOIN, VDDQ voltage range: 1.2 V–1.8 V
- Build-in, onboard transient load (with both sinking and sourcing capability) to emulate the sink/source transient behavior which helps to evaluate the dynamic performance. For ease of use, both load step and timing of transient can be modified by onboard resistors.
  - DDR2 (0.9VTT): ± 1.8-A sink/source transient load
  - DDR3 (0.75VTT): ± 1.5-A sink/source transient load
  - DDR3L (0.675VTT): ± 1.35-A sink/source transient load
  - DDR4 (0.6VTT): ± 1.2-A sink/source transient load
- Switch S1, S2 for S3 and S5 Enable function
- Convenient test points for probing VTT, VTTREF, CLK_IN and loop response testing
- Four-layer, printed-circuit board (PCB) with all the components on the bottom side

2 Electrical Performance Specifications

Table 1. TPS51206EVM-745 Electrical Performance Specifications(1)

Parameter	Test Conditions	Min	Typ	Max	Units
Input Characteristics					
VDD voltage range			5/3.3		V
VDDQ voltage range		1.2		1.8	V
VLDOIN voltage range		VTT+0.4		3.5	V
VTT and VTTREF Termination Voltage					
DDR2 (0.9VTT)	VTT		0.9		V
	VTTREF		0.9		
DDR3 (0.75VTT)	VTT		0.75		V
	VTTREF		0.75		V
DDR3L (0.675VTT)	VTT		0.675		V
	VTTREF		0.675		V
	VTT		0.6		V
DDR4 (0.6VTT)	VTTREF		0.6		V
VTT and VTTREF Termination Current					
VTT termination current(I_{VTT})	For DDR2(0.9VTT) and DDR3(0.75VTT)	-2		2	A
	For DDR3L(0.675VTT) and DDR4(0.6VTT)	–1.5		1.5	
VTTREF termination current(IV_{TTREF})		–10		10	mA
VTT Current Limit					
VTT sink current limit		2			A
VTT source current limit		2			A

(1) Note: Jumpers set to default locations, See Section 5 of this user's guide

Table 1. TPS51206EVM-745 Electrical Performance Specifications[(1)] (continued)

Parameter	Test Conditions	Min	Typ	Max	Units
VTT and VTTREF Termination Voltage Tolerance					
VTT termination voltage tolerance	$\|I_{VTT}\|$ < 2 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	–40		40	mV
	$\|I_{VTT}\|$ < 1.5 A, 1.2 V ≤ $V_{VDDQSNS}$ < 1.4 V	–40		40	mV
VTT termination voltage tolerance	$\|I_{VTTREF}\|$ < 10 mA, 1.5 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49%		51%	
	$\|I_{VTTREF}\|$ < 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ < 1.5 V	48.75%		51.25%	
Operating temperature			25		ºC

3 Schematics

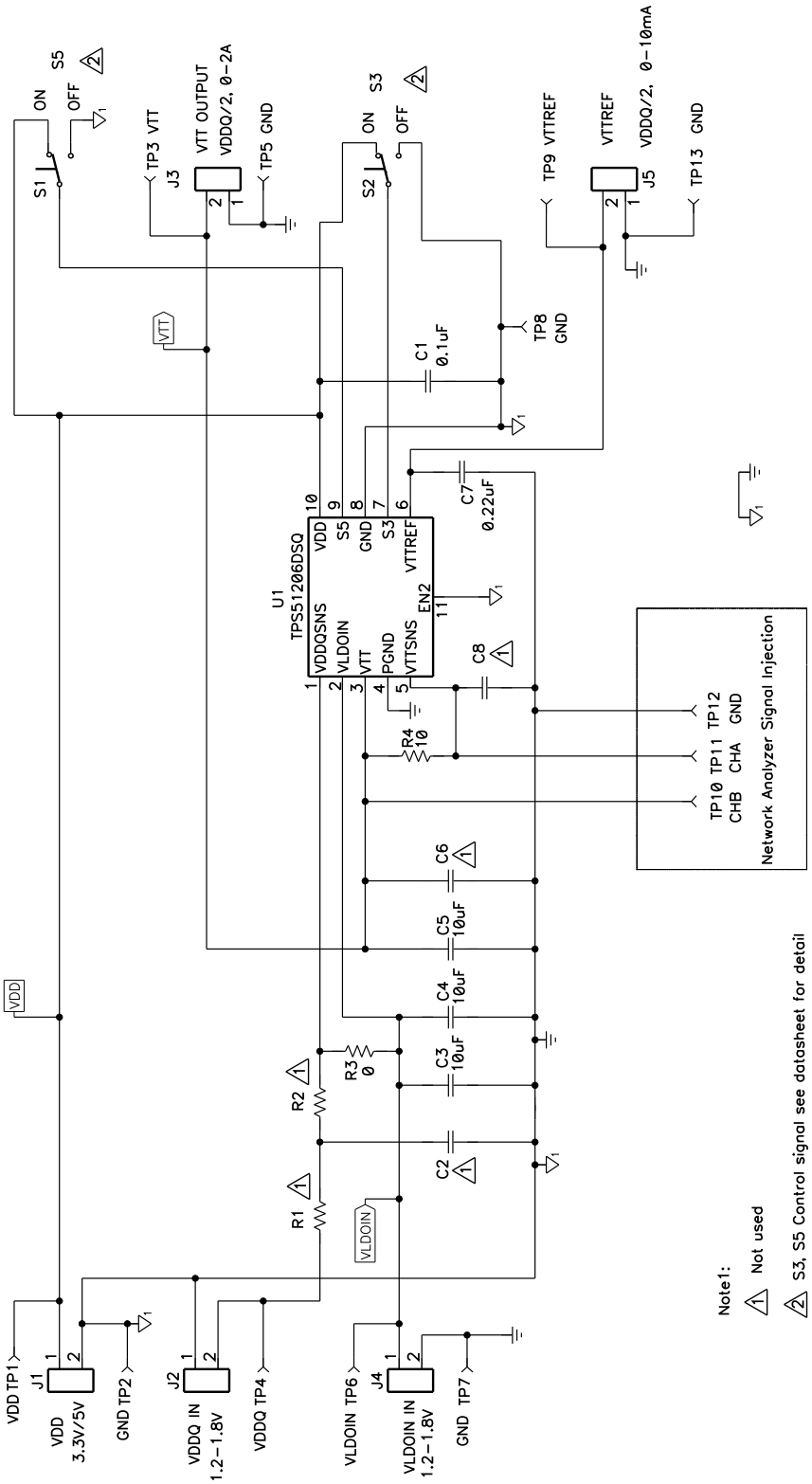


Figure 1. TPS51206EVM-745, Schematic 1

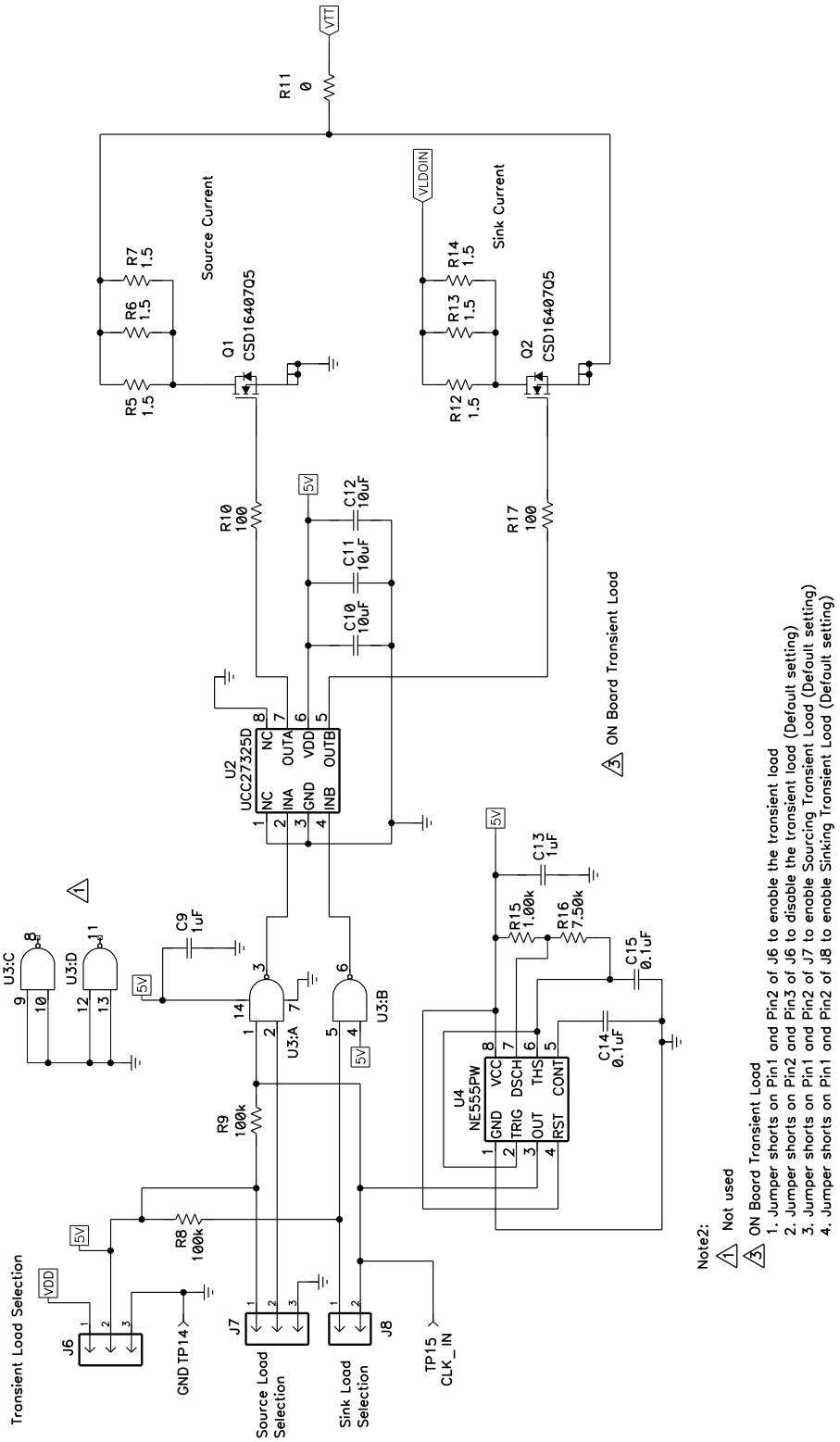


Figure 2. TPS51206EVM-745, Schematic 2

4 Test Setup

4.1 Test Equipment

4.1.1 Voltage Source

- **VDD:** The VDD dc Source1 must be a 0-V to 10-V variable dc source capable of supplying 1 Adc.
- **VLDOIN:** The VLDOIN DC Source2 must be a 0-V to 10-V variable dc source capable of supplying 10 Adc.

4.1.2 Meters

- V1: dc voltmeter for VDD at TP1 (VDD) and TP2 (GND)
- V2: dc voltmeter for VLDOIN at TP6 (VLDOIN) and TP7 (GND)
- V3: dc voltmeter for VTT at TP3 (VTT) and TP5 (GND)
- V4: dc voltmeter for VTTREF at TP9 (VTTREF) and TP13 (GND)

4.1.3 Load

- LOAD: The VTT load must be an electronic constant-current load capable of 0 A to 10 A at 0.9 Vdc

4.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure VTT sink/source current transient. The oscilloscope must be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 200- µs/division horizontal resolution, 50-mV/division vertical resolution for VTT transient test. Test point TP3 (VTT) and TP5 (GND) can be used to measure VTT transient. Set horizontal cursor to measure transient load regulation.

4.2 Recommended Wire Gauge

4.2.1 VDD dc Source1 to J1

The connection between the voltage dc Source1 and J1 of the EVM can carry as much as 0.5-Adc current. The recommended wire size is AWG 18 with the total length of wire less than 4 feet (2-foot input, 2-foot return).

4.2.2 VLDOIN dc Source2 to J4

The connection between the voltage dc Source2 and J4 of the EVM can carry as much as 5-Adc current. The recommended wire size is AWG 16 with the total length of wire less than 4 feet (2-foot input, 2-foot return).

4.2.3 VTT Load to J3

The connection between the VTT load and J3 of the EVM can carry as much as 5-Adc current. The recommended wire size is AWG 16 with the total length of wire less than 4 feet (2-foot input, 2-foot return).

4.3 Recommended Test Setup

Figure 3 is the recommended test setup to evaluate the TPS51206EVM-745. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM.

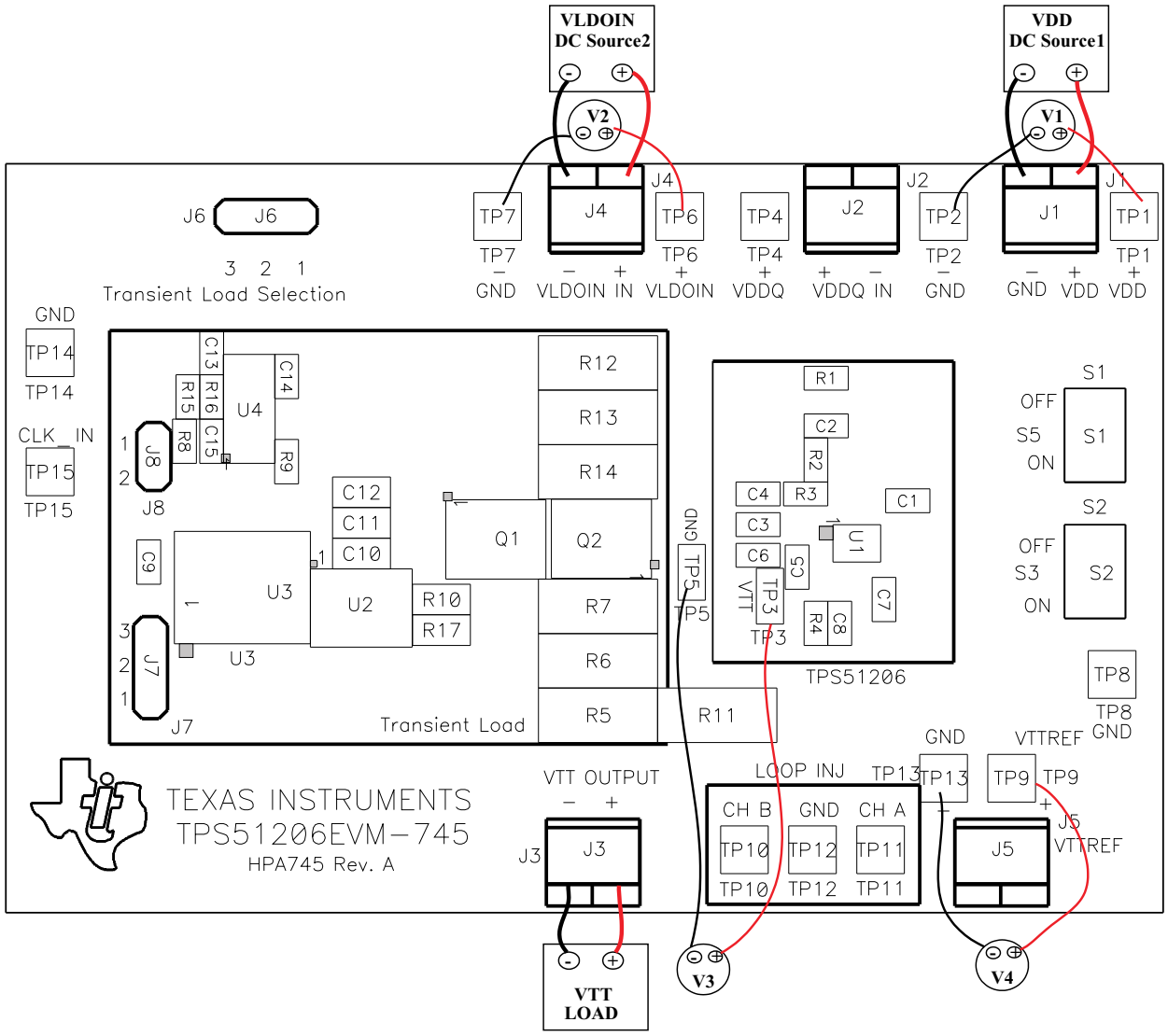


Figure 3. TPS51206EVM-745 Recommended Test Setup

5 Configurations

All jumper selections must be made prior to applying power to the EVM. Users can configure this EVM per the following configurations.

5.1 Transient Load Selection

The transient load selection can be set by J6.
Default setting: Jumper shorts on Pin2 and Pin3 of J6 to disable transient load.

Table 2. Transient Load Selection

Jumper Set to	Transient Load
1-2 pin shorted	Enable
2-3 pin shorted	**Disable**

5.2 Source Transient Load Selection

The source transient load selection can be set by J7.
Default setting: Jumper shorts on Pin1 and Pin2 of J7 to enable source transient load.

Table 3. Source Transient Load Selection

Jumper Set to	Transient Load
1-2 pin shorted	**Enable**
2-3 pin shorted	Disable

5.3 Sink Transient Load Selection

The sink transient load selection can be set by J8.
Default setting: Jumper shorts on Pin1 and Pin2 of J8 to enable sink transient load.

Table 4. Sink Transient Load Selection

Jumper Set to	Transient Load
1-2 pin shorted	**Enable**
No Jumper shorted	Disable

5.4 S1, S2 Enable Selection

The controller can be enabled and disabled by switch S1 and S2.
Default setting: Push S1 and S2 to the TOP (OFF position) to disable the controller.

Table 5. S3, S5 Enable Selection

S2 Switch(S3) Set to	S1 Switch(S5) Set to	VTTREF	VTT
ON position	ON position	ON	ON
OFF position	ON position	ON	OFF(High-Z)
OFF position	**OFF position**	**OFF(Discharge)**	**OFF(Discharge)**

6 Test Procedure

6.1 DDR2 (0.9VTT)/DDR3 (0.75VTT)/DDR3L (0.675VTT)/DDR4 (0.6VTT) Source Load Regulation

1. Ensure jumper shorts on Pin2 and Pin3 of J6.
2. Ensure jumper shorts on Pin1 and Pin2 of J7, J8.
3. Ensure switches S1 and S2 to OFF position.
4. Set VTT load to 0 A.
5. Increase VDD (VDD dc Source1) from 0 V to 5 V at J1. This is the bias supply needed for TPS51206 operation. Using V1, verify VDD voltage between 4.8 V and 5 V.
6. Increase VLDOIN voltage (VLDOIN dc Source2) from 0 V to 1.8 V for DDR2 or 1.5 V for DDR3 or 1.35 V for DDR3 or 1.2 V for DDR3L at J4. This is the LDO input. Using V2, verify VLDOIN voltage.
7. Set switches S1, S2 to ON position.
8. Use V3, V4 to measure VTT, VTTREF voltage.
9. Increase load from 0 A to 1.5 A.
10. Verify V2 and adjust VLDOIN if necessary.
11. Use V3, V4 to measure VTT, VTTREF voltage.
12. Decrease load to 0 A.
13. Set switches S1, S2 to OFF position.

6.2 DDR2 (0.9VTT)/DDR3 (0.75VTT)/DDR3L (0.675VTT)/DDR4 (0.6VTT) Sink/Source Current Transient

1. Remove VTT load from J3.
2. Remove V3 from TP3 (VTT) and TP5 (GND).
3. Add scope probe on TP3 (VTT) and TP5 (GND).
4. Remove jumper on Pin2 and Pin3 of J6 and put this jumper on Pin1 and Pin2 of J6.
5. Set switches S1, S2 to ON position.
6. TPS51206 is now operating at sink/source load transient.
7. Verify V2 and adjust VLDOIN if necessary.
8. Use scope probe at TP3 (VTT) and TP5 (GND) to monitor VTT load transient operation, and use cursor to make measurement. The waveform is shown in Section 7.4.
9. Set switch S1, S2 to OFF position.
10. Decrease dc source 1.2 V to 0 V.

6.3 DDR2 (0.9VTT)/DDR3 (0.75VTT)/DDR3L (0.675VTT)/DDR4 (0.6VTT) Loop Stability Measurement

TPS51206EVM-745 contains an R4 (10-Ω) series resistor in the feedback loop for loop response analysis.

1. Set up EVM as described in Section 4 and Figure 3.
2. Connect isolation transformer to test points marked TP11 and TP10.
3. Connect input signal amplitude measurement probe (channel A) to TP11. Connect output signal amplitude measurement probe (channel B) to TP10.
4. Connect ground lead of channel A and channel B to TP12.
5. Inject approximately 50-mV or less signal through the isolation transformer.
6. Sweep the frequency from 1 kHz to 1 MHz with 10-Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect isolation transformer from bode plot test points before making other measurements. Signal injection into feedback may interfere with accuracy of other measurements.

6.4 List of Test Points

Table 6. Functions of Each Test Point

Test Points	Name	Description
TP1	VDD	Device power supply input (3.3 V or 5 V)
TP2	GND	Ground
TP3	VTT	VTT Output
TP4	VDDQ	VDDQSNS sense input, when VLDOIN is different from VDDQSNS voltage
TP5	GND	Ground
TP6	VLDOIN	Power supply input for VTT/VTTREF
TP7	GND	Ground
TP8	GND	Ground
TP9	VTTREF	VTTREF buffered reference output
TP10	CHB	Input B for loop injection
TP11	CHA	Input A for loop injection
TP12	GND	Ground
TP13	GND	Ground
TP14	GND	Ground
TP15	CLK_IN	Sink/source load transient timing signal

6.5 Equipment Shutdown

1. Shut down VDD dc Source1 and VLDOIN dc Source2
2. Shut down VTT load.
3. Shut down oscilloscope.

7 Performance Data and Typical Characteristic Curves

7.1 VTT Load Regulation

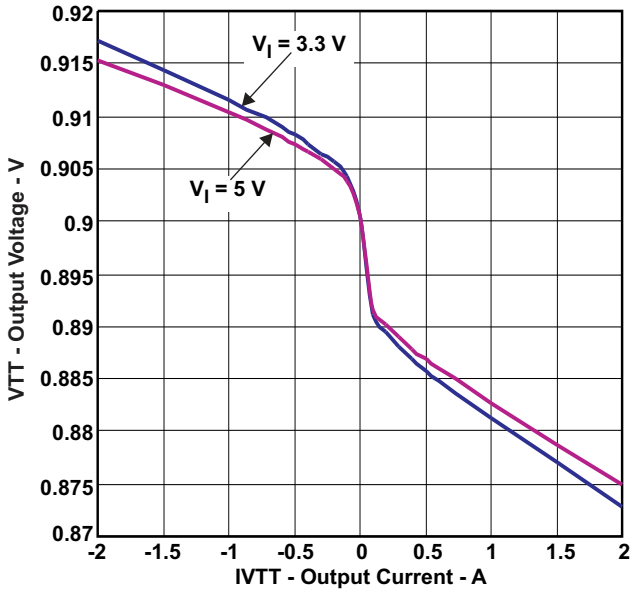


Figure 4. DDR2(0.9VTT) Load Regulation

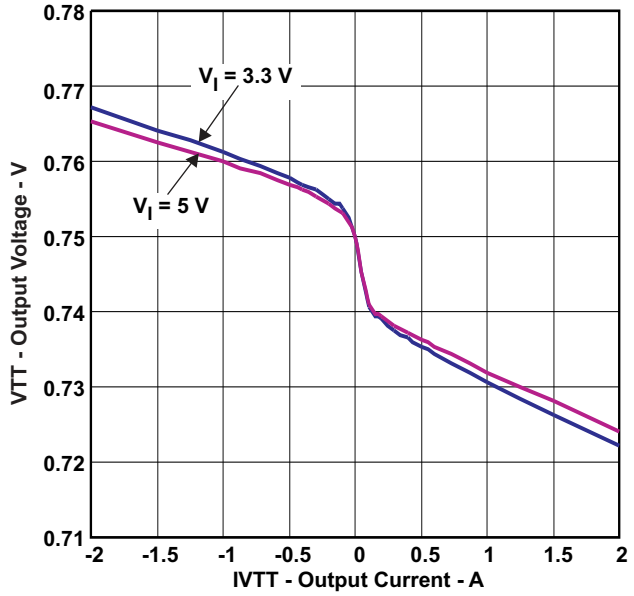


Figure 5. DDR3 (0.75VTT) Load Regulation

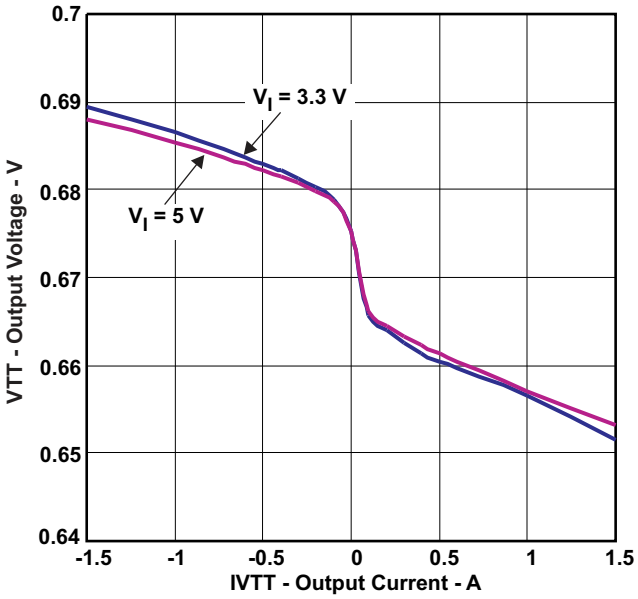


Figure 6. DDR3L (0.675VTT) Load Regulation

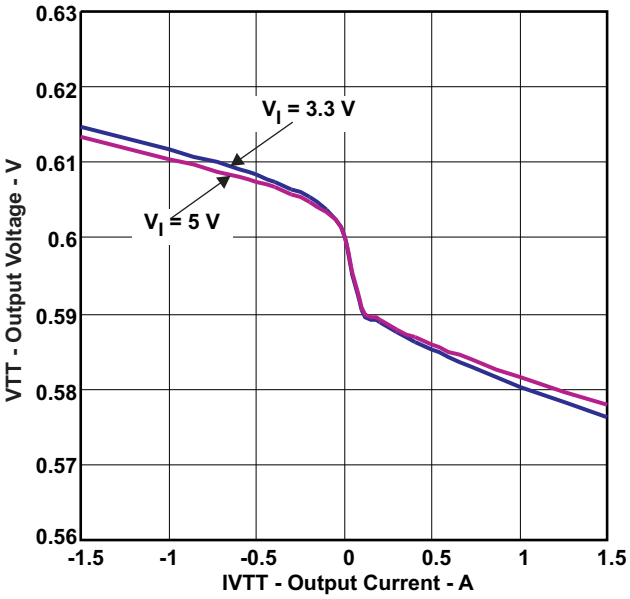


Figure 7. DDR4 (0.6VTT) Load Regulation

7.2 VTTREF Load Regulation

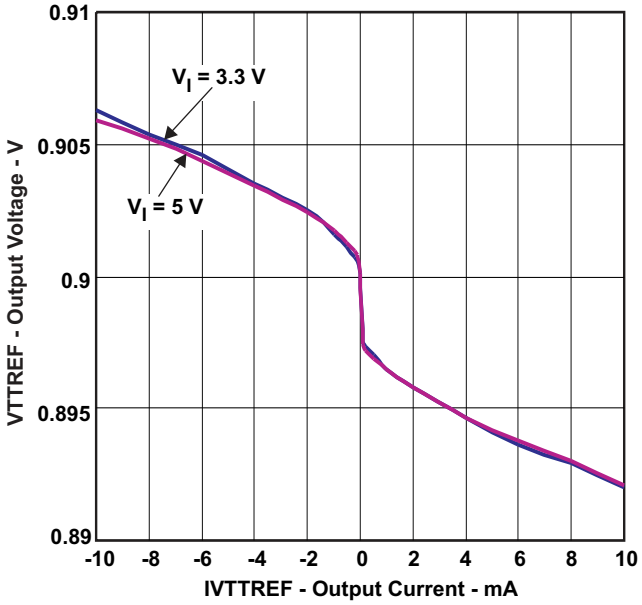


Figure 8. DDR2 (0.9VTTREF) Load Regulation

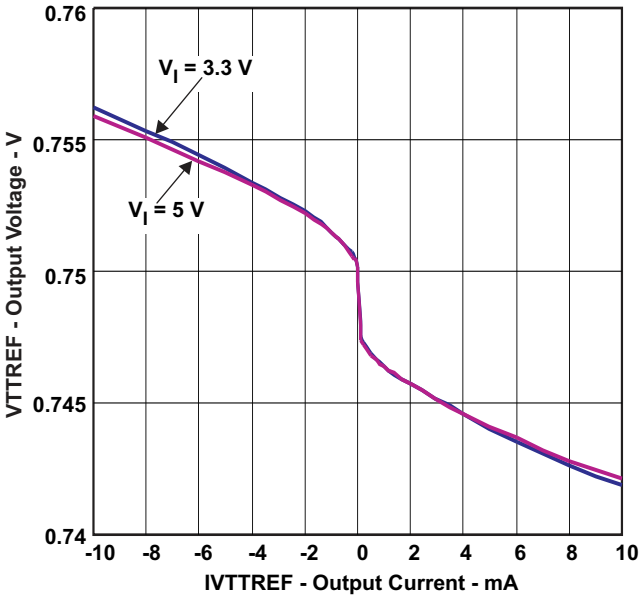


Figure 9. DDR3 (0.75VTTREF) Load Regulation

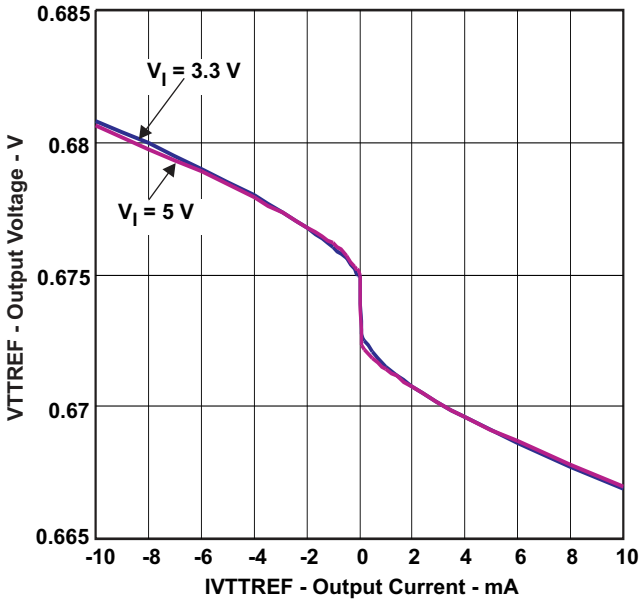


Figure 10. DDR3L (0.675VTTREF) Load Regulation

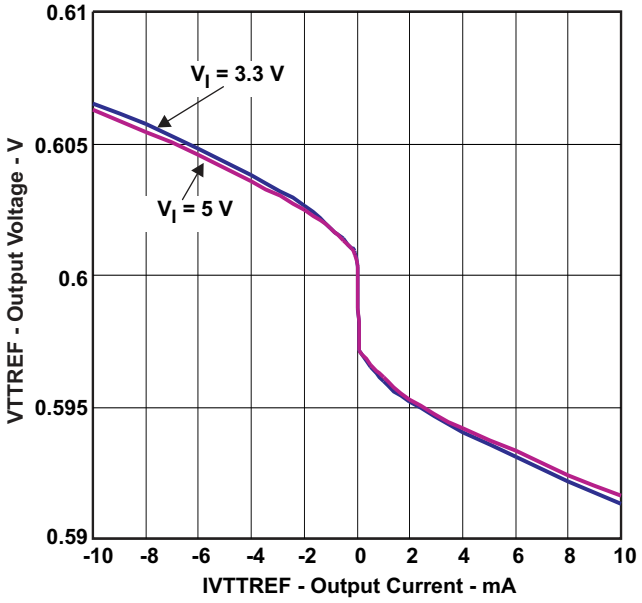


Figure 11. DDR4 (0.6VTTREF) Load Regulation

7.3 VTT Dropout Voltage

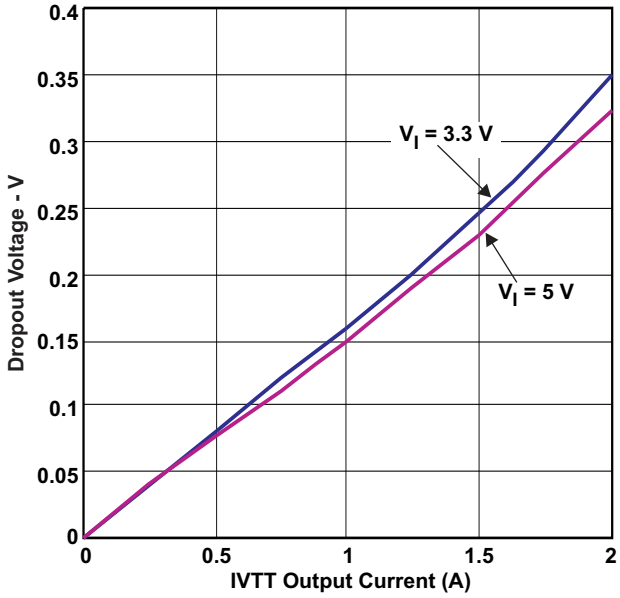


Figure 12. DDR2 (0.9VTT) Dropout Voltage

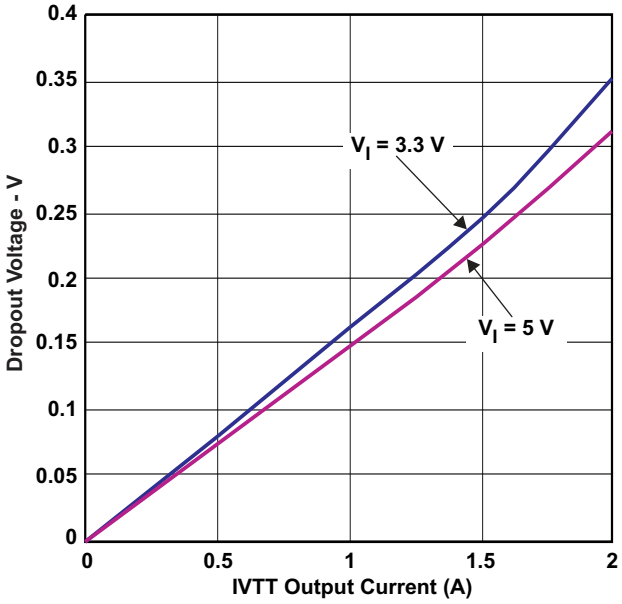


Figure 13. DDR3 (0.75VTT) Dropout Voltage

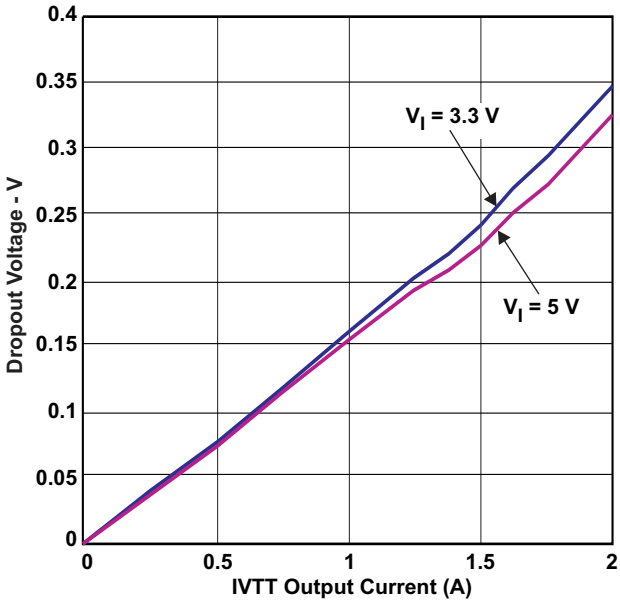


Figure 14. DDR3L (0.675VTT) Dropout Voltage

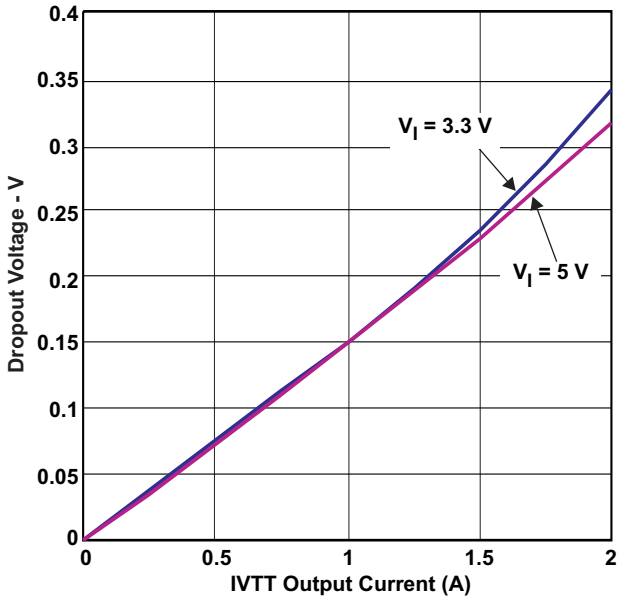


Figure 15. DDR4 (0.6VTT) Dropout Voltage

7.4 VTT Sink/Source Load Transient

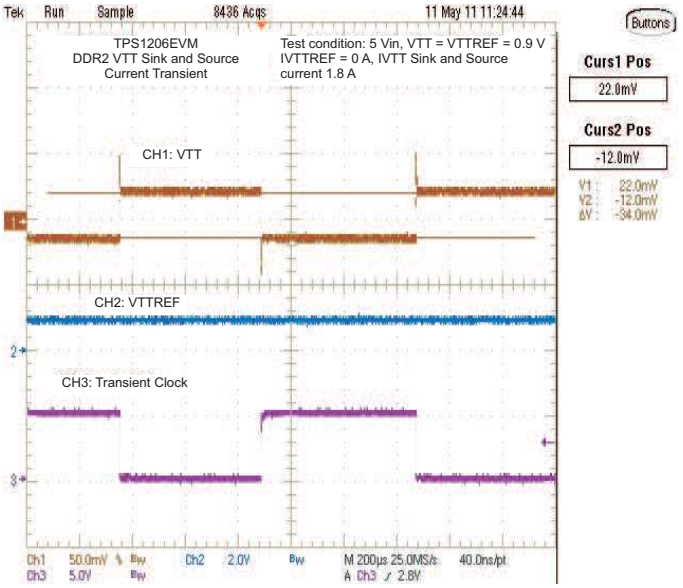


Figure 16. DDR2 (0.9VTT) 1.8-A Sink/Source

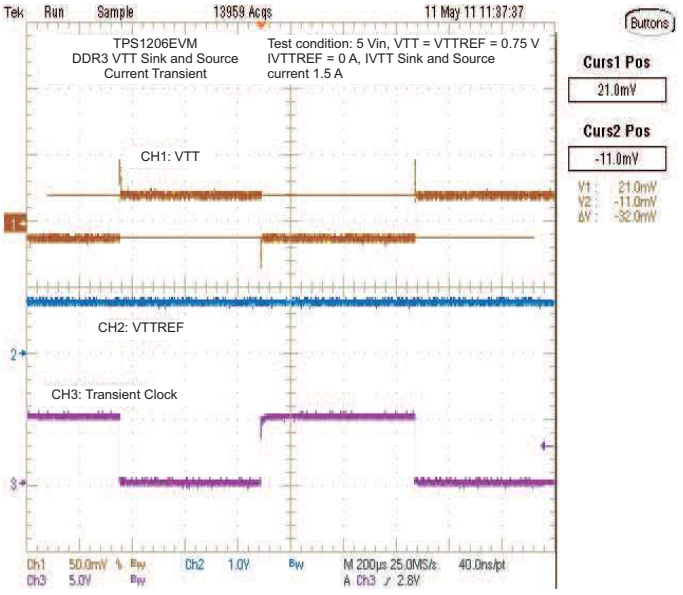


Figure 17. DDR3 (0.75VTT) 1.5-A Sink/Source

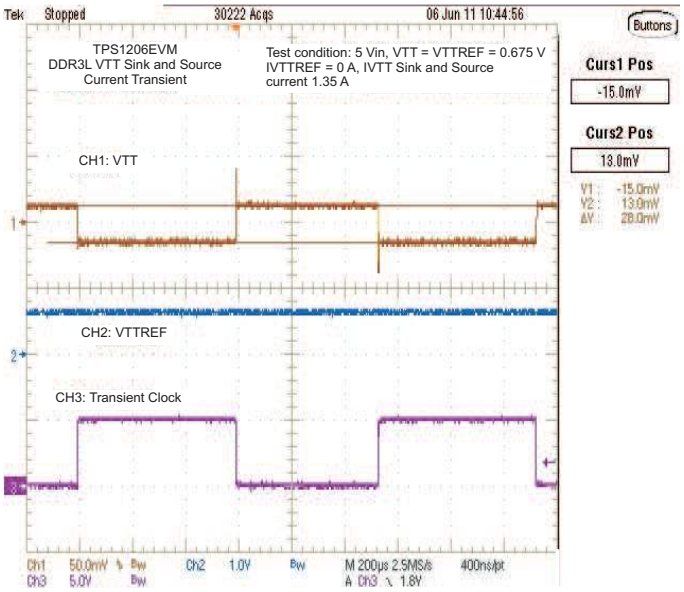


Figure 18. DDR3L (0.75VTT) 1.35-A Sink/Source

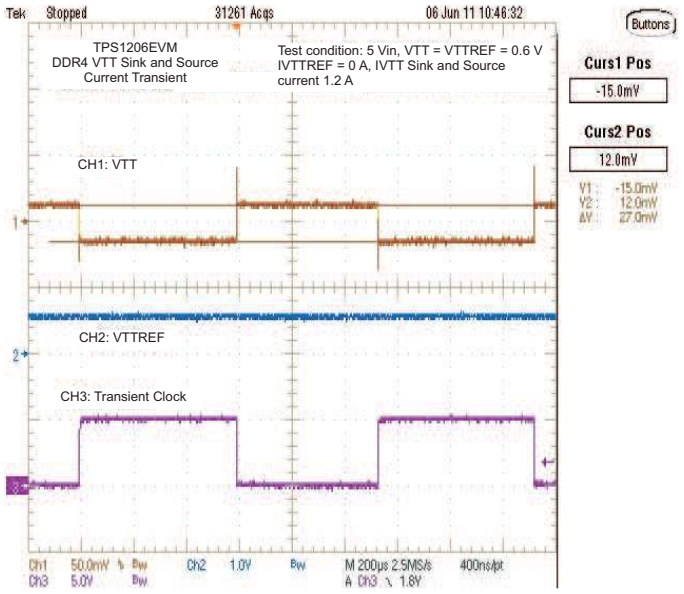


Figure 19. DDR4 (0.6VTT) 1.2-A Sink/Source

7.5 DDR3(0.75VTT) S5 Enable Turnon/Turnoff

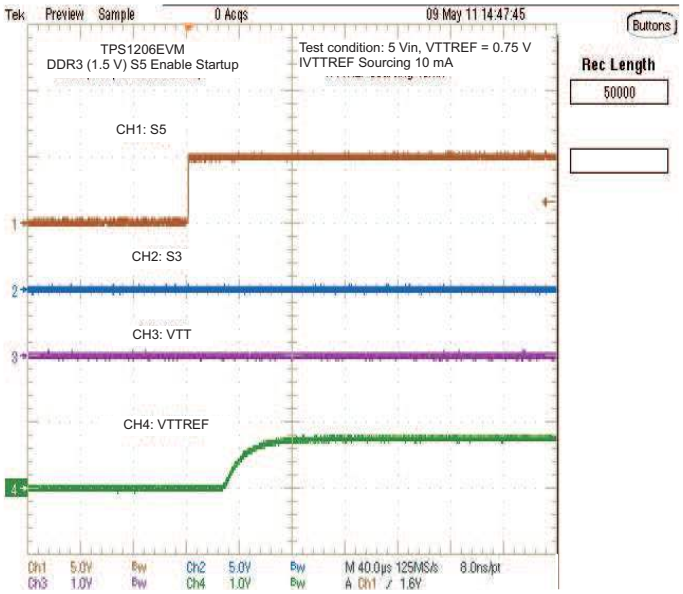


Figure 20. DDR3 (0.75VTT) S5 Enable Turnon

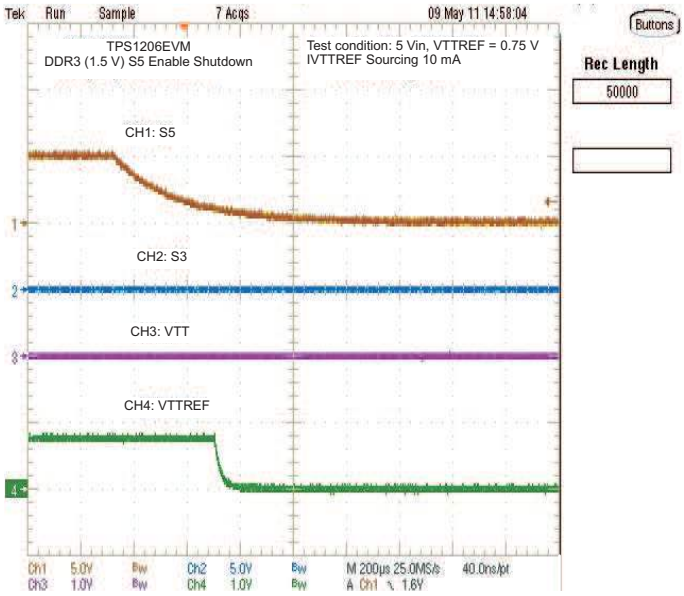


Figure 21. DDR3 (0.75VTT) S5 Enable Turnoff

7.6 DDR3 (0.75VTT) S3 Enable Turnon/Turnoff

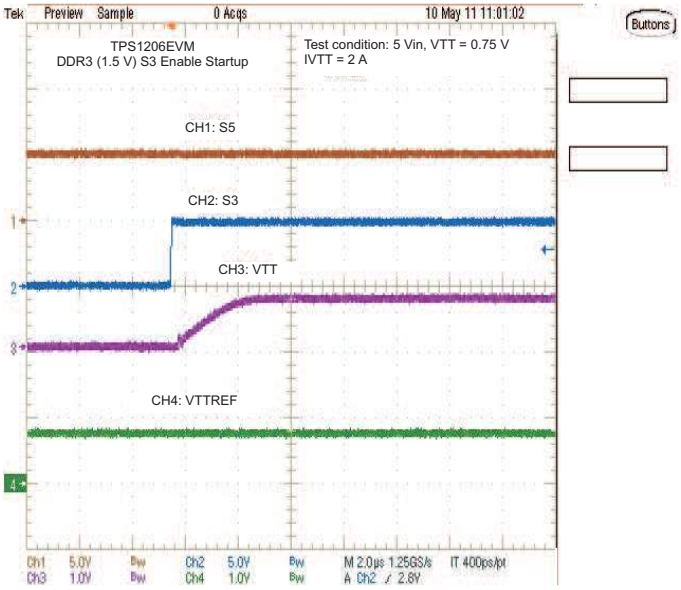


Figure 22. DDR3 (0.75VTT) S3 Enable Turnon

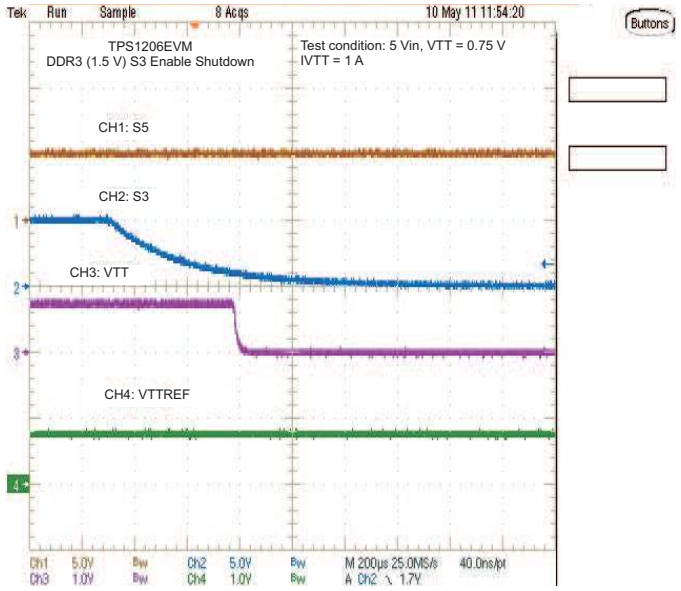
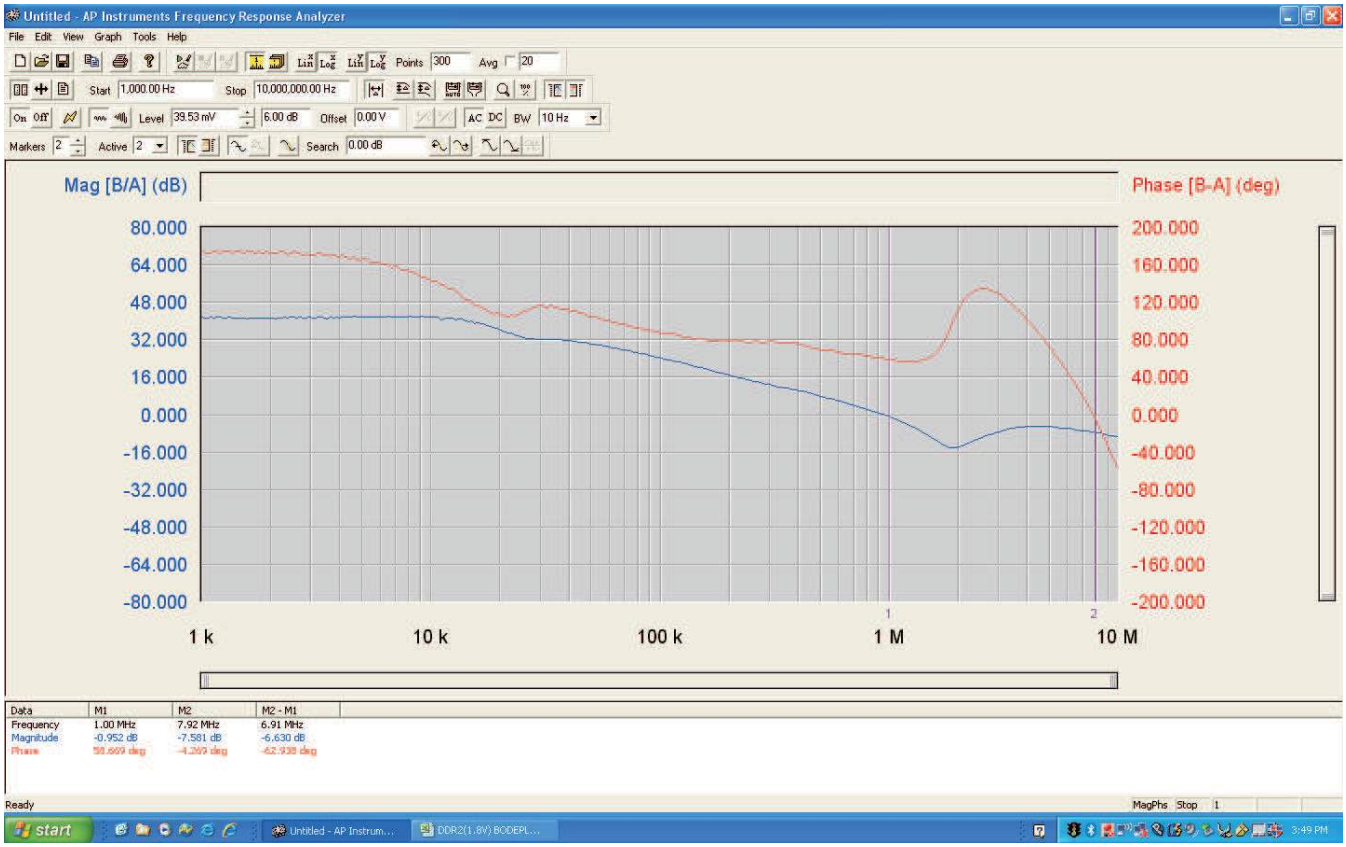


Figure 23. DDR3 (0.75VTT) S3 Enable Turnoff

7.7 DDR3 (0.75VTT) Bode Plot



Test condition: 5 Vin, VLDOIN = VDDQ = 1.5 V, VTT = VTTREF = 0.75 V, I_{VTT} = 2 A Source Current
Phase Margin: 58.7Deg, **Gain Margin:** 7.6dB, Crossover Frequency: 1MHz

Figure 24. DDR3 Bode plot

8 EVM Assembly Drawing and PCB Layout

Figure 25 through Figure 30 show the design of the TPS51206EVM-745 printed-circuit board. The EVM has been designed using a four-layer, 2-oz copper, printed-circuit board.

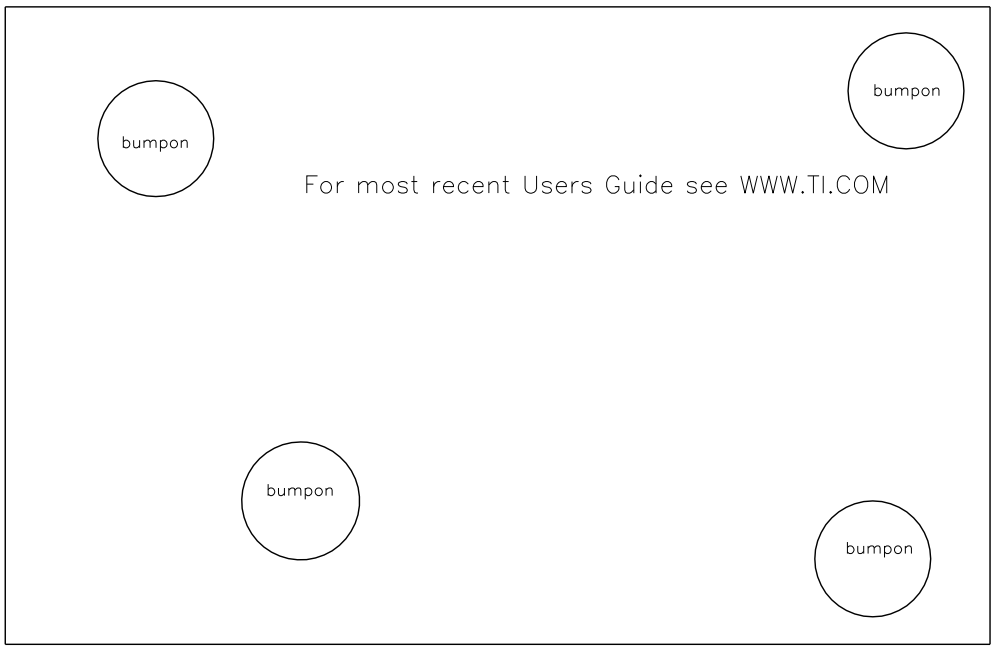


Figure 25. TPS51206EVM-745 Top Layer Assembly Drawing

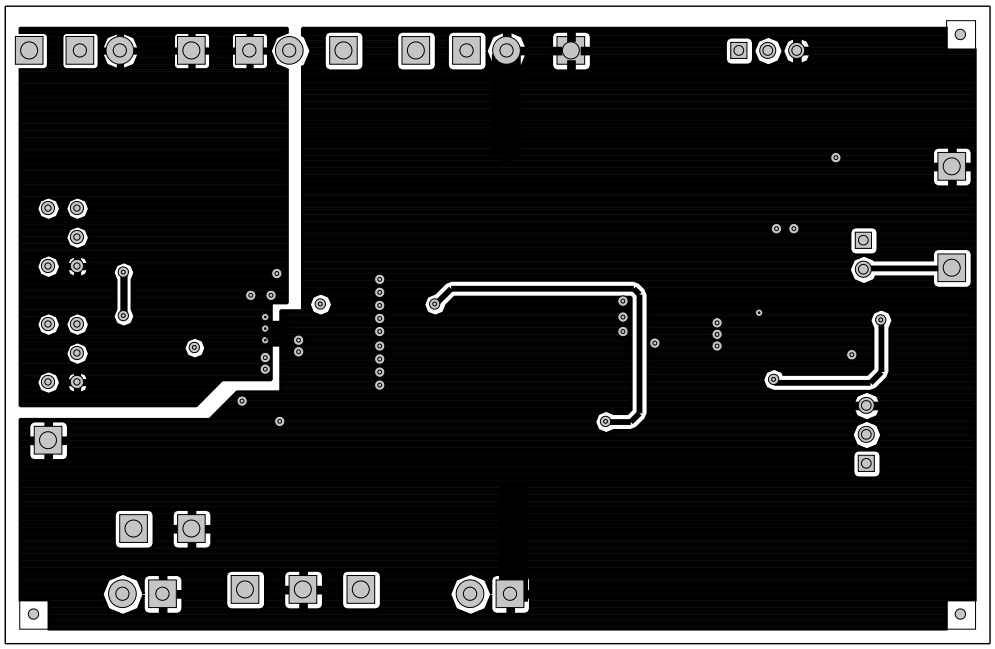


Figure 26. TPS51206EVM-745 Top Layer

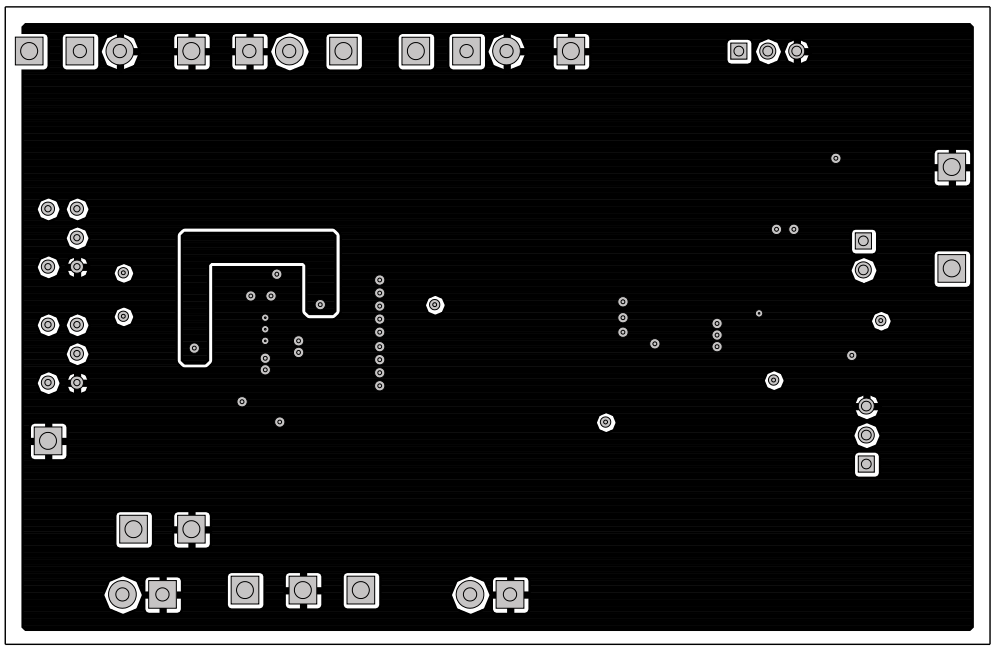


Figure 27. TPS51206EVM-745 Internal Layer 1

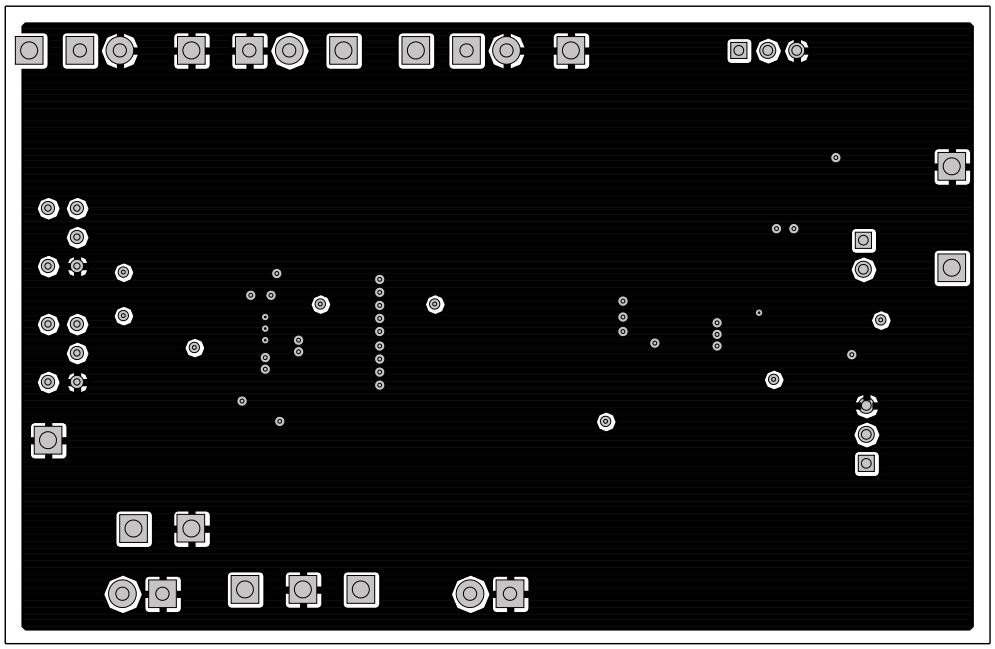


Figure 28. TPS51206EVM-745 Internal Layer 2

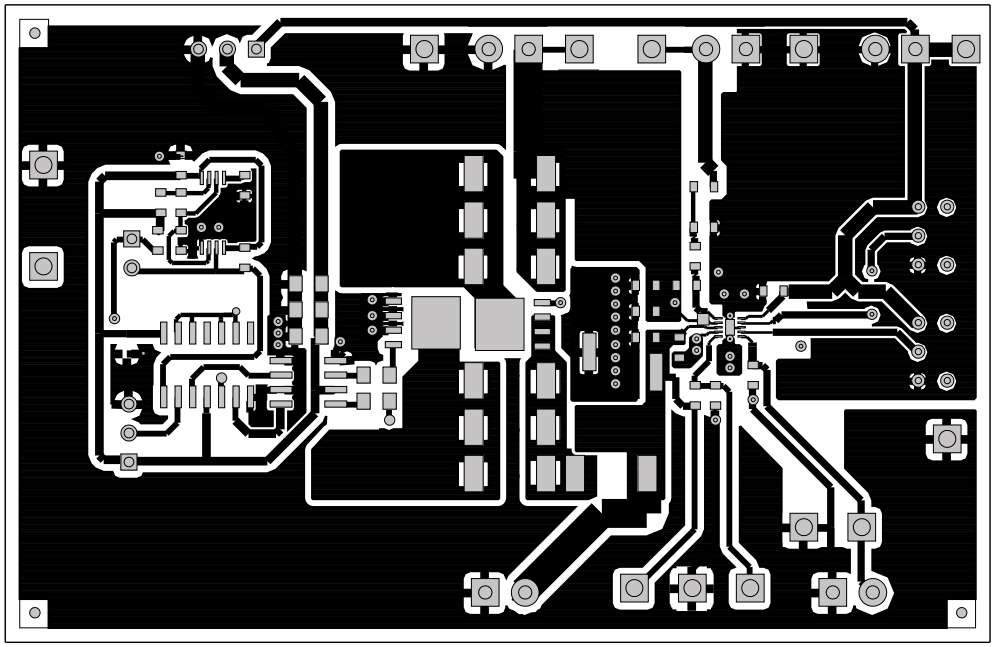


Figure 29. TPS51206EVM-745 Bottom Layer

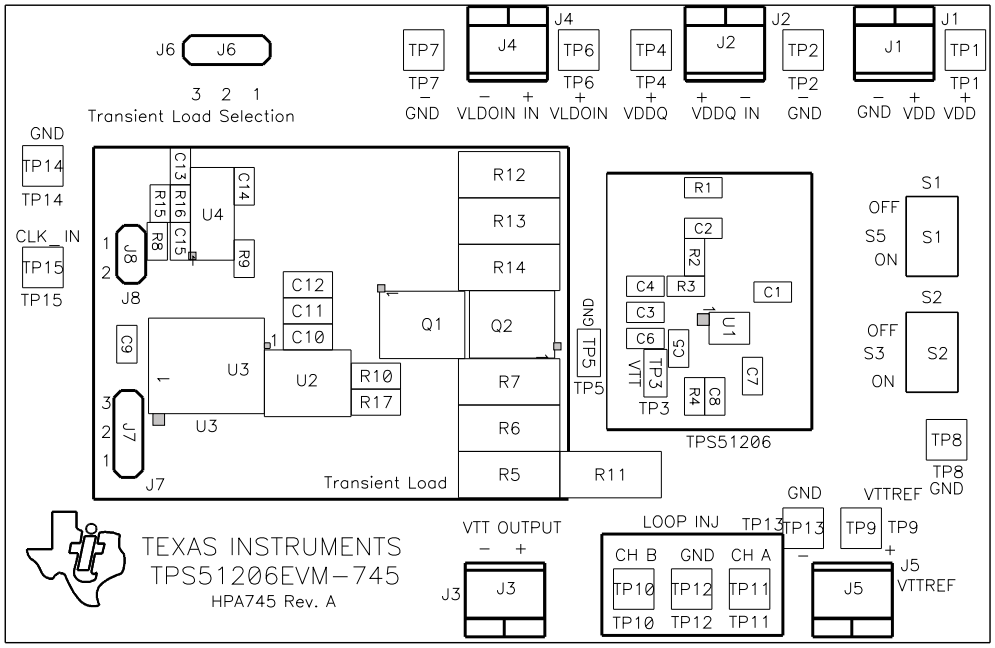


Figure 30. TPS51206EVM-745 Bottom Layer Assembly

9 Bill of Materials

Table 7 provides the EVM components list according to the schematics shown in Figure 1 and Figure 2.

Table 7. Bill of Materials

QTY	RefDes	Description	MFR	Part Number
3	C1, C14, C15	Capacitor, Ceramic, 0.1 µF, 10V, X7R, 20%, 0603	STD	STD
3	C10, C11, C12	Capacitor, Ceramic, 10 µF, 10V, X5R, 20%, 0805	STD	STD
3	C3, C4, C5	Capacitor, Ceramic, 10 µF, 10V, X5R, 20%, 0603	STD	STD
1	C7	Capacitor, Ceramic, 0.22 µF, 10V, X7R, 20%, 0603	STD	STD
2	C9, C13	Capacitor, Ceramic, 1 µF, 10V, X7R, 20%, 0603	STD	STD
2	Q1, Q2	MOSFET, Nch, 25V, 31A, 2.5mΩ	TI	CSD16407Q5
2	R10, R17	Resistor, Chip, 100, 1/10W, 5%, 0805	STD	STD
1	R11	Resistor, Chip, 0, 1W, 5%, 2512	STD	STD
1	R15	Resistor, Chip, 1.00k, 1/16W, 1%, 0603	STD	STD
1	R16	Resistor, Chip, 7.50k, 1/16W, 1%, 0603	STD	STD
1	R3	Resistor, Chip, 0, 1/16W, 5%, 0603	STD	STD
1	R4	Resistor, Chip, 10, 1/16W, 5%, 0603	STD	STD
6	R5, R6, R7, R12, R13, R14	Resistor, Chip, 1.5, 1W, 5%, 2512	STD	STD
2	R8, R9	Resistor, Chip, 100k, 1/16W, 1%, 0603	STD	STD
1	U1	IC, 2A Peak sink/source DDR termination regulator	TI	TPS51206DSQ
1	U2	IC, Dual, 4A high speed low side power MOSFET drivers	TI	UCC27325D
1	U3	IC, Quad, 2-Input Positive NAND Gates	TI	SN74AHCT00D
1	U4	IC, Precision Timer	TI	NE555PW

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 5.5 V and the output voltage range of 0.6 V to 1.8 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265