



**CY7C164**  
**CY7C166**

**16K x 4 Static RAM**

**Features**

- High speed  
— 15 ns
- Output enable ( $\overline{OE}$ ) feature (7C166)
- CMOS for optimum speed/power
- Low active power  
— 633 mW
- Low standby power  
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

**Functional Description**

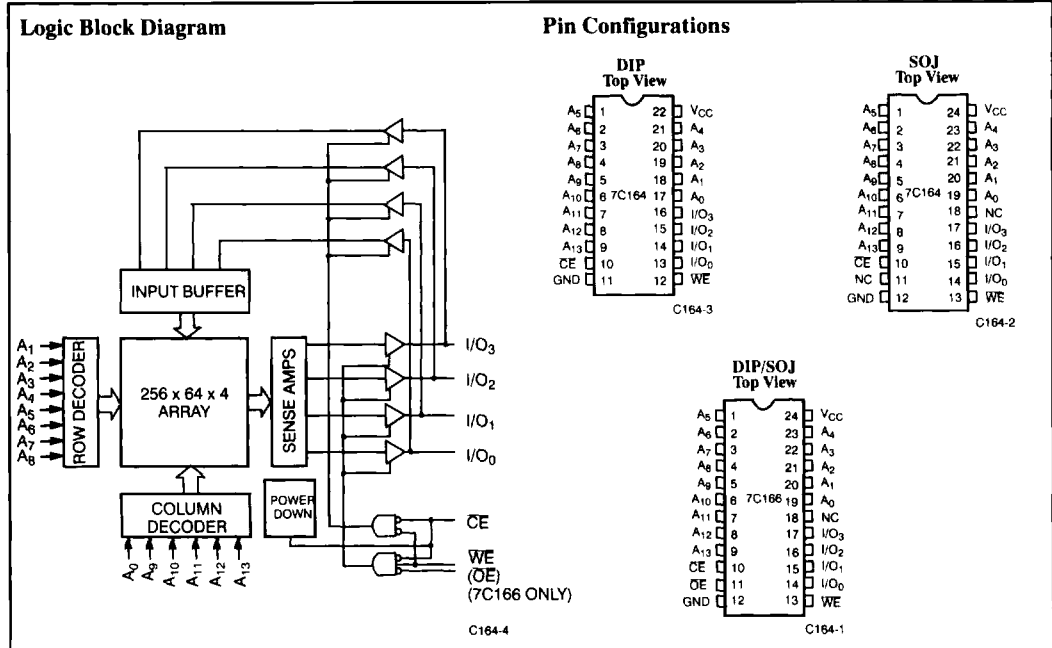
The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C166 has an active low output enable ( $\overline{OE}$ ) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW (and the output enable ( $\overline{OE}$ ) is LOW for the 7C166).

Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW (and  $\overline{OE}$  LOW for 7C166), while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data  $I/O$  pins.

The  $I/O$  pins stay in a high-impedance state when chip enable ( $\overline{CE}$ ) is HIGH (or output enable ( $\overline{OE}$ ) is HIGH for 7C166). A die coat is used to insure alpha immunity.



**Selection Guide<sup>(1)</sup>**

	7C164-12 7C166-12	7C164-15 7C166-15	7C164-20 7C166-20	7C164-25 7C166-25	7C164-35 7C166-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	160	115	80	70	70
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20

Shaded area contains preliminary information.

**Note:**

1. For military specifications, see the CY6C164A/CY7C166A datasheet.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to +7.0V  
 DC Input Voltage<sup>[2]</sup> ..... -0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

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**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	7C164-12 7C166-12		7C164-15 7C166-15		7C164-20 7C166-20		7C164-25, 35 7C166-25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	µA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	µA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		160		115		80		70	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current <sup>[4]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , Min. Duty Cycle = 100%		40		40		40		20	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current <sup>[4]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		20		20		20		20	mA

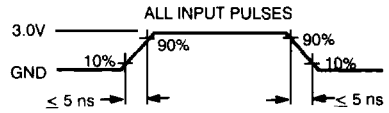
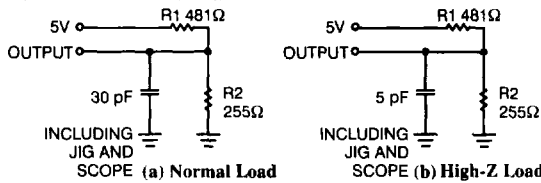
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**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

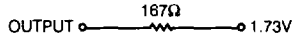
- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


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Equivalent to: THÉVENIN EQUIVALENT

C164-5

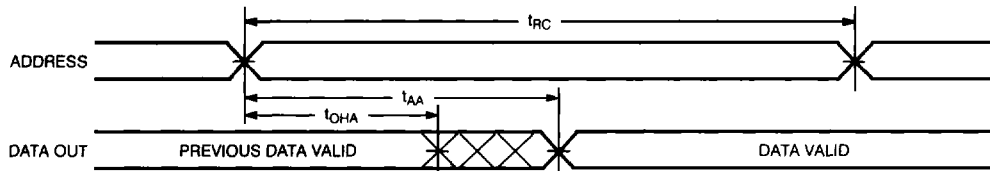

**Switching Characteristics Over the Operating Range<sup>[6]</sup>**

Parameter	Description	7C164-12 7C166-12		7C164-15 7C166-15		7C164-20 7C166-20		7C164-25 7C166-25		7C164-35 7C166-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE<sup>[9]</sup></b>												
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		12		15		20		25		35	ns
t <sub>OHA</sub>	Output Hold from Address Change	3		3		5		5		5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		10		10		12		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	7C166	0		3		3		3		3	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z	7C166	7		8		8		10		12	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>		3		3		5		5		5	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		7		8		8		10		15	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		20	ns
<b>WRITE CYCLE<sup>[9]</sup></b>												
t <sub>WC</sub>	Write Cycle Time	12		15		20		20		25		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		12		15		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	9		12		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		12		15		15		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		10		10		10		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>		3		5		5		5		5	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>		6		7		7		7		10	ns

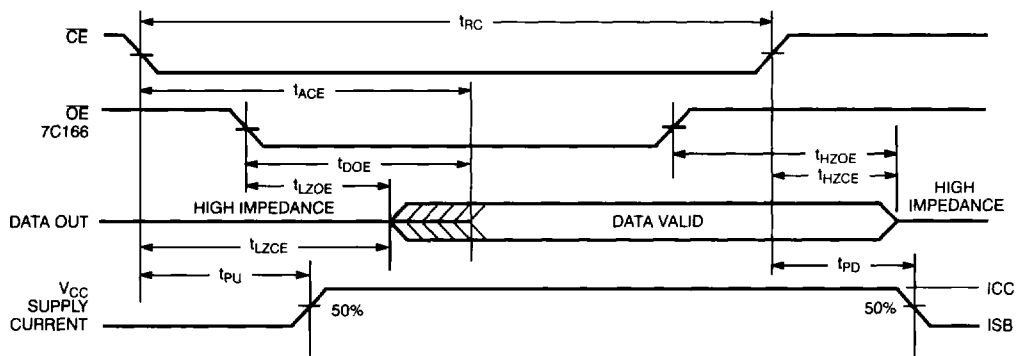
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**Notes:**

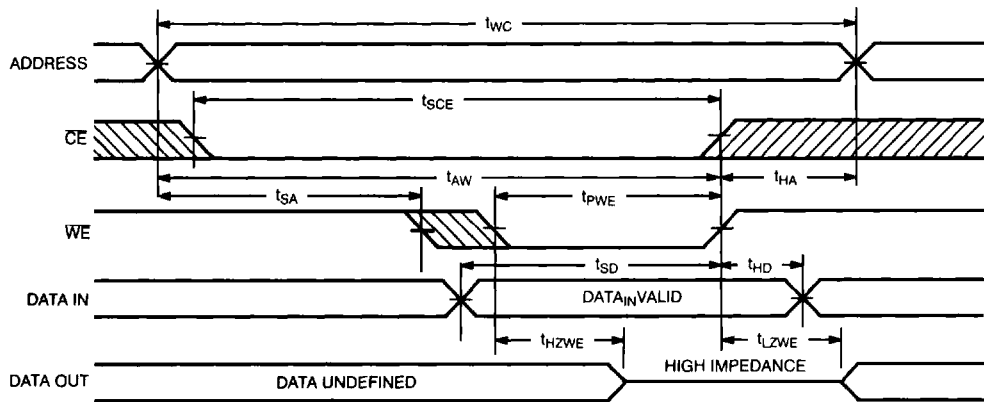
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device. These parameters are guaranteed by design and not 100% tested.
- t<sub>HZCE</sub> and t<sub>LZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**


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**Read Cycle No. 2<sup>[10, 12]</sup>**


C164-8

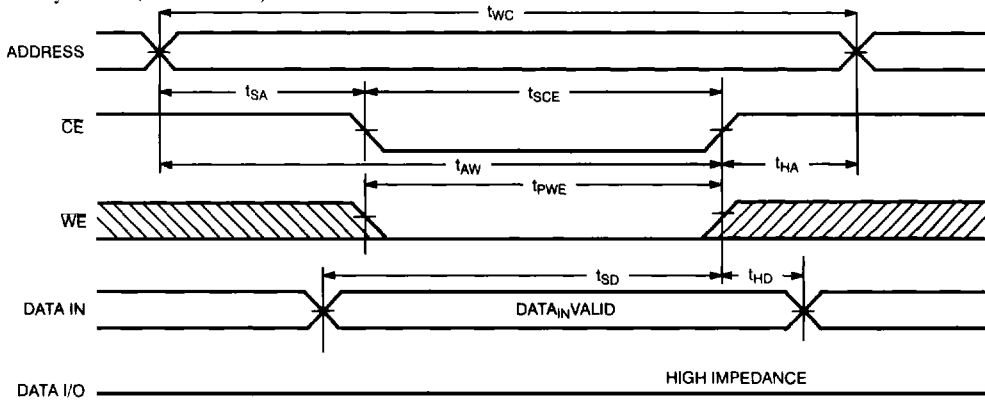
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[9, 13]</sup>**


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**Notes:**

10.  $\overline{WE}$  is HIGH for read cycle. 12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.  
 11. Device is continuously selected,  $\overline{CE} = V_{IL}$ . (7C166:  $\overline{OE} = V_{IL}$  also). 13. 7C166 only: Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

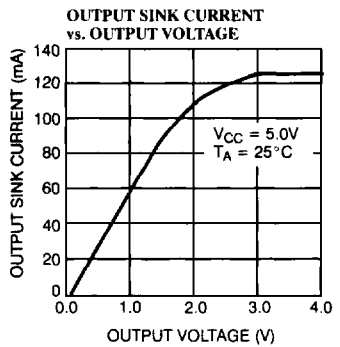
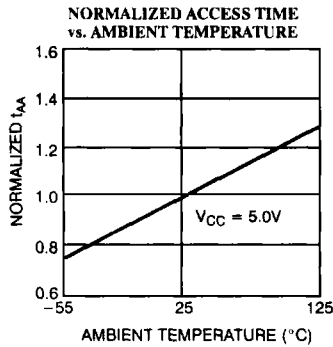
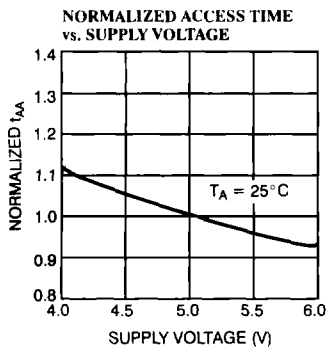
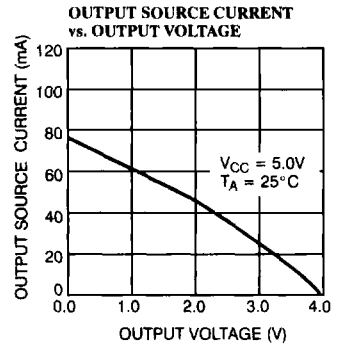
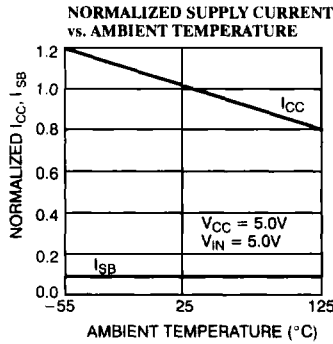
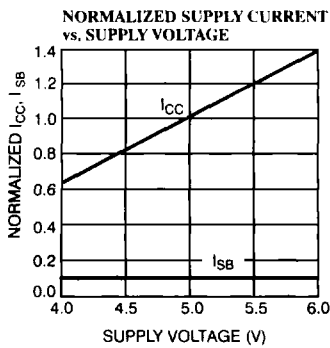
**Switching Waveforms (continued)**

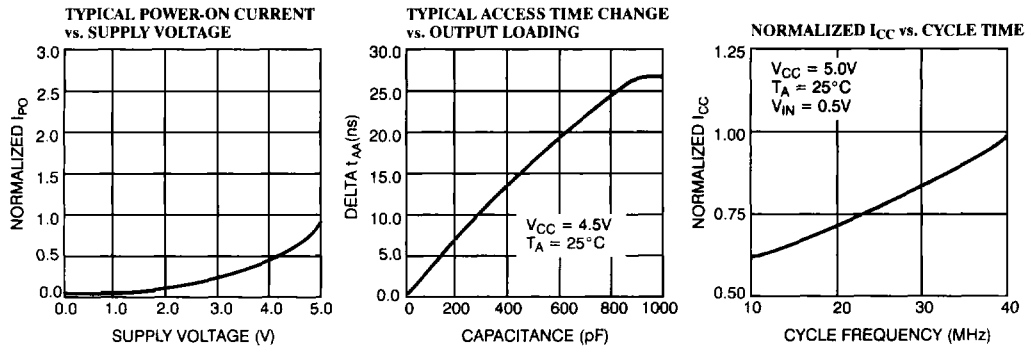
 Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>9, 13, 14</sup>


C164-10

**Note:**

 14. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

**Typical DC and AC Characteristics**


**Typical DC and AC Characteristics (continued)**

**2**
**CY7C164 Truth Table**

CE	WE	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

**CY7C166 Truth Table**

CE	WE	OE	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	H	Data In	Write
L	H	H	High Z	Write

**Address Designators**

Address Name	Address Function	CY 7C164 Pin Number	CY7C166 Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23



**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C164-12PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-12VC	V13	24-Lead Molded SOJ	
15	CY7C164-15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-15VC	V13	24-Lead Molded SOJ	
20	CY7C164-20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-20VC	V13	24-Lead Molded SOJ	
25	CY7C164-25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-25VC	V13	24-Lead Molded SOJ	
35	CY7C164-35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C164-35VC	V13	24-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C166-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-12VC	V13	24-Lead Molded SOJ	
15	CY7C166-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-15VC	V13	24-Lead Molded SOJ	
20	CY7C166-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-20VC	V13	24-Lead Molded SOJ	
25	CY7C166-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-25VC	V13	24-Lead Molded SOJ	
35	CY7C166-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C166-35VC	V13	24-Lead Molded SOJ	

Shaded areas contain preliminary information.

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