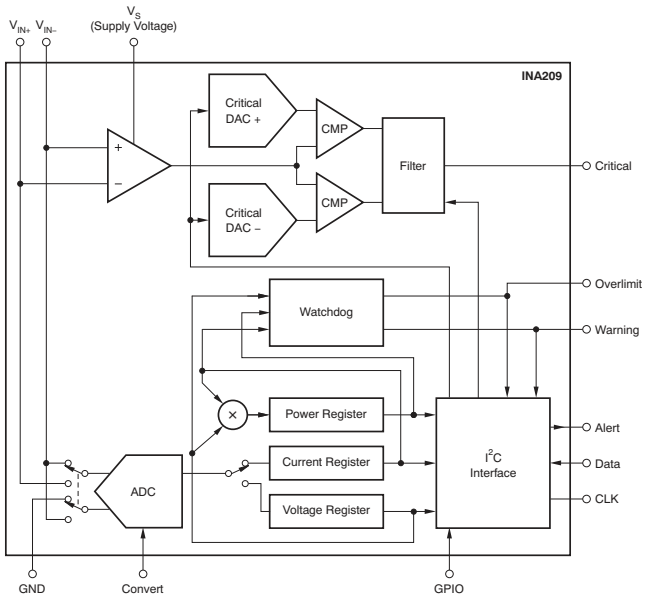
High-Side Measurement, Bi-Directional Current/Power Monitor with I²C™ Interface

FEATURES

- SENSES BUS VOLTAGES FROM 0V TO +26V
- REPORTS CURRENT, VOLTAGE, AND POWER; STORES PEAKS
- TRIPLE WATCHDOG LIMITS:
  - Lower Warning with Delay
  - Upper Over-limit, No Delay
  - Fast Analog Critical
- HIGH ACCURACY: 1% MAX OVER TEMP

APPLICATIONS

- SERVERS
- TELECOM EQUIPMENT
- AUTOMOTIVE
- POWER MANAGEMENT
- BATTERY CHARGERS
- WELDING EQUIPMENT
- POWER SUPPLIES
- TEST EQUIPMENT



DESCRIPTION

The INA209 is a high-side current shunt and power monitor with an I²C interface. The INA209 monitors both shunt drop and shunt bus voltage. A programmable calibration value, combined with an internal multiplier, enables direct readouts in amperes. An additional multiplying register calculates power in watts. The INA209 features two separate, onboard watchdog capabilities: a warning comparator and an over-limit comparator. The warning comparator is useful for monitoring lower warning limits and incorporates a user-defined delay. The over-limit comparator assists with monitoring upper limits that could require immediate system shutdown.

The INA209 also includes an analog comparator and a programmable digital-to-analog converter (DAC) that combine to provide the fastest possible responses to current overload conditions.

The INA209 can be used together with hot swap controllers that already use a current sense resistor. The INA209 full-scale range can be selected to be either within the hot-swap controller sense limits, or wide enough to include them.

The INA209 senses across shunts on buses that can vary from 0V to 26V. The device uses a single +3V to +5.5V supply, drawing a maximum of 1.5mA of supply current. It is specified for operation from –25°C to +85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA209	TSSOP-16	PW	INA209A

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		INA209	UNIT
Supply Voltage, V_S		6	V
Analog Inputs, V_{IN+}, V_{IN-}	Differential $(V_{IN+}) - (V_{IN-})$(2)	–26 to +26	V
	Common-Mode	–0.3 to +26	V
Open-Drain Digital Outputs		GND – 0.3 to +6	V
GPIO, Convert Pins		GND – 0.3 to V_S + 0.3	V
Input Current Into Any Pin		5	mA
Open-Drain Digital Output Current		10	mA
Operating Temperature		–40 to +125	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings	Human Body Model	2000	V
	Charged-Device Model	1000	V
	Machine Model (MM)	150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) V_{IN+} and V_{IN-} may have a differential voltage of –26V to +26V; however, the voltage at these pins must not exceed the range –0.3V to +26V.

ELECTRICAL CHARACTERISTICS: V_S = +3.3V

Boldface limits apply over the specified temperature range, **T_A = –25°C to +85°C.**
At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = ÷ 1, and BRNG(1) = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA209 MIN	INA209 TYP	INA209 MAX	UNIT
INPUT						
Full-Scale Current Sense (Input) Voltage Range		PGA = ÷ 1	0		±40	mV
		PGA = ÷ 2	0		±80	mV
		PGA = ÷ 4	0		±160	mV
		PGA = ÷ 8	0		±320	mV
Bus Voltage (Input Voltage) Range(2)		BRNG = 1	0		32	V
		BRNG = 0	0		16	V
Common-Mode Rejection	CMRR	V_{IN+} = 0V to 26V	100	120		dB
Offset Voltage, RTI(3)	V_{OS}	PGA = ÷ 1		±10	±100	µV
		PGA = ÷ 2		±20	±125	µV
		PGA = ÷ 4		±30	±150	µV
		PGA = ÷ 8		±40	±200	µV
vs Temperature				**0.1**		**µV/°C**
vs Power Supply	PSRR	V_S = 3V to 5.5V		10		µV/V
Current Sense Gain Error				±40		m%
vs Temperature				**10**		**ppm/°C**
Input Impedance		Active Mode				
V_{IN+} Pin				20		µA
$V_{IN–}$ Pin				20 || 320		µA || kΩ
Input Leakage		Power-Down Mode				
V_{IN+} Pin				0.1	±0.5	µA
$V_{IN–}$ Pin				0.1	±0.5	µA
DC ACCURACY						
ADC Basic Resolution				12		Bits
1 LSB Step Size						
Shunt Voltage				10		µV
Bus Voltage				4		mV
Current Measurement Error				±0.2	±0.5	%
over Temperature					**±1**	**%**
Bus Voltage Measurement Error				±0.2	±0.5	%
over Temperature					**±1**	**%**
Differential Nonlinearity				±0.1		LSB
Critical DAC Full-Scale Range				255		mV
Critical DAC Accuracy				±0.5	±1	%
Critical DAC Resolution				8		Bits
Critical DAC 1 LSB Step Size				1		mV
Critical DAC Comparator Offset				±0.3	±1.6	mV
Critical DAC Comparator Hysteresis(4)				See (4)		
Critical DAC Comparator Delay				5		µs

(1) BRNG is bit 13 of the Configuration Register.
(2) This parameter only expresses the full-scale range of the ADC scaling. In no event should more than 26V be applied to this device.
(3) Referred-to-input (RTI).
(4) User-programmable. See the *Critical Comparator* and *Register* sections.

ELECTRICAL CHARACTERISTICS: V_S = +3.3V (continued)

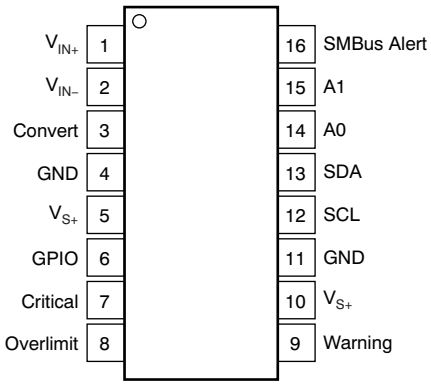
Boldface limits apply over the specified temperature range, **T_A = –25°C to +85°C.**
At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	INA209 MIN	INA209 TYP	INA209 MAX	UNIT
ADC TIMING					
ADC Conversion Time	12-Bit		532	586	µs
	11-Bit		276	304	µs
	10-Bit		148	163	µs
	9-Bit		84	93	µs
Minimum Convert Input Low Time		4			µs
SMBus					
SMBus Timeout(5)			28	35	ms
DIGITAL INPUTS (Convert, GPIO and SDA as Input, SCL, A0, A1)					
Input Capacitance			3		pF
Leakage Input Current	$0 \le V_{IN} \le V_S$		0.1	1	µA
Input Logic Levels:					
V_{IH}		0.7 (V_S)		6	V
V_{IL}		–0.3		0.3 (V_S)	V
Hysteresis			500		mV
DIGITAL OUTPUTS					
GPIO Pin Output Low	I_{SINK} = 3mA		0.15	0.4	V
GPIO Pin Output High	I_{SOURCE} = 3mA	V_S – 0.4	V_S – 0.15		V
OPEN-DRAIN DIGITAL OUTPUTS (Critical, Over-Limit, Warning, Alert, SDA)					
Logic '0' Output Level	I_{SINK} = 3mA		0.15	0.4	V
High-Level Output Leakage Current	$V_{OUT} = V_S$		0.1	1	µA
POWER SUPPLY					
Operating Supply Range		+3		+5.5	V
Quiescent Current			1	1.5	mA
Quiescent Current, Power-Down Mode			6	15	µA
Power-On Reset Threshold			2		V
TEMPERATURE RANGE					
Specified Temperature Range		–25		+85	°C
Operating Temperature Range		–40		+125	°C
Thermal Resistance θ_{JA}					
TSSOP-16			+150		°C/W

(5) SMBus timeout in the INA209 resets the interface any time SCL or SDA is low for over 28ms.

PIN CONFIGURATION

INA209
Top View



PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	V_{IN+}	Positive differential shunt voltage. Connect to positive side of shunt resistor.
2	V_{IN-}	Negative differential shunt voltage. Connect to negative side of shunt resistor. Bus voltage is measured from this pin to ground.
3	Convert	Used to trigger conversions in triggered mode. In triggered mode, this pin should normally be high and taken low to initiate conversion. It may be returned high after 4µs. If held low, the ADC converts each time a triggered mode command is written via the I^2C bus. If not used, this line should be tied high.
4	GND	Connect together with pin 11 to ground.
5	V_{S+}	Connect together with pin 10 to supply, 3V to 5.5V.
6	GPIO	General-purpose, user-programmable input/output. Totem-pole output. Connect to ground or supply if not used. Default state is as an input.
7	Critical	Open-drain critical watchdog output (filter set in Critical DAC– Register). Default state is disabled; active-low; transparent (non-latched).
8	Overlimit	Open-drain over-limit watchdog output. Default state is disabled; active-low; transparent (non-latched).
9	Warning	Open-drain warning watchdog output (delay set in Critical DAC– Register). Default state is disabled; active-low; transparent (non-latched).
10	V_{S+}	Connect together with pin 5 to supply, 3V to 5.5V.
11	GND	Connect together with pin 4 to ground.
12	SCL	Serial bus clock line.
13	SDA	Serial bus data line.
14	A0	Address pin. Table 1 shows pin settings and corresponding addresses.
15	A1	Address pin. Table 1 shows pin settings and corresponding addresses.
16	SMBus Alert	Open-drain SMBus alert output. Controlled in SMBus Alert Mask Register. Default state is disabled.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

FREQUENCY RESPONSE

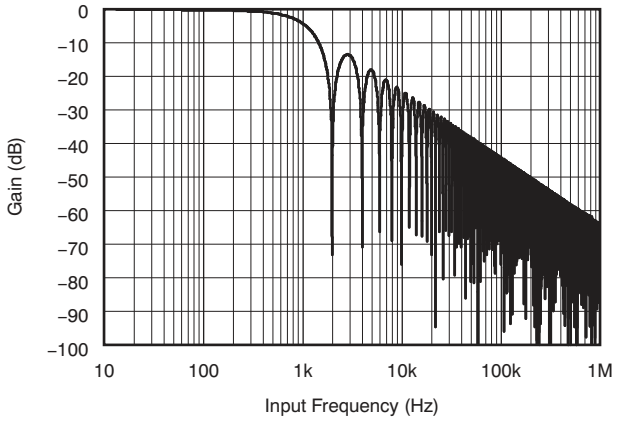


Figure 1.

ADC SHUNT OFFSET vs TEMPERATURE

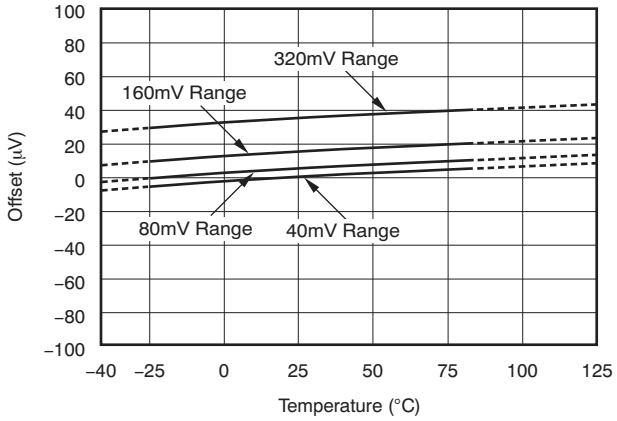


Figure 2.

ADC SHUNT GAIN ERROR vs TEMPERATURE

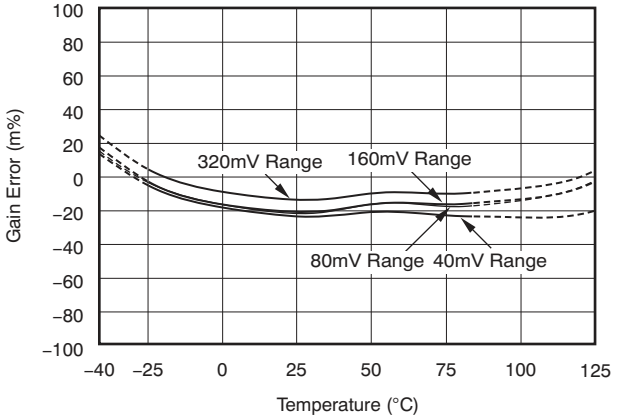


Figure 3.

ADC BUS VOLTAGE OFFSET vs TEMPERATURE

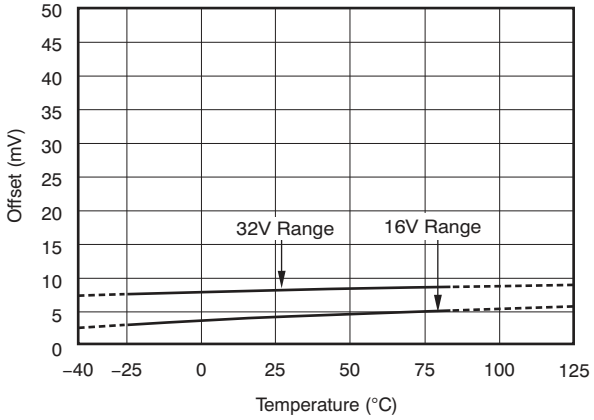


Figure 4.

ADC BUS GAIN ERROR vs TEMPERATURE

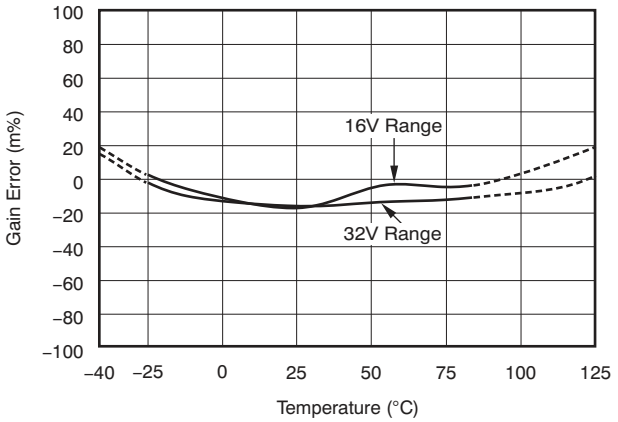


Figure 5.

INTEGRAL NONLINEARITY vs INPUT VOLTAGE

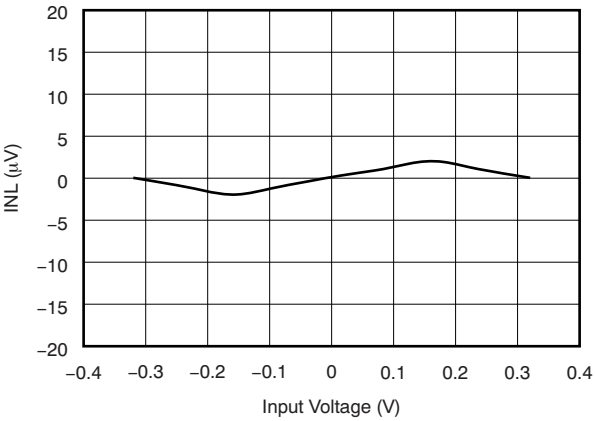


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

CRITICAL COMPARATOR OFFSET vs TEMPERATURE

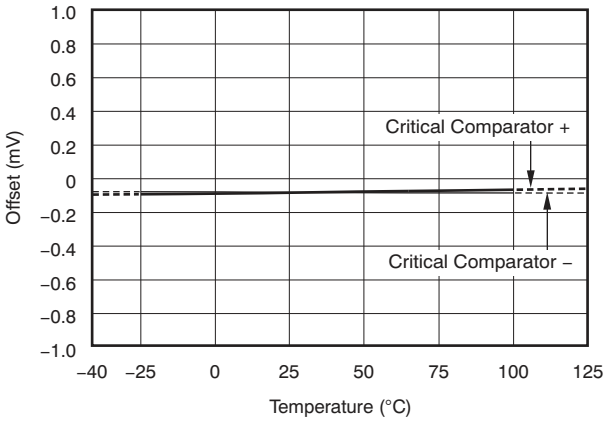


Figure 7.

CRITICAL COMPARATOR FULL-SCALE ERROR vs TEMPERATURE

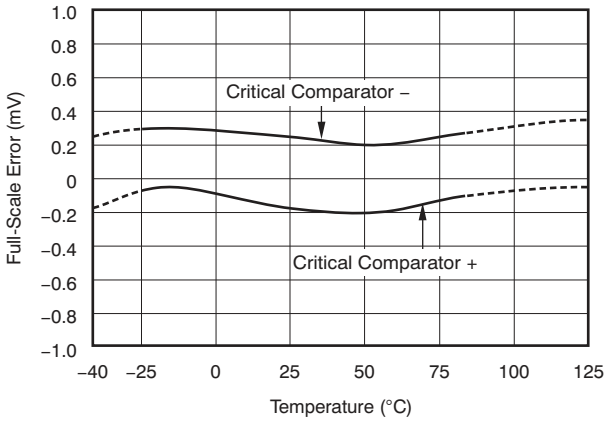


Figure 8.

INPUT CURRENTS WITH LARGE DIFFERENTIAL VOLTAGES (V_{IN+} at 12V, Sweep of $V_{IN–}$)

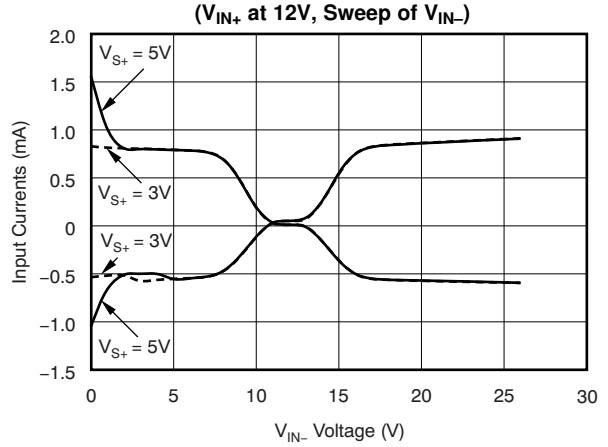


Figure 9.

ACTIVE I_Q vs TEMPERATURE

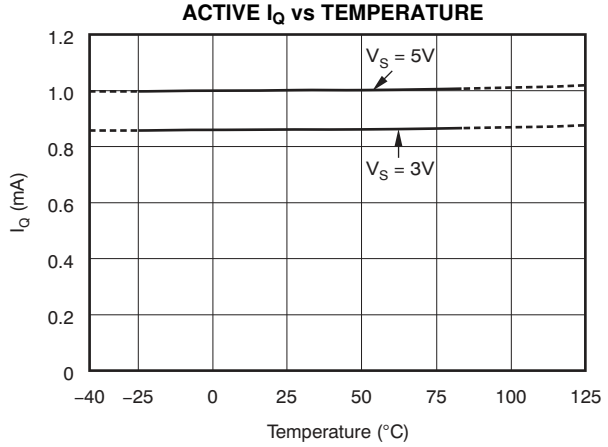


Figure 10.

SHUTDOWN I_Q vs TEMPERATURE

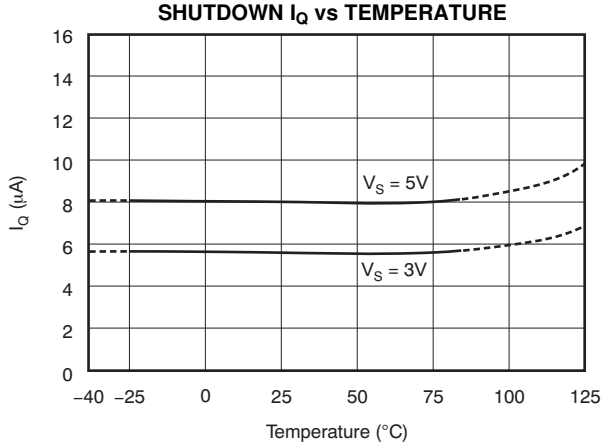


Figure 11.

ACTIVE I_Q vs I^2C CLOCK FREQUENCY

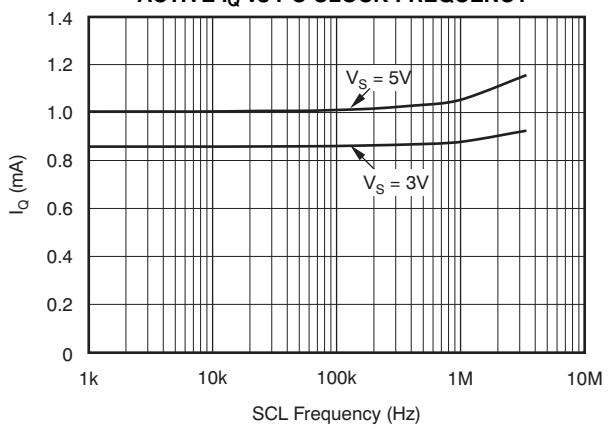


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

SHUTDOWN I_Q vs I^2C CLOCK FREQUENCY

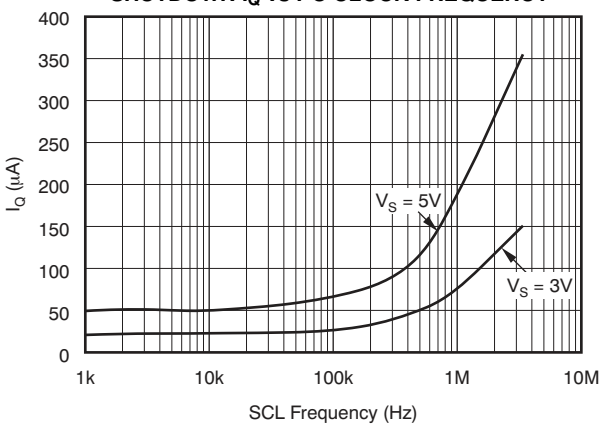


Figure 13.

FUNCTIONAL BLOCK DIAGRAM

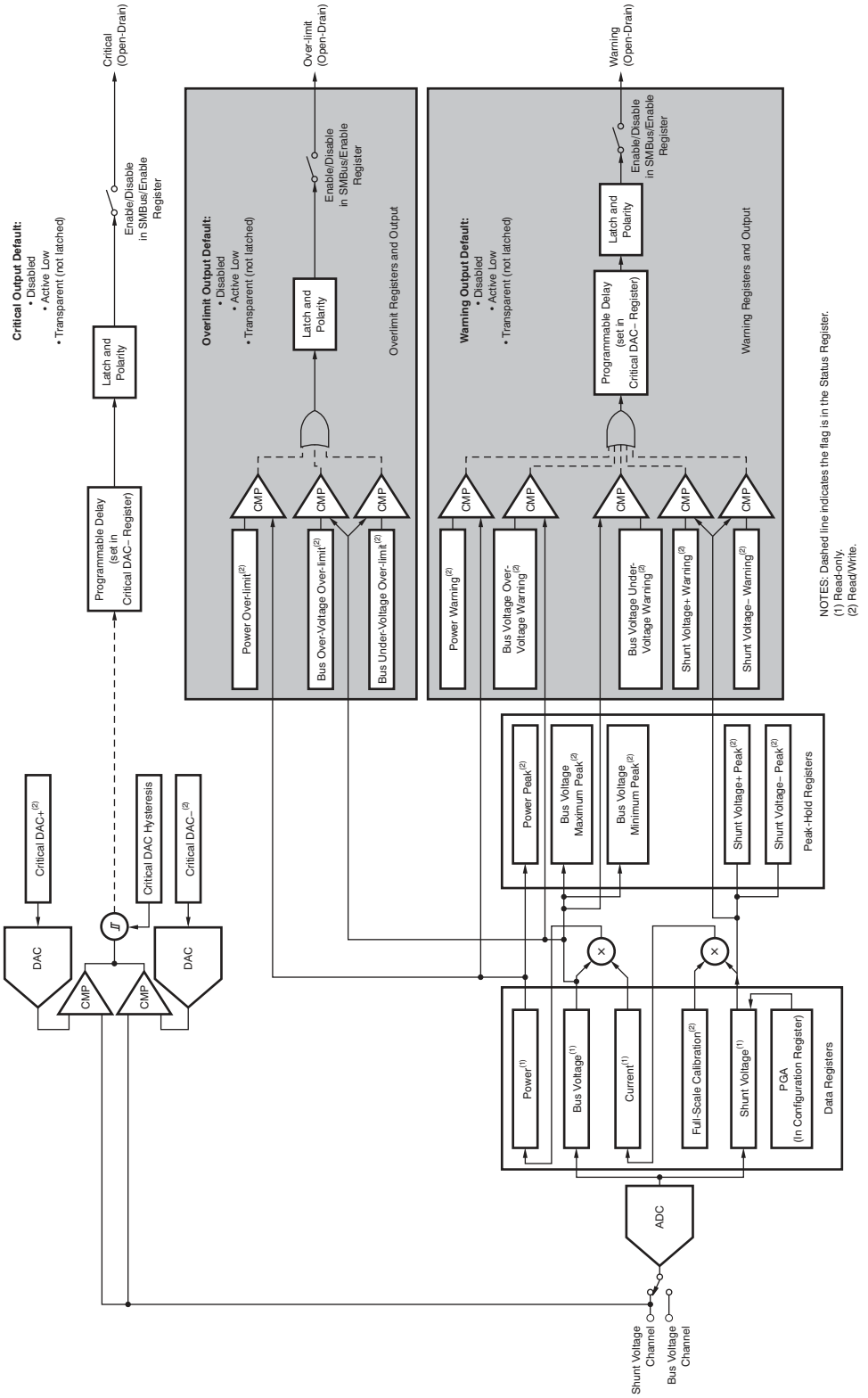


Figure 14.

APPLICATION INFORMATION

The INA209 is a digital current-shunt monitor with an I^2C and SMBus-compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for setting warning limits, measurement resolution, and continuous-versus-triggered operation. Detailed register information appears at the end of this data sheet, beginning with Table 2. See the Functional Block Diagram for a block diagram of the INA209.

The INA209 offers compatability with I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with each other. I^2C will be used throughout this document, with SMBus being specified only when a difference between the two systems is being addressed. Two bi-directional lines, SCL and SDA, connect the INA209 to the bus. Both SCL and SDA are open-drain connections. Figure 15 shows a typical application circuit.

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an *Acknowledge* bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The INA209 includes a 28ms timeout on its interface to prevent locking up an SMBus.

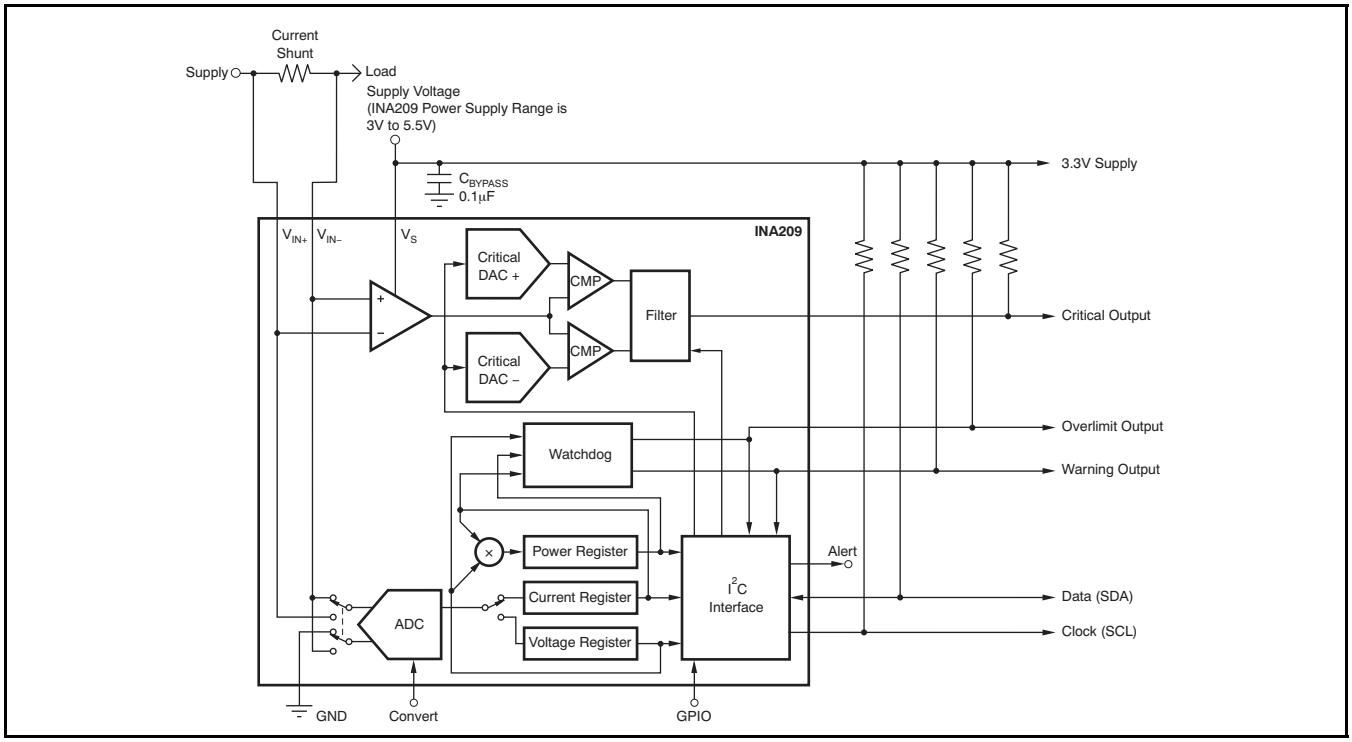


Figure 15. Typical Application Circuit

Serial Bus Address

To communicate with the INA209, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The INA209 has two address pins, A0 and A1. Table 1 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

Table 1. INA209 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V_{S+}	GND	1000100
V_{S+}	V_{S+}	1000101
V_{S+}	SDA	1000110
V_{S+}	SCL	1000111
SDA	GND	1001000
SDA	V_{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

The INA209 operates only as a slave device on the I^2C bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The INA209 supports the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted most significant byte first.

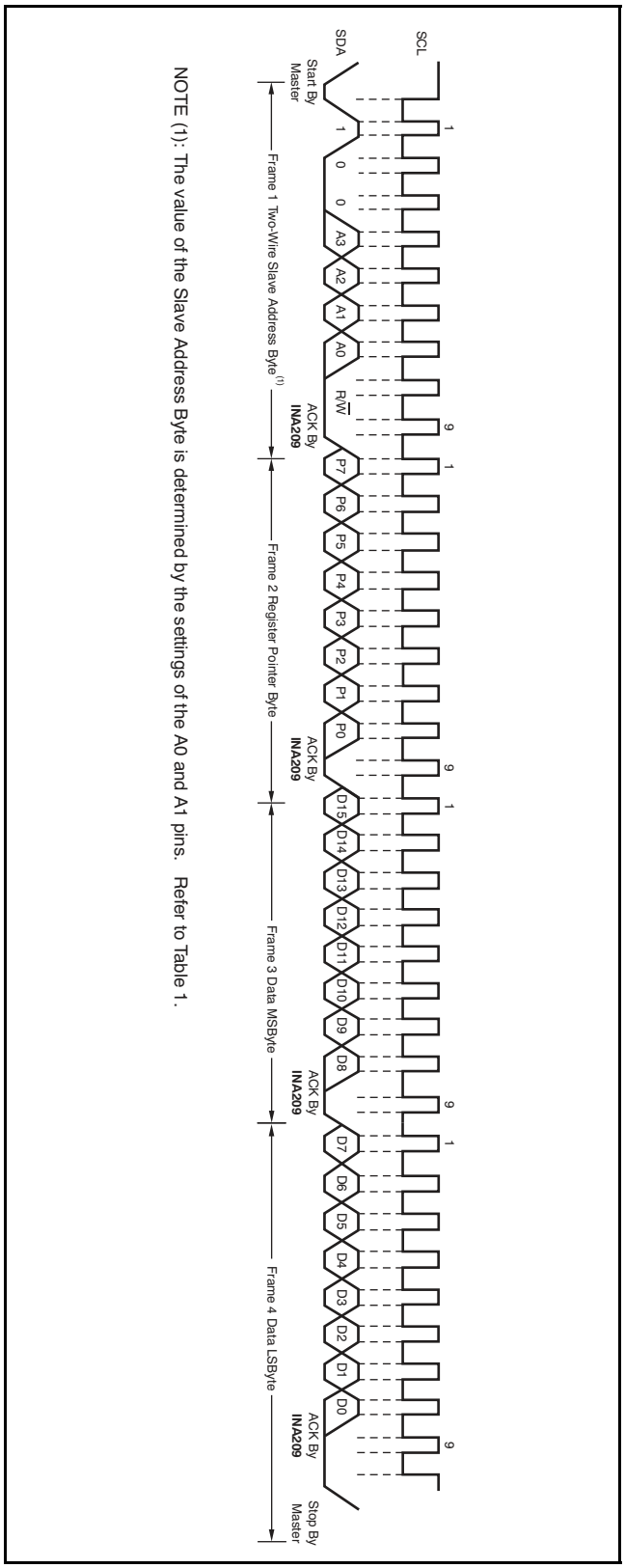
WRITING TO/READING FROM THE INA209

Accessing a particular register on the INA209 is accomplished by writing the appropriate value to the register pointer. Refer to Table 2 for a complete list of registers and corresponding addresses. The value for the register pointer as shown in Figure 19 is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the INA209 requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit LOW. The INA209 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA209 acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

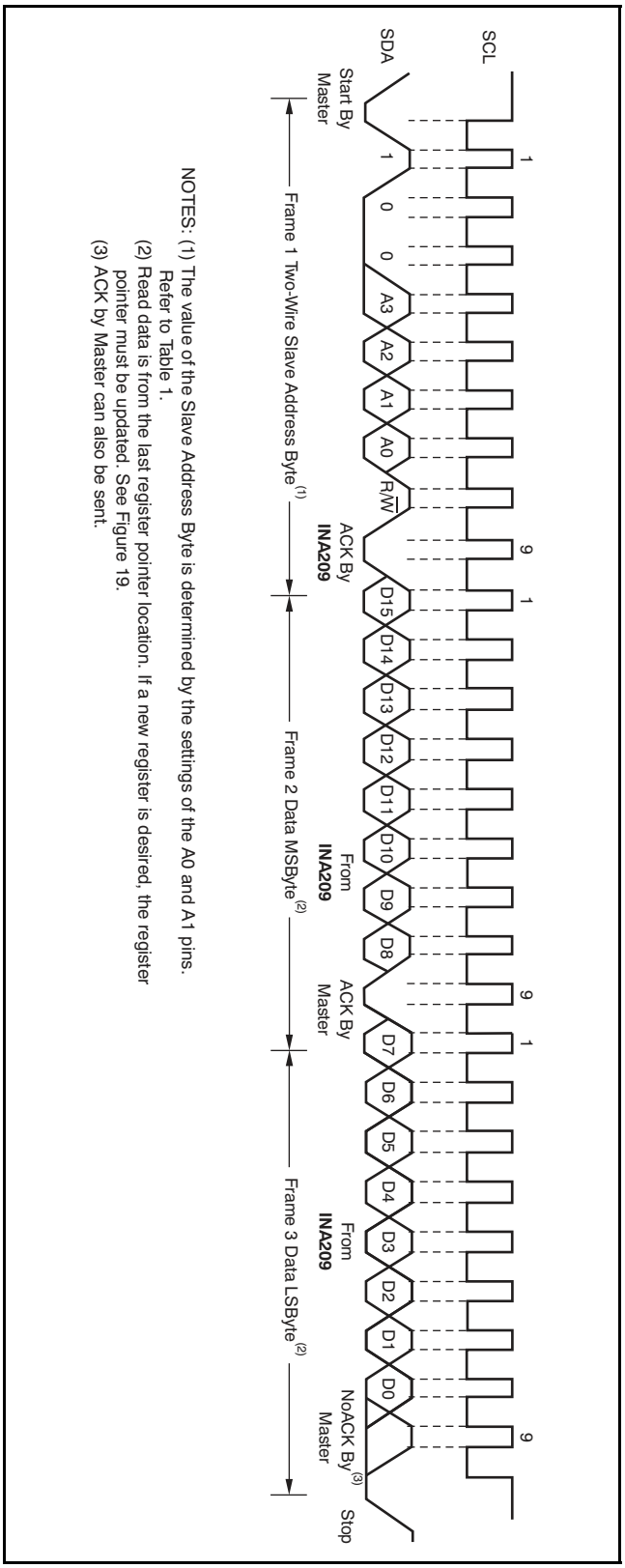
When reading from the INA209, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the register pointer byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA209 retains the register pointer value until it is changed by the next write operation.

Figure 16 and Figure 17 show read and write operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte. Figure 18 shows the timing diagram for the SMBus Alert response operation. Figure 19 illustrates a typical register pointer configuration.



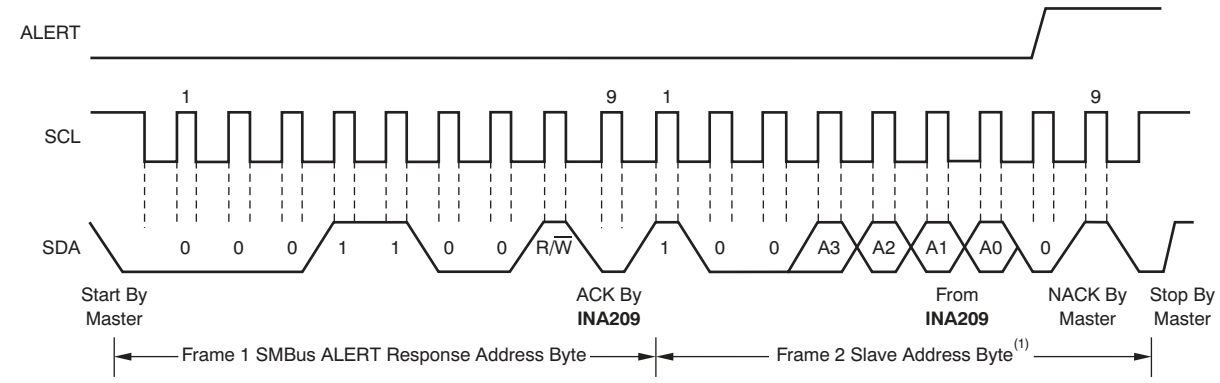
NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 16. Timing Diagram for Write Word Format



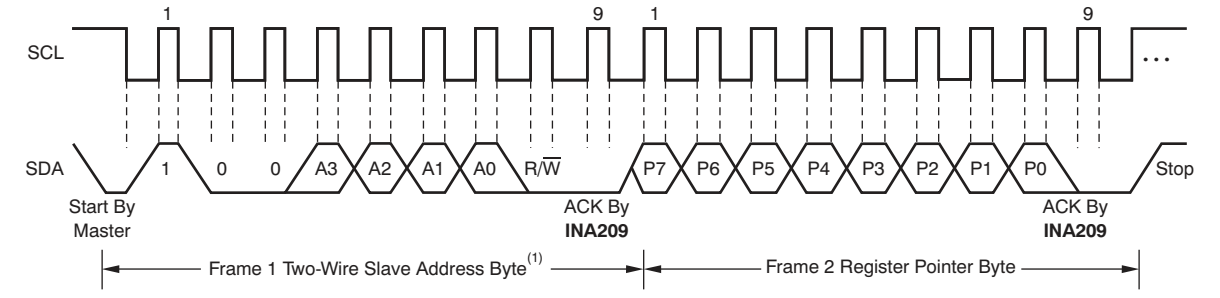
NOTES: (1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 19.
(3) ACK by Master can also be sent.

Figure 17. Timing Diagram for Read Word Format



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 18. Timing Diagram for SMBus ALERT



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 19. Typical Register Pointer Set

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing High-Speed (HS) master code *00001XXX*. This transmission is made in fast (400kbps) or standard (100kbps) (F/S) mode at no more than 400kbps. The INA209 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the INA209 to support the F/S mode.

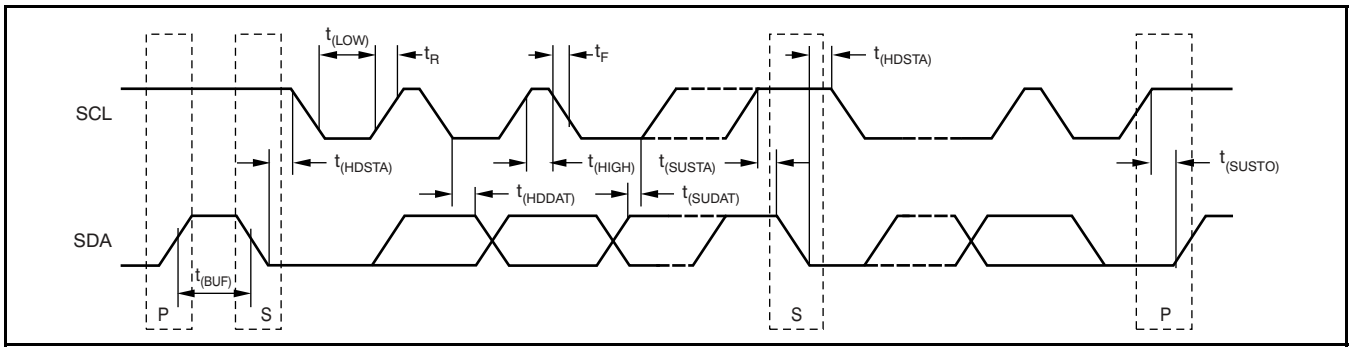


Figure 20. Bus Timing Diagram

Bus Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		1000			ns

Power-Up Conditions

Power-up conditions apply to a software reset via the RST bit (bit 15) in the Configuration Register, or the I²C bus General Call Reset. At device power up, all Status bits are masked. Warning, Over-Limit, Critical, and SMBus Alert functions are disabled. All watchdog outputs default to active low and transparent (non-latched) modes.

BASIC ADC FUNCTIONS

The two analog inputs to the INA209, V_{IN+} and V_{IN-}, connect to a shunt resistor in the bus of interest. The INA209 is typically powered by a separate supply from +3V to +5.5V. The bus being sensed can vary from 0V to 26V. There are no special considerations for power-supply sequencing (for example, a bus voltage can be present with the supply voltage off, and vice-versa). The INA209 senses the small drop across the shunt for shunt voltage, and senses the voltage with respect to ground from V_{IN-} for the bus voltage. Figure 21 illustrates this operation.

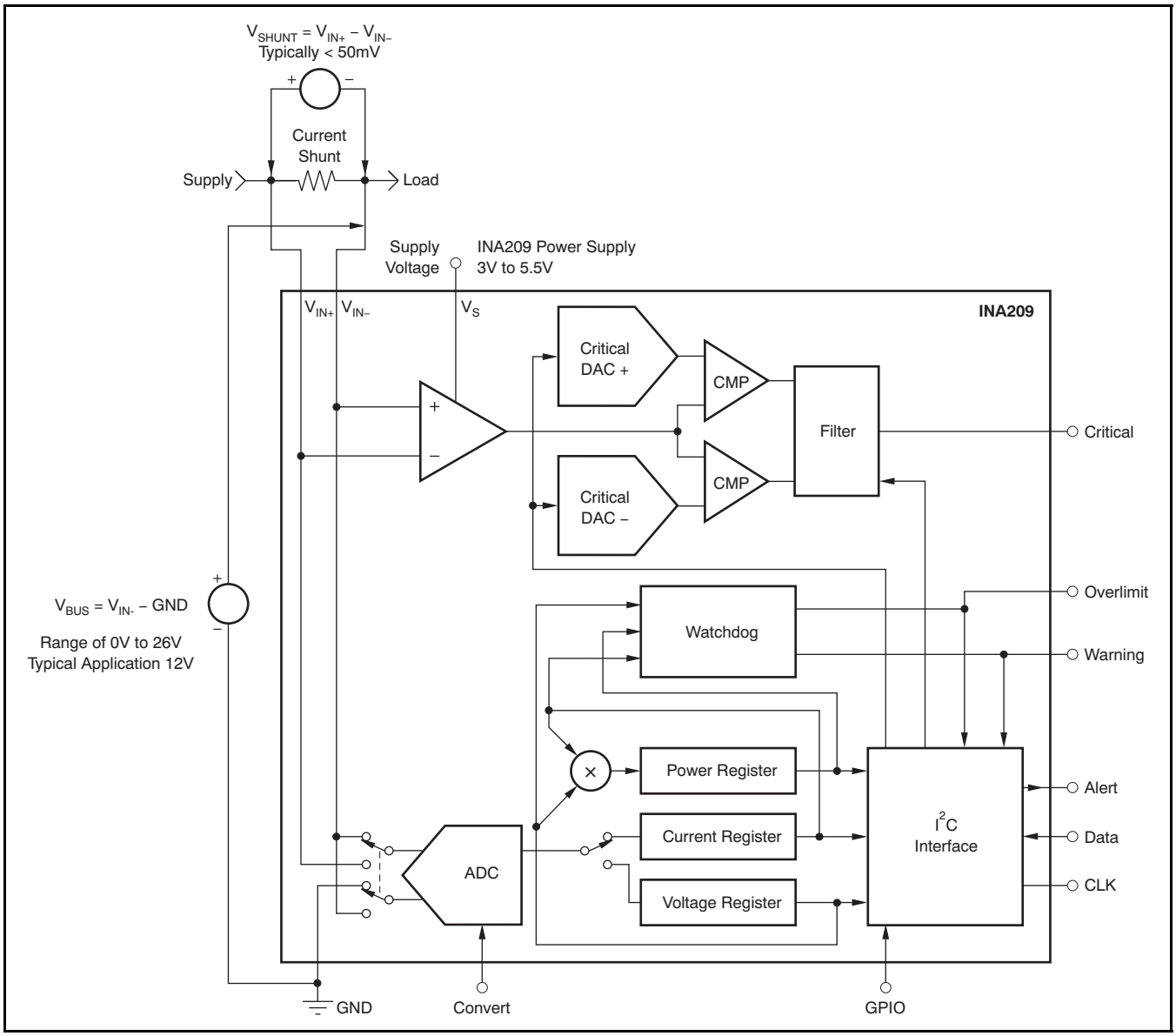


Figure 21. INA209 Configured for Shunt and Bus Voltage Measurement

When the INA209 is in the normal operating mode (that is, MODE bits of the Configuration Register are set to '111'), it continuously converts the shunt voltage up to the number set in the shunt voltage averaging function (Configuration Register, SADC bits). The device then converts the bus voltage up to the number set in the bus voltage averaging (Configuration Register, BADC bits). The Mode control in the Configuration Register also permits selecting modes to convert only voltage or current, either continuously or in response to an event (triggered).

All current and power calculations are performed in the background and do not contribute to conversion time; conversion times shown in the Electrical Characteristics table can be used to determine the actual conversion time.

Power-Down mode reduces the quiescent current and turns off current into the INA209 inputs, avoiding any supply drain. Full recovery from Power-Down requires 40µs. ADC Off mode (set by the Configuration Register, MODE bits) stops all conversions.

In triggered mode, the external Convert line becomes active. Convert commands are initiated by taking the Convert line low for a minimum of 4µs. The Convert line may be connected high when unused. Any re-trigger of the Convert line during a conversion is ignored, and the Convert line state is disregarded until the conversion ends. There are several available triggered modes; however, all conversions are performed repeatedly up to the number set in the Averaging function (Configuration Register, BADC and SADC bits).

If the Convert line is held low, writing any of the triggered convert modes into the Configuration Register (even if the desired mode is already programmed into the register) triggers a single-shot conversion.

Although the INA209 can be read at any time, and the data from the last conversion remain available, the Conversion Ready bit (Status Register, CNVR bit) is provided to help co-ordinate one-shot or triggered conversions. The Conversion Ready bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready bit clears under these conditions:

1. Writing to the Configuration Register, except when configuring the MODE bits for Power Down or ADC off (Disable) modes;
2. Reading the Status Register; or
3. Triggering a single-shot conversion with the Convert pin.

Power Measurement

Current and bus voltage are converted at different points in time, depending on the resolution and averaging mode settings. For instance, when configured for 12-bit and 128 sample averaging, up to 68ms in time between sampling these two values is possible. Again, these calculations are performed in the background and do not add to the overall conversion time.

Peak-Hold Registers

Shunt voltage peak registers hold the lowest and highest converted reading for the shunt value. The shunt value may be either positive or negative; as a result, there is a need for a sign bit in either register. For instance, the Shunt Voltage Positive Peak Register in most systems records a positive voltage; in most unidirectional current measurement applications, the Shunt Voltage Negative Peak Register also records a positive voltage. However, certain conditions can occur in normally unidirectional systems that cause a negative polarity across the shunt; these events are recorded in the Shunt Voltage Negative Peak Register.

Peak-hold registers do not record conditions that trigger a Critical Comparator shutdown. A Critical Comparator shutdown occurs within 5µs of detecting a critical condition, while the ADC conversion necessary to record a peak-hold requires 532µs. Therefore, a system shutdown removes the fault before the analog-to-digital conversion (ADC) can record it.

Critical Comparator

The Critical Comparator function is included to provide the fastest possible response to overload events. This function bypasses the digital circuit by capturing the event in the analog domain.

The Critical Comparator responds only to shunt voltage, and can be programmed for a value from 0mV to 255mV (in 1mV increments) in the Critical DAC+ and Critical DAC– Registers. Two thresholds are provided, allowing users to set different thresholds in systems where bi-directional current measurement occurs. For example, a power supply may readily allow sourcing of 10A, but must indicate an alarm whenever sinking more than 1A. The SMBus Alert Mask/Enable Control Register allows the user to enable or disable the Critical pin output through the CREN bit. The CREN bit affects only the Critical pin; it does not affect the CRIT+ or CRIT– flags within the Status Register.

The Critical Comparator output filter is set by the CF bits of the Critical DAC– Register. This filter determines the duration of time that the CMP output must be continuously active (not toggling) to propagate to the Critical pin output and set the CRIT+ or CRIT– flags within the Status Register.

While the Critical Comparator output filter provides settings from 0ms to 0.96ms, the CMP is actually strobed every 4µs, providing multiple samples per delay period. For the Critical output pin to become active, the critical condition must be true for every sample during the specified delay period.

When using the Critical Comparator in unidirectional applications, where the Critical DAC– Register is unused, the Comparator could trip in error if the input is near zero, because the comparator can have an offset of up to ±1.5mV. Noise also contributes to false tripping. To avoid false tripping in unidirectional applications, the Critical DAC– should be programmed to a value beyond –2mV to account for the offset, and an additional amount to provide a noise margin. Alternatively, the Critical DAC– can be programmed to negative full-scale range (–255mV), in order to eliminate false tripping.

PGA Function

If larger full-scale shunt voltages are desired, the INA209 provides a PGA function that increases the full-scale range up to 2, 4, or 8 times (320mV). Additionally, the bus voltage measurement has two full-scale ranges: 16V or 32V.

Compatibility with TI Hot Swap Controllers

The INA209 is designed for compatibility with hot swap controllers such the TI TPS2490. The TPS2490 uses a high-side shunt with a limit at 50mV; the INA209 full-scale range of 40mV enables the use of the same shunt for current sensing below this limit. When sensing is required at (or through) the 50mV sense point of the TPS2490, the PGA of the INA209 can be set to ÷2 to provide an 80mV full-scale range.

A typical application connects the Critical pin output to the TPS2490 enable line; this configuration enables user-programmable current limits. Note that the latched mode should be used for the Critical pin output to avoid oscillation at the trip level.

Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA209 offers several options for filtering by choosing resolution and averaging in the Configuration Register. These filtering options can be set independently for either voltage or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500kHz (±10%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1MHz and higher, they can be dealt with by incorporating filtering at the input of the INA209. The high frequency enables the use of low-value series resistors on the filter for negligible effects on measurement accuracy. Figure 22 shows the INA209 with an additonal filter added at the input.

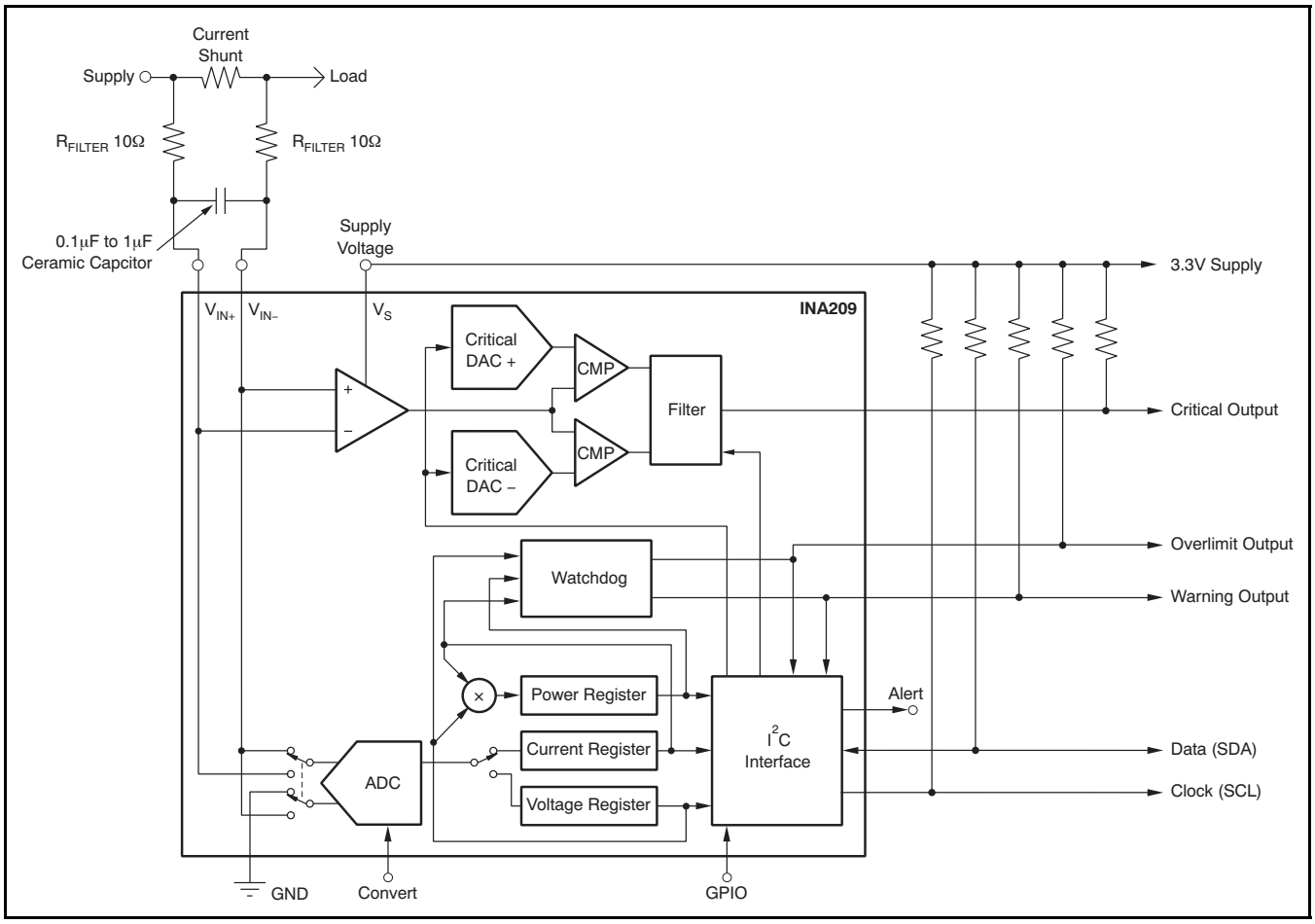


Figure 22. INA209 with Input Filtering

Overload conditions are another consideration for the INA209 inputs. The INA209 inputs are specified to tolerate 26V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the 26V differential and common-mode rating of the INA209. Inductive kickback voltages are best dealt with by zener-type transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the INA209 in systems where large currents are available. Testing has demonstrated that the addition of 10Ω resistors in series with each input of the INA209 sufficiently protects the inputs against dV/dt failure up to the 26V rating of the INA209. These resistors have no significant effect on accuracy.

SMBus Alert Response

The ALERT interrupt pin is set whenever Warning, Over-Limit, Critical faults, or Conversion Ready states (in triggered modes) occur. The ALERT interrupt output signal is latched and can be cleared only by either reading the Status Register or by successfully responding to an alert response address. If the fault is still present, the ALERT pin re-asserts. Asserting the ALERT pin does not halt automatic conversions that are already in progress. The ALERT output pin is open-drain, allowing multiple devices to share a common interrupt line. The ALERT output can be disabled via the SMBus Alert Mask/Enable Control Register using the SMAEN bit. When disabled, the ALERT pin goes to a high state.

The INA209 responds to the SMBus alert response address, an interrupt pointer return-address feature. The SMBus alert response interrupt pointer provides

quick fault identification for simple slave devices. When an ALERT occurs, the master can broadcast the alert response slave address (0001 100). Following this alert response, any slave devices that generated interrupts identify themselves by putting the respective addresses on the bus.

The alert response can activate several different slave devices simultaneously, similar to the I^2C General Call. If more than one slave attempts to respond, bus arbitration rules apply; the device with the lower address code wins. The losing device does not generate an Acknowledge and continues to hold the ALERT line low until the interrupt is cleared. Successful completion of the read alert response protocol clears the SMBus ALERT pin, provided that the condition causing the alert no longer exists. The SMBus Alert flag is cleared separately by either reading the Status Register or by disabling the SMBus Alert function.

The Status Register flags indicate which (if any) of the watchdogs have been activated. After power-on reset (POR), the normal state of all flag bits is '0', assuming that no alarm conditions exist. The flags are cleared by any successful read of the Status Register, after a conversion is complete and the fault no longer exists.

All Other Latches

The latches in the Configuration Register for the Warning, Over-Limit, and Critical outputs are not associated with the SMBus alert response, and are cleared whenever the Status Register is read. If the fault remains, they continue to set (they may also be cleared by setting the latch enable to transparent, and then returning it to latch mode).

The values in the Peak-Hold Registers must be cleared by writing a '1' to the respective LSBs.

Multichannel Data Acquisition

The INA209 can be used in multiple current measurement channels where the controlling processor sums the currents of all the channels for a total current. Often these current measurements must occur simultaneously. Use the GPIO output from one of the INA209s and connect it to the Convert pin of the other INA209s. This architecture allows for sending conversion commands via the I^2C bus to the master device, and all devices will convert simultaneously. Figure 23 illustrates this architecture using four INA209s.

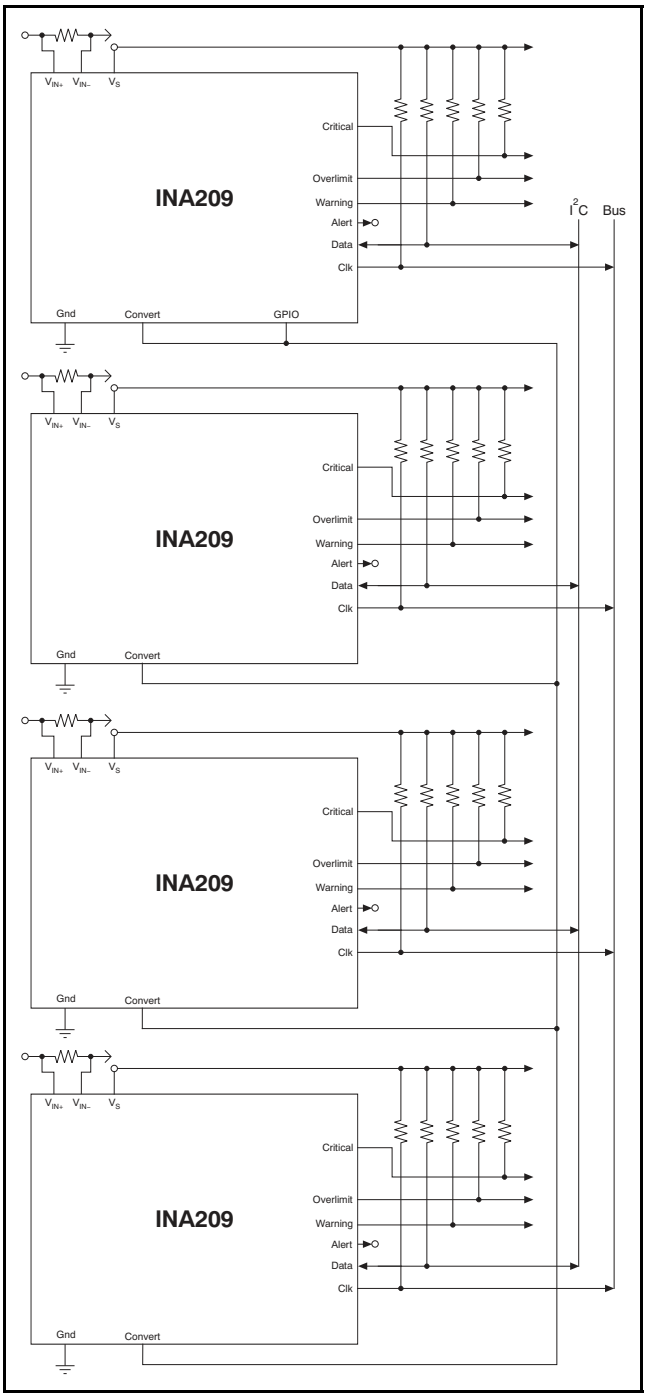


Figure 23. Multichannel Data Acquisition with Simultaneous Sampling

External Circuitry for Additional V_{BUS} Input

The INA209 GPIO can be used to control an external circuit to switch the V_{BUS} measurement to an alternate location. Switching is most often done to perform bus voltage measurements on the opposite side of a MOSFET switch in series with the shunt resistor.

Consideration must be given to the typical 20µA input current of each INA209 input, along with the 320kΩ impedance present at the V_{IN-} input where the bus voltage is measured. These effects can create errors through the resistance of any external switching method used. The easiest way to avoid these errors is by reducing this resistance to a minimum; select switching MOSFETs with the lowest possible $R_{DS(on)}$ values.

The circuit shown in Figure 24 uses MOSFET pairs to reduce package count. Back-to-back MOSFETs must be used in each leg because of the built-in back diodes from source-to-drain. In this circuit, the normal connection for V_{IN-} is at the shunt, with the optional voltage measurement at the output of the control FET.

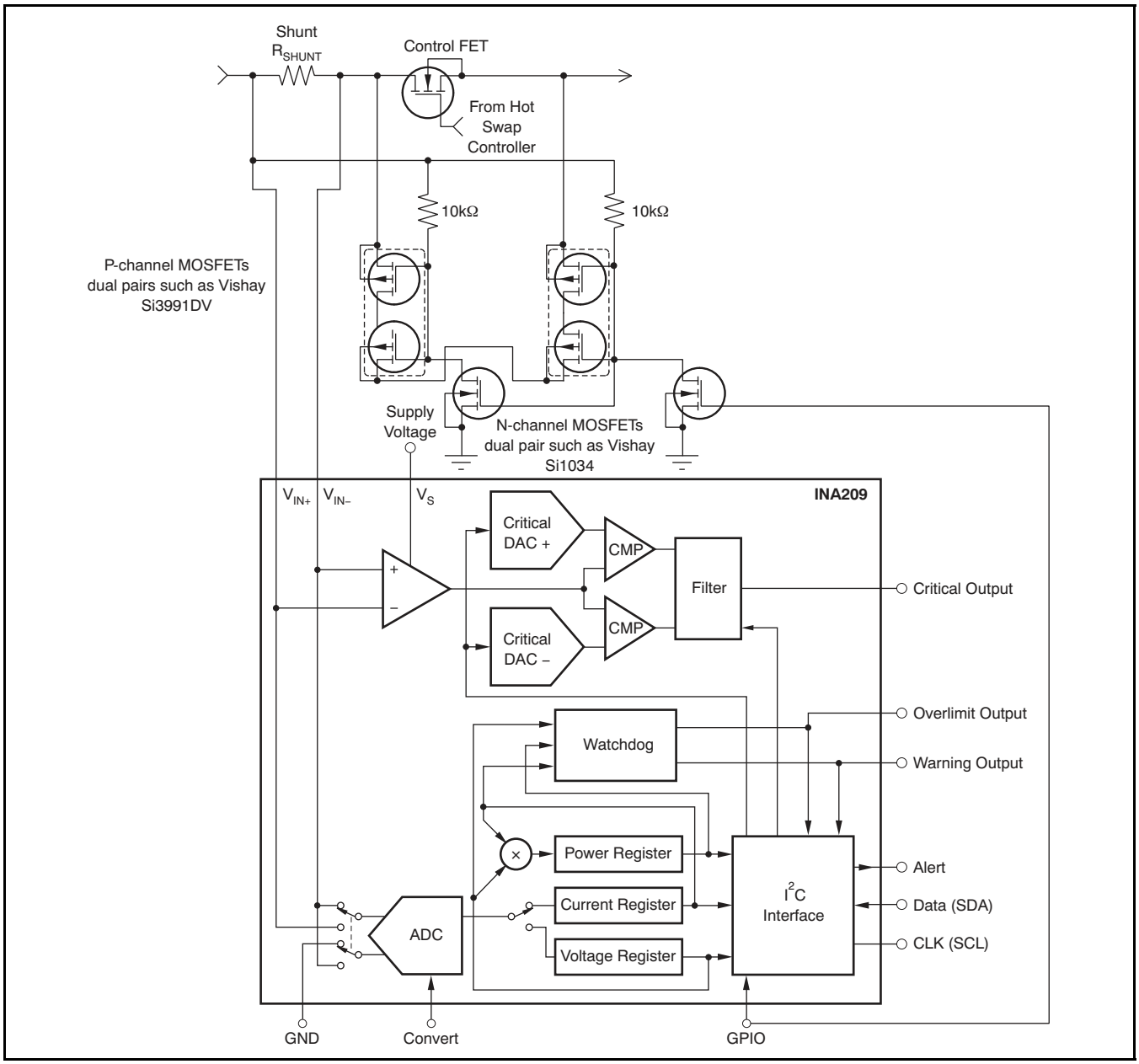


Figure 24. External Circuitry for Additional V_{BUS} Input

PROGRAMMING THE INA209 POWER MEASUREMENT ENGINE

Calibration Register and Scaling

The Calibration Register makes it possible to set the scaling of the Current and Power Registers to whatever values are most useful for a given application. One strategy may be to set the Calibration Register such that the largest possible number is generated in the Current Register or Power Register at the expected full-scale point; this approach yields the highest resolution. The Calibration Register can also be selected to provide values in the Current and Power Registers that either provide direct decimal equivalents of the values being measured, or yield a round LSB number. After these choices have been made, the Calibration Register also offers possibilities for end user system-level calibration, where the value is adjusted slightly to cancel total system error.

Below are two examples for configuring the INA209 calibration. Both examples are written so the information directly relates to the calibration set up found in the INA209EVM softwar.

Calibration Example 1: Calibrating the INA209 with no possibility for overflow. (Note that the numbers used in this example are the same used with the INA209EVM software as shown in Figure 25.

1. Establish the following parameters:

   V_{BUS_MAX} = 32

   V_{SHUNT_MAX} = 0.32

   R_{SHUNT} = 0.5

2. Using Equation 1, determine the maximum possible current .

$$\text{MaxPossible\_I} = \frac{V_{SHUNT\_MAX}}{R_{SHUNT}}$$

$$\text{MaxPossible\_I} = 0.64 \quad (1)$$

3. Choose the desired maximum current value. This value is selected based on system expectations.

   Max_Expected_I = 0.6

4. Calculate the possible range of current LSBs. To calculate this range, first compute a range of LSBs that is appropriate for the design. Next, select an LSB within this range. Note that the results will have the most resolution when the minimum LSB is selected. Typically, an LSB is selected to be the nearest round number to the minimum LSB value.

$$\text{Minimum\_LSB} = \frac{\text{Max\_Expected\_I}}{32767}$$

$$\text{Minimum\_LSB} = 18.311 \times 10^{-6} \quad (2)$$

$$\text{Maximum\_LSB} = \frac{\text{Max\_Expected\_I}}{4096}$$

$$\text{Maximum\_LSB} = 146.520 \times 10^{-6} \quad (3)$$

   Choose an LSB in the range: Minimum_LSB<Selected_LSB < Maximum_LSB

   Current_LSB = 20×10^{-6}

   Note:

   This value was selected to be a round number near the Minimum_LSB. This selection allows for good resolution with a rounded LSB.

5. Compute the Calibration Register value using Equation 4:

$$\text{Cal} = \text{trunc}\left(\frac{0.04096}{\text{Current\_LSB} \times R_{SHUNT}}\right)$$

$$\text{Cal} = 4096 \quad (4)$$

6. Calculate the Power LSB, using Equation 5. Equation 5 shows a general formula; because the bus voltage measurement LSB is always 4mV, the power formula reduces to the calculated result.

$$\text{Power\_LSB} = 20 \times \text{Current\_LSB}$$

$$\text{Power\_LSB} = 400 \times 10^{-6} \quad (5)$$

7. Compute the maximum current and shunt voltage values (before overflow), as shown by Equation 6 and Equation 7. Note that both Equation 6 and Equation 7 involve an *If - then* condition:

$$\text{Max\_Current} = \text{Current\_LSB} \times 32767$$

$$\text{Max\_Current} = 0.65534 \quad (6)$$

If Max_Current ≥ Max Possible_I then
Max_Current_Before_Overflow = MaxPossible_I
Else
Max_Current_Before_Overflow = Max_Current
End If

(Note that Max_Current is greater than MaxPossible_I in this example.)

Max_Current_Before_Overflow = 0.64 (Note: This result is displayed by software as seen in Figure 25.)

$$\text{Max\_ShuntVoltage} = \text{Max\_Current\_Before\_Overflow} \times R_{SHUNT}$$

$$\text{Max\_ShuntVoltage} = 0.32 \quad (7)$$

If Max_ShuntVoltage ≥ V_{SHUNT_MAX}
Max_ShuntVoltage_Before_Overflow = V_{SHUNT_MAX}
Else
Max_ShuntVoltage_Before_Overflow= Max_ShuntVoltage
End If

(Note that Max_ShuntVoltage is greater than V_{SHUNT_MAX} in this example.)

Max_ShuntVoltage_Before_Overflow = 0.32 (Note: This result is displayed by software as seen in Figure 25.)

8. Compute the maximum power with Equation 8.

$$\text{MaximumPower} = \text{Max\_Current\_Before\_Overflow} \times V_{BUS\_MAX}$$

$$\text{MaximumPower} = 20.48 \quad (8)$$

9. (Optional second Calibration step.) Compute corrected full-scale calibration value based on measured current.

INA209_Current = 0.63484

MeaShuntCurrent = 0.55

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA209\_Current}}\right)$$

$$\text{Corrected\_Full\_Scale\_Cal} = 3548 \quad (9)$$

Figure 25 illustrates how to perform the same procedure discussed in this example using the automated INA209EVM software. Note that the same numbers used in the nine-step example are used in the software example in Figure 25. Also note that Figure 25 illustrates which results correspond to which step (for example, the information entered in Step 1 is enclosed in a box in Figure 25 and labeled).

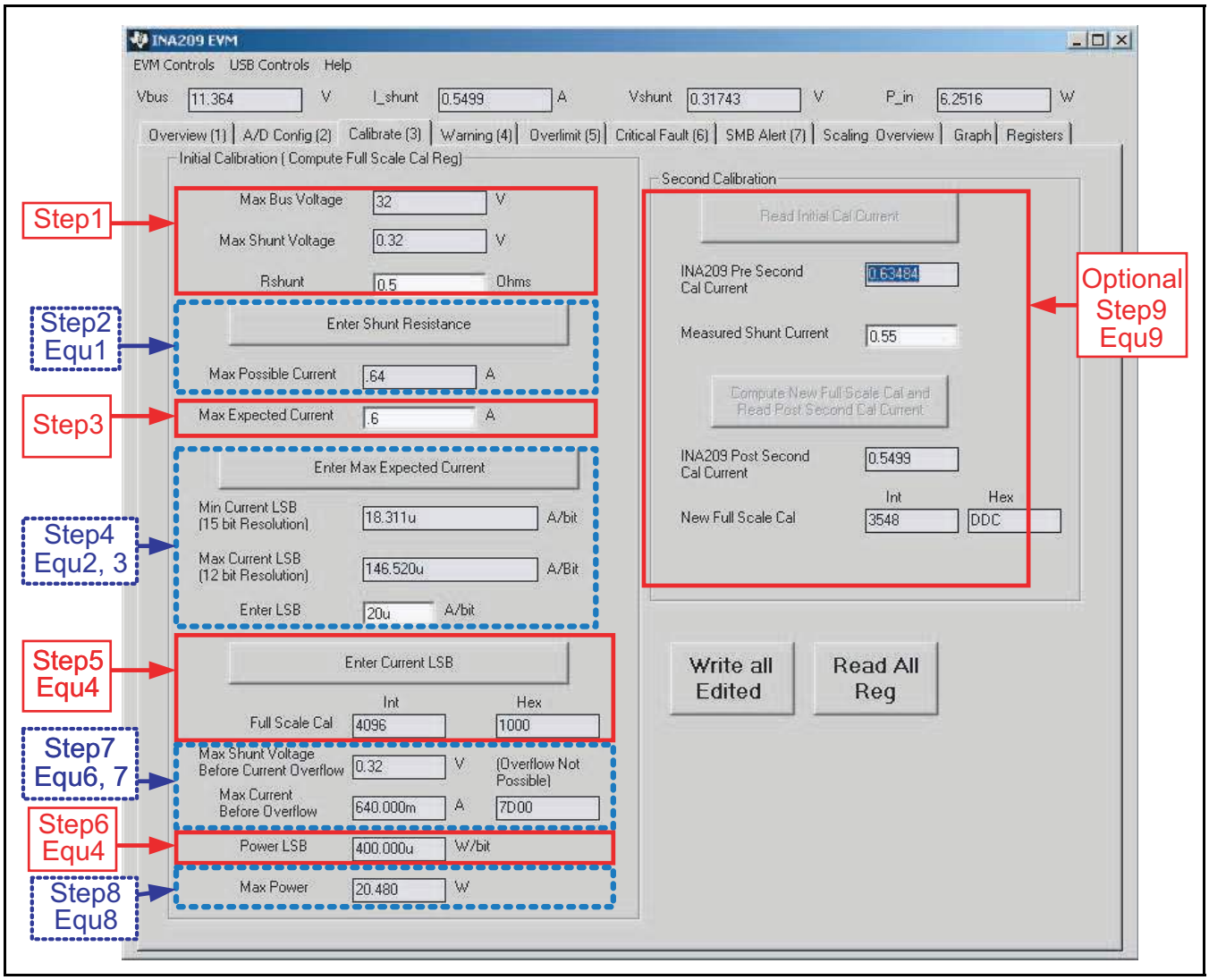


Figure 25. INA209 Calibration Sofware Automatically Computes Calibration Steps 1-9

Calibration Example 2 (Overflow Possible)

This design example uses the nine-step procedure for calibrating the INA209 where overflow is possible. Figure 26 illustrates how the same procedure is performed using the automated INA209EVM software. Note that the same numbers used in the nine-step example are used in the software example in Figure 26. Also note that Figure 26 illustrates which results correspond to which step (for example, the information entered in Step 1 is circled in Figure 26 and labeled).

1. Establish the following parameters:

   V_{BUS_MAX} = 32

   V_{SHUNT_MAX} = 0.32

   R_{SHUNT} = 5

2. Determine the maximum possible current using Equation 10:

$$\text{MaxPossible\_I} = \frac{V_{SHUNT\_MAX}}{R_{SHUNT}}$$

$$\text{MaxPossible\_I} = 0.064 \tag{10}$$

3. Choose the desired maximum current value: Max_Expected_I, ≤ MaxPossible_I. This value is selected based on system expectations.

   Max_Expected_I = 0.06

4. Calculate the possible range of current LSBs. This calculation is done by first computing a range of LSB's that is appropriate for the design. Next, select an LSB withing this range. Note that the results will have the most resolution when the minimum LSB is selected. Typically, an LSB is selected to be the nearest round number to the minimum LSB.

$$\text{Minimum\_LSB} = \frac{\text{Max\_Expected\_I}}{32767}$$

$$\text{Minimum\_LSB} = 1.831 \times 10^{-6} \tag{11}$$

$$\text{Maximum\_LSB} = \frac{\text{Max\_Expected\_I}}{4096}$$

$$\text{Maximum\_LSB} = 14.652 \times 10^{-6} \tag{12}$$

   Choose an LSB in the range: Minimum_LSB<Selected_LSB<Maximum_LSB

   Current_LSB = 1.9×10^{-6}

   Note:

   This value was selected to be a round number near the Minimum_LSB. This section allows for good resolution with a rounded LSB.

5. Compute the calibration register using Equation 13:

$$\text{Cal} = \text{trunc}\left(\frac{0.04096}{\text{Current\_LSB} \times R_{SHUNT}}\right) \quad \text{Cal} = 4311 \tag{13}$$

6. Calculate the Power LSB using Equation 14. Equation 14 shows a general formula; because the bus voltage measurement LSB is always 4mV, the power formula reduces to calculate the result.

$$\text{Power\_LSB} = 20\ \text{Current\_LSB}$$

$$\text{Power\_LSB} = 38 \times 10^{-6} \tag{14}$$

7. Compute the maximum current and shunt voltage values (before overflow), as shown by Equation 15 and Equation 16. Note that both Equation 15 and Equation 16 involve an *If - then* condition.

$$\text{Max\_Current} = \text{Current\_LSB} \times 32767$$
$$\text{Max\_Current} = 0.06226 \quad (15)$$

If Max_Current ≥ Max Possible_I then
Max_Current_Before_Overflow = MaxPossible_I
Else
Max_Current_Before_Overflow = Max_Current
End If

(Note that Max_Current is less than MaxPossible_I in this example.)

Max_Current_Before_Overflow = 0.06226 (Note: This result is displayed by software as seen in Figure 26.)

$$\text{Max\_ShuntVoltage} = \text{Max\_Current\_Before\_Overflow} \times R_{SHUNT}$$
$$\text{Max\_ShuntVoltage} = 0.3113 \quad (16)$$

If Max_ShuntVoltage ≥ V_{SHUNT_MAX}
Max_ShuntVoltage_Before_Overflow = V_{SHUNT_MAX}
Else
Max_ShuntVoltage_Before_Overflow= Max_ShuntVoltage
End If

(Note that Max_ShuntVoltage is less than V_{SHUNT_MAX} in this example.)

Max_ShuntVoltage_Before_Overflow = 0.3113 (Note: This result is displayed by software as seen in Figure 26.)

8. Compute the maximum power with equation 8.

$$\text{MaximumPower} = \text{Max\_Current\_Before\_Overflow} \times V_{BUS\_MAX}$$
$$\text{MaximumPower} = 1.992 \quad (17)$$

9. (Optional second calibration step.) Compute the corrected full-scale calibration value based on measured current.

INA209_Current = 0.06226

MeaShuntCurrent = 0.05

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left[\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA209\_Current}}\right]$$
$$\text{Corrected\_Full\_Scale\_Cal} = 3462 \quad (18)$$

Figure 26 illustrates how to perform the same procedure discussed in this example using the automated INA209EVM software. Note that the same numbers used in the nine-step example are used in the software example in Figure 26. Also note that Figure 26 illustrates which results correspond to which step (for example, the information entered in Step 1 is enclosed in a box in Figure 26 and labeled).

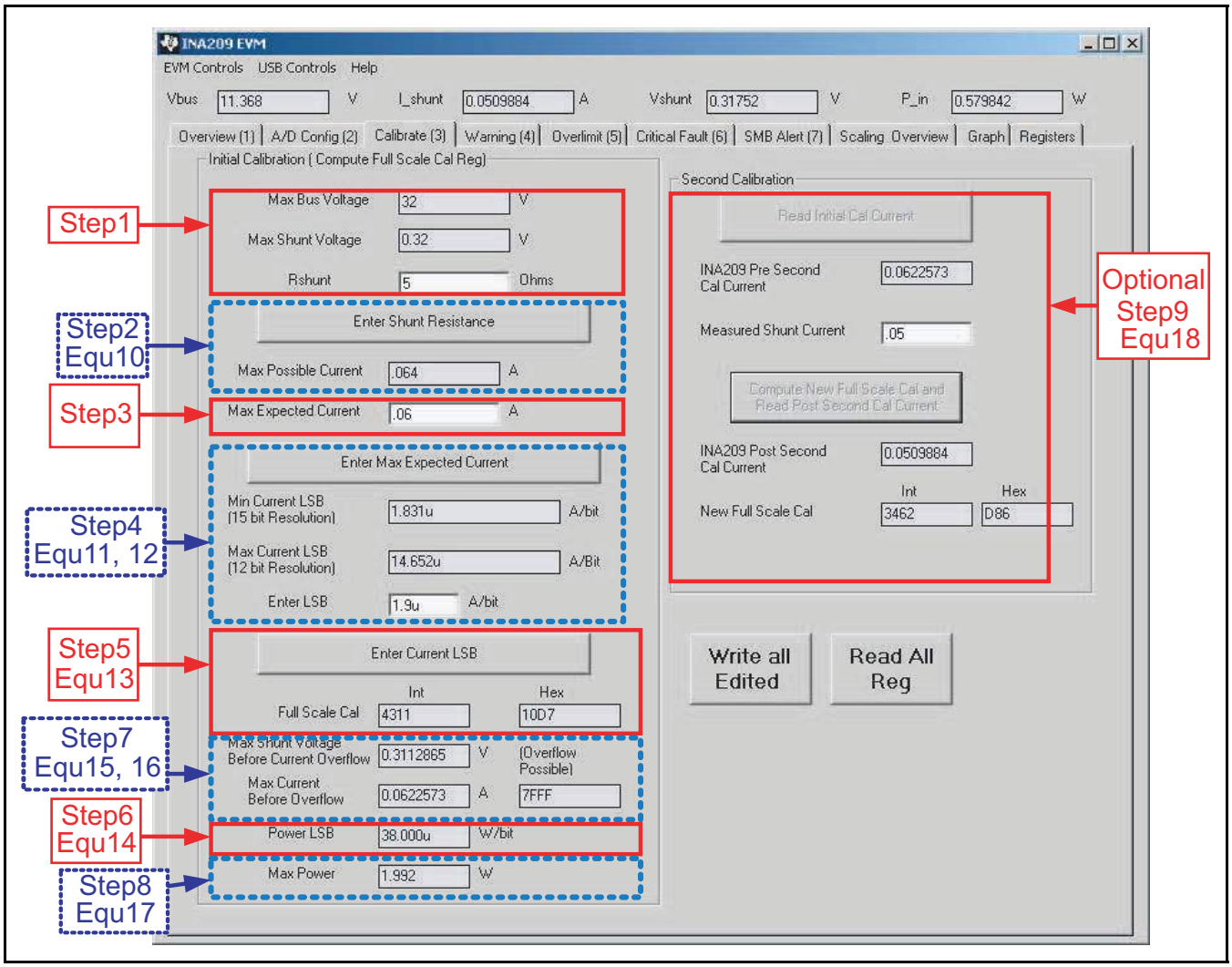


Figure 26. Calibration Software Automatically Computes Calibration Steps 1-9

REGISTER INFORMATION

The INA209 uses a bank of registers for holding configuration settings, measurement results, maximum/minimum limits, and status information. Table 2 summarizes the INA209 registers; Figure 14 illustrates registers.

Register contents are updated 4µs after completion of the write command. Therefore, a 4µs delay is required between completion of a write to a given register and a subsequent read of that register (without changing the pointer) when using SCL frequencies in excess of 1MHz.

Table 2. Summary of Register Set

POINTER ADDRESS			POWER-ON RESET		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE(1)
00	Configuration Register	All-register reset, settings for bus voltage range, PGA Gain, ADC resolution/averaging.	00111001 10011111	399F	R/$\overline{W}$
01	Status Register	Status flags for warnings, over-/under-limits, conversion ready, math overflow, and SMBus Alert.	00000000 00000000	0000	R
02	SMBus Alert Mask/Enable Control Register	Enables/disables flags in the Status Register	00000000 00000000	0000	R/$\overline{W}$
03	Shunt Voltage	Shunt voltage measurement data.	00000000 00000000	0000	R
04	Bus Voltage	Bus voltage measurement data.	00000000 00000000	0000	R
05	Power	Power measurement data.	00000000 00000000	0000	R
06	Current(2)	Contains the value of the current flowing through the shunt resistor.	00000000 00000000	0000	R
07	Shunt Voltage Positive Peak	Contains most positive voltage reading of Shunt Voltage Register.	10000000 00000000	8000	R/$\overline{W}$
08	Shunt Voltage Negative Peak	Contains most negative voltage reading of Shunt Voltage Register.	01111111 11111111	7FFF	R/$\overline{W}$
09	Bus Voltage Maximum Peak	Contains highest voltage reading of Bus Voltage Register.	00000000 00000000	0000	R/$\overline{W}$
0A	Bus Voltage Minimum Peak	Contains lowest voltage reading of Bus Voltage Register.	11111111 11111000	FFF8	R/$\overline{W}$
0B	Power Peak	Contains highest power reading of Power Register.	00000000 00000000	0000	R/$\overline{W}$
0C	Shunt Voltage Positive Warning	Warning watchdog register. Sets positive shunt voltage limit that triggers a warning flag in the Status Register, and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
0D	Shunt Voltage Negative Warning	Warning watchdog register. Sets negative shunt voltage limit that triggers a warning flag in the Status Register, and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
0E	Power Warning	Warning watchdog register. Sets power limit that triggers a warning flag in the Status Register, and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
0F	Bus Over-Voltage Warning	Warning watchdog register. Sets high Bus voltage limit that triggers a warning flag in the Status Register, and activates Warning pin. Also contains bits to set Warning pin polarity and latch feature.	00000000 00000000	0000	R/$\overline{W}$

(1) Type: **R** = Read-Only, **R/$\overline{W}$** = Read/Write.
(2) Current Register defaults to '0' because the Calibration Register defaults to '0', yielding a zero current value until the Calibration Register is programmed.

Table 2. Summary of Register Set (continued)

POINTER ADDRESS			POWER-ON RESET		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE(1)
10	Bus Under-Voltage Warning	Warning watchdog register. Sets low Bus voltage limit that triggers a warning flag in the Status Register and activates Warning pin.	00000000 00000000	0000	R/$\overline{W}$
11	Power Over-Limit	Over-limit watchdog register. Sets power limit that triggers an over-limit flag in the Status Register, and activates the Overlimit pin.	00000000 00000000	0000	R/$\overline{W}$
12	Bus Over-Voltage Over-Limit	Over-limit watchdog register. Sets Bus over-voltage limit that triggers an over-limit flag in the Status Register, and activates the Overlimit pin. Also contains bits to set Overlimit pin polarity and latch feature.	00000000 00000000	0000	R/$\overline{W}$
13	Bus Under-Voltage Over-Limit	Over-limit watchdog register. Sets Bus under-voltage limit that triggers an over-limit flag in the Status Register, and activates the Overlimit pin.	00000000 00000000	0000	R/$\overline{W}$
14	Critical DAC+ Register (Critical Shunt Positive Voltage)	Sets a positive limit for internal Critical DAC+. Contains bits for GPIO pin status and mode of operation, Critical Comparator latch feature and hysteresis.	00000000 00000000	0000	R/$\overline{W}$
15	Critical DAC– Register (Critical Shunt Negative Voltage)	Sets a negative limit for internal Critical DAC–. Contains bits for Warning pin delay, and Critical Comparator output filter configuration.	00000000 00000000	0000	R/$\overline{W}$
16	Calibration	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/$\overline{W}$

REGISTER DETAILS

All INA209 registers are 16-bit registers. 16-bit register data are sent in two 8-bit bytes via the I^2C interface.

Configuration Register 00h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	BRNG	PG1	PG0	BADC4	BADC3	BADC2	BADC1	SADC4	SADC3	SADC2	SADC1	MODE3	MODE2	MODE1
POR VALUE	0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	1

Bit Descriptions

RST: **Reset Bit**

Bit 15 Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.

BRNG: **Bus Voltage Range**

Bit 13
0 = 16V FSR
1 = 32V FSR (default value)

PG: **PGA (Shunt Voltage Only)**

Bits 11, 12 Sets PGA gain and range. Note that the PGA defaults to ÷8 (320mV range). Table 3 shows the gain and range for the various product gain settings.

Table 3. PG Bit Settings(1)

PG1	PG0	GAIN	RANGE
0	0	1	±40mV
0	1	÷2	±80mV
1	0	÷4	±160mV
1	1	÷8	±320mV

(1) Shaded values are default.

BADC: **BADC Bus ADC Resolution/Averaging**

Bits 7–10 These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (04h).

SADC: **SADC Shunt ADC Resolution/Averaging**

Bits 3–6 These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (03h).
BADC (Bus) and SADC (Shunt) ADC resolution/averaging and conversion time settings are shown in Table 4.

Table 4. ADC Settings(1)

ADC4	ADC3	ADC2	ADC1	MODE/SAMPLES	CONVERSION TIME
0	X(2)	0	0	9-bit	84µs
0	X(2)	0	1	10-bit	148µs
0	X(2)	1	0	11-bit	276µs
0	X(2)	1	1	12-bit	532µs
1	0	0	0	12-bit	532µs
1	0	0	1	2	1.06ms
1	0	1	0	4	2.13ms
1	0	1	1	8	4.26ms
1	1	0	0	16	8.51ms
1	1	0	1	32	17.02ms
1	1	1	0	64	34.05ms
1	1	1	1	128	68.10ms

(1) Shaded values are default.
(2) X = Don't care.

MODE: **Operating Mode**

Bits 0–2 Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 5.

Table 5. Mode Settings(1)

MODE3	MODE2	MODE1	MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	ADC Off (disabled)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

(1) Shaded values are default.

Status Register 01h (Read)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	WOV	WUV	WP	WS+	WS–	OLOV	OLUV	OLP	CRIT+	CRIT–	CNVR	SMBA	OVF	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Status Register flags activate whenever any limit is violated, and latch when corresponding latch bits are set. These flags are cleared when the Status Register is read (unless a limit is exceeded, at which time the flag immediately sets again).

After power-up and initial setup, the Status Register should be read once to clear any flags set as as a result of power-up values prior to setup.

Bit Descriptions

WOV: **Warning Bus Over-Voltage**

Bit 15 This bit is set to '1' when the result in the Bus Voltage Register (04h) exceeds the level set in the Bus Over-Voltage Warning Register (0Fh).

WUV: **Warning Bus Under-Voltage**

Bit 14 This bit is set to '1' when the result in the Bus Voltage Register (04h) is less than the value set in the Bus Under-Voltage Warning Register (10h).

WP: **Warning Power**

Bit 13 This bit is set to '1' when the value of the Power Register (05h) exceeds the level set in the Power Warning Register (0Eh).

WS+: **Warning Shunt+ Voltage**

Bit 12 This bit is set to '1' when the value of the Shunt Voltage Register (03h) exceeds the level set in the Shunt Voltage Positive Warning Register (0Ch).

WS–: **Warning Shunt– Voltage**

Bit 11 This bit is set to '1' when the value of the Shunt Voltage Register (03h) is more negative than the level set in the Shunt Voltage Negative Warning Register (0Dh).

OLOV: **Over-Limit Bus Over-Voltage**

Bit 10 This bit is set to '1' when the result in the Bus Voltage Register (04h) exceeds the level set in the Bus Over-Voltage Over-Limit Register (12h).

OLUV: **Over-Limit Bus Under-Voltage**

Bit 9 This bit is set to '1' when the result in the Bus Voltage Register (04h) is less than the level set in the Bus Under-Voltage Over-Limit Register (13h).

OLP: **Over-Limit Power**

Bit 8 This bit is set to '1' when the value of the Power Register (05h) exceeds the level set in the Power Over-Limit Register (11h).

Bit Descriptions (continued)

CRIT+:	**Critical Shunt Positive Voltage**
Bit 7	This bit is set to '1' when the value of the shunt voltage exceeds the positive limit set in the Critical DAC+ Register (14h).
CRIT–:	**Critical Shunt Negative Voltage**
Bit 6	This bit is set to '1' when the value of the shunt voltage is more negative than the negative limit set in the Critical DAC– Register (15h).
CNVR:	**Conversion Ready**
Bit 5	Although the INA209 can be read at any time, and the data from the last conversion are available, the Conversion Ready line is provided to help coordinate one-shot or triggered conversions. The Conversion bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready clears under the following conditions: 1. Writing the Configuration Register (except for Power-Down or Disable mode selections). 2. Reading the Status Register. 3. Trigger a single-shot conversion with the Convert pin.
SMBA:	**SMBus Alert**
Bit 4	Clears only on reading Status Register or by disabling SMBus Alert function.
OVF:	**Math Overflow**
Bit 3	This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be meaningless. It does not set any watchdog outputs.

SMBus Alert Mask/Enable Control Register 02h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	MWOV	MWUV	MWP	MWS+	MWS–	MOLOV	MOLUV	MOLP	MCRIT+	MCRIT–	MCNVR	—	SMAEN	CREN	OLEN	WRNEN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits D5–D15 of the SMBus Alert Mask Register mask correspond to bits D5 to D15 of the Status Register to prevent them from initiating an SMBus Alert. It does not prevent the Status Register bit from setting. Writing a '0' to an SMBus Alert Mask bit masks it from activating the SMBus Alert. All default values are '0'.

Bit Descriptions

MWOV: **Warning Bus Over-Voltage Mask**

Bit 15 When set to '0', this bit masks the WOV bit of the Status Register.

MWUV: **Warning Bus Under-Voltage Mask**

Bit 14 When set to '0', this bit masks the WUV bit of the Status Register.

MWP: **Warning Power Mask**

Bit 13 When set to '0', this bit masks the WP bit of the Status Register.

MWS+: **Warning Shunt Positive Voltage Mask**

Bit 12 When set to '0', this bit masks the WS+ bit of the Status Register.

MWS–: **Warning Shunt Negative Voltage Mask**

Bit 11 When set to '0', this bit masks the WS– bit of the Status Register.

MOLOV: **Over-Limit Bus Over-Voltage Mask**

Bit 10 When set to '0', this bit masks the OLOV bit of the Status Register.

MOLUV: **Over-Limit Bus Under-Voltage Mask**

Bit 9 When set to '0', this bit masks the OLUV bit of the Status Register.

MOLP: **Over-Limit Power Mask**

Bit 8 When set to '0', this bit masks the OLP bit of the Status Register.

MCRIT+: **Critical Shunt Positive Voltage Mask**

Bit 7 When set to '0', this bit masks the CRIT+ bit of the Status Register.

MCRIT–: **Critical Shunt Negative Voltage Mask**

Bit 6 When set to '0', this bit masks the CRIT– bit of the Status Register.

MCNVR: **Conversion Ready Mask**

Bit 5 When set to '0', this bit masks the CNVR bit of the Status Register.

SMAEN: **SMBus Alert Enable**

Bit 3
1 = Enable SMBus Alert
0 = Disable SMBus Alert (default)

CREN: **Critical DAC Enable**

Bit 2
Enables/disables operation of the Critical pin output.
1 = Enabled
0 = Disabled (default)

OLEN: **Over-Limit Enable**

Bit 1
Enables/disables operation of the Overlimit pin output.
1 = Enabled
0 = Disabled (default)

WRNEN: **Warning Enable**

Bit 0
Enables/disables operation of the Warning pin output.
1 = Enabled
0 = Disabled (default)

DATA OUTPUT REGISTERS

Shunt Voltage Register 03h (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT}. Shunt Voltage Register bits are shifted according to the PGA setting selected in the Configuration Register (00h). When multiple sign bits are present, they will all be the same value. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = '1'. Extend the sign to any additional sign bits to form the 16-bit word.

Example: For a value of V_{SHUNT} = –320mV:

1. Take the absolute value (include accuracy to 0.01mV)==> 320.00
2. Translate this number to a whole decimal number ==> 32000
3. Convert it to binary==> 111 1101 0000 0000
4. Complement the binary result : 000 0010 1111 1111
5. Add 1 to the Complement to create the Two's Complement formatted result ==> 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h (Remember to extend the sign to all sign-bits, as necessary based on the PGA setting.)

At PGA = ÷8, full-scale range = ±320mV (decimal = 32000, positive value hex = 7D00, negative value hex = 8300), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = ÷4, full-scale range = ±160mV (decimal = 16000, positive value hex = 3E80, negative value hex = C180), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = ÷2, full-scale range = ±80mV (decimal = 8000, positive value hex = 1F40, negative value hex = E0C0), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = ÷1, full-scale range = ±40mV (decimal = 4000, positive value hex = 0FA0, negative value hex = F060), and LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6. Shunt Voltage Register Format(1)

V_{SHUNT} Reading (mV)	Decimal Value	PGA = ÷ 8 (D15.....D0)	PGA = ÷ 4 (D15.....D0)	PGA = ÷ 2 (D15.....D0)	PGA = ÷ 1 (D15.....D0)
320.02	32002	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.01	32001	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.00	32000	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.99	31999	0111 1100 1111 1111	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.98	31998	0111 1100 1111 1110	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
160.02	16002	0011 1110 1000 0010	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.01	16001	0011 1110 1000 0001	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.00	16000	0011 1110 1000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
159.99	15999	0011 1110 0111 1111	0011 1110 0111 1111	0001 1111 0100 0000	0000 1111 1010 0000
159.98	15998	0011 1110 0111 1110	0011 1110 0111 1110	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
80.02	8002	0001 1111 0100 0010	0001 1111 0100 0010	0001 1111 0100 0000	0000 1111 1010 0000
80.01	8001	0001 1111 0100 0001	0001 1111 0100 0001	0001 1111 0100 0000	0000 1111 1010 0000
80.00	8000	0001 1111 0100 0000	0001 1111 0100 0000	0001 1111 0100 0000	0000 1111 1010 0000
79.99	7999	0001 1111 0011 1111	0001 1111 0011 1111	0001 1111 0011 1111	0000 1111 1010 0000
79.98	7998	0001 1111 0011 1110	0001 1111 0011 1110	0001 1111 0011 1110	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
40.02	4002	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0000
40.01	4001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0000
40.00	4000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000
39.99	3999	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111
39.98	3998	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110
⋮	⋮	⋮	⋮	⋮	⋮
0.02	2	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010
0.01	1	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001
0	0	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000
–0.01	–1	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111
–0.02	–2	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110
⋮	⋮	⋮	⋮	⋮	⋮
–39.98	–3998	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010
–39.99	–3999	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001
–40.00	–4000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000
–40.01	–4001	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0110 0000
–40.02	–4002	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–79.98	–7998	1110 0000 1100 0010	1110 0000 1100 0010	1110 0000 1100 0010	1111 0000 0110 0000
–79.99	–7999	1110 0000 1100 0001	1110 0000 1100 0001	1110 0000 1100 0001	1111 0000 0110 0000
–80.00	–8000	1110 0000 1100 0000	1110 0000 1100 0000	1110 0000 1100 0000	1111 0000 0110 0000
–80.01	–8001	1110 0000 1011 1111	1110 0000 1011 1111	1110 0000 1100 0000	1111 0000 0110 0000
–80.02	–8002	1110 0000 1011 1110	1110 0000 1011 1110	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–159.98	–15998	1100 0001 1000 0010	1100 0001 1000 0010	1110 0000 1100 0000	1111 0000 0110 0000
–159.99	–15999	1100 0001 1000 0001	1100 0001 1000 0001	1110 0000 1100 0000	1111 0000 0110 0000
–160.00	–16000	1100 0001 1000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.01	–16001	1100 0001 0111 1111	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.02	–16002	1100 0001 0111 1110	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–319.98	–31998	1000 0011 0000 0010	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–319.99	–31999	1000 0011 0000 0001	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.00	–32000	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.01	–32001	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.02	–32002	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000

(1) Out-of-range values are shown in grey shading.

Bus Voltage Register 04h (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, V_{BUS}.

At full-scale range = 32V (decimal = 8000, hex = 1F40), and LSB = 4mV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At full-scale range = 16V (decimal = 4000, hex = 0FA0), and LSB = 4mV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	0	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Power Register 05h (Read-Only)

Full-scale range and LSB are set by the Calibration Register. See the *Programming the INA209 Power Measurement Engine* section.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Power Register records power in watts by multiplying the values of the current with the value of the bus voltage according to the equation:

$$\text{Power} = \frac{\text{Current} \times \text{BusVoltage}}{5000}$$

Current Register 06h (Read-Only)

Full-scale range and LSB depend on the value entered in the Calibration Register. See the *Programming the INA209 Power Measurement Engine* section. Negative values are stored in two's complement format.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value of the Current Register is calculated by multiplying the value in the Shunt Voltage Register with the value in the Calibration Register according to the equation:

$$\text{Current} = \frac{\text{ShuntVoltage} \times \text{Calibration Register}}{4096}$$

PEAK-HOLD REGISTERS

Note: All peak-hold registers are cleared and reset to POR values by writing a '1' into the respective D0 bits.

Shunt Voltage Positive Peak Register 07h (Read/Write)

Mirrors highest voltage reading of the Shunt Voltage Register (03h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SPP SIGN	SPP14	SPP13	SPP12	SPP11	SPP10	SPP9	SPP8	SPP7	SPP6	SPP5	SPP4	SPP3	SPP2	SPP1	SPP0/RS
POR VALUE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Shunt Voltage Negative Peak Register 08h (Read/Write)

Mirrors lowest voltage reading (positive or negative) of the Shunt Voltage Register (03h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SPN SIGN	SPN14	SPN13	SPN12	SPN11	SPN10	SPN9	SPN8	SPN7	SPN6	SPN5	SPN4	SPN3	SPN2	SPN1	SPN0/RS
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bus Voltage Maximum Peak Register 09h (Read/Write)

Mirrors highest voltage reading of the Bus Voltage Register (04h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BH12	BH11	BH10	BH9	BH8	BH7	BH6	BH5	BH4	BH3	BH2	BH1	BH0	—	—	BPK/RS
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Minimum Peak Register 0Ah (Read/Write)

Mirrors lowest voltage reading of the Bus Voltage Register (04h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BL12	BL11	BL10	BL9	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	—	—	BL/RS
POR VALUE	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Power Peak Register 0Bh (Read/Write)

Mirrors highest reading of the Power Register (05h).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PPK15	PPK14	PPK13	PPK12	PPK11	PPK10	PPK9	PPK8	PPK7	PPK6	PPK5	PPK4	PPK3	PPK2	PPK1	PPK0/RS
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WARNING WATCHDOG REGISTERS

These registers set warning limits that trigger flags in the Status Register and activate the Warning pin. **Note:** Delayed output is set in the Critical DAC– Register (15h).

Shunt Voltage Positive Warning Register 0Ch (Read/Write)

At full-scale range = ±320mV, 15-bit + sign, LSB = 10μV (decimal = 32000, positive value hex = 7D00, negative value hex = 8300).

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SWP SIGN	SWP14	SWP13	SWP12	SWP11	SWP10	SWP9	SWP8	SWP7	SWP6	SWP5	SWP4	SWP3	SWP	SWP1	SWP0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

SWP: **Sets the shunt voltage positive warning limit.**

Bits 15–0 If the value of the Shunt Voltage Register (03h) exceeds this limit, the WS+ bit of the Status Register (01h) is set to '1' and the Warning pin asserts if the WRNEN bit is set.

Shunt Voltage Negative Warning Register 0Dh (Read/Write)

At full-scale range = ±320mV (decimal = 32000, positive value hex = 7D00, negative value hex = 8300), 15 bit + sign, LSB = 10μV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SWN SIGN	SWN14	SWN13	SWN12	SWN11	SWN10	SWN9	SWN8	SWN7	SWN6	SWN5	SWN4	SWN3	SWN2	SWN1	SWN0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

SWN: **Sets the shunt voltage negative warning limit.**

Bits 15–0 If the value of the Shunt Voltage Register (03h) is below this limit, the WS– bit of the Status Register (01h) is set to '1' and the Warning pin asserts if the WRNEN bit is set.

Power Warning Register 0Eh (Read/Write)

At full-scale range, same as the Power Register.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PW15	PW14	PW13	PW12	PW11	PW10	PW9	PW8	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

PW: **Sets the power warning limit.**

Bits 15–0 If the value of the Power Register (05h) exceeds this limit, the WP bit of the Status Register (01h) is set to '1' and the Warning pin asserts if the WRNEN bit is set.

Bus Over-Voltage Warning Register 0Fh (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BWO12	BWO11	BWO10	BWO9	BWO8	BWO7	BWO6	BWO5	BWO4	BWO3	BWO2	BWO1	BWO0	—	WPL	WNL
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BWO:	**Sets the bus over-voltage warning limit.**
Bits 15–3	If a Bus Voltage Register (04h) value exceeds this limit, the WOV bit of the Status Register (01h) is set to '1' and the Warning pin asserts if the WRNEN bit is set.
WPL:	**The Warning Polarity bit sets the Warning pin polarity.**
Bit 1	1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)
WNL:	**The Warning Latch bit configures the latching feature of the Warning pin.**
Bit 0	1 = Latch enabled 0 = Transparent (default)

Bus Under-Voltage Warning Register 10h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BWU12	BWU11	BWU10	BWU9	BWU8	BWU7	BWU6	BWU5	BWU4	BWU3	BWU2	BWU1	BWU0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BWU:	**Sets the bus over-voltage warning limit.**
Bits 15–3	If a Bus Voltage Register (04h) value is below this limit, the WUV bit of the Status Register (01h) is set to '1' and the Warning pin asserts if the WRNEN bit is set.

OVER-LIMIT/CRITICAL WATCHDOG REGISTERS

These registers set the over-limit and critical DAC limits that trigger flags to be set in the Status Register and activate the Overlimit pin or the Critical pin.

Power Over-Limit Register 11h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PO15	PO14	PO13	PO12	PO11	PO10	PO9	PO8	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

PO: **Sets the power over-limit value.**

Bits 15–0 If the value of the Power Register (05h) exceeds this limit, the OLP bit of the Status Register (01h) is set to '1' and the Overlimit pin asserts if the OLEN bit is set.

Bus Over-Voltage Over-Limit Register 12h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BOO12	BOO11	BOO10	BOO9	BOO8	BOO7	BOO6	BOO5	BOO4	BOO3	BOO2	BOO1	BOO0	—	OLP	OLL
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BOO: **Sets the bus over-voltage over-limit value.**

Bits 15–3 If a Bus Voltage Register (04h) value exceeds this limit, the OLOV bit of the Status Register (01h) is set to '1' and the Overlimit pin asserts if the OLEN bit is set.

OLP: **The Over-Limit Polarity bit sets the Overlimit pin polarity.**

Bit 1
1 = Inverted (asserts high)
0 = Normal (asserts low) (default)

OLL: **The Over-Limit Latch bit configures the latching feature of the Overlimit pin.**

Bit 0
1 = Latch enabled
0 = Transparent (default)

Bus Under-Voltage Over-Limit Register 13h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BUO12	BUO11	BUO10	BUO9	BUO8	BUO7	BUO6	BUO5	BUO4	BUO3	BUO2	BUO1	BUO0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

BUO: **Sets the bus under-voltage over-limit value.**

Bits 15–3 If a Bus Voltage Register (04h) value is below this limit, the OLUV bit of the Status Register (01h) is set to '1' and the Overlimit pin asserts if the OLEN bit is set.

Critical DAC+ Register (Critical Shunt Positive Voltage) 14h (Read/Write)

No sign bit (sets a positive limit only). At full-scale range = 255mV; LSB = 1mV; 8-bit.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CDP7	CDP6	CDP5	CDP4	CDP3	CDP2	CDP1	CDP0	GP	GMP1	GPM0	CP	CHYST 2	CHYST 1	CHYST 0	CRL
POR VALUE	0	0	0	0	0	0	0	0	(1)	0	0	0	0	0	0	0

(1) POR value reflects the state of the GPIO pin.

Bit Descriptions

CDP: **Critical DAC+ limit setting.**

Bits 15–8

GP: **GPIO read back.**

Bit 7 Shows state of the GPIO pin.

GPM: **GPIO mode bit.**

Bits 6, 5 The GPIO mode settings are shown in Table 7.

Table 7. GPIO Mode Settings(1)

GPM1	GPM0	STATE	NOTES
0	0	Hi-Z	Use as an input in either of these modes.
0	1	Hi-Z	
1	0	0	
1	1	1	

(1) Shaded values are default.

CP: **Configures the Critical output pin polarity (open-drain output).**

Bit 4
1 = Active high
0 = Active low (default)

CHYST: **Configures Critical comparator hysteresis.**

Bits 3–1 The CHYST settings are shown in Table 8.

Table 8. CHYST Settings(1)

CHYST2	CHYST1	CHYST0	HYSTERESIS
0	0	0	0mV
0	0	1	2mV
0	1	0	4mV
0	1	1	6mV
1	0	0	8mV
1	0	1	10mV
1	1	0	12mV
1	1	1	14mV

(1) Shaded values are default.

CRL: **Configures Critical pin latch feature.**

Bit 0
1 = Latch enabled
0 = Transparent (default)

Critical DAC– Register (Critical Shunt Negative Voltage) 15h (Read/Write)

No sign bit (sets negative limit only). At full-scale range = –255mV; LSB = 1mV; 8-bit.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CDP7	CDP6	CDP5	CDP4	CDP3	CDP2	CDP1	CDP0	CF3	CF2	CF1	CF0	WD3	WD2	WD1	WD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions

CDP: **Critical DAC- limit setting.**

Bits 15–8

CF: **Configures DAC Comparator output filter.**

Bits 7–4 Ranges from 0 to 0.96ms; 64s/LSB. CF settings are listed in Table 9.

WD: **Configures Warning pin Output Delay from 0 to 1.5s; 0.1 second/LSB.**

Bits 3–0 Default = 0. WD settings are listed in Table 10.

Table 9. CF Settings

CF3	CF2	CF1	CF0	FILTER SETTING (ms)
0	0	0	0	0
0	0	0	1	0.064
0	0	1	0	0.128
0	0	1	1	0.192
0	1	0	0	0.256
0	1	0	1	0.320
0	1	1	0	0.384
0	1	1	1	0.448
1	0	0	0	0.512
1	0	0	1	0.576
1	0	1	0	0.640
1	0	1	1	0.704
1	1	0	0	0.768
1	1	0	1	0.832
1	1	1	0	0.896
1	1	1	1	0.960

Table 10. WD Settings

WD3	WD2	WD1	WD0	DELAY SETTING (s)
0	0	0	0	0
0	0	0	1	0.1
0	0	1	0	0.2
0	0	1	1	0.3
0	1	0	0	0.4
0	1	0	1	0.5
0	1	1	0	0.6
0	1	1	1	0.7
1	0	0	0	0.8
1	0	0	1	0.9
1	0	1	0	1.0
1	0	1	1	1.1
1	1	0	0	1.2
1	1	0	1	1.3
1	1	1	0	1.4
1	1	1	1	1.5

Calibration Register 16h (Read/Write)

Current and power calibration are set by bits D15 to D1 of the Calibration Register. Note that bit D0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full-scale range and the LSB of the current and power measurement depend on the value entered in this register. See the *Programming the INA209 Power Measurement Engine* section. This register is suitable for use in overall system calibration. Note that the '0' POR values are all default.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0(1)
BIT NAME	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0	FRB
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D0 is a *void* bit and will always be '0'. It is not possible to write a '1' to D0. CALIBRATION is the value stored in D15:D1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA209AIPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA209A	Samples
INA209AIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA209A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

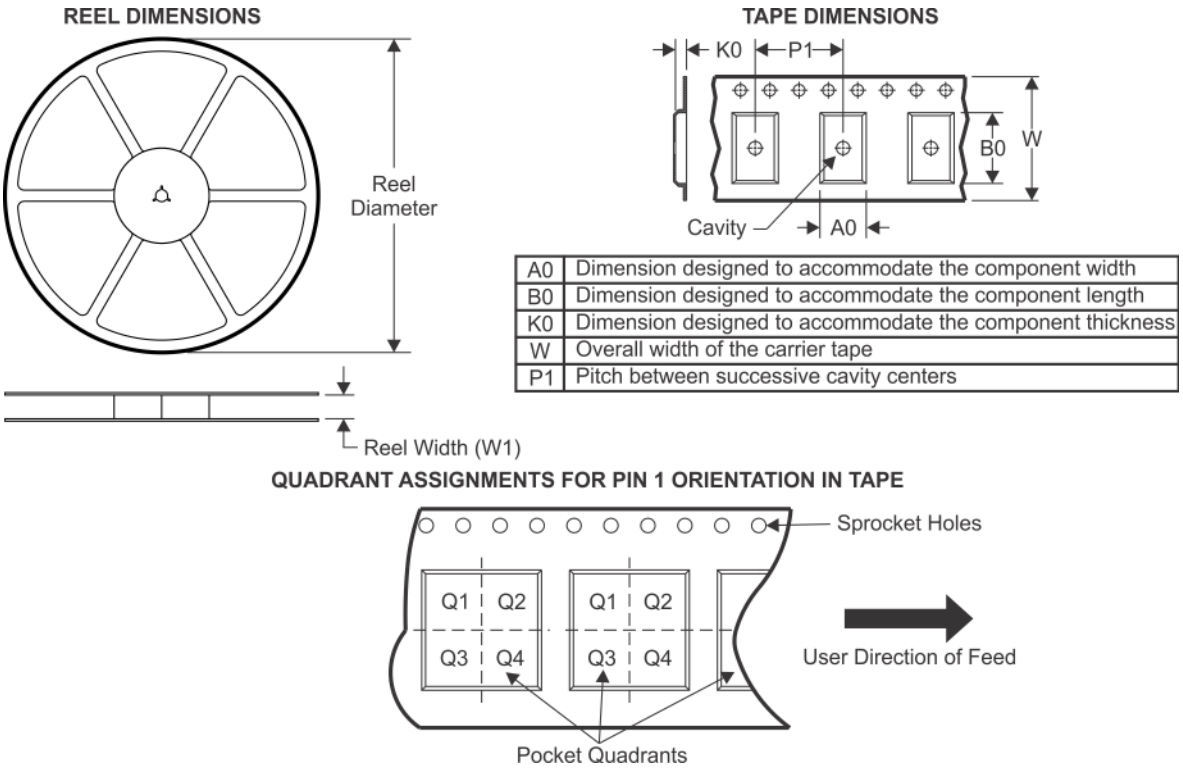
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

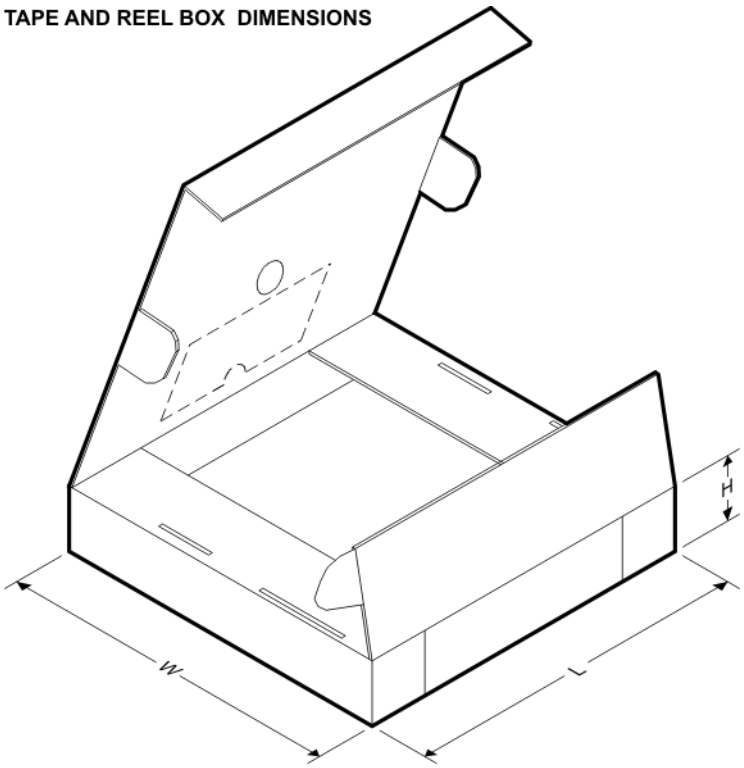


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA209AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

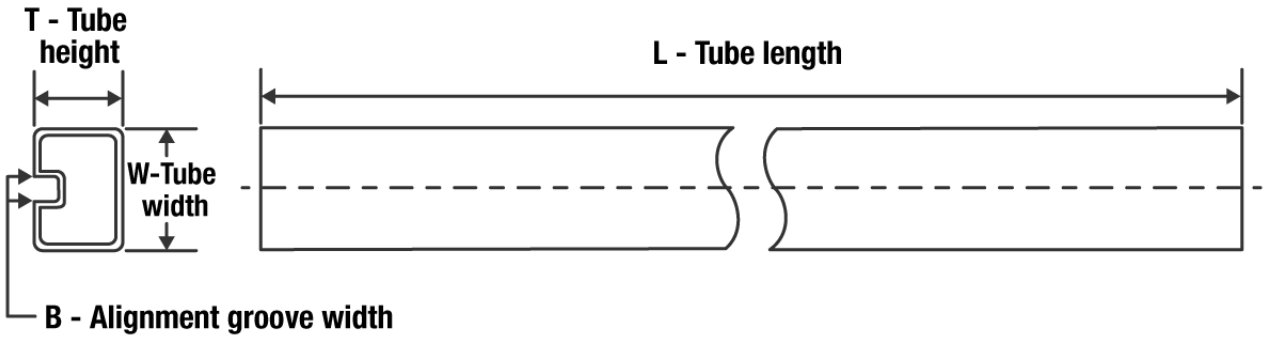
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA209AIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

TUBE

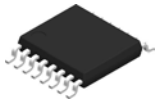


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA209AIPW	PW	TSSOP	16	90	530	10.2	3600	3.5

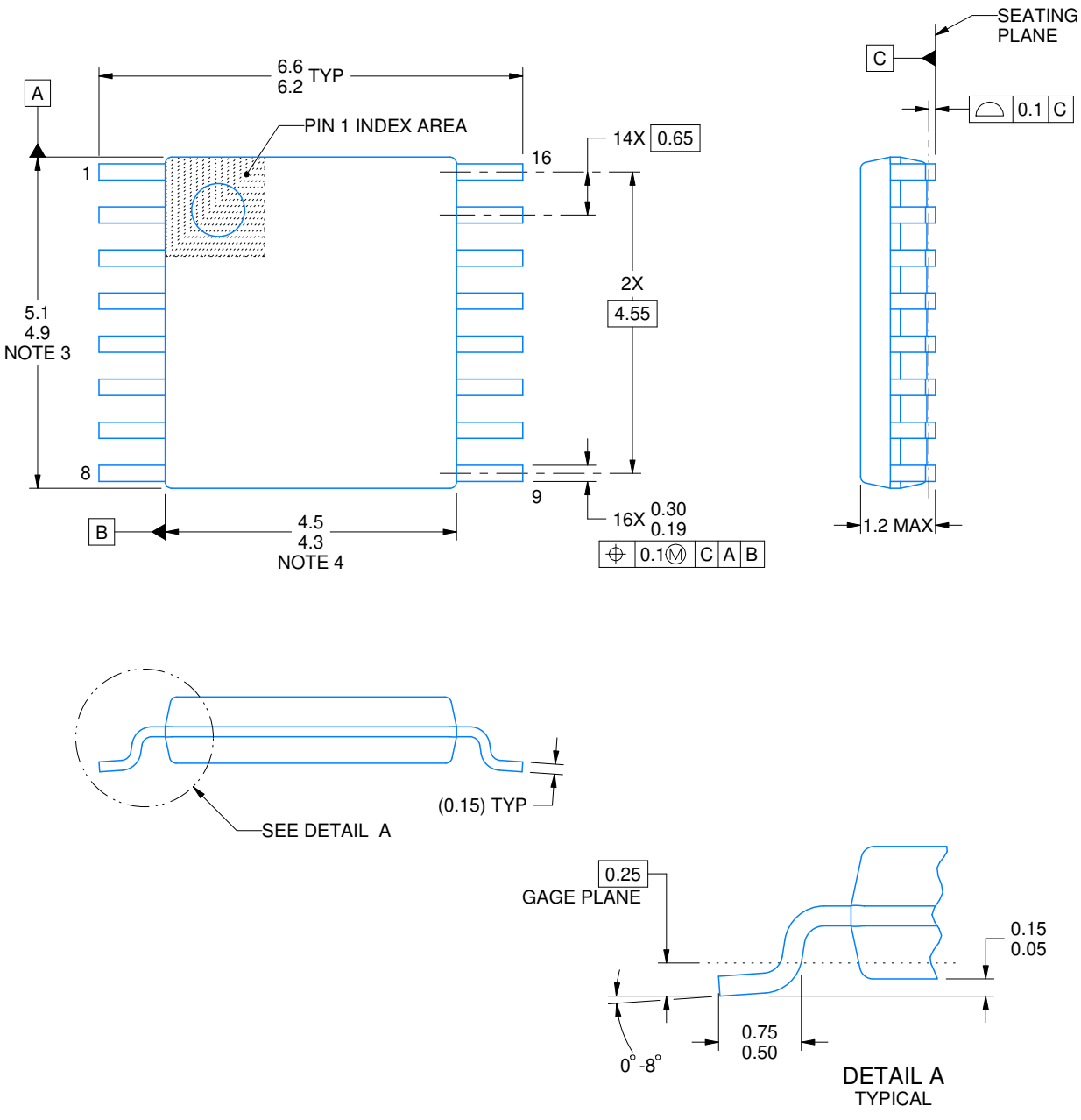
PACKAGE OUTLINE

PW0016A



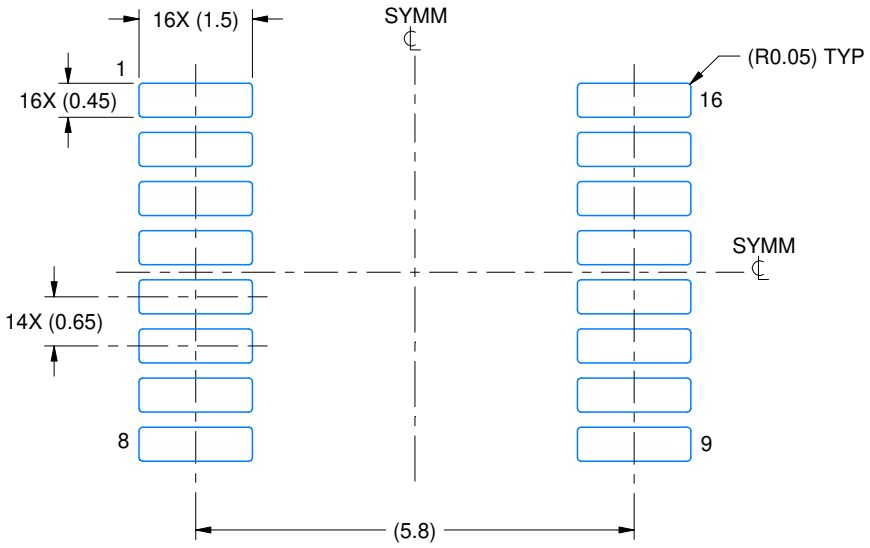
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

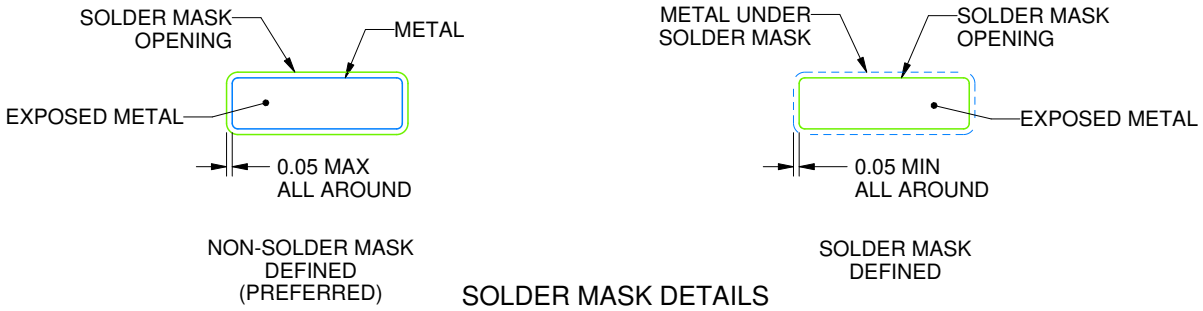


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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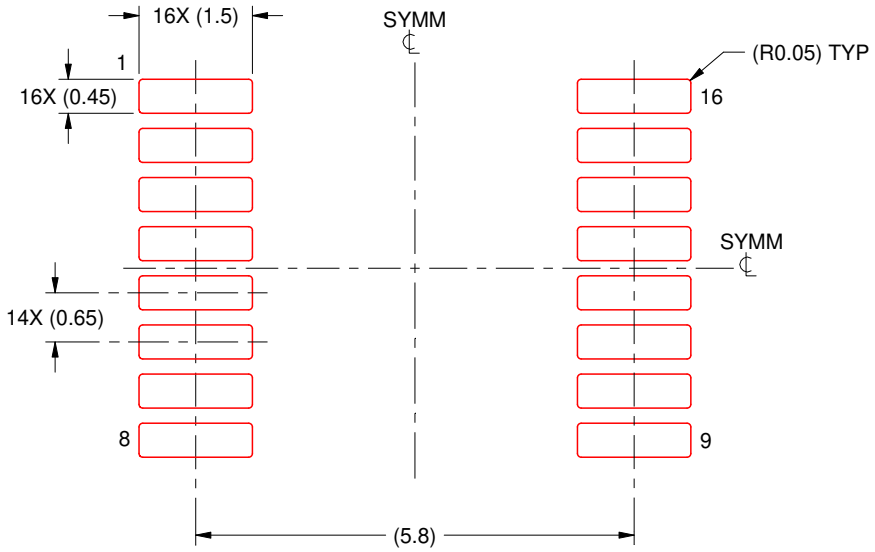
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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