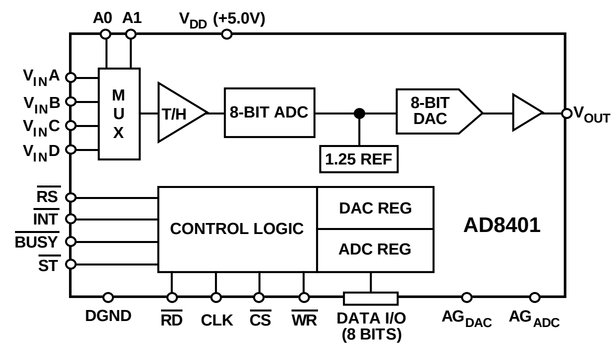
8-Bit, 4-Channel Data Acquisition System

AD8401

FEATURES
- **2 µs ADC with T/H**
- **4-Channel MUX**
- **AD899 Compatible**
- **+5 Volt Operation**
- **On-Chip Reference**
- **4 µs Voltage Output DAC**
- **Fast Bus Access Time—75 ns**

APPLICATIONS
- **Servo Controls**
- **Digitally Controlled Calibration**
- **Process Control Equipment**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8401 is a complete data acquisition and control system containing ADC, DAC, 4-channel MUX, and internal voltage reference. Built using CBCMOS, this monolithic circuit offers the user a complete system with very high package density and reliability.

The converter is a successive approximation ADC with T/H, and is capable of operating with conversion times as short as 2 µs. Analog input bandwidth is 200 kHz, and DAC output voltage settling time is less than 4 µs, making the AD8401 capable of controlling servo loops with speed and precision.

The 8-bit data interface provides both read and write operation for parallel bus interfaces to microcontrollers and DSP processors. An external 5 MHz clock sets the 2 µs conversion rate. Slower clocks reduce the conversion time and the internal power dissipation. The standard control lines: Reset, Busy, Interrupt, Read and Write complete the handshaking signals for microprocessor communication. A start trigger $\overline{ST}$ input allows precise sampling intervals in synchronous sampling applications.

The input multiplexer addressing is designed for direct interface to the AD899 hard-disk drive, read-channel device with no extra hardware or special software. Analog input range levels are likewise compatible with the AD899.

The AD8401 is designed to operate from a single +5 volt supply, which will give an ADC input range of 0 V to 3.0 V, and DAC output range of 0 V to 2.5 V.

The AD8401 is offered in the SOIC-28 surface mount package, and is guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD8401–SPECIFICATIONS

ADC ELECTRICAL CHARACTERISTICS
($@ V_{DD} = +5.0\ V \pm 5\%$, $AG_{DAC} = AG_{ADC} = 0.0\ V$; $f_{CLK} = 5\ MHz$; $-40°C \leq T_A \leq +85°C$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N		8			Bits
Total Unadjusted Error	TUE			±3		LSB
Relative Accuracy	INL		–1		+1	LSB
Differential Nonlinearity	DNL		–1		+1	LSB
Offset Error	V_{OSE}	$T_A = +25°C$	–4		+4	LSB
		T_A = Full Temp Range	–6		+6	LSB
Full-Scale Error	A_E	$T_A = +25°C$	–4		+4	LSB
		T_A = Full Temp Range	–6		+6	LSB
ΔFull-Scale/ΔV_{DD}		$T_A = +25°C$			1	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio	SNR			44		dB
Total Harmonic Distortion	THD			48		dB
Intermodulation Distortion	IMD			60		dB
Frequency Response		0 to 200 kHz		0.1		dB
Track/Hold Acquisition Time	t_{AQ}			200		ns
ANALOG INPUTS (Applies to Inputs A, B, C, D)						
Unipolar Input Range	V_{IN}		0		3	V
Input Current	I_{IN}		–500		+500	µA
Input Capacitance	C_{IN}			10		pF
LOGIC INPUTS						
Clock Input Current Low	I_{CKL}	$V_{IN} = 0\ V$	1.6			mA
Clock Input Current High	I_{CKH}	$V_{IN} = V_{DD}$			40	µA
Input Leakage Current	I_L	$\overline{CS}$, $\overline{RD}$, $\overline{RS}$, $\overline{ST}$			10	µA
LOGIC OUTPUTS (Applies to Outputs DB0–DB7, $\overline{INT}$, $\overline{BUSY}$)						
Logic Output Low Voltage	V_{OL}	$I_{OL} = 1.6\ mA$			0.4	V
Logic Output High Voltage	V_{OH}	$I_{OH} = 200\ \mu A$	4.0			V
Output Leakage Current	I_{OZ}	$\overline{CS} = 1$ (Except $\overline{INT}$ & $\overline{BUSY}$)			10	µA
Output Capacitance	C_{OZ}	$\overline{CS} = 1$ (Except $\overline{INT}$ & $\overline{BUSY}$)			10	pF
CONVERSION TIME	t_C	External Clock			2	µs

Specifications subject to change without notice.

Table I. Multiplexer Address Input Decode

A1	A0	Input Selected
0	0	$V_{IN}A$
0	1	$V_{IN}B$
1	0	$V_{IN}C$
1	1	$V_{IN}D$

DAC ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5.0 V ± 5%, AG_{DAC} = AG_{ADC} = 0.0 V; R_L = 2 kΩ, C_L = 100 pF to AG_{DAC}; –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N		8			Bits
Total Unadjusted Error	TUE			±2		LSB
Relative Accuracy	INL		–1		+1	LSB
Differential Nonlinearity	DNL		–1		+1	LSB
Offset Error	V_{OSE}	T_A = +25°C	–2		+2	LSB
		T_A = Full Temp Range	–2.5		+2.5	LSB
Full-Scale Error	A_E	T_A = +25°C	–3		+3	LSB
		T_A = Full Temp Range	–4		+4	LSB
ΔFull-Scale/ΔV_{DD}		T_A = +25°C	–0.5		+0.5	LSB
Load Regulation at Full-Scale			–0.2		+0.2	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio	SNR			44		dB
Total Harmonic Distortion	THD			48		dB
ANALOG OUTPUT						
Output Voltage Range	OVR		0		+2.5	V
LOGIC INPUTS (Applies to DB0–DB7, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RS}$)						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_L		–10		10	µA
Input Capacitance	C_{IL}				10	pF
AC CHARACTERISTICS						
Voltage Output Settling Time	t_S	To ±1/2 LSB of Final Value		2	4	µs
Positive Full-Scale Change	t_{POS}	10% to 90%		1	2	µs
Negative Full-Scale Change	t_{NEG}	90% to 10%		2	4	µs
DAC Glitch Impulse				15		nV s
Digital Feedthrough				1		nV s
V_{IN} to V_{OUT} Isolation		f = 50 kHz		60		dB
POWER REQUIREMENTS						
Positive Supply Current	I_{DD}	No Load			13	mA

Specifications subject to change without notice.

TIMING ELECTRICAL SPECIFICATIONS (@ V_{DD} = +5.0 V ± 5%, AG_{DAC} = AG_{ADC} = 0.0 V; f_{CLK} = 5 MHz; –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameters[1, 2, 3]	Symbol	Condition	Min	Typ	Max	Units
DAC TIMING (See Figure 8 Timing Diagram)						
$\overline{WR}$ Pulse Width	t_1		50			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_2		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3		0			ns
Data Setup Time	t_4		60			ns
Data Hold Time	t_5		0			ns
ADC TIMING (See Figures 6 and 7 Timing Diagrams)						
$\overline{ST}$ Pulse Width	t_6		40			ns
$\overline{ST}$ to $\overline{BUSY}$ Delay	t_7				110	ns
$\overline{BUSY}$ to $\overline{INT}$ Delay	t_8				30	ns
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_9		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{10}		0			ns
$\overline{RD}$ Pulse Width[4]	t_{11}		75			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{12}		0			ns
Data Access after $\overline{RD}$	t_{13}	C_L = 20 pF	10		75	ns
Data Access after $\overline{RD}$	t_{13}	C_L = 100 pF	10		135	ns
Bus Relinquish after $\overline{RD}$	t_{14}		10		70	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{15}				85	ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_{16}				110	ns
Data Valid after $\overline{BUSY}$	t_{17}	C_L = 20 pF			90	ns
Data Valid after $\overline{BUSY}$	t_{17}	C_L = 100 pF			135	ns

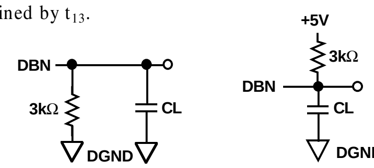
NOTES

[1]All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross either 0.8 V or 2.4 V.

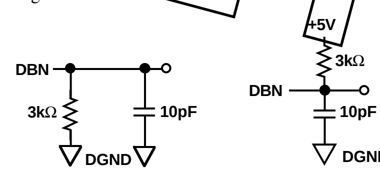
[3]t_{14} is defined as the time required for the data line to change 0.5 V when loaded with the circuit of Figure 2.

[4]t_{15} is determined by t_{13}.



a. High Z to V_{OH}   *b. High Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z   *b. V_{OL} to High Z*

Figure 2. Load Circuits for Bus Relinquish Time Test

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) . . . . +8 V
Input Voltages . . . . –0.3 V to V_{DD} + 0.3 V
Output Short-Circuit Duration . . . . Indefinite
Package Power Dissipation . . . . (T_J max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}
28-Lead SOIC (R) . . . . 53°C/W
Storage Temperature Range . . . . –65°C to +150°C
Operating Temperature Range . . . . –40°C to +85°C
Junction Temperature Range (T_J max) . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . . +300°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

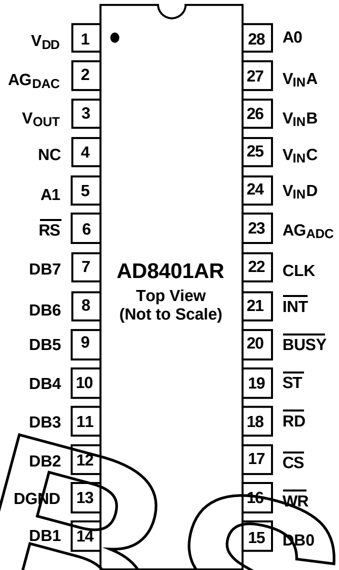
Model*	Temperature Range	Package Description	Package Option
AD8401AR	–40°C to +85°C	28-Lead SOIC	SOL-28
AD8401Chips	+25°C	Die	

*The AD8401 contains 1257 transistors.

CAUTION

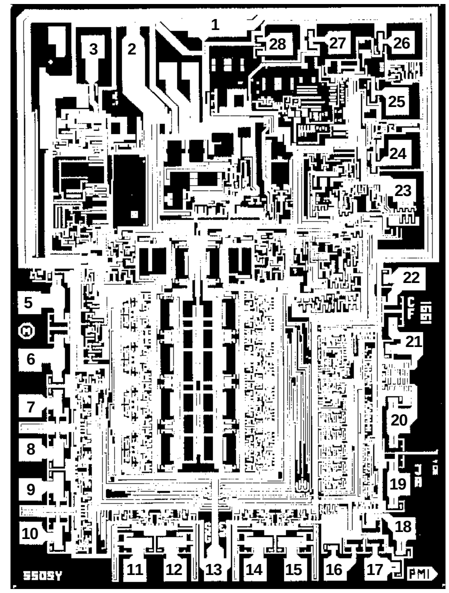
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8401 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NC = NO CONNECT

DICE CHARACTERISTICS



Die Size 91 X 121 mil = 11,011 sq mil

PIN DESCRIPTIONS

Pin#	Name	Description
1	V_{DD}	Positive Supply. Nominal value +5 volts. This pad requires 2 bonds for die assembly. The substrate is common with V_{DD}.
2	AG_{DAC}	Analog Ground for the DAC. There is a separate analog ground for the ADC.
3	V_{OUT}	Voltage Output from the DAC.
4	NC	No Connect.
5	A1	Address Input that controls multiplexer. See Table I for address decode.
6	RESET ($\overline{RS}$)	Active Low Digital Input that clears the DAC register to zero, setting the DAC to minimum scale. It also asynchronously clears the $\overline{INT}$ line of the ADC.
7–12, 14, 15	DB7 to DB0	Digital I/O Lines. DB7 (7) is the Most Significant Bit (MSB), for both the ADC and the DAC, and DB0 (15) is the Least Significant Bit (LSB).
13	DGND	Digital Ground.
16	$\overline{WR}$	Rising Edge Triggered Write Input. Used to load data into the DAC register.
17	$\overline{CS}$	Chip Select. Active Low Input
18	$\overline{RD}$	Active Low Read Input. When this input is active, ADC data can be read from the part. $\overline{RD}$ going low starts the ADC conversion.
19	$\overline{ST}$	Falling Edge Triggered Start Input. Used for applications requiring precise sample timing. The falling edge of $\overline{ST}$ starts the conversion and sets the $\overline{BUSY}$ low. The $\overline{ST}$ is not gated by $\overline{CS}$.
20	$\overline{BUSY}$	ADC Active Low, Status Output. When the ADC is performing a conversion, the $\overline{BUSY}$ output is low.
21	$\overline{INT}$	Active Low Output. The Interrupt output notifies the system that the ADC has completed its conversion. $\overline{INT}$ goes high on the rising edge of $\overline{CS}$ or $\overline{RD}$. It will also be forced high when RESET is asserted.
22	CLK	External Clock Input Pin. Accepts a TTL or 5 V CMOS input logic levels.
23	AG_{ADC}	Analog ADC Ground
27–24	V_{IN}A, B, C, D	Four Analog Inputs
28	A0	Address input that controls multiplexer. See Table I for address decode.

OPERATION

The AD8401 is a complete data acquisition and control system. It contains the DAC, a four channel input multiplexer, a track/hold, an ADC, as well as an internal bandgap reference. It interfaces to the microcontroller via an 8-bit digital I/O port.

D/A CONVERTER SECTION

The DAC is an 8-bit voltage mode DAC with an output that swings from AG_{DAC} to the 1.25 volt bandgap voltage. It uses an R-2R ladder fed by PNP current sources which allow the output to swing to ground so that the DAC operates in a unipolar mode.

AMPLIFIER SECTION

The DAC's output is buffered by an internal high speed op amp. The op amps output range is set at 0 V to 2.5 V. The op amp has a 500 ns typical settling time to 0.2% for positive slewing signals. There are differences in settling time for negative slewing signals. Signals going to zero volts will settle slightly slower to ground than is seen in the positive direction.

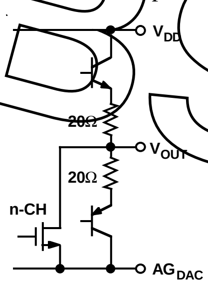


Figure 3. Equivalent Amplifier Output Stage

Current sinking capability is also limited near zero volts in single supply operation. Figure 3 provides an equivalent amplifier output stage schematic.

INTERNAL REFERENCE

An on-chip bandgap is provided as a voltage reference to both the DAC and the ADC. This reference is internal to the AD8401 and is not accessible to the user. It is laser trimmed for both absolute accuracy and temperature coefficients. The reference is internally buffered by a separate control amplifier for both the DAC and ADC to improve isolation between the converters.

DIGITAL I/O

The 8-bit parallel data I/O port on the AD8401 provides access to both the DAC and the ADC. This port is TTL/CMOS compatible with three-state outputs that are ESD protected.

The data format is binary. This data coding applies to both the DAC and the ADC. See the applications information section.

ADC SECTION

A fast successive approximation ADC is used to attain a conversion time of 2 microseconds. Start of conversion is initiated by $\overline{CS}$ and $\overline{RD}$. Following a Start command the $\overline{BUSY}$ signal will become active and another Start command should not be given until the conversion is complete.

The RESET ($\overline{RS}$) input does not affect A/D conversion, but the $\overline{INT}$ (Interrupt or conversion complete) which normally goes active low at the end of a conversion will be forced high by RESET asynchronously.

Figure 4 shows the wave forms for a conversion cycle. The track and hold begins holding the input voltage V_{IN} approximately 50 ns after the falling edge of the Start command. The MSB decision is made approximately 50 ns after the second falling edge of the CLK. If t_X is greater than 50 ns, then the falling edge of the CLK will be seen as the first falling clock edge. If t_X is less than 50 ns, the first MSB conversion will not occur until one clock cycle later. The following bits will each be converted in a similar manner 50 ns after each CLK edge until all eight bits have been converted. After the end of conversion the contents of the ADC SAR register are transferred to the output data latch, the track and hold is returned to the track mode, $\overline{INT}$ goes low and the SAR is reset.

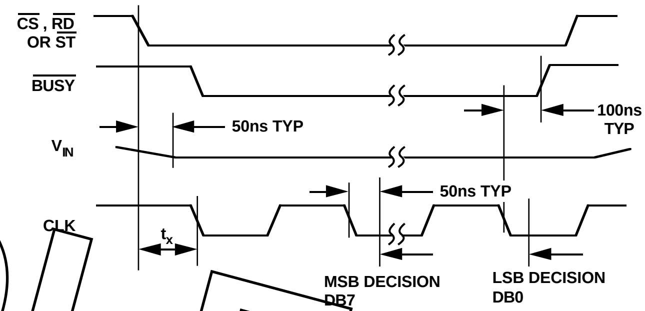


Figure 4. Operating Waveforms Using the External Clock

ANALOG INPUT

The analog inputs of the AD8401 are fed into resistor voltage divider networks with a typical value of 8.5 kΩ. The amplifiers driving these inputs must have an output resistance low enough to drive these nodes without losing accuracy. Taps from the voltage dividers are connected to the track and hold amplifier by the multiplexer switches.

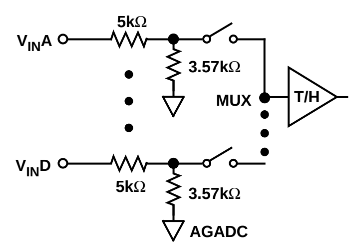


Figure 5. Equivalent Analog Input Circuit

TRACK-AND-HOLD AMPLIFIER

Following the resistive divider at the input of the AD8401 is a track-and-hold amplifier that captures input signals accurately up to the 200 kHz Nyquist frequency of the ADC. To attain this performance the T/H amplifier must have a much greater bandwidth than the signal of interest. Because of this the user must be careful to band limit the input signal to avoid aliasing high frequency components and noise into the passband.

The track-and-hold amplifier is internally controlled by the Start command and is not directly available to the user. After the Start command signal the track-and-hold is placed into the hold mode; it returns to the track mode after the conversion is complete.

CLOCK

The AD8401 uses an external clock that is TTL or 5 V CMOS compatible. The external clock speed is 5 MHz and the duty cycle may vary from 30% to 70%. The external clock can be continuously operated between conversions.

DIGITAL INTERFACE: ADC TIMING AND CONTROL

Two basic ADC operating modes are available with the AD8401. The first mode uses the Start ($\overline{ST}$) pin to trigger a synchronized A/D conversion. As soon as the $\overline{ST}$ pin is asserted, the T/H switches from tracking to the hold mode capturing the present analog input-voltage sample. With the T/H holding the analog sample the successive-approximation analog-to-digital conversion is completed on that sample value. At the end of conversion the T/H returns to the tracking mode. This mode of conversion is ideal for digital signal processing applications where precise interval sampling is necessary to minimize errors due to sampling uncertainty or jitter. A precise clock source can be used to drive the $\overline{ST}$ input.

The second mode of conversion is started by the $\overline{RD}$ and $\overline{CS}$ inputs going low, after which the $\overline{BUSY}$ line puts the microprocessor into a WAIT state until end of conversion. Mode 2 is asserted by connecting the $\overline{ST}$ pin to logic high. The major advantage of this interface is that a single Read Instruction will start and complete a new analog-to-digital conversion without the need for carefully tailored software delays that often are not portable when software routines are taken to a different processor running at a different clock speed.

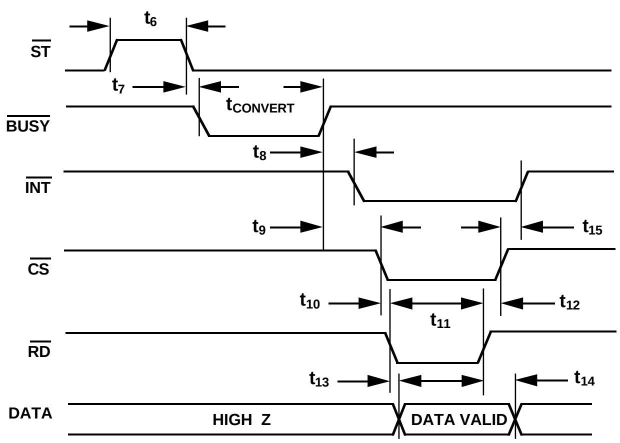


Figure 6. Mode 1, ADC Interface Timing

Mode 1 Interface

As shown in Figure 6, the falling edge of the $\overline{ST}$ pulse initiates a conversion and puts the T/H amplifier into the hold mode. The $\overline{BUSY}$ signal goes low during the whole A/D conversion time and returns high signaling end of conversion. The $\overline{INT}$ line can be used to interrupt the microprocessor. When the microprocessor performs a READ to access the AD8401 data, the rising edges of $\overline{CS}$ or $\overline{RD}$ will reset the $\overline{INT}$ output to high after the t_{15} timing specification. $\overline{INT}$ can also be used to externally trigger a pulse that activates the $\overline{CS}$ and $\overline{RD}$ and places the new data into a buffer or First In First Out FIFO memory. The microprocessor can then load a series of readings from this buffer memory at a convenient time. Care must be taken not to have the $\overline{ST}$ input high when $\overline{RD}$ is brought low; otherwise, the AD8401 will not operate properly. Also triggering the $\overline{ST}$ line a second time before conversion is complete will cause erroneous readings.

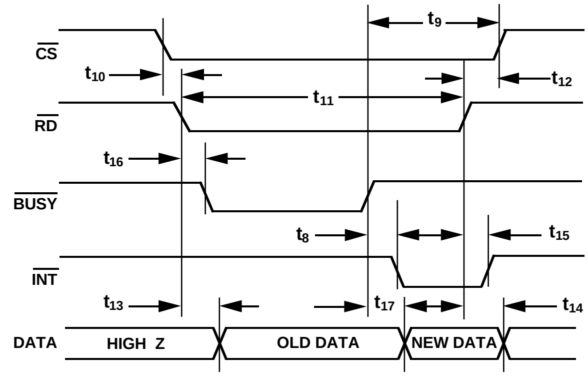


Figure 7. Mode 2, ADC Interface Timing

Mode 2 Interface

This interface mode can be used with microprocessors that can be put into a WAIT state for at least 2 microseconds. The $\overline{ST}$ pin must be tied to logic high for proper operation. The microprocessor begins a conversion by executing a READ instruction that asserts the $\overline{CS}$ and $\overline{RD}$ pins at the AD8401's decoded address. The AD8401 $\overline{BUSY}$ output then goes low, forcing the microprocessor's READY (or WAIT) line into a WAIT state. The analog input signal is captured by the T/H on the falling edge of $\overline{RD}$. When the conversion is complete (8 clocks later), the $\overline{BUSY}$ line returns high, and then the µP completes its READ of the new data now on the digital output port of the AD8401. Note that while conversion is in progress the ADC places the results from the last conversion (Old Data) on the data bus. The Figure 7 timing diagram details the applicable timing specification requirements.

DIGITAL INTERFACE: DAC TIMING AND CONTROL

Table II shows the truth table for DAC operation. The internal 8-bit DAC register contents are loaded from the data bus when both $\overline{WR}$ and $\overline{CS}$ are asserted. The DAC register determines the D/A converter analog-output voltage. The $\overline{WR}$ input is a positive edge triggered input that loads the bus data into the DAC register subject to the data setup and data hold timing requirements. When $\overline{CS}$ and $\overline{WR}$ are low, the DAC register contents will not change with changing data bus values. Figure 8 provides the detail timing diagram for write cycle operation.

Table II. DAC Register Logic

$\overline{CS}$	$\overline{WR}$	$\overline{RS}$	DAC Function
H	H	H	No Effect
L	L	H	No Effect
L	∧	H	DAC Register Updated
∧	L	H	DAC Register Updated
X	X	L	DAC Register Loaded with all Zeros

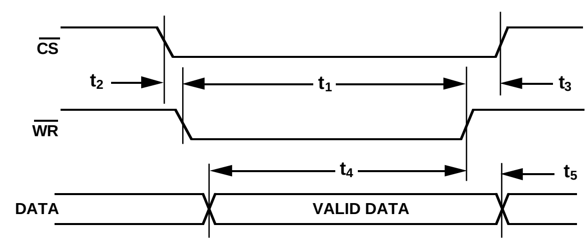


Figure 8. Write Cycle Timing

An active low pulse, at any time, on the RESET pin asynchronously forces all DAC register bits to zero. The DAC output voltage becomes zero volts and stays at that value until a new data word is loaded into the DAC register with a new $\overline{WR}$ command. The equivalent input logic for the DAC register loading is shown in Figure 9.

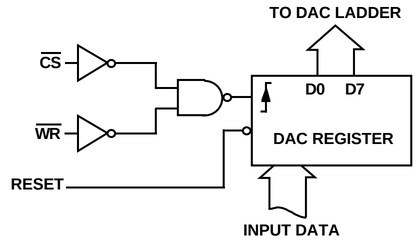


Figure 9. Equivalent DAC Register Control Logic

TYPICAL PERFORMANCE CHARACTERISTICS

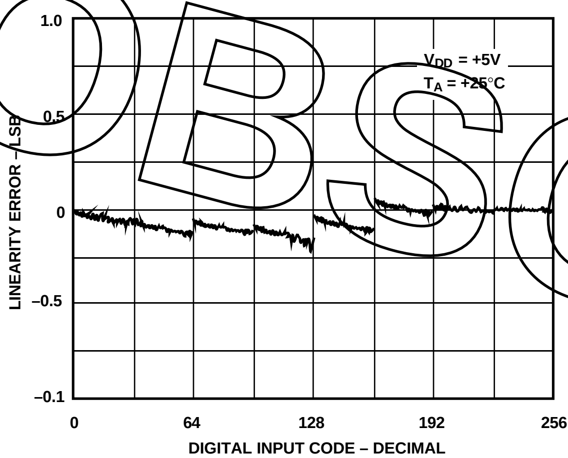


Figure 10. ADC Linearity Error vs. Digital Code

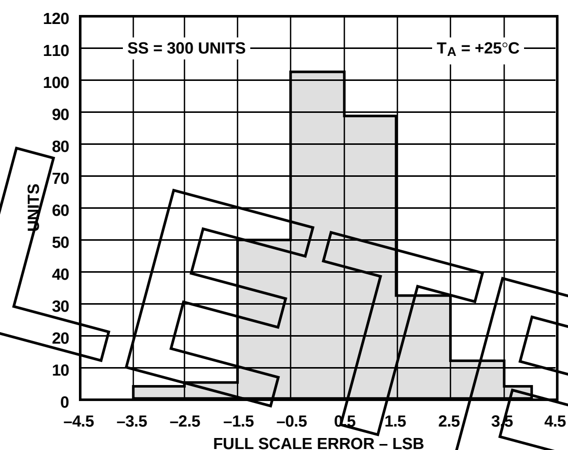


Figure 12. ADC Full-Scale Error Histogram

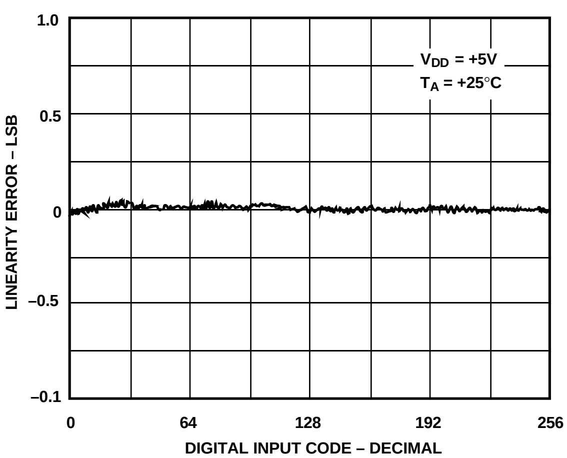


Figure 11. DAC Linearity Error vs. Digital Code

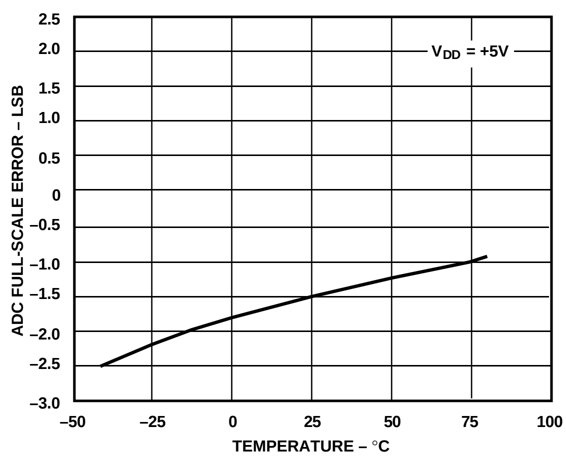


Figure 13. ADC Full-Scale Error vs. Temperature

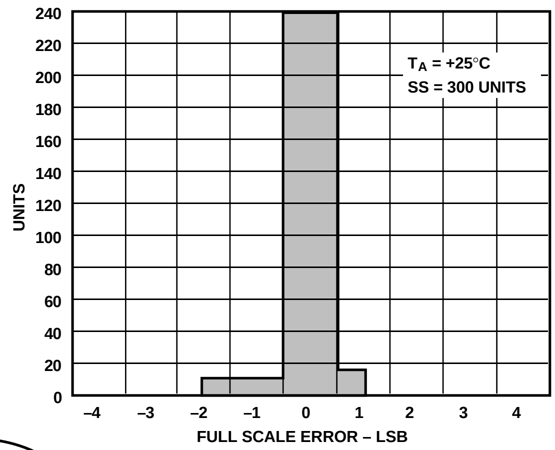


Figure 14. DAC Full-Scale Error Histogram

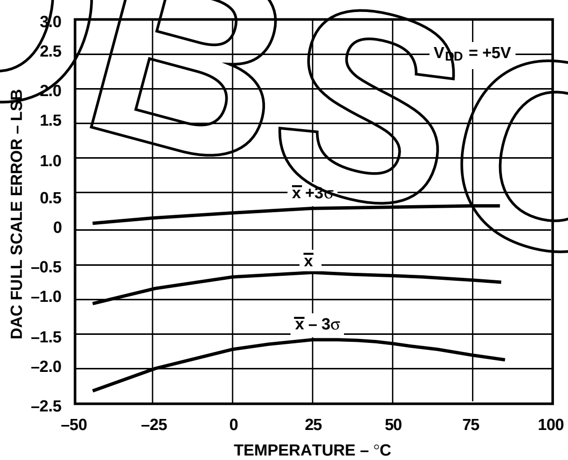


Figure 15. DAC Full-Scale Error vs. Temperature

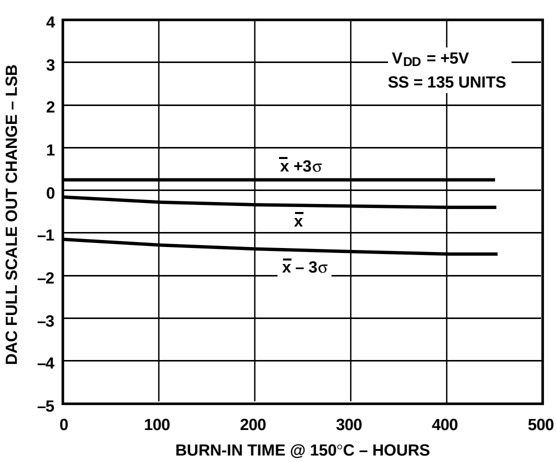


Figure 16. DAC Full-Scale Out Change vs Time Accelerated by Burn-In

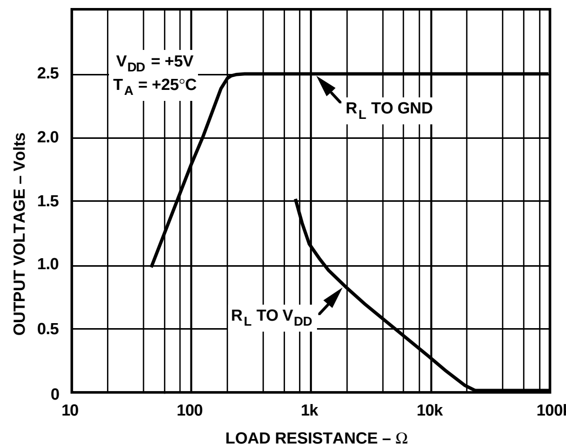


Figure 17. DAC Output Swing vs. Load Resistance

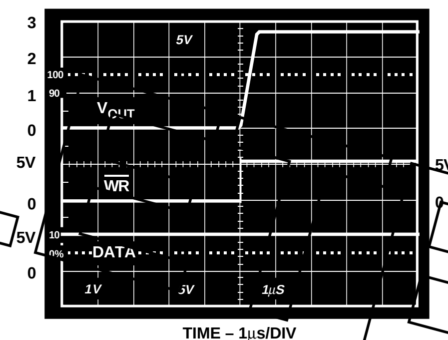


Figure 18. DAC Output Slew Rate Positive Transition

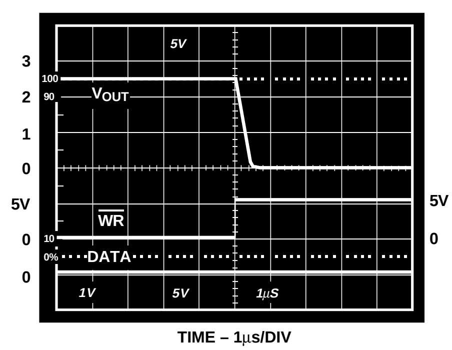


Figure 19. DAC Output Slew Rate Negative Transition

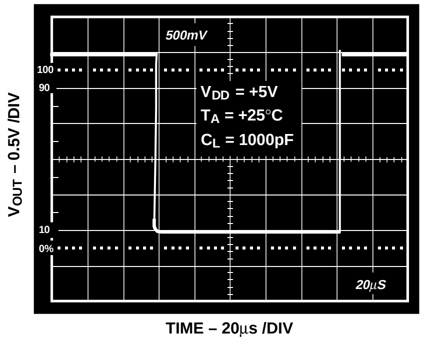


Figure 20. DAC Output Swing with Capacitive Load

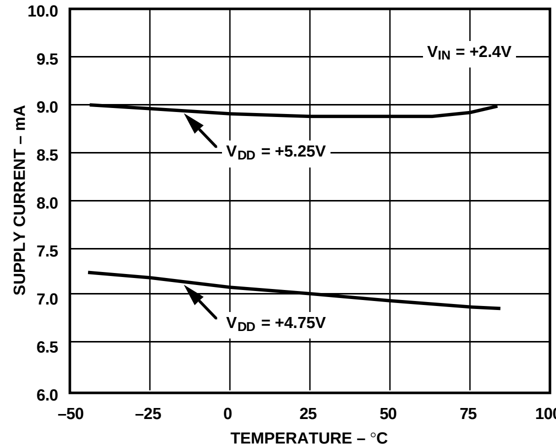


Figure 21. Supply Current vs. Temperature

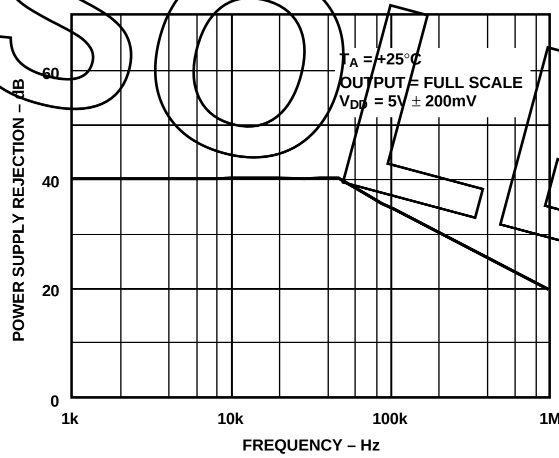


Figure 22. Power Supply Rejection Ratio vs. Frequency

APPLICATIONS INFORMATION

The software programming needs to format data as defined by the transfer equations and Code Tables that follow.

DAC Transfer Equation

$$V_{OUT} = 2.500 \times \frac{D}{256} = 2.500 \times \frac{255}{256} \text{ for a 2.50 V full scale}$$

where D is the decimal value 0 through 255 of the 8-bit data word.

Table III. DAC Unipolar Code

DAC Register Contents		General Transfer	Nominal Analog
Decimal	**Binary**	**Equation**	**Output V_{OUT}**
255	1111 1111	$2.500 \times \frac{255}{256}$	2.490 V
129	1000 0001	$2.500 \times \frac{129}{256}$	1.260 V
128	1000 0000	$2.500 \times \frac{128}{256}$	1.250 V
127	0111 1111	$2.500 \times \frac{127}{256}$	1.240 V
1	0000 0001	$2.500 \times \frac{1}{256}$	0.010 V
0	0000 0000	$2.500 \times \frac{0}{256}$	0.000 V

The nominal output voltages listed in the Code Table are subject to the static performance specifications. The INL, Zero-Scale and Full-Scale errors describe the total specified variation that will be encountered from part to part. One LSB of error for the 2.5 V FS range is 9.766 millivolts (= 2.50/256).

Although separate AGNDs exist for both the DAC and ADC to minimize crosstalk, writing data to the DAC while the ADC is performing a conversion may result in an incorrect conversion from the ADC due to signal interaction between the DAC and ADC. Therefore, to ensure correct operation of the ADC, the DAC register should not be updated while the ADC is converting.

The AD8401 is configured for an input range of +3.0 volts Full Scale. The nominal transfer characteristic for this range is plotted in Figure 23. The output coding is natural binary with one LSB equal to 11.72 millivolts. Note that the first code transition between 0 LSB and 1 LSB occurs at 5.8 mV, one half of the 11.72 mV LSB step size. The last code transition occurs at Full Scale minus 1.5 LSBs, which is a 2.982 V input.

The AD8401 is easily interfaced to most microprocessors by using either address bits or address decode to select the appropriate multiplexer channel. Figure 24 shows how easily the AD8401 interfaces to the AD899. No additional hardware is required.

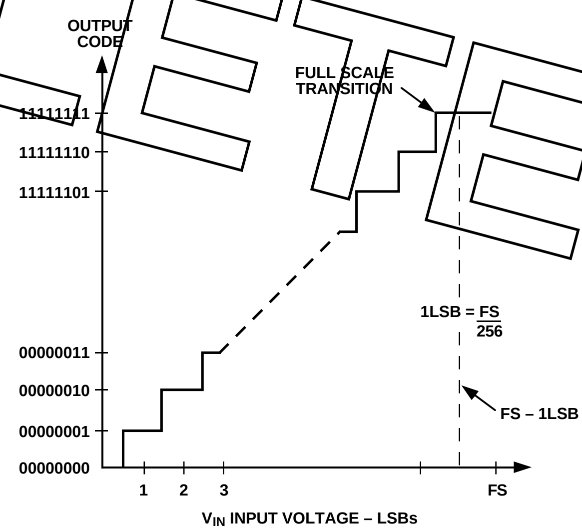


Figure 23. ADC 0 V to +3 V Input Transfer Characteristic

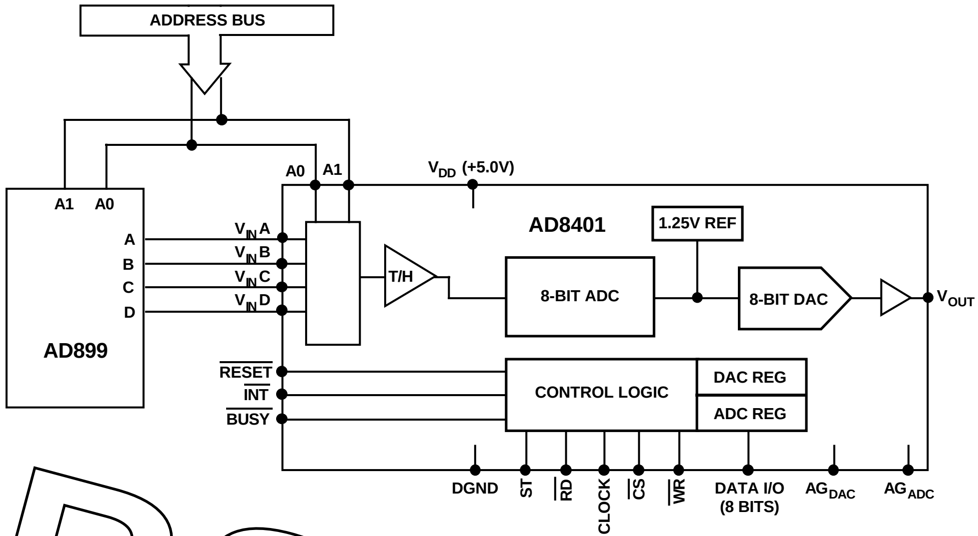
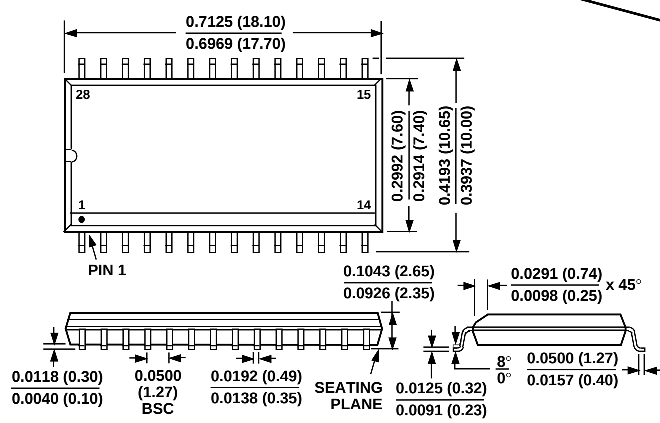


Figure 24. AD8401 Interface to the AD899 Read-Channel Hard Disk Drive Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Wide-Body SO (SOL-28)



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