

IRF720/721/722/723 IRF720R/721R/722R/723R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

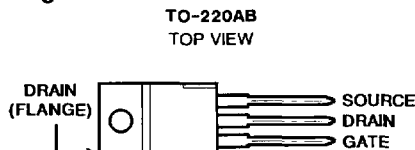
- 2.8A and 3.3A, 350V - 400V
- $r_{DS(on)} = 1.8\Omega$ and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRF720, IRF721, IRF722, and IRF723 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF720R, IRF721R, IRF722R and IRF723R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

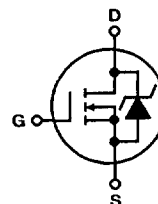
The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRF720 IRF720R	IRF721 IRF721R	IRF722 IRF722R	IRF723 IRF723R	UNITS
Drain-Source Voltage (1)	V_{DS} 400	350	400	350	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 400	350	400	350	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 3.3	3.3	2.8	2.8	A
$T_C = +100^\circ\text{C}$	I_D 2.1	2.1	1.8	1.8	A
Pulsed Drain Current (3)	I_{DM} 13	13	11	11	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$	P_D 50	50	50	50	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM} 12	12	10	10	A
(See Figure 14, $L = 100\mu\text{H}$)					
Single Pulse Avalanche Energy Rating (4)	E_{AS}^* 190	190	190	190	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
 - Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
 - Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
 - $V_{DD} = 50\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 31\text{mH}$, $R_{GS} = 25\Omega$, $I_{PEAK} = 3.3\text{A}$. See Figure 15.
- *R Suffix Types Only

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IRF720, IRF721, IRF722, IRF723 IRF720R, IRF721R, IRF722R, IRF723R

Electrical Characteristics $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF720/722, IRF720R/722R IRF721/723, IRF721R/723R	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	400	-	-	V
			350	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V	-	-	250	μA
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF720/721, IRF720R/721R IRF722/723, IRF722R/723R	I _{D(ON)}	V _{DS} > I _{D(ON)} x R _{DS(ON)} Max, V _{GS} = 10V	3.3	-	-	A
			2.8	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF720/721, IRF720R/721R IRF722/723, IRF722R/723R	r _{DS(ON)}	V _{GS} = 10V, I _D = 1.8A	-	1.5	1.8	Ω
			-	1.8	2.5	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} ≥ 50V, I _D = 1.8A	1.8	2.7	-	S(V)
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	-	360	-	pF
Output Capacitance	C _{OSS}	See Figure 10	-	55	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	20	-	pF
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 200V, I _D ≈ 3.3A, R _G = 18Ω	-	10	15	ns
Rise Time	t _r	See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	14	21	ns
Turn-Off Delay Time	t _{d(OFF)}		-	30	45	ns
Fall Time	t _f		-	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	V _{GS} = 10V, I _D = 3.3A, V _{DS} = 0.8V Max Rating. See Figure 17 for test circuit.	-	12	20	nC
Gate-Source Charge	Q _{gs}	(Gate charge is essentially independent of operating temperature.)	-	2.0	-	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	6.0	-	nC
Internal Drain Inductance	L _D	Measured from the contact screw on tab to center of die	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	R _{θJC}		-	-	2.5	°C/W
Case-to-Sink	R _{θCS}	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	R _{θJA}	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	13	A
Diode Forward Voltage (Note 2)	V _{SD}	T _J = +25°C, I _S = 3.3A, V _{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t _{rr}	T _J = +25°C, I _F = 3.3A, dI _F /dt = 100A/μs	120	-	600	ns
Reverse Recovered Charge	Q _{RR}	T _J = +25°C, I _F = 3.3A, dI _F /dt = 100A/μs	0.64	-	3.0	μC
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

4. V_{DD} = 50V, Start T_J = +25°C, L = 31mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A (See Figure 15)

Performance Curves

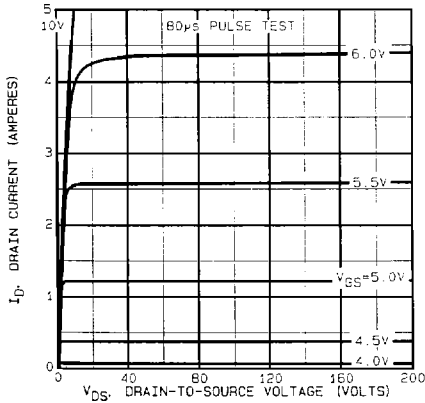


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

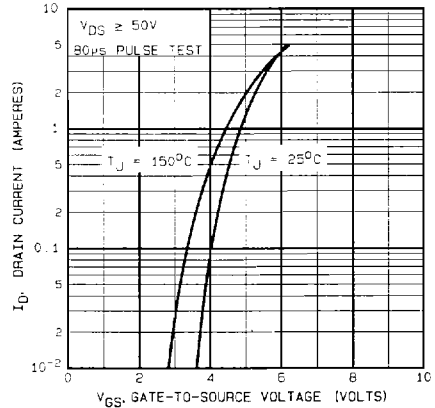


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

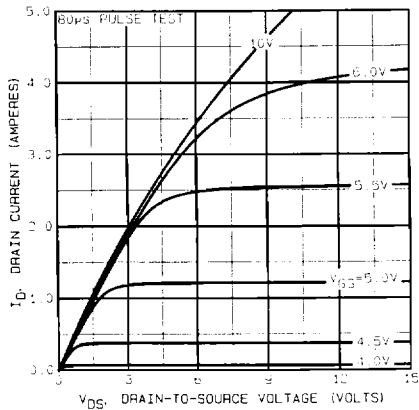


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

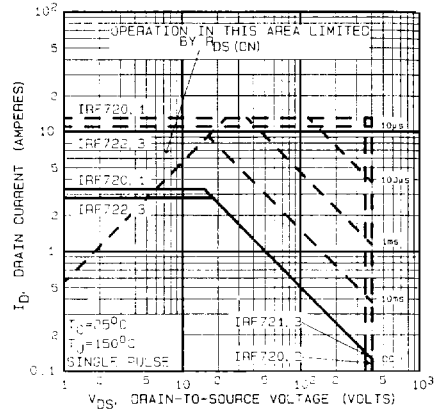


FIGURE 4. MAXIMUM SAFE OPERATING AREA

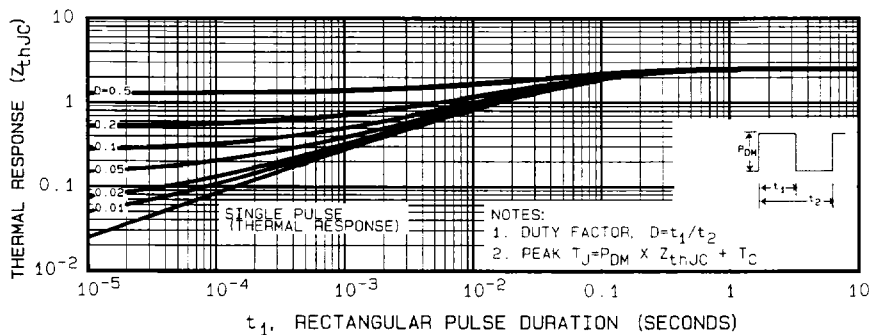


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

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Performance Curves (Continued)

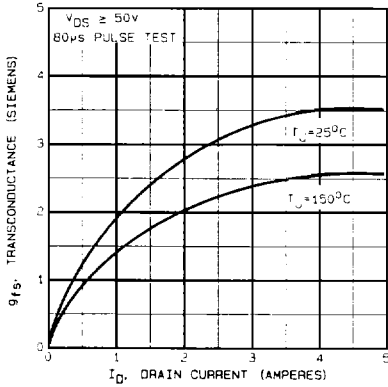


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

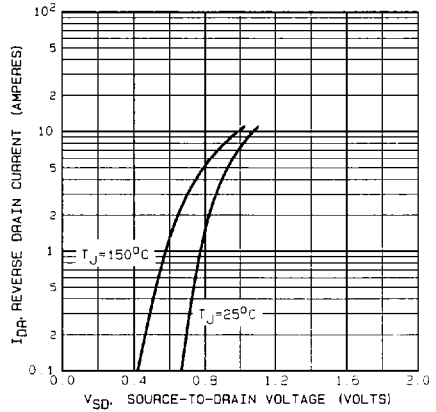


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

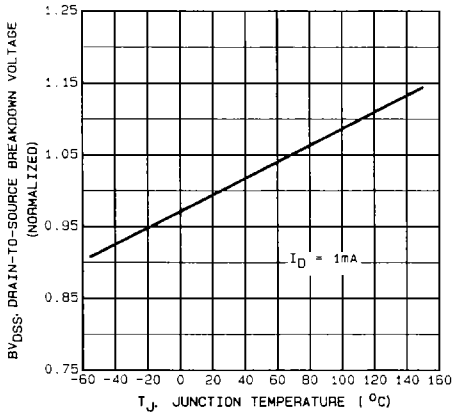


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

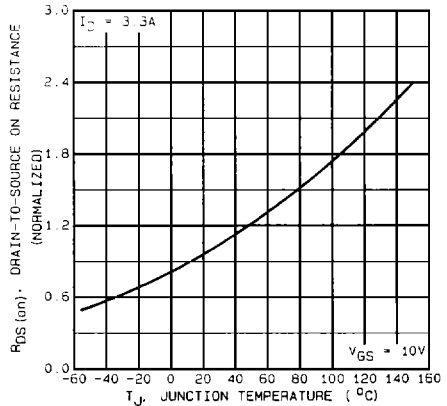


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

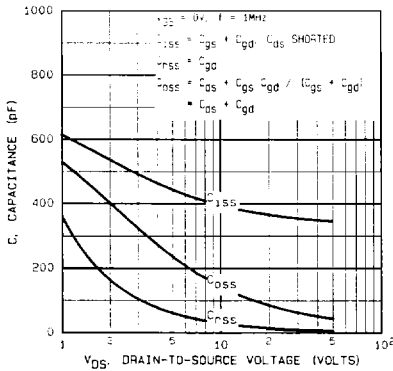


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

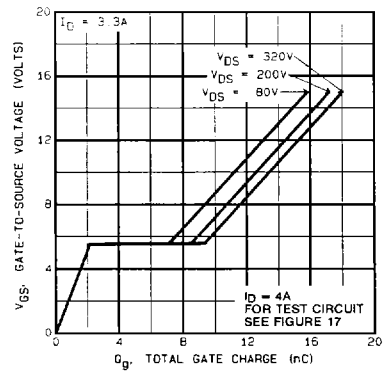


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

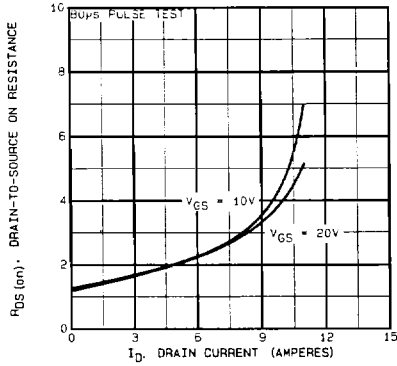


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

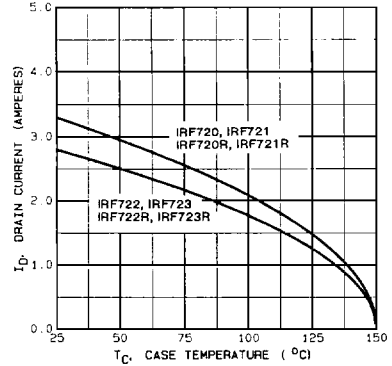


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

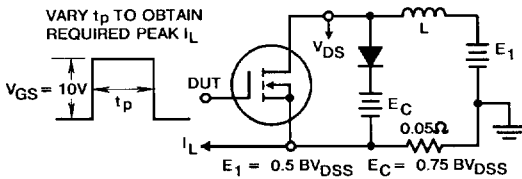


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

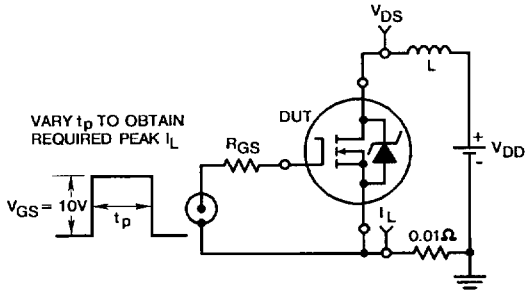


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

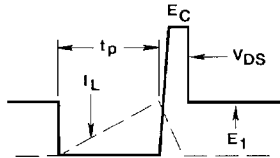


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

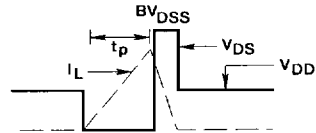


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

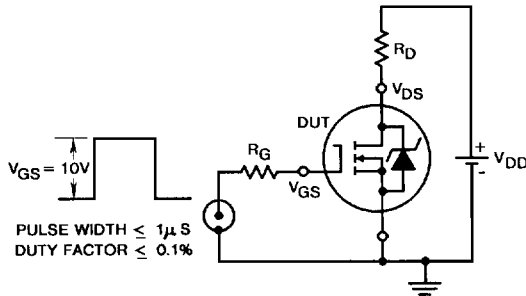


FIGURE 16. SWITCHING TIME TEST CIRCUIT

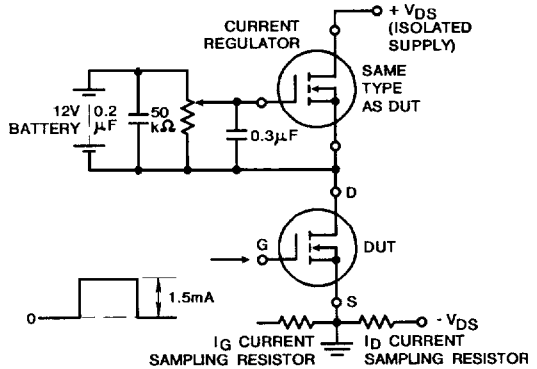


FIGURE 17. GATE CHARGE TEST CIRCUIT

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