A Product Line of
Diodes Incorporated

PI2EQX22024

USB Type-C 10Gbps Bi-directional Retimer with Adaptive Equalizer, Low-latency with 1.8V Single Power Supply

Features

- Compliant for USB 10Gbps and 5Gbps Standards
- Support Dual-port USB Jitter cleaning
- -23dB at 5GHz channel loss compensation
- Low Latency < 1ns.
- Adaptive Continuous Time Linear Equalizer (CTLE)
- No reference clock design.
- Rx termination detection for power saving control
- Selectable adjustment of 3-taps transmitter.
- Single power supply of 1.8 ± 90mV.
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

Application(s)

- Source Devices : Tablets, Smart Phone, Notebook, Desktop, All-In-One PCs
- Sink Devices : Monitors, TVs
- PC Docking, Active Cables, Dongles (Adapters)

Description

The DIODES™ PI2EQX22024 is a bit level ReTimer with receiver adaptive CTLE and transmitter 3-tap equalization which can compensate channel loss up to -23dB for 5GHz signal transmission. It supports USB3.2 standards for USB Type-C® data mode operation. The operation configurations are programmable via I2C interface to select 1 lane USB3.2 Gen1x1/Gen2x1, 1/2 lane USB3.2 Gen1x1/Gen2x1 or USB3.2 Gen2x2.

To achieve good power saving management, this device uses the common 1.8v Vdd power supply. It complies with USB link power management states for active mode (U0) and power saving mode (U1, U2, U3). USB Rx detection monitors the plug condition of the TX terminals continuously. The LFPS signal detector detects the LBPM (LFPS Based PWM Message) of USB mode.

With the merit of the bit level ReTimer design, PI2EQX22024 has very low latency from signal input to output (< 1ns) that serves good interoperability among various USB devices.

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX22024XEAEX	XEA	32-pin, X1-QFN2845-32 (2.85x4.5mm), 0.4mm pitch, 0.45mm height

Notes:
- E = Pb-free and Green
- X suffix = Tape/Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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2. General Information

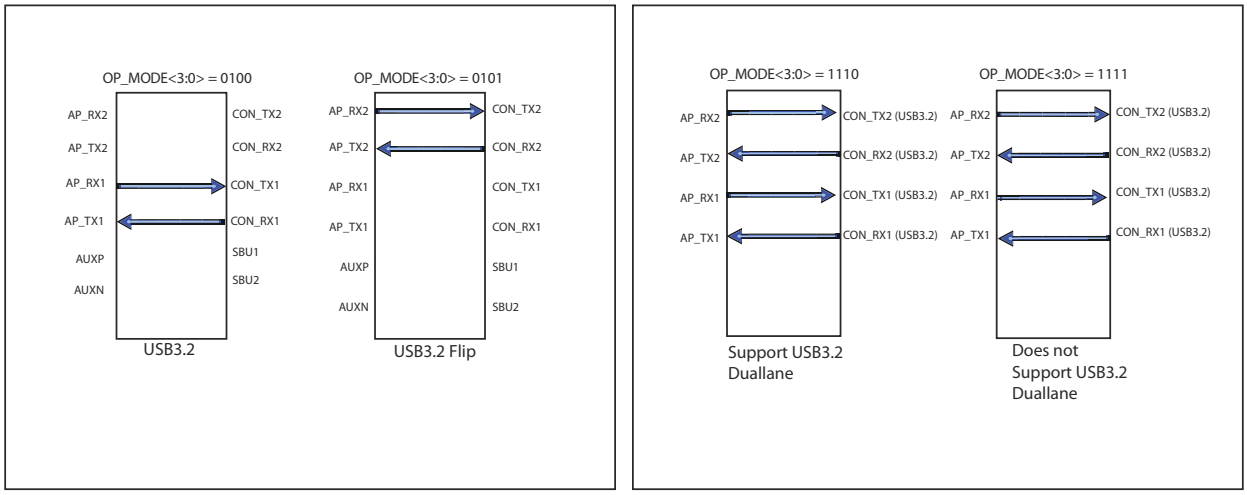

Figure 2-1 The Channel Configuration Against the OP_MODE<3:0>

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3. Pin Configuration

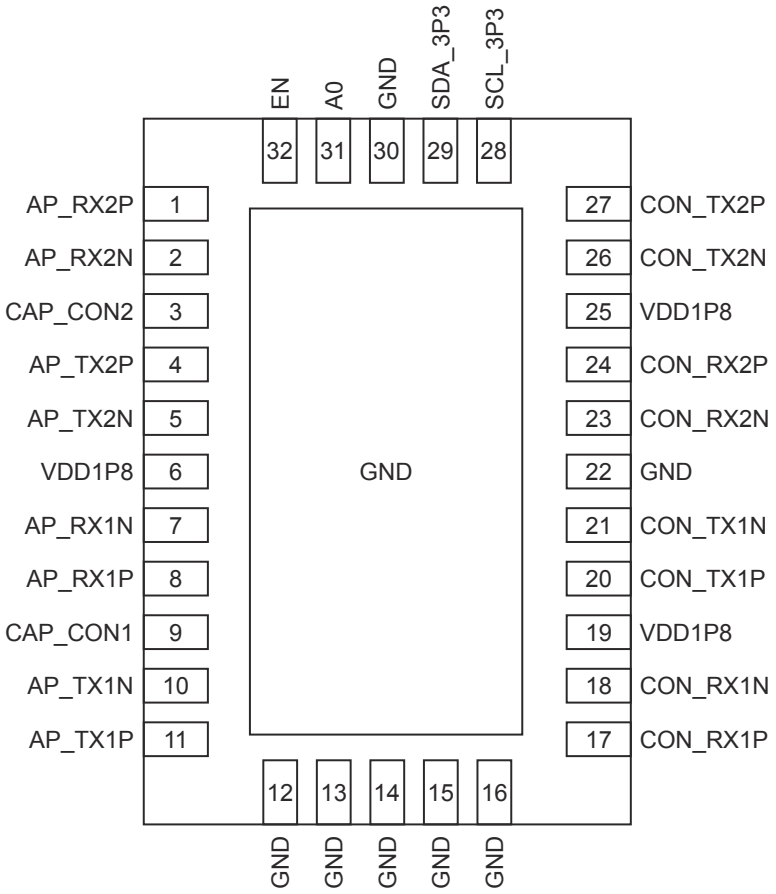


Figure 3-1 PI2EQX22024 Pin Configuration

3.1 Pin Description

Pin #	Pin Name	Type	Description
Power and GND			
6, 19, 25	VDD1P8	Power	1.8V power supply, +/- 5%
12, 13, 14, 15, 16, 22, 30, Center Pad	GND	GND	Supply Ground
3	CAP_CON2	Power	The CON2 VDD1V external decoupling capacitor.
9	CAP_CON1	Power	The CON1 VDD1V external decoupling capacitor.
Control Pins			
32	EN	I	Chip Enable. With internal 340kΩ pull-up resistor. “Low”: Chip Power Down “High”: Normal Operation (Default)
28	SCL_3P3	I	SCL is I2C control bus clock. Open drain structure (3.3V tolerance)
29	SDA_3P3	I/O	SDA is I2C control bus data. Open drain structure. (3.3V tolerance)
31	A0	I	2-level I2C address selection pins. With internal 340kΩ pull-down resistor.
High Speed I/O Pins			
1, 2 24, 23 8, 7 17, 18	AP_RX2P/N, CON_RX2P/N AP_RX1P/N, CON_RX1P/N	I	RX CML input terminals. Input with termination 50Ω to GND or 75kΩ to GND.
27, 26 4, 5 20, 21 11, 10	CON_TX2P/N, AP_TX2P/N CON_TX1P/N, AP_TX1P/N	O	TX CML output terminals. Output termination 50/1.5kΩ to VbiasTX, 3kΩ to GND or 75kΩ to GND.

4. Functional Description

4.1 Detail Features

USB Type-C 10Gbps Mode

- Maximum channel loss compensation up to -23dB at 5GHz
- Bit-level USB Retimer for low latency
- Adaptive receiver Continuous Time Linear Equalizer (CTLE)
- No reference clock design
- I2C slave to configure the channel setting and operation mode
- USB standard mode support: USB 1-lane only, USB 2-lane for type A and USB Gen 2x2 normal/flip modes

USB Channels

- USB3.2 Gen1x1, Gen2x1 and Gen2x2 Retiming mode
- Bit-level USB Retimer

Tx/Rx IO Channels

- Rx termination detection for power saving control
- RX termination: 50Ω to GND or 75kΩ to GND
- TX driver output termination: 50/1.5kΩ to VbiasTx, 3k/75kΩ to GND.
- Selectable adjustment of 3-taps transmitter.

Power

- Single power supply of 1.8±90mV
- 650mW active power consumption for 2-ch USB 10Gbps operating mode
- <500uW target in power down mode

4.2 Functional Block Diagram

Below is shown the simple bi-directional re-timer. The RX termination resistor is terminated to GND and TX termination resistor is terminated to VbiasTX. The TX driver is a 3-taps Feed Forward Equalization (FFE) driver with programmable tuning coefficient to meet multiple standards. The Continuous-Time-Linear Equalizer (CTLE) is adaptive and controlled by the digital state machine after the training.

The signal detector is used to decode the LBPM (LFPS Based PWM Message) and control the power status.

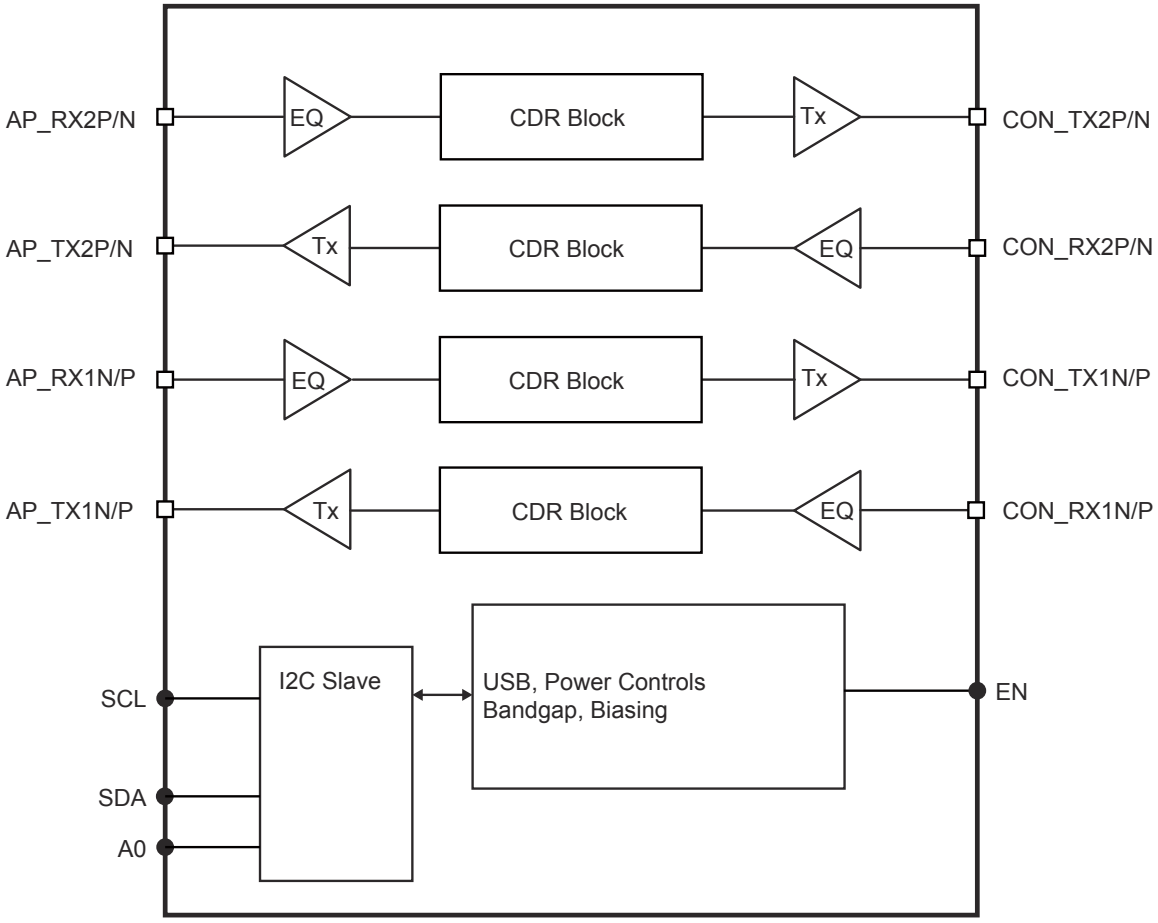


Figure 4-1 PI2EQX22024 Bi-directional Retimer Block Diagram

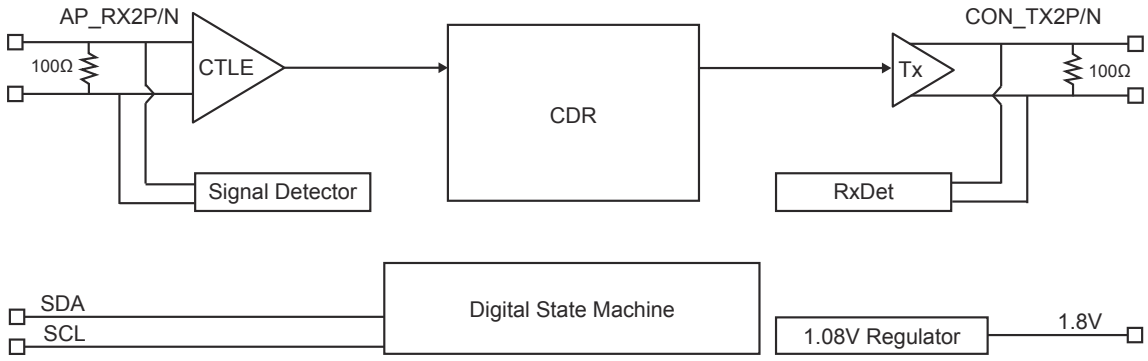


Figure 4-2 PI2EQX22024 Functional Retimer Block Diagram

4.3 USB Mode

To be able to enhanced the re-timer's power efficiency, the supported power state in USB SSP is following: U0 and non-U0s (RXDET/ U1/U2/U3).

The I/O termination resistance under different conditions

Symbol	Parameter	Resistance	Units
RX terminal			
Rin-pd	Input resistance at power down mode	75k to GND	Ω
Rin-U0	Input resistance at U0 condition	50 to GND	Ω
Rin-U1	Input resistance inU1 (1)	50 to GND	Ω
Rin-U2/U3	Input resistance in U2/U3 (1)	50 to GND	Ω
Rin-RXDet	Input resistance in RXDET (1)	75k to GND	Ω
TX terminal			
Rout-pd	Output resistance at power down mode	75k to GND	Ω
Rout-U0	Output resistance at U0 condition	50 to VbiasTx	Ω
Rout-U1	Output resistance in U1 mode (1)	1.5k to VbiasTx	Ω
Rout-U2/U3	Output resistance in U2/U3 mode (1)	3k to GND	Ω
Rout-RXDet	Output resistance in RXDET mode (1)	3k to GND	Ω

Notes: (1) The value of Rin-RxDet will be updated only after the receiver evaluation has been done. Thus, the value can be 50Ω or 75kΩ to GND.

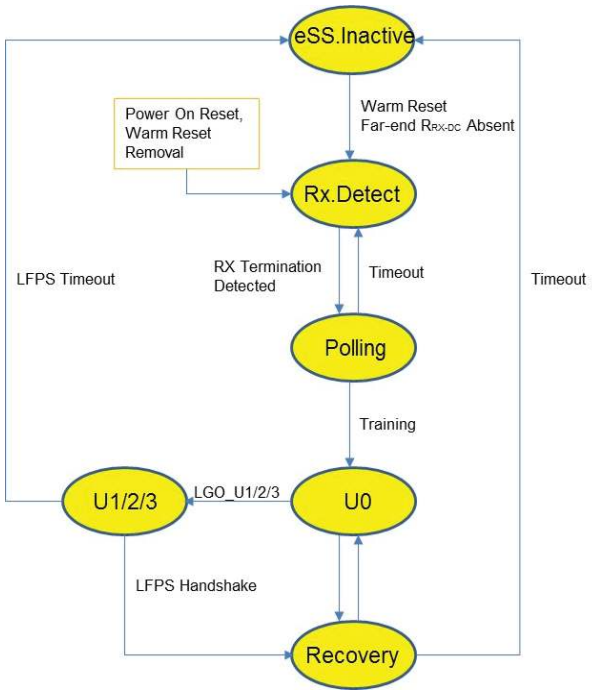


Figure 4-3 Re-timer Supported USB Power State Diagram

4.4 I2C Programming

4.4.1 I2C Address

	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address	1	0	1	0	0	0	A0	0/1 (W/R)

4.4.2 I2C Operation

- I2C interface operates as a slave device.
- The device supports Indexed read/write
- Support operating speed up to 1MHz
- Supported 7-bit addressing
- The data byte format is 8-bit bytes with the most significant bit (MSB) first.
- Will never hold the clock line SCL LOW to force the master into a wait state.
- No response when the data on common bus is matched to the device address.
- If I2C master want read/write invalid register, i.e. the I2C slave just write/read from a dummy RO register with FF by default.

4.4.3 Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

4.4.4 Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first. It will never hold the clock line SCL LOW to force the master into a wait state.

4.4.5 Start & Stop Condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below

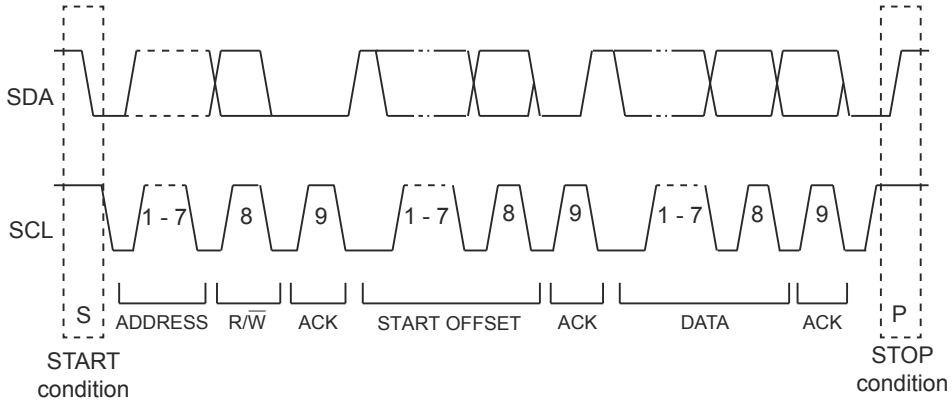


Figure 4-4 I2C Start and STOP Condition

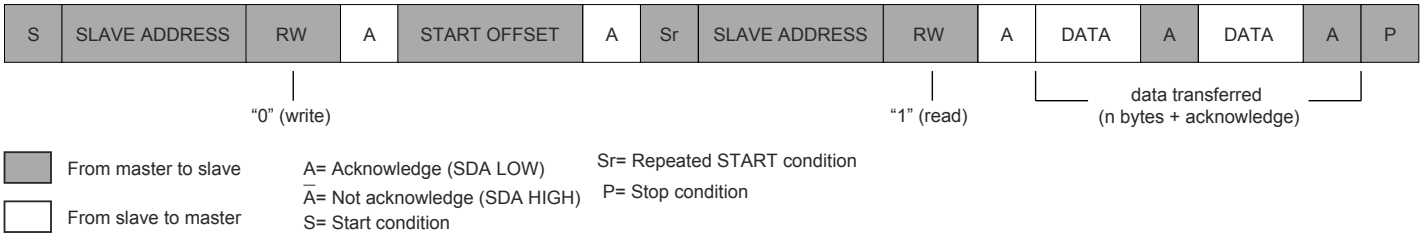


Figure 4-5 Indexed Read Protocol

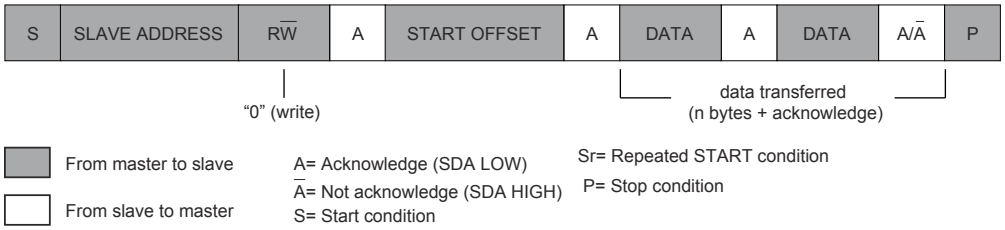


Figure 4-6 Indexed Write Protocol

4.5 Register Assignment

Byte 0 (Vendor ID Register)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Revision ID	Revision ID = 0010
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0	Vendor ID	Pericom ID = 0011
2	RO	0		
1	RO	1		
0	RO	1		
Byte 1 (Device Type/Device ID register)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Device Type	Device Type 0010 = Retimer
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0	Device ID	Device ID =0001
2	RO	0		
1	RO	0		
0	RO	1		
Byte 2 (Byte count Register)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	1	Register Byte count	I2C byte count = 128 bytes
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		

Byte 3 (Channel assignment)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	OP_MODE<3>	Selects the Application Mode
6	R/W	0	OP_MODE<2>	
5	R/W	0	OP_MODE<1>	
4	R/W	0	OP_MODE<0>	
3	R/W	0	Reserved	
2	R/W	0	Reserved	
1	R/W	0	Reserved	
0	R/W	0	Reserved	
Byte 4 (Override the power down control)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	PD_CON_TX2	CONx power down override 0 – Do not force the CONx to power down state 1 – Force the CONx to power down state
6	R/W	0	PD_CON_RX2	
5	R/W	0	PD_CON_TX1	
4	R/W	0	PD_CON_RX1	
3	R/W	1	Reserved	
2	R/W	0	Reserved	
1	R/W	0	Reserved	
0	R/W	0	Reserved	
Byte 5 (Reserved)				
Byte 6 (CON2 USB mode Pre-shot and De-emphasis setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	CON_TX2_USB_GEN2_SW_PE_DE<1>	USB mode CON2: USB Gen2 Pre-shot and De-emphasis setting USB_GEN2_SW_PE_DE<1:0> 00 PE=0dB, DE=0dB 01 PE=2.2dB, DE=0dB 10 PE=0dB, DE = -3.1dB 11 PE=2.2dB, DE=-3.1dB
6	R/W	0	CON_TX2_USB_GEN2_SW_PE_DE<0>	
5	R/W	0	CON_RX2_USB_GEN2_SW_PE_DE<1>	
4	R/W	0	CON_RX2_USB_GEN2_SW_PE_DE<0>	
3	R/W	0	CON_TX2_USB_GEN1_SW_DE<1>	USB mode CON2: USB Gen1 De-emphasis setting USB_GEN1_SW_DE<1:0> 00 DE=0dB 01 DE = -3.5dB 1x DE = -6dB
2	R/W	0	CON_TX2_USB_GEN1_SW_DE<0>	
1	R/W	0	CON_RX2_USB_GEN1_SW_DE<1>	
0	R/W	0	CON_RX2_USB_GEN1_SW_DE<0>	

Byte 7 (CON1 USB mode Pre-shot and De-emphasis setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	CON_TX1_USB_GEN2_SW_PE_DE<1>	USB mode CON1: USB Gen2 Pre-shot and De-emphasis setting USB_GEN2_SW_PE_DE<1:0> 00 PE=0dB, DE=0dB 01 PE=2.2dB, DE=0dB 10 PE=0dB, DE = -3.1dB 11 PE=2.2dB, DE=-3.1dB
6	R/W	0	CON_TX1_USB_GEN2_SW_PE_DE<0>	
5	R/W	0	CON_RX1_USB_GEN2_SW_PE_DE<1>	
4	R/W	0	CON_RX1_USB_GEN2_SW_PE_DE<0>	
3	R/W	0	CON_TX1_USB_GEN1_SW_DE<1>	USB mode CON1: USB Gen1 De-emphasis setting USB_GEN1_SW_DE<1:0> 00 DE=0dB 01 DE = -3.5dB 1x DE = -6dB
2	R/W	0	CON_TX1_USB_GEN1_SW_DE<0>	
1	R/W	0	CON_RX1_USB_GEN1_SW_DE<1>	
0	R/W	0	CON_RX1_USB_GEN1_SW_DE<0>	
Byte 8-15 Reserved RW: 0x00h				
Byte 16-17 Reserved RO: 0x02h				
Byte 18 (Monitor the channel feature setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	1	CON_TX2_AP2CON_SEL	Signal flow of channel 0: Signal is from CON side to AP side 1: Signal is from AP side to CON side
6	RO	1	CON_RX2_AP2CON_SEL	
5	RO	1	CON_TX1_AP2CON_SEL	
4	RO	1	CON_RX1_AP2CON_SEL	
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	USB_DUAL_LANE_FEATURE_EN	Enable/Disable the USB Gen2x2 feature 0 – USB Gen2x2 feature is disabled 1 – USB Gen2x2 feature is enabled
0	RO	0	Reserved	
Byte 19-23 Reserved R/W: 0x00h				
Byte 24 Reserved R/W: 0x20h				
Byte 25-27 Reserved R/W: 0x00h				
Read Only Register Section				
Byte 28-30 Reserved RO: 0x00h				
Byte 31-32 Reserved RO: 0xAAh and 0x08h				

Byte 33 (Common Monitor for CON2 Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	Reserved	
3	RO	0	CON2_USB_DUALLANE_MON	Monitor the CON2 USB LBPM dual lane decoded value 0 – Duallane service is not detected. 1 – Duallane service is detected
2	RO	0	CON2_USB_DATARATE_MON	Monitor the CON2 USB LBPM datarate decoded value 0 – USB Gen1 1 – USB Gen2
1	RO	0	CON2_WARMRESET_MON	Monitor the CON2 USB LBPM warmreset decoded value 0 – WarmReset pattern is not detected 1 – WarmReset pattern is detected
0	RO	0	CON2_DSM_TIMEOUT_MON	Monitor the CON2 USB 328ms electrical IDLE Timeout 0 – The electrical idle is shorter than 328ms typ 1 – The electrical idle is longer than 328ms typ
Byte 34 Reserved RO: 0x08h				
Byte 35 (Common Monitor for CON1 Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	Reserved	
6	R/W	0	Reserved	
5	R/W	0	Reserved	
4	R/W	0	Reserved	
3	R/W	0	CON1_USB_DUALLANE_MON	Monitor the CON2 USB LBPM dual lane decoded value 0 – Duallane service is not detected 1 – Duallane service is detected
2	R/W	0	CON1_USB_DATARATE_MON	Monitor the CON2 USB LBPM datarate decoded value 0 – USB Gen1 1 – USB Gen2
1	R/W	0	CON1_WARMRESET_MON	Monitor the CON2 USB LBPM warmreset decoded value 0 – WarmReset pattern is not detected 1 – WarmReset pattern is detected
0	R/W	0	CON1_DSM_TO_MON	Monitor the CON2 USB 328ms electrical IDLE Timeout 0 – The electrical idle is shorter than 328ms typ. 1 – The electrical idle is longer than 328ms typ.
Byte 36 Reserved RO: 0x00h				

Byte 37 (Monitor for CON_TX2 CDR lock status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX2_CDR_LOCKED	CON_TX2 CDR_LOCKED Monitor
4	RO	0	CON_TX2_PLL_LOCKED	CON_TX2 PLL LOCKED Monitor
3	RO	0	Reserved	Reserved
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 38 (Monitor for CON_TX2 RX Auto CTLE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX2_CTLE_CAL_DONE	CON_TX2 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_TX2_CTLE_CODE<3>	CON_TX2 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_TX2_CTLE_CODE<2>	
1	RO	0	CON_TX2_CTLE_CODE<1>	
0	RO	0	CON_TX2_CTLE_CODE<0>	
Byte 39 Reserved RO: 0x00h				
Byte 40 (Monitor Channel PD Status and CON_TX2 LFPS_Decoder Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	1	CON_TX2_PD#	CON_TX2 PD# status monitor
5	RO	0	Reserved	
4	RO	0	CON_TX2 USB_DUAL_LANE	CON_TX2 LBPM USB Duallane decoded value
3	RO	0	CON_TX2_USB_DATARATE	CON_TX2 LBPM USB Datarate decoded value
2	RO	0	CON_TX2_USB_WARMRESET	CON_TX2 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 41 Reserved RO: 0x00h				

Byte 42 (Monitor for CON_TX2 operating mode Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_TX2_HS_IDLE	CON_TX2 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_TX2_LFPS_IDLE	CON_TX2 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_TX2 DET_5Gbps	CON_TX2 input signal type 0 – LFPS signal 1 – 5Gbps/10Gbps high speed signal
4	RO	0	CON_TX2_HS_OP_MODE<4>	CON_TX2 channel operating mode
3	RO	0	CON_TX2_HS_OP_MODE<3>	
2	RO	0	CON_TX2_HS_OP_MODE<2>	
1	RO	0	CON_TX2_HS_OP_MODE<1>	
0	RO	0	CON_TX2_HS_OP_MODE<0>	
Byte 43 (Monitor for CON_TX2 RX signal status and USB Compliance test mode status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_TX2_RX50	CON_TX2 50Ω load status 0 – No 50Ω load is detected 1 – 50Ω load is detected
6	RO	0	Reserved	
5	RO	0	CON_TX2_COMP_MODE_EN	CON_TX2 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_TX2_COMP_MODE<4>	CON_TX2 compliance test mode state monitor • CON_TX2_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping .LFPS pulse of the adjacent channels.
3	RO	0	CON_TX2_COMP_MODE<3>	
2	RO	0	CON_TX2_COMP_MODE<2>	
1	RO	0	CON_TX2_COMP_MODE<1>	
0	RO	0	CON_TX2_COMP_MODE<0>	

Byte 44 (Monitor for CON_TX2 TX SW & DE & PE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<4>	CON_TX2 SW&DE&PE setting monitor
3	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<3>	
2	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<2>	
1	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<1>	
0	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<0>	
Byte 45 Reserved RO: 0x00h				
Byte 46 (Monitor for CON_RX2 CDR lock status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX2_CDR_LOCKED	CON_RX2 CDR_LOCKED Monitor
4	RO	0	CON_RX2_PLL_LOCKED	CON_RX2 PLL LOCKED Monitor
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 47 (Monitor for CON_RX2 RX Auto CTLE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX2_CTLE_CAL_DONE	CON_RX2 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_RX2_CTLE_CODE<3>	CON_RX2 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_RX2_CTLE_CODE<2>	
1	RO	0	CON_RX2_CTLE_CODE<1>	
0	RO	0	CON_RX2_CTLE_CODE<0>	
Byte 48 Reserved RO: 0x00h				

Byte 49 (Monitor Channel PD Status and CON_RX2 LFPS_Decoder Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	1	CON_RX2_PD#	CON_RX2 PD# status monitor
5	RO	0	Reserved	
4	RO	0	CON_RX2 USB_DUAL_LANE	CON_RX2 LBPM USB Duallane decoded value
3	RO	0	CON_RX2_USB_DATARATE	CON_RX2 LBPM USB Datarate decoded value
2	RO	0	CON_RX2_USB_WARMRESET	CON_RX2 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 50 Reserved RO: 0x00h				
Byte 51 (Monitor for CON_RX2 operating mode Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_RX2_HS_IDLE	CON_RX2 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_RX2_LFPS_IDLE	CON_RX2 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_RX2 DET_5Gbps	CON_RX2 input signal type 0 – LFPS signal 1 – 5Gbps/10Gbps high speed signal
4	RO	0	CON_RX2_HS_OP_MODE<4>	CON_RX2 channel operating mode
3	RO	0	CON_RX2_HS_OP_MODE<3>	
2	RO	0	CON_RX2_HS_OP_MODE<2>	
1	RO	0	CON_RX2_HS_OP_MODE<1>	
0	RO	0	CON_RX2_HS_OP_MODE<0>	

Byte 52 (Monitor for CON_RX2 RX signal status and USB Compliance test mode status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_RX2_RX50	CON_RX2 50Ω load status 0 – No 50Ω load is detected 1 – 50Ω load is detected
6	RO	0	CON_RX2_LOW_VCM_SEL	CON_RX2 channel status 0 – The channel is in DSM/UPM mode 1 – The Channel is in SM/AM mode
5	RO	0	CON_RX2_COMP_MODE_EN	CON_RX2 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_RX2_COMP_MODE<4>	CON_RX2 compliance test mode state monitor • CON_RX2_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping. LFPS pluse of the adjacent channels.
3	RO	0	CON_RX2_COMP_MODE<3>	
2	RO	0	CON_RX2_COMP_MODE<2>	
1	RO	0	CON_RX2_COMP_MODE<1>	
0	RO	0	CON_RX2_COMP_MODE<0>	
Byte 53 (Monitor for CON_RX2 TX SW & DE & PE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_RX2_TX_SW_DE_PE_CTRL<4>	CON_RX2 SW&DE&PE setting monitor
3	RO	0	CON_RX2_TX_SW_DE_PE_CTRL<3>	
2	RO	0	CON_RX2_TX_SW_DE_PE_CTRL<2>	
1	RO	0	CON_RX2_TX_SW_DE_PE_CTRL<1>	
0	RO	0	CON_RX2_TX_SW_DE_PE_CTRL<0>	
Byte 54 Reserved RO: 0x00h				

Byte 55 (Monitor for CON_TX1 CDR lock status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX1_CDR_LOCKED	CON_TX1 CDR_LOCKED Monitor
4	RO	0	CON_TX1_PLL_LOCKED	CON_TX1 PLL LOCKED Monitor
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 56 (Monitor for CON_TX1 RX Auto CTLE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX1_CTLE_CAL_DONE	CON_TX1 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_TX1_CTLE_CODE<3>	CON_TX1 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_TX1_CTLE_CODE<2>	
1	RO	0	CON_TX1_CTLE_CODE<1>	
0	RO	0	CON_TX1_CTLE_CODE<0>	
Byte 57 Reserved RO: 0x00h				
Byte 58 (Monitor Channel PD Status and CON_TX1 LFPS_Decoder Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	1	CON_TX1_PD#	CON_TX1 PD# status monitor
5	RO	0	Reserved	
4	RO	0	CON_TX1 USB_DUAL_LANE	CON_TX1 LBPM USB Duallane decoded value
3	RO	0	CON_TX1_USB_DATARATE	CON_TX1 LBPM USB Datarate decoded value
2	RO	0	CON_TX1_USB_WARMRESET	CON_TX1 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 59 Reserved RO: 0x00h				

Byte 60 (Monitor for CON_TX1 operating mode Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_TX1_HS_IDLE	CON_TX1 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_TX1_LFPS_IDLE	CON_TX1 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_TX1 DET_5Gbps	CON_TX1 input signal type 0 – LFPS signal 1 – 5Gbps/10Gbps high speed signal
4	RO	0	CON_TX1_HS_OP_MODE<4>	CON_TX1 channel operating mode
3	RO	0	CON_TX1_HS_OP_MODE<3>	
2	RO	0	CON_TX1_HS_OP_MODE<2>	
1	RO	0	CON_TX1_HS_OP_MODE<1>	
0	RO	0	CON_TX1_HS_OP_MODE<0>	
Byte 61 (Monitor for CON_TX1 RX signal status and USB Compliance test mode status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_TX1_RX50	CON_TX1 50Ohm load status 0 – No 50Ohm load is detected. 1 – 50Ohm load is detected
6	RO	0	CON_TX1_LOW_VCM_SEL	CON_TX1 channel status 0 – The channel is in DSM/UPM mode 1 – The Channel is in SM/AM mode
5	RO	0	CON_TX1_COMP_MODE_EN	CON_TX1 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_TX1_COMP_MODE<4>	CON_TX1 compliance test mode state monitor • CON_TX1_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping. LFPS pulse of the adjacent channels.
3	RO	0	CON_TX1_COMP_MODE<3>	
2	RO	0	CON_TX1_COMP_MODE<2>	
1	RO	0	CON_TX1_COMP_MODE<1>	
0	RO	0	CON_TX1_COMP_MODE<0>	

Byte 62 (Monitor for CON_TX1 TX SW & DE & PE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_TX1_TX_SW_DE_PE_CTRL<4>	CON_TX1 SW&DE&PE setting monitor
3	RO	0	CON_TX1_TX_SW_DE_PE_CTRL<3>	
2	RO	0	CON_TX1_TX_SW_DE_PE_CTRL<2>	
1	RO	0	CON_TX1_TX_SW_DE_PE_CTRL<1>	
0	RO	0	CON_TX1_TX_SW_DE_PE_CTRL<0>	
Byte 63 Reserved RO: 0x00h				
Byte 64 (Monitor for CON_RX1 CDR lock status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX1_CDR_LOCKED	CON_RX1 CDR_LOCKED Monitor
4	RO	0	CON_RX1_PLL_LOCKED	CON_RX1 PLL LOCKED Monitor
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 65 (Monitor for CON_RX1 RX Auto CTLE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX1_CTLE_CAL_DONE	CON_RX1 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_RX1_CTLE_CODE<3>	CON_RX1 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_RX1_CTLE_CODE<2>	
1	RO	0	CON_RX1_CTLE_CODE<1>	
0	RO	0	CON_RX1_CTLE_CODE<0>	
Byte 66 Reserved RO: 0x00h				

Byte 67 (Monitor Channel PD Status and CON_RX1 LFPS_Decoder Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	Reserved
6	RO	1	CON_RX1_PD#	CON_RX1 PD# status monitor
5	RO	0	Reserved	
4	RO	0	CON_RX1 USB_DUAL_LANE	CON_RX1 LBPM USB Duallane decoded value
3	RO	0	CON_RX1_USB_DATARATE	CON_RX1 LBPM USB Datarate decoded value
2	RO	0	CON_RX1_USB_WARMRESET	CON_RX1 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 68 Reserved RO: 0x00h				
Byte 69 (Monitor for CON_RX1 operating mode Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_RX1_HS_IDLE	CON_RX1 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_RX1_LFPS_IDLE	CON_RX1 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_RX1 DET_5Gbps	CON_RX1 input signal type 0 – LFPS signal 1 – 5Gbps/10Gbps high speed signal
4	RO	0	CON_RX1_HS_OP_MODE<4>	CON_RX1 channel operating mode
3	RO	0	CON_RX1_HS_OP_MODE<3>	
2	RO	0	CON_RX1_HS_OP_MODE<2>	
1	RO	0	CON_RX1_HS_OP_MODE<1>	
0	RO	0	CON_RX1_HS_OP_MODE<0>	

Byte 70 (Monitor for CON_RX1 RX signal status and USB Compliance test mode status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_RX1_RX50	CON_RX1 50Ohm load status 0 – No 50Ohm load is detected 1 – 50Ohm load is detected
6	RO	0	CON_RX1_LOW_VCM_SEL	CON_RX1 channel status 0 – The channel is in DSM/UPM mode 1 – The Channel is in SM/AM mode
5	RO	0	CON_RX1_COMP_MODE_EN	CON_RX1 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_RX1_COMP_MODE<4>	CON_RX1 compliance test mode state monitor • CON_RX1_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping. LFPS pulse of the adjacent channels.
3	RO	0	CON_RX1_COMP_MODE<3>	
2	RO	0	CON_RX1_COMP_MODE<2>	
1	RO	0	CON_RX1_COMP_MODE<1>	
0	RO	0	CON_RX1_COMP_MODE<0>	
Byte 71 (Monitor for CON_RX1 TX SW & DE & PE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<4>	CON_RX1 SW&DE&PE setting monitor
3	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<3>	
2	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<2>	
1	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<1>	
0	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<0>	
Byte 72-Byte 95 Reserved RO registers				
Byte 96-Byte 127 Reserved RW register				

4.5.1 Each Lane Configuration Setting

Below is showing the configuration of each lane after decoded from the I2C OP_MODE<3:0>

Table 4-1. The Channel Configuration Against the OP_MODE<3:0>

OP_MODE<3:0>	CON_TX2	CON_RX2	CON_TX1	CON_RX1	Support Gen2x2	Mode
0000	X	X	X	X	X	Safe Sate
0001	X	X	X	X	X	Safe Sate
0100	X	X	AP_RX1	AP_TX1	X	1 lane USB3.x (AP1 Active)
0101	AP_RX2	AP_TX2	X	X	X	1 lane USB3.x (AP2 Active) flipped
1110	AP_RX2	AP_TX2	AP_RX1	AP_TX1	Yes	2 lane USB3.x (Supports Type-C Gen2x2
1111	AP_RX2	AP_TX2	AP_RX1	AP_TX1	No	2 lane USB3.x (Supports two Type-A USB lane

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage.....-0.3V to 2.0V
I/O Voltage (AP_RX, AP_TX, CON_RX, CON_TX, CAP_CON1, CAP_CON2)..-0.3V to 1.15V
I/O Voltage (SDA, SCL).....-0.3V to 3.8V
I/O Voltage (EN, A0).....-0.3V to 2.0V
Storage Temperature .....–65°C to +150°C
Max junction temperature.....125°C
ESD HBM ..... ±2kV
ESD CDM ..... ±500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect inoperability and degradation of device reliability and performance.

5.2 Recommended Operating Conditions

Over Operating Temperature Range (unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max	Units
V_{DD}	VDD Supply Voltage		1.71	1.8	1.89	V
V_{DD_I2C}	VDD I2C Supply Voltage				3.6	V
V_{NOISE}	Supply Noise up to 50 MHz(1)			100		mVpp
T_A	Ambient Temperature	Commercial range	0		70	°C
		Industrial range	-40		85	
CAP_CON1 CAP_CON2	External VDD1V_CON1/2 decoupling capacitors with max ±20% tolerance				15	nF

Notes:
(1) Allowed supply noise (mVpp sign wave) under typical condition
(2) Industrial temperature -40 to +85 °C can be guaranteed by design. Commercial temperature 0 to +70 °C is supported by the production-tested.

5.3 Power Consumption

Symbol	Parameter	Condition		Min.	Typ.	Max	Units
I_{U0_USB}	Current in USB U0 mode	EN=1, USB Gen2, U0 mode	Gen2x1		180	210	mA
			Gen2x2		360	420	
I_{U1_USB}	Current in USB U1 mode	EN=1, USB U1 mode, VDD=1.8V	1 Lane		16	20	mA
			2 Lane		32	40	
$I_{U2/U3\_USB}$	Current in USB U2/U3 modes	EN=1, USB U2/U3 mode, VDD= 1.8V	1 Lane		800	1800	µA
			2 Lane		900	2000	
I_{RXDET_USB}	Current in USB RXDET mode	EN=1, USB RXDET mode, VDD =1.8V	1 Lane		735	1700	µA
			2 Lane		800	1900	

5.4 AC/DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
LVCMOS I/O DC Specifications						
V_{IH}	DC input logic High		V_{DD}*0.65			V

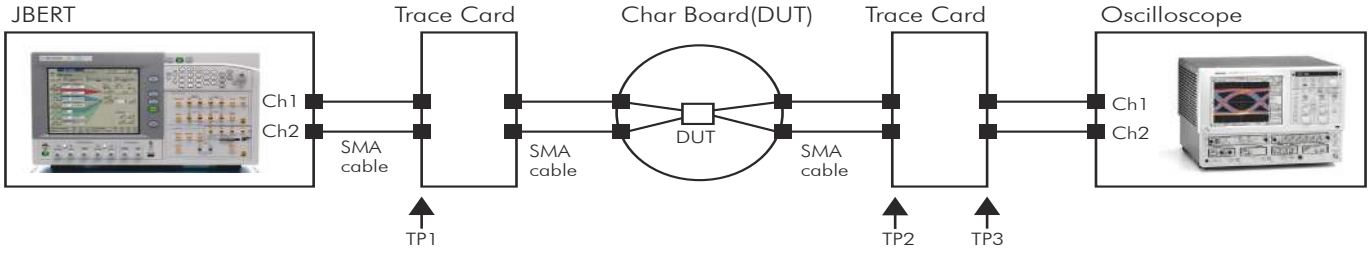
Symbol	Parameter	Condition	Min.	Typ.	Max	Units
V_{IL}	DC input logic Low				V_{DD}*0.35	V
I_{IH}	Input High current				25	uA
I_{IL}	Input Low current		-25			uA

5.5 USB Electrical Specification

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
USB Differential Input						
UI	Unit Interval	Gen 2 10Gbps	99.97 100.17		100.03 100.23	ps
		Gen 1 5Gbps	199.94 200.34		200.06 200.46	ps
CRXPARA-SITIC	The parasitic capacitor for RX				1.0	pF
RRX-DIFF-DC	DC Differential Input Impedance		72		120	Ω
RRX-SINGLE_DC	DC single ended input impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max	18		30	Ω
ZRX-HIZ-DC-PD	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
CAC_COU-PLING	AC coupling capacitance		75		265	nF
VRX-CM-DC_CONN	Instantaneous DC common mode voltage coupled from the far-end Tx	Apply to all link states and during power-on, and power-off. (min1, max) is observed at receiver side of the connector when Rx termination is equivalent of 200KΩ, and (min2, max) when Rx termination is 50Ω.	-0.5 (min1) -0.3 (min2)		1.0	V
VRX-CM-AC-P	Common mode peak voltage	AC up to 5GHz			150	mVpeak
VRX-CM-DC-Active-Idle-Del-ta-P	Common mode peak voltage(1)	Between U0 and U1. AC up to 5GHz			200	mVpeak
USB Differential Output						
UI	Unit Interval	Gen 2 10Gbps	99.97 100.17		100.03 100.23	ps
		Gen 1 5Gbps	199.94 200.34		200.06 200.46	ps
VTX-DIFF-PP	Output differential p-p voltage swing	2*|VTX-D+-VTX-D-|	0.8		1.2	Vppd
RTX-DIFF-DC	DC Differential TX Impedance		72		120	Ω

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
VTX-RCV-DET	The amount of voltage change allowed during RxDet				600	mV
Cac_coupling	AC coupling capacitance		75		265	nF
$T_{TJ\_TP3\_10Gbps}$	Total Jitter with pattern CP9, 10Gbps	Measure over 1E6 consecutive UI and extrapolated to BER=1E-12, Measure at TP3 with Compliance RX EQ function.			0.671	UI
$T_{TJ\_TP3\_5Gbps}$	Total Jitter with pattern CP0, 5Gbps				0.66	UI
$T_{RJ\_TP3\_10Gbps}$	Random jitter with pattern CP10, 5GHz	Measure over 1E6 consecutive UI and extrapolated to BER=1E-12. The RJ is calculated as 14.069 x RMS random jitter for BER=1E-12. Measure at TP3.			0.53	UI
$T_{RJ\_TP3\_5Gbps}$	Random Jitter with pattern CP1, 2.5GHz				0.43	UI
$V_{eyeh\_TP3\_10Gbps}$	Eye height for the CP9, 10Gbps	Measure over 1E6 consecutive UI and extrapolated to BER=1E-12. Measure at TP3 with Compliance RX EQ. Eye height measures the min opening over the range from the center of the eye +/- 0.05UI.	70		1200	mVppd
$V_{eyeh\_TP3\_5Gbps}$	Eye height for the CP9, 5Gbps		100		1200	mVppd
CTXPARA-SITIC	The parasitic capacitor for TX				1.1	pF
RTX-DC-CM	Common mode DC output Impedance		18		30	Ω
VTX-DC-CM	The instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors. min1 is measured with a 200KΩ receiver load, and min2 is measured with a 50Ω receiver load.	-0.5V (min1) -0.3V (min2)		1.0	V
VTx-CM-IDLE-DELTA	Transmitter idle common-mode voltage change	The maximum allowed instantaneous common-mode voltage at TP2 while the transmitter is in U2 or U3 and not actively transmitting LFPS. Note that this is an absolute voltage spec referenced to the receive-side termination ground but serves the purpose of limiting the magnitude and/or slew rate of Tx common mode changes.	-300		600	mV
VTX-C	Common-Mode Voltage	|VTX-D++VTX-D-|/2	0		1.15	V

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
VTX-CM-AC-PP-Active	Active mode TX AC common mode voltage	VTX-D++VTX-D- for both time and amplitude			100	mVpp
VTX-CM-DC-Ac-tive_Idle-Delta	Common mode delta voltage |Avguo(|V-TEX-D+ + VTX-D-|)/2-Avgu1(|VTX-D+ + VTX-D-|)/2|	Between U0 to U1			200	mVpeak
VTX-Idle-Diff-AC-pp	Idle mode AC common mode delta voltage|VTX-D+-VTX-D-|	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals .			10	mVppd
VTX-Idle-Diff-DC	Idle mode DC common mode delta voltage|VTX-D+-VTX-D-|	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.			10	mV
Signal and Frequency Detectors						
VTH_UPM	Unplug mode detector threshold	Threshold of LFPS when the input impedance of the retimer is 75kΩ to GND only. Used in the unplug mode.	200		600	mVppd
VTH_DSM	Deep slumber mode detector threshold	LFPS signal threshold in Deep slumber mode	200		600	mVppd
VTH_AM	Active mode detector threshold	Signal threshold in Active and slumber mode	50		100	mVppd
FTH	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz
TON_UPM	Turn on of unplug mode	TX pin to RX pin latency when input signal is LFPS			3	ms
TON-DSM	Turn on of deep slumber mode				5	us
TON_SM	Turn on of slumber mode				20	ns



1) Trace card between before DUT is designed to emulate FR4 trace loss.
2) All jitter is measured at BER=1E-9/BER=1E-12 for the USB applications respectively.
3) Trace card after the DUT is designed to emulate the Compliance Cable Model.
4) VDD = 1.8V, RT = 50Ω

Figure 5-1 AC Electrical Parameter Test Setup

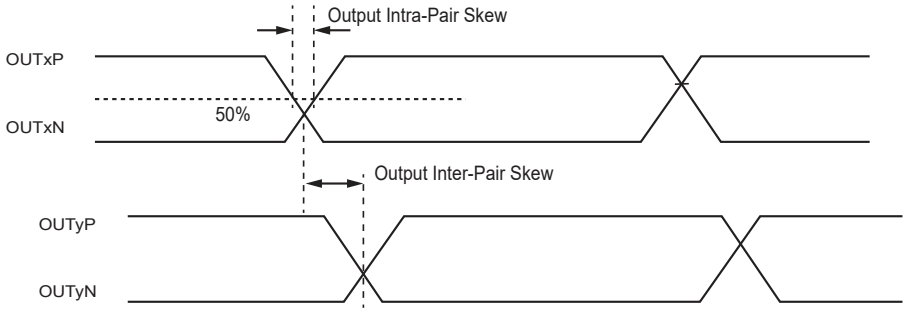


Figure 5-2 Intra and Inter-pair Differential Skew Definition

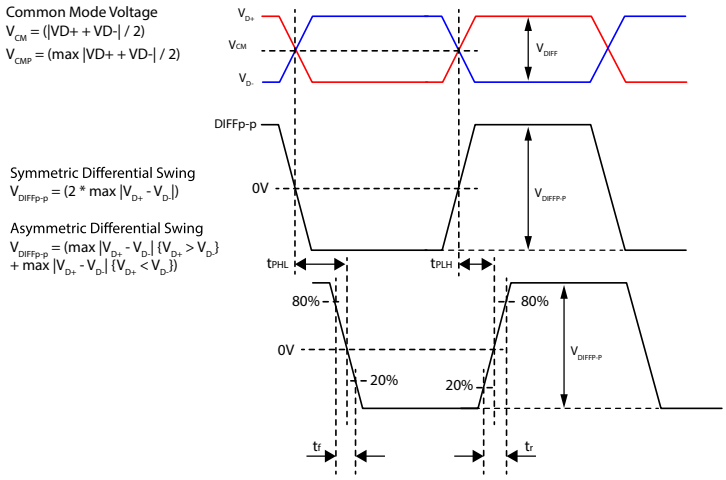


Figure 5-3 Definition of Differential voltage (VDIFF) and Differential Voltage Peak to peak (VDIFFPP)

5.6 I2C Interface Electrical Specification

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IL}	DC input logic LOW		-0.5		0.4	V
V_{IH}	DC input logic HIGH		1.2		V_{DD}	V
V_{OL1}	DC output logic LOW voltage	(open-drain or open-collector) at 3 mA sink current;	0		0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	20			mA
		V_{OL} = 0.6V	6			mA
I_i	Input current each I/O pin		-10		10	uA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	Bus Operation Frequency				1000	KHz
t_{BUF}	Bus Free Time Between Stop and Start condition		1.3			us

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$t_{HD:STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
$t_{SU:STA}$	Repeated start condition setup time		0.26			us
$t_{SU:STO}$	Stop condition setup time		0.26			us
$t_{HD:DAT}$	Data hold time		0			ns
$t_{SU:DAT}$	Data setup time		50			ns
t_{LOW}	Clock Low period		0.5			us
t_{HIGH}	Clock High period		0.26		50	us
t_F	Clock/Data fall time				120	ns
t_R	Clock/Data rise time				120	ns

Notes:
(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) VIL = 0.4V and VIH = 1.2V because the silicon needs to support both SCL/SDA with 1.8V/3.3V signaling level.

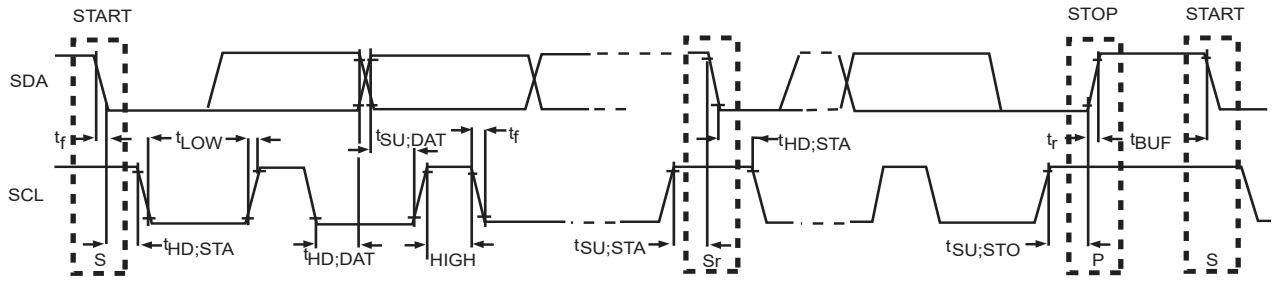


Figure 5-4 Definition of Timing on the I2C-Bus

6. Application

Note: Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 PI2EQX22024 Reference Schematics

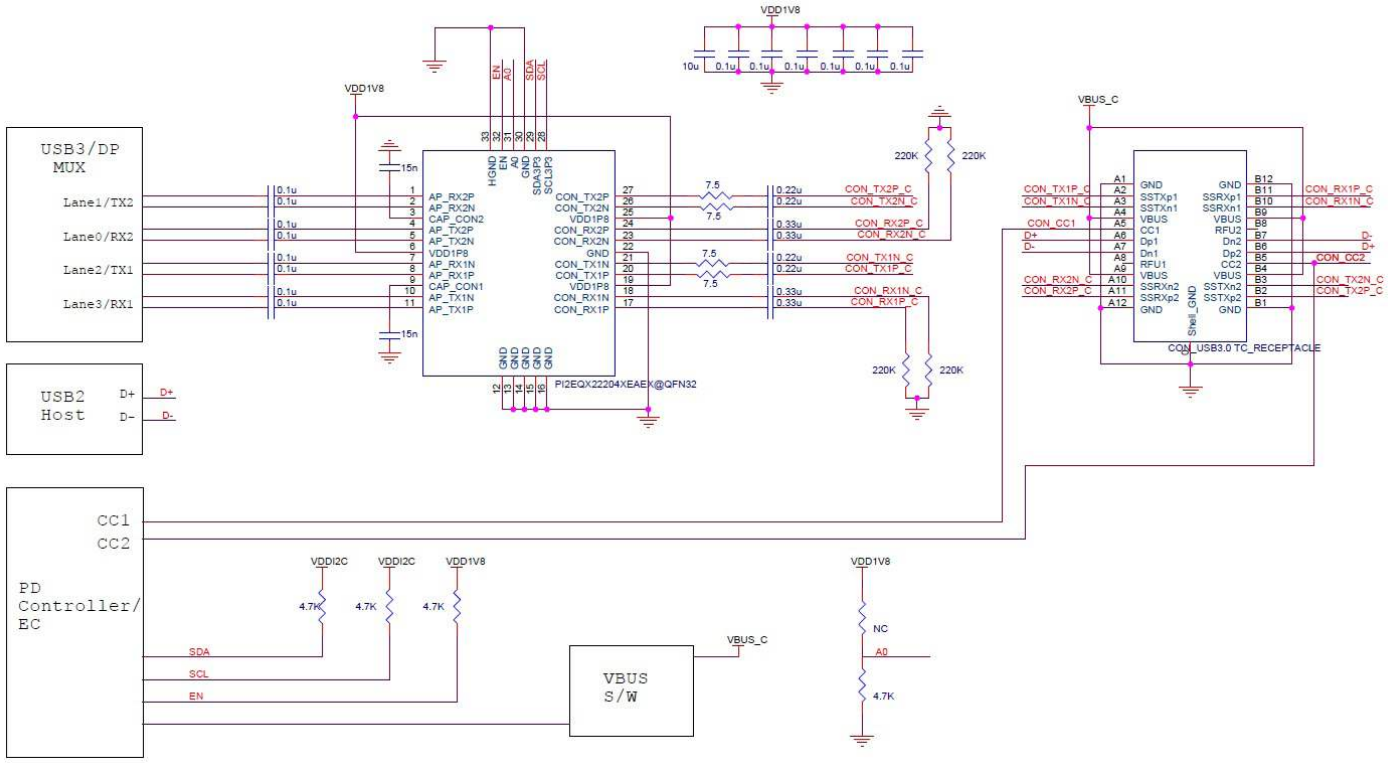


Figure 6-1 PI2EQX22024 Reference Schematic

6.2 PCB Layout Guideline

6.2.1 General Power and Ground Guideline

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

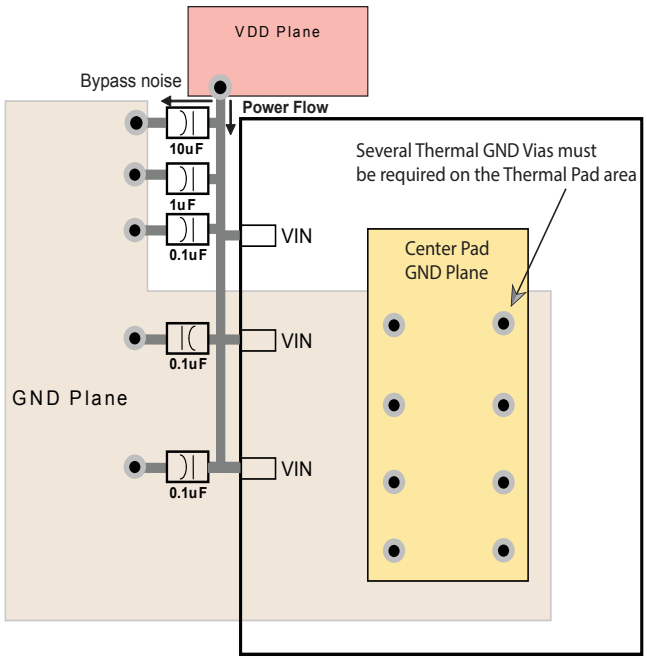


Figure 6-2 Decoupling Capacitor Placement Diagram

6.2.2 High-speed Signal Routing Guideline

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

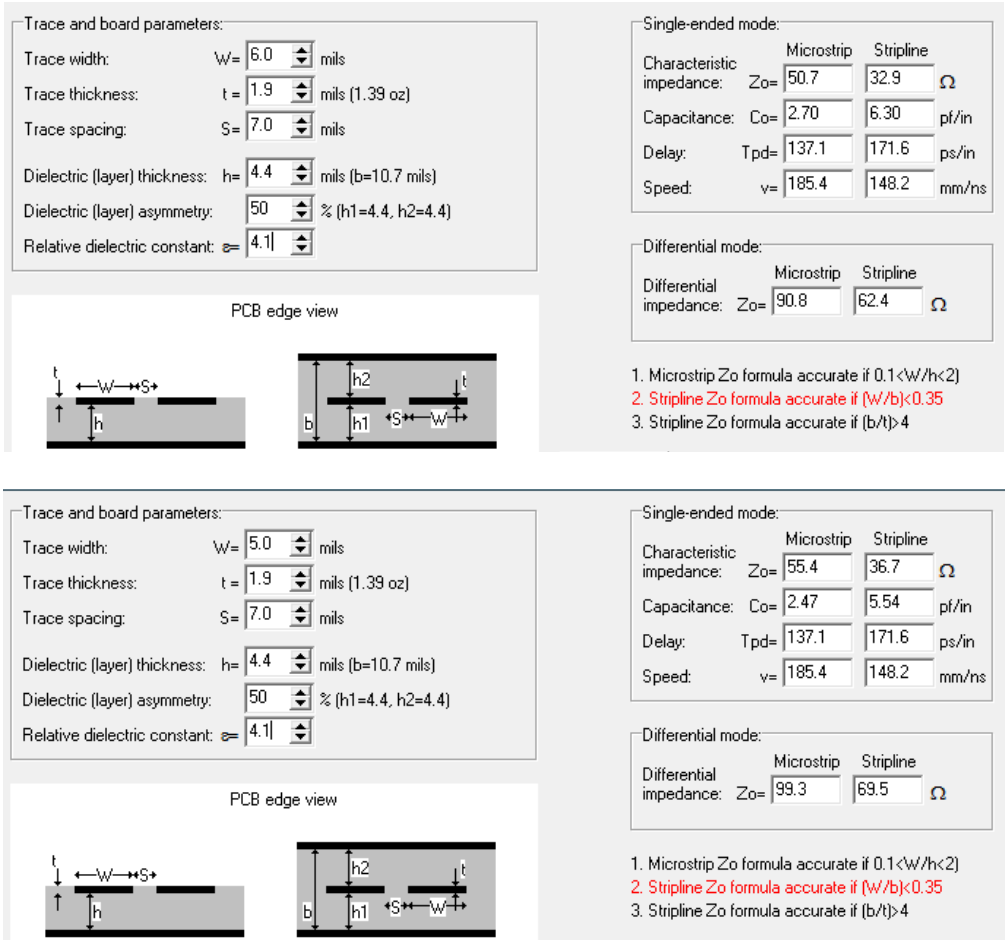


Figure 6-3 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

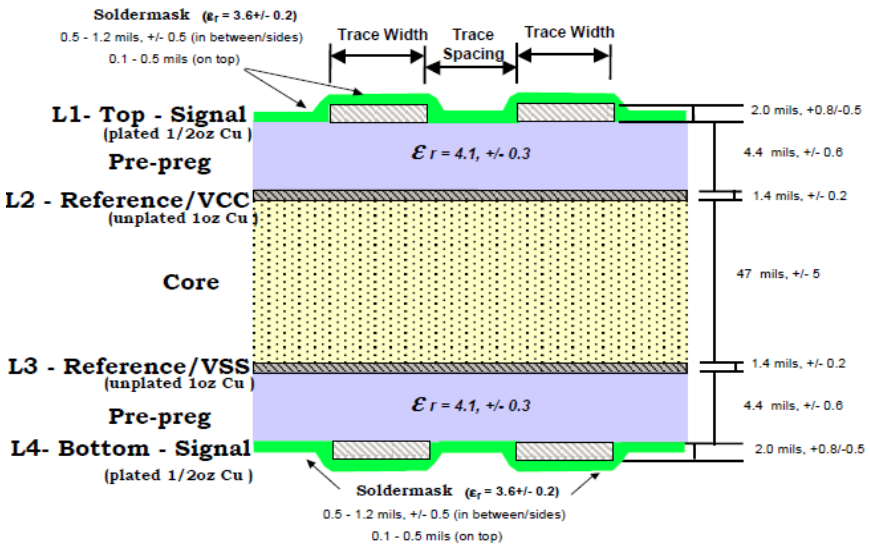


Figure 6-4 4-Layer PCB Stack-up Example

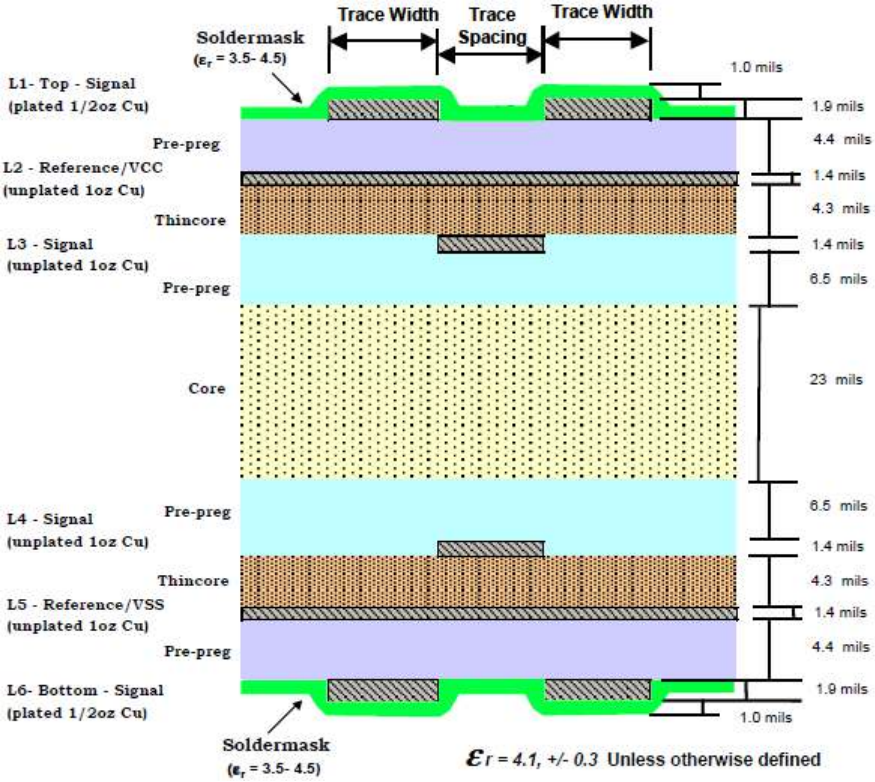


Figure 6-5 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

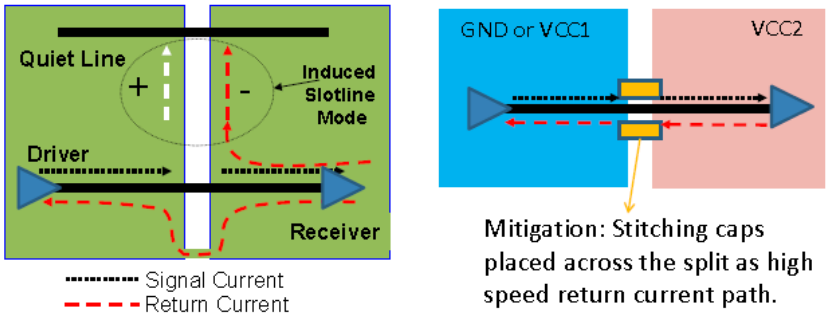


Figure 6-6 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

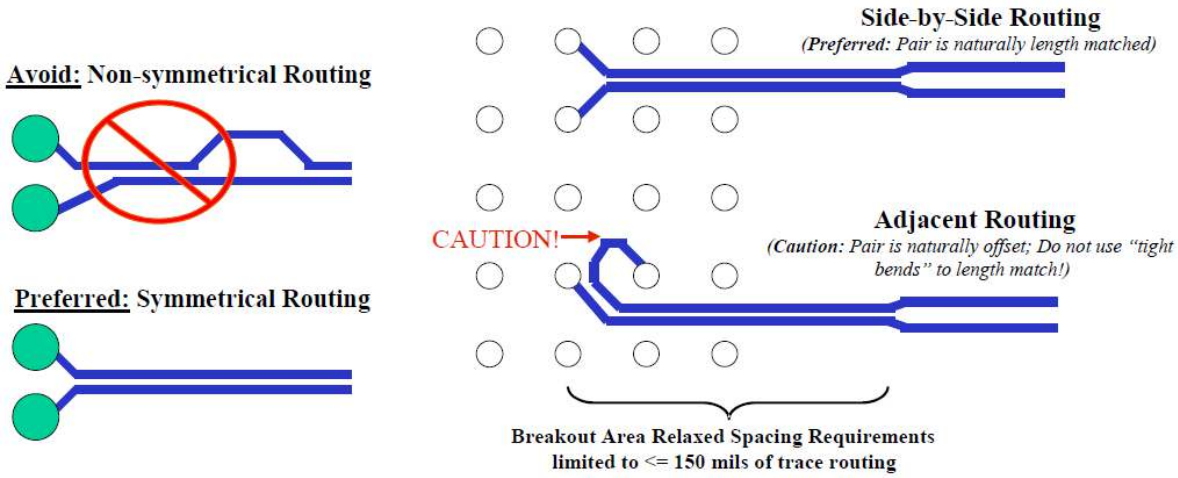


Figure 6-7 Layout Guidance of Matched Differential Pair

- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the spacing between the Trace and Reference plane.

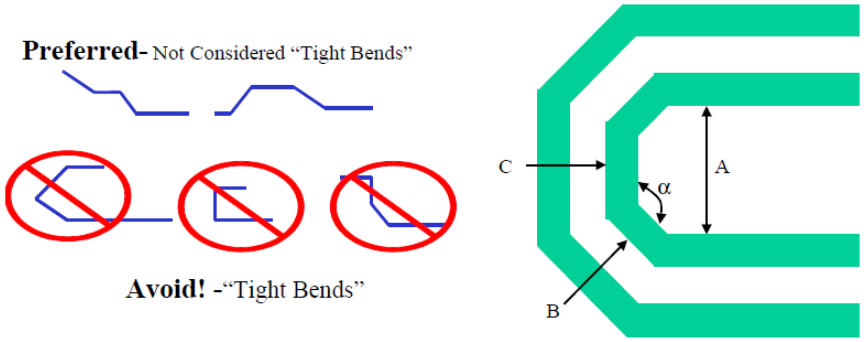


Figure 6-8 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

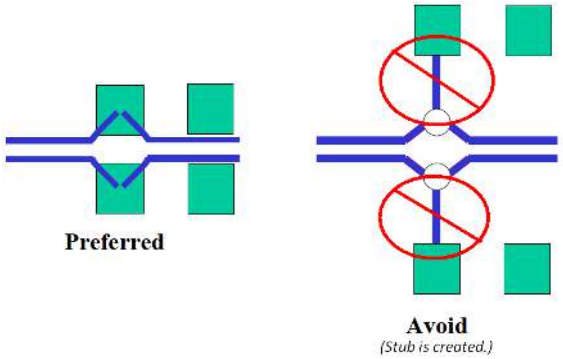


Figure 6-9 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

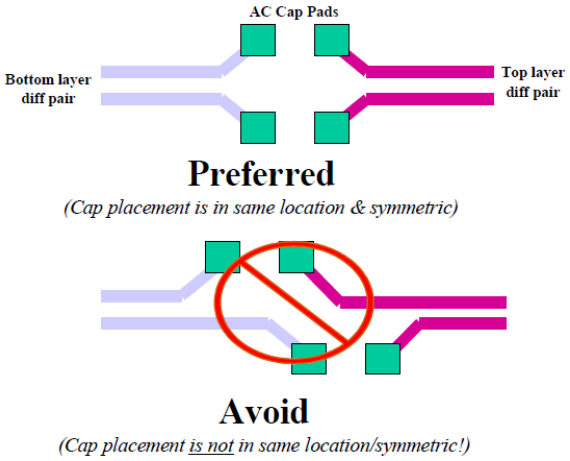


Figure 6-10 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

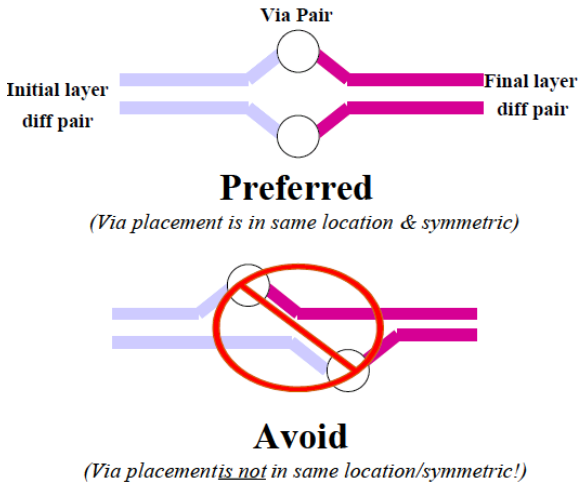


Figure 6-11 Layout Guidance of Stitching Via

6.2.3 PCB Crosstalk Minimization recommendation

- Breakout Tx and Rx I/O on different PCB layers.
- Non-interleaved routing. Eliminates a key source of near end crosstalk.
- Inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the spacing between the Trace and Reference plane.
- Places requirements on Tx & Rx I/O placement as shown below.

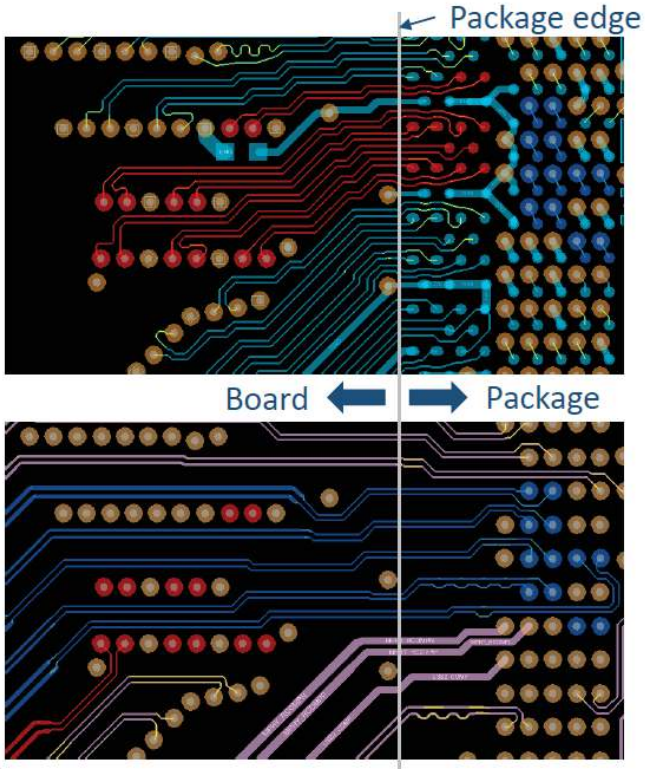
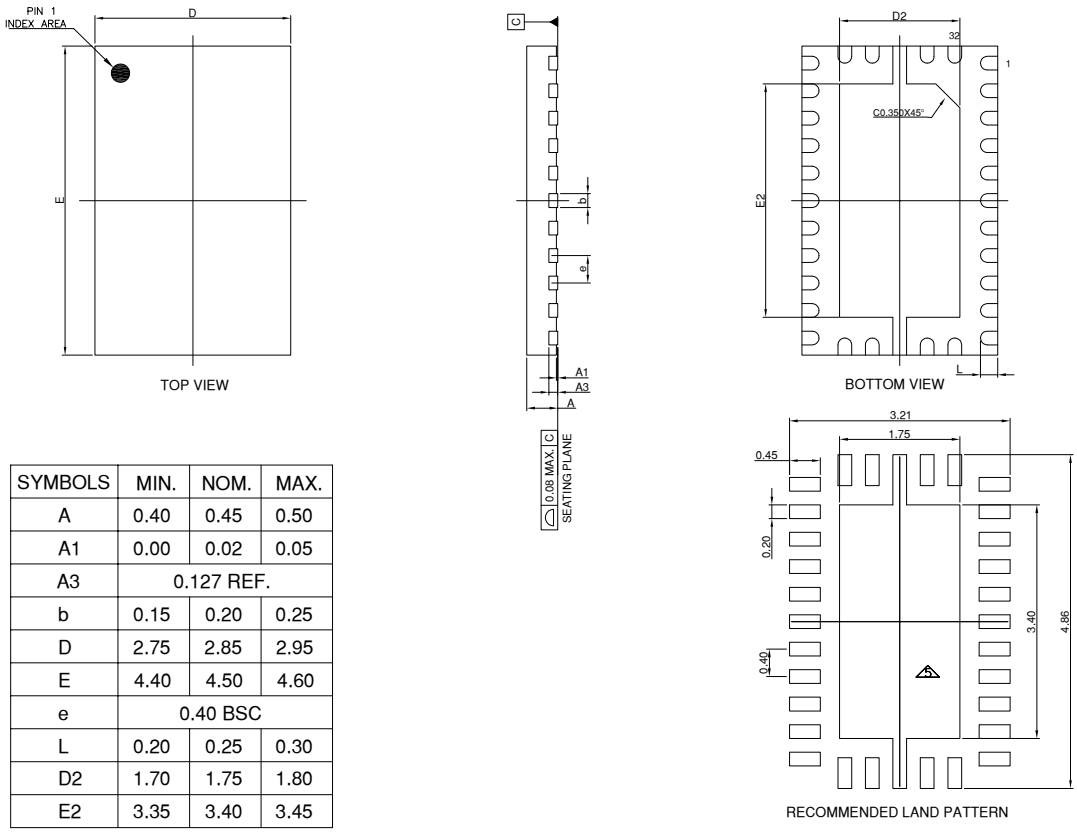


Figure 6-12 Breakout Tx and Rx I/O on Different PCB Layers

7. Mechanical/Packaging Information

7.1 Mechanical Outline



SYMBOLS	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127 REF.	
b	0.15	0.20	0.25
D	2.75	2.85	2.95
E	4.40	4.50	4.60
e		0.40 BSC	
L	0.20	0.25	0.30
D2	1.70	1.75	1.80
E2	3.35	3.40	3.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DATE: 01/14/22

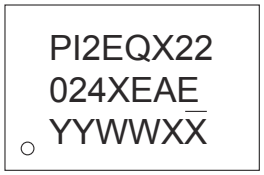
DESCRIPTION: 32-contact, X1-QFN2845-32

PACKAGE CODE: XEA (XEA32)

DOCUMENT CONTROL #: PD-2259 **REVISION:** B

22-1546

Figure 7-1 Package Mechanical Dimension



YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Bar above 2nd “X” means Cu wire

Figure 7-2 Part Marking Information

7.2 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 7-3 and 7-4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 7-2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 7-4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

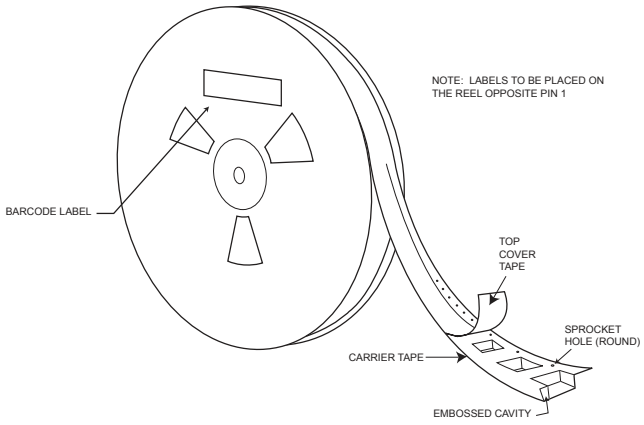


Figure 7-3 Tape & Reel Label Information

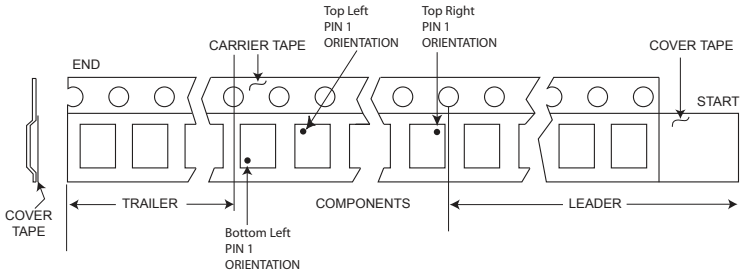


Figure 7-4 Tape Leader and Trailer Pin 1 Orientations

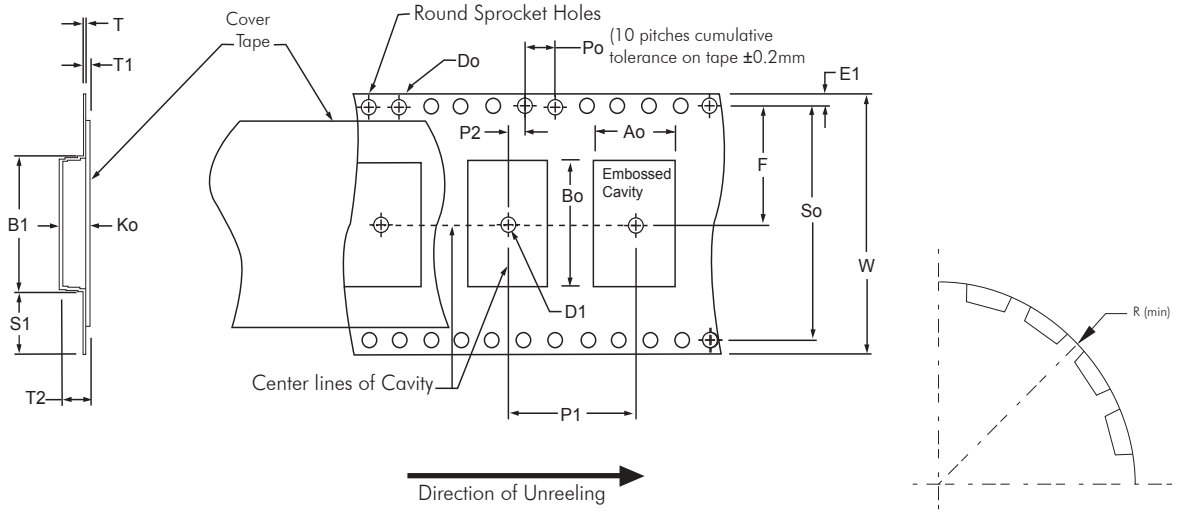


Figure 7-5 Standard Embossed Carrier Tape Dimensions

Table 7-1. Constant Dimensions

Tape Size	D_0	D_1 (Min)	E_1	P_0	P_2	R (See Note 2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

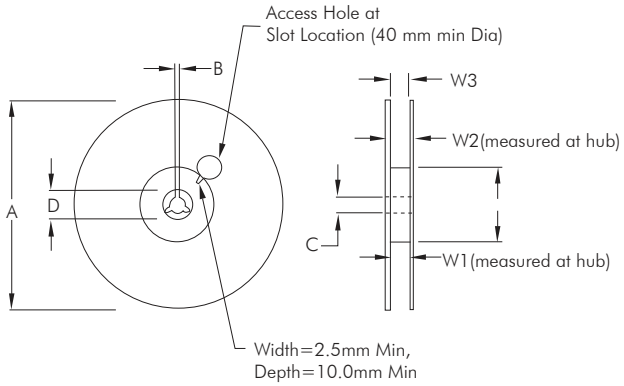


Figure 7-6 Reel Dimensions

Table 7-3. Reel dimensions by Tape Size

Tape Size	A	N (Min) See Note A	W_1	W_2(Max)	W_3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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