TOSHIBA Photocoupler IRED + Photo IC

TLP701F

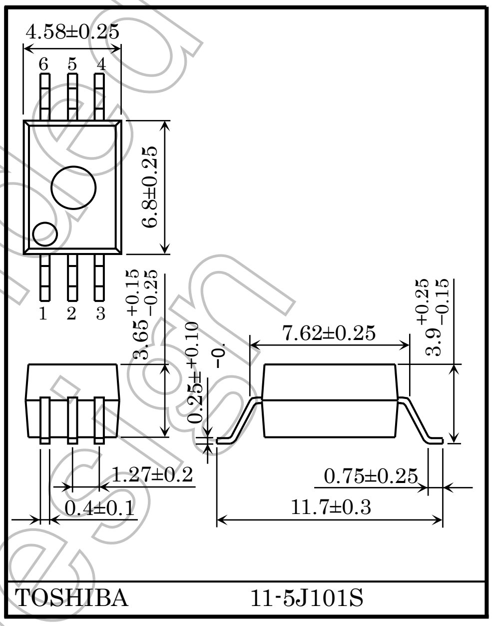
Industrial inverters
Inverter for air conditioners
IGBT/Power MOS FET gate drive

TLP701F consists of an infrared LED and an integrated photodetector.

This unit is 6-lead SDIP package. The TLP701F is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The TLP701F is suitable for gate driving circuits for IGBTs or power MOSFETs. In particular, the TLP701 is capable of “direct” gate driving of low-power IGBTs.

Unit in



Weight : 0.26 g (typ.)

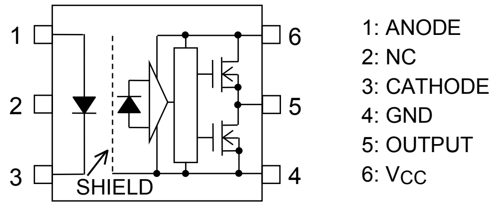
- Peak output current : ±0.6 A (max)
- Guaranteed performance over temperature : −40 to 100°C
- Supply current : 2 mA (max)
- Power supply voltage : 10 to 30 V
- Threshold input current : I_{FLH} = 5 mA (max)
- Switching time (t_{pLH} / t_{pHL}) : 700 ns (max)
- Common mode transient immunity : ±10 kV/μs (min)
- Isolation voltage : 5000 Vrms (min)
- Construction mechanical rating

	10.16-mm pitch TLPXXXF type
Creepage Distance Clearance Insulation Thickness	8.0 mm (min) 8.0 mm (min) 0.4 mm (min)

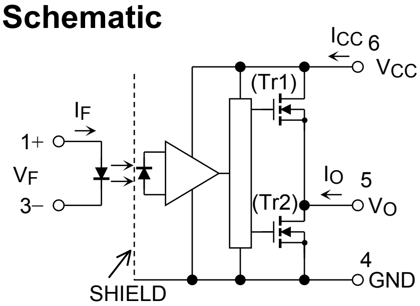
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved: EN 60747-5-5 , EN 62368-1 (Note 1)

Note 1 : When a VDE approved type is needed, please designate the **Option(D4)**.

Pin Configuration (Top View)



Schematic



A 0.1-μF bypass capacitor must be connected between pins 6 and 4.

Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Start of commercial production
2004-04

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics			Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 85°C)		$\Delta I_F/\Delta Ta$	−0.54	mA/°C
	Pulse transient forward current	(Note 1)	I_{FP}	1	A
	Reverse voltage		V_R	5	V
	Input power dissipation		P_D	40	mW
	Input power dissipation derating (Ta ≥ 85°C)		$\Delta P_D/\Delta Ta$	-1.0	mW/°C
	Junction temperature		Tj	125	°C
Detector	"H" peak output current	(Note 2)	I_{OPH}	−0.6	A
	"L" peak output current	(Note 2)	I_{OPL}	0.6	A
	Output voltage		V_O	35	V
	Supply voltage		V_{CC}	35	V
	Output power dissipation		P_O	400	mW
	Output power dissipation derating (Ta ≥ 85°C)		$\Delta P_O/\Delta Ta$	-1.0	mW/°C
	Junction temperature		Tj	125	°C
Operating frequency		(Note 3)	f	25	kHz
Operating temperature range			Topr	−40 to 100	°C
Storage temperature range			Tstg	−55 to 125	°C
Lead soldering temperature (10 s)		(Note 4)	Tsol	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %)		(Note 5)	BV_S	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Pulse width P_W ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P_W ≤ 2 μs, f ≤15 kHz

Note 3: Exponential waveform I_{OPH} ≤ −0.3 A (≤ 2 μs), I_{OPL} ≤+0.3 A (≤ 2 μs), Ta = 100 °C

Note 4: For the effective lead soldering area

Note 5: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Recommended Operating Conditions

Characteristics		Symbol	Min	Typ.	Max	Unit
Input current, ON	(Note 6)	$I_{F\ (ON)}$	7.5	—	10	mA
Input voltage, OFF		$V_{F\ (OFF)}$	0	—	0.8	V
Supply voltage		V_{CC}	10	—	30	V
Peak output current		I_{OPH} / I_{OPL}	—	—	± 0.2	A
Operating temperature		Topr	−40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 6: Input signal rise time (fall time) < 0.5 μs.

Electrical Characteristics (Ta = −40 to 100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage		V_F	—	I_F = 5 mA, Ta = 25 °C		—	1.55	1.70	V
Temperature coefficient of forward voltage		$\Delta V_F/\Delta Ta$	—	I_F = 5 mA		—	−2.0	—	mV/°C
Input reverse current		I_R	—	V_R = 5 V, Ta = 25 °C		—	—	10	μA
Input capacitance		C_T	—	V =0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Output current (Note 7)	"H" Level	I_{OPH1}	1	V_{CC} = 15 V, I_F = 5 mA	$V_{6\text{-}5}$ = 4 V	—	−0.38	−0.2	A
Output current (Note 7)	"H" Level	I_{OPH2}	1	V_{CC} = 15 V, I_F = 5 mA	$V_{6\text{-}5}$ = 10 V	—	−0.60	−0.4	A
Output current (Note 7)	"L" Level	I_{OPL1}	2	V_{CC} = 15 V, I_F = 0 mA	$V_{5\text{-}4}$ = 2 V	0.2	0.36	—	A
Output current (Note 7)	"L" Level	I_{OPL2}	2	V_{CC} = 15 V, I_F = 0 mA	$V_{5\text{-}4}$ = 10 V	0.4	0.62	—	A
Output voltage	"H" Level	V_{OH}	3	V_{CC} = 10 V	I_O = −100 mA, I_F = 5 mA	6.0	8.5	—	V
Output voltage	"L" Level	V_{OL}	4	V_{CC} = 10 V	I_O = 100 mA, V_F = 0.8 V	—	0.4	1.0	V
Supply current	"H" Level	I_{CCH}	5	V_{CC} = 10 to 30 V, V_O = Open	I_F = 10 mA	—	1.4	2.0	mA
Supply current	"L" Level	I_{CCL}	6	V_{CC} = 10 to 30 V, V_O = Open	I_F = 0 mA	—	1.3	2.0	mA
Threshold input current	L → H	I_{FLH}	—	V_{CC} = 15 V, V_O > 1 V		—	2.5	5	mA
Threshold input voltage	H → L	V_{FHL}	—	V_{CC} = 15 V, V_O < 1 V		0.8	—	—	V
Supply voltage		V_{CC}	—	—		10	—	30	V

(*): All typical values are at Ta = 25°C

Note: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design.It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Note 7: Duration of I_O time ≤ 50 μs, 1 pulse

Isolation Characteristics (Ta = 25 °C)

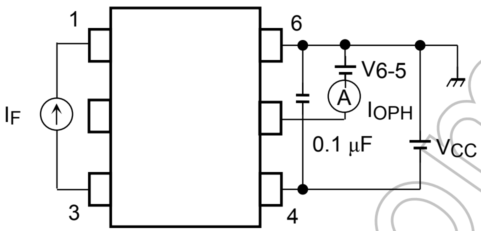
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C_S	V_S = 0 V , f = 1 MHz (Note 5)	—	1.0	—	pF
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 V (Note 5)	10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 60 s (Note 5)	5000	—	—	Vrms

Switching Characteristics (Ta = −40 to 100 °C, unless otherwise specified)

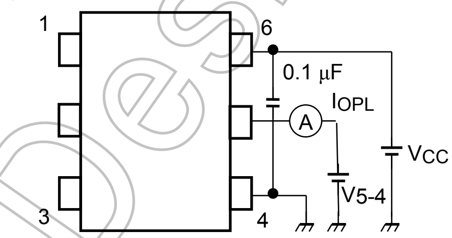
Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Propagation delay time	L → H	t_{pLH}	7	V_{CC} = 30 V, R_g = 47 Ω, C_g = 3 nF	I_F = 0 → 5 mA	100	—	700	ns
	H → L	t_{pHL}			I_F = 5 → 0 mA	100	—	700	
Output rise time (10−90 %)		tr			I_F = 0 → 5 mA	—	50	—	
Output fall time (90−10 %)		tf			I_F = 5 → 0 mA	—	50	—	
Switching time dispersion between ON and OFF		$\vert t_{pHL}$- $t_{pLH} \vert$			I_F = 0 ⇔ 5 mA	—	—	500	
Common mode transient immunity at HIGH level output		CM_H	8	V_{CM} = 1000 Vp-p, V_{CC} = 30 V, Ta = 25 °C	I_F = 5 mA, $V_{O\ (min)}$ = 26 V	−10000	—	—	V/μs
Common mode transient immunity at LOW level output		CM_L			I_F = 0 mA, $V_{O\ (max)}$ = 1 V	10000	—	—	

(*): All typical values are at Ta = 25 °C.

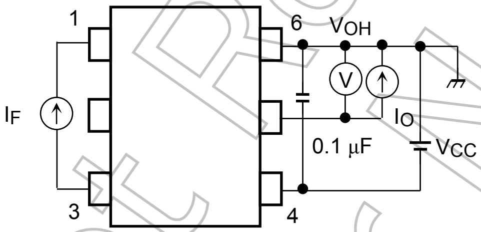
Test Circuit 1: I_{OPH}



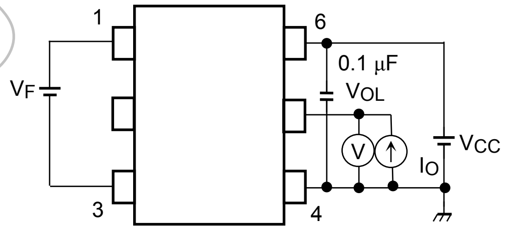
Test Circuit 2: I_{OPL}



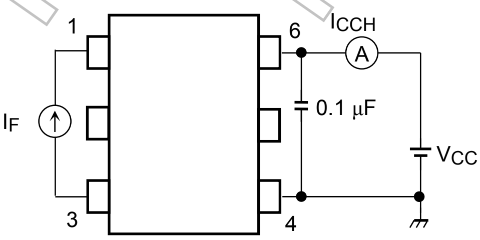
Test Circuit 3: V_{OH}



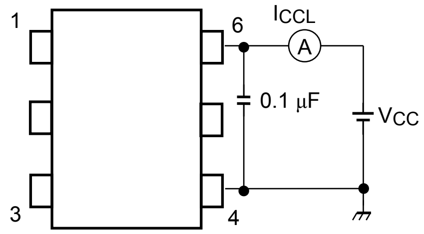
Test Circuit 4: V_{OL}



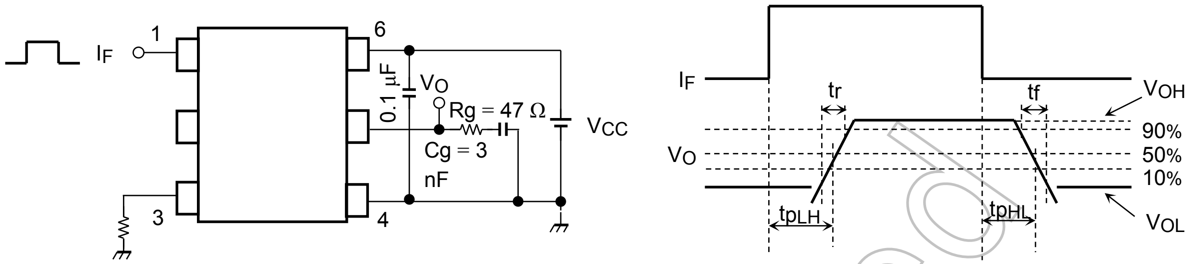
Test Circuit 5: I_{CCH}



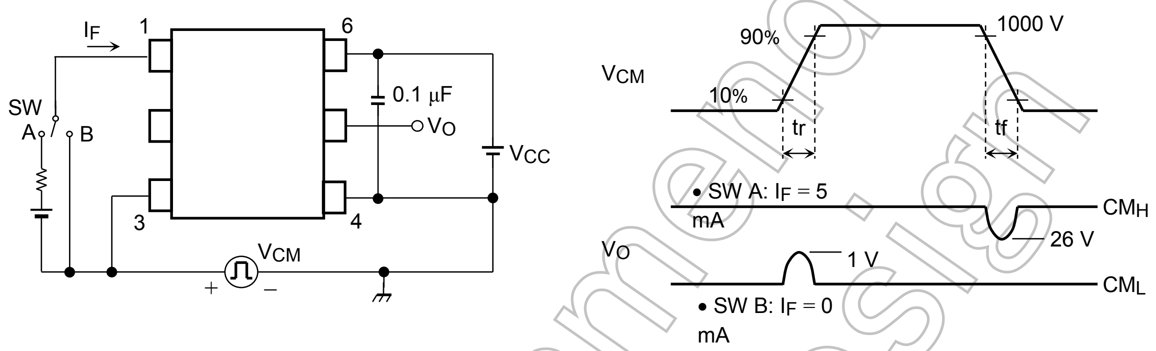
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH}, t_{pHL}, t_r, t_f, PDD



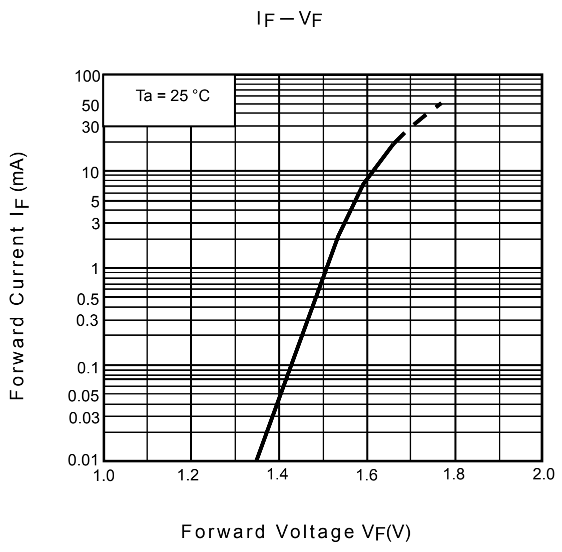
Test Circuit 8: CM_H, CM_L

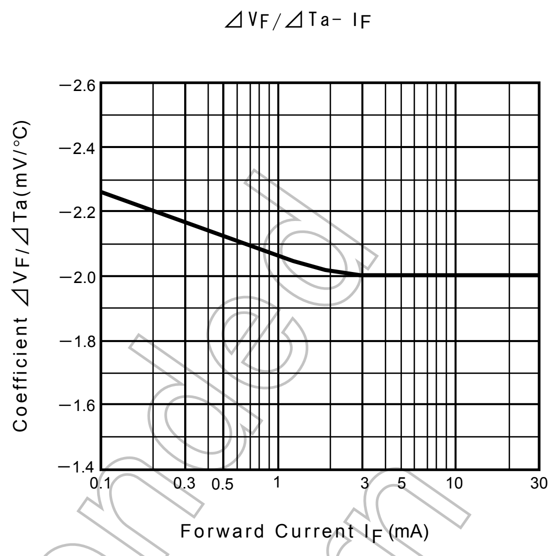


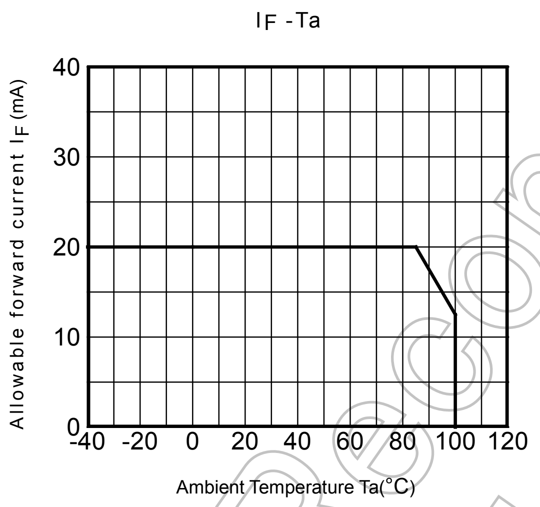
$$CM_L = \frac{800\ V}{t_r\ (\mu s)}$$

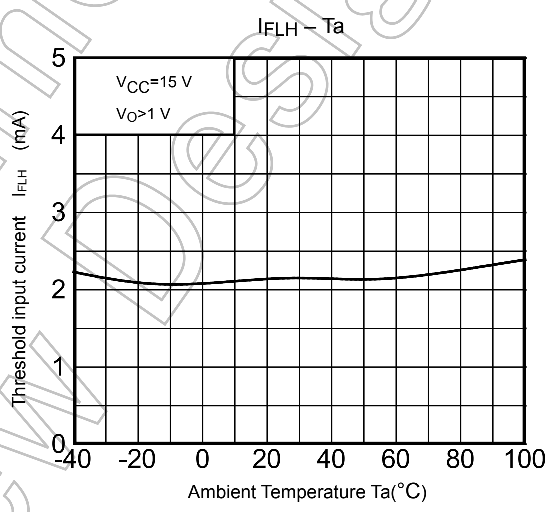
$$CM_H = -\frac{800\ V}{t_f\ (\mu s)}$$

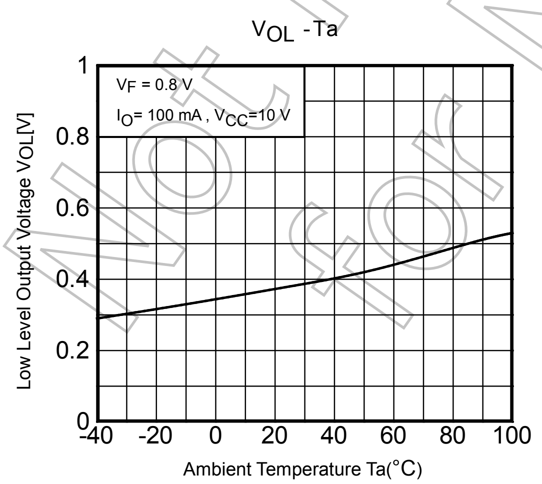
CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.

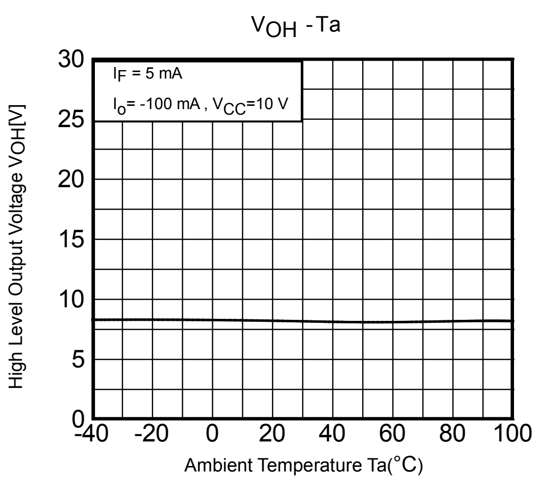




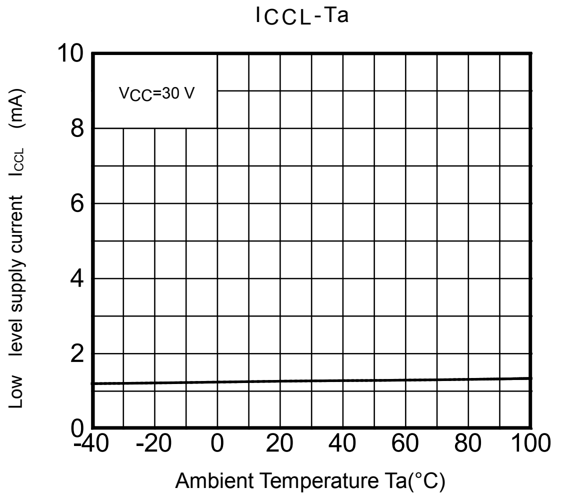


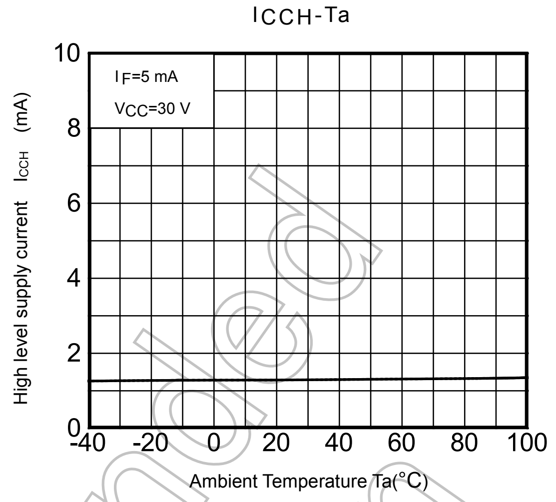


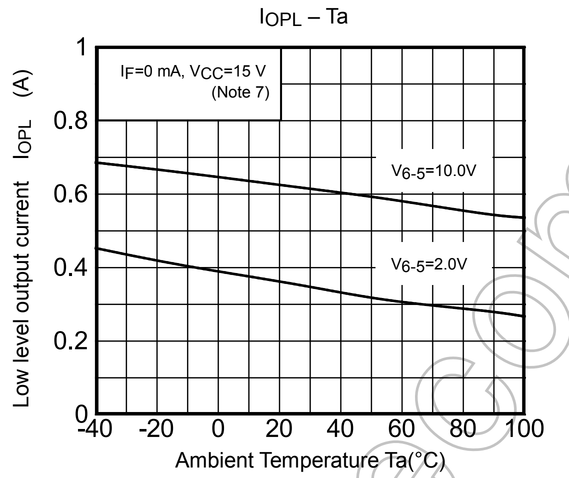


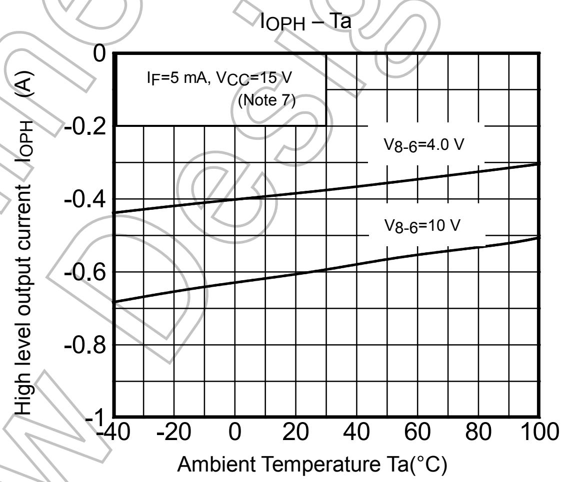


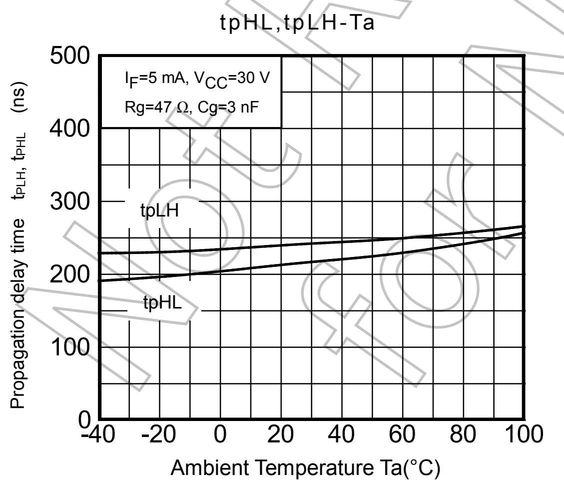
NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.











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