Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY91F583AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK
CY91F584AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK
CY91F585AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK

CY91580M/S Series, FR81S 32-bit Microcontroller Datasheet

This series is a Cypress 32-bit microcontroller for automobile motor control. They use the FR81S CPU that is compatible with the FR family.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 128MHz (Source oscillation= 4.0MHz, 32 multiplied (PLL clock multiplication system))
- General-purpose register: 32 bits × 16 sets
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instructions
  - Bit manipulation instructions
  - Barrel shift instructions
- High-level language support instructions
  - Function entry/exit instructions
  - Register content multi-load and store instructions
- Bit search instructions

Logical 1 detection, 0 detection, and change-point detection

- Branch instructions with delay slot

Overhead decrement during branch process

- Register interlock function

Easy assembler writing

- Built-in multiplier and instruction level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)

6 cycles (16 priority levels)

- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and data.
  - Control access privilege in both privilege mode and user mode
- Built-in FPU (floating-point operation)
  - IEEE754 compliant
  - Floating-point register: 32 bits × 16 sets

Peripheral functions

- Clock generation (SSCG function is available)
  - Main oscillation (4 MHz to 20 MHz)
  - PLL multiplication rate:1 to 32 times
- CR oscillation
  - Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)
  - Trimming is enabled
  - To be used as a count clock of hardware watchdog
  - Oscillation stop feature during standby is not available
    CY91F583AMJ/F584AMJ/F585AMJ/F583AMK/F584AMK/F585AMK
    CY91F583ASJ/F584ASJ/F585ASJ/F583ASK/F584ASK/F585ASK
  - Oscillation stop feature during standby is available
    CY91F583AMG/F584AMG/F585AMG/F583AMH/F584AMH/F585AMH
    CY91F583ASG/F584ASG/F585ASG/F583ASH/F584ASH/F585ASH
- Built-in program flash memory capacity

CY91F583: 256+64 Kbytes
CY91F584: 384+64 Kbytes
CY91F585: 512+64 Kbytes

- Built-in data flash (WorkFlash) 64 Kbytes
- Built-in RAM capacity
  - Main RAM
    CY91F583: 32 Kbytes
    CY91F584: 48 Kbytes
    CY91F585: 48 Kbytes
  - Backup RAM 8 Kbytes
- General-purpose port:
  CY91F583AM/F584AM/F585AM 76 ports
  Including eight I^2C pseudo open drain corresponding ports
  CY91F583AS/F584AS/F585AS 44ports
  Including two I^2C pseudo open drain corresponding ports

- DMA controller
  - Up to 8 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- External interrupt input

CY91F583AM/F584AM/F585AM: 8 channels
CY91F583AS/F584AS/F585AS: 7 channels
Level ("H" / "L") or edge detection (rising or falling) enabled

- Multi-function serial communication (built-in transmission/reception FIFO memory)

CY91F583AM/F584AM/F585AM: 4 channels
CY91F583AS/F584AS/F585AS: 2 channels

  - UART (Asynchronous serial interface)
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - Parity or no parity is selectable.
    - Built-in dedicated baud rate generator
    - An external clock can be used as the transfer clock
    - Parity, frame, and overrun error detection functions provided
    - DMA transfer supported
  - CSIO (Synchronous serial interface)
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
    - Built-in dedicated baud rate generator (Master operation)
    - An external clock can be entered. (Slave operation)
    - Overrun error detection function is provided.
    - Built-in chip selection function
    - DMA transfer supported
  - LIN interface (v2.1)
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - LIN protocol revision2.1 supported.
    - Master and slave systems supported
    - Framing error and overrun error detection
    - LIN sync break generation and detection; LIN sync delimiter generation
    - Built-in dedicated baud rate generator
    - An external clock can be adjusted by the reload counter.
    - DMA transfer supported
  - I^2C
    - CY91F583AM/F584AM/F585AM: Supported for 3 channels: ch.0,ch.2,and ch.3
      CY91F583AS/F584AS/F585AS: Supported for 1 channel: ch.0
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - Standard mode (Max. 100 kbps) / high-speed mode (Max. 400 kbps) supported
    - DMA transfer supported (for transmission only)
- CAN controller (CAN)

CY91F583AM/F584AM/F585AM: 2 channels
CY91F583AS/F584AS/F585AS: 1 channel

  - Transfer speed: Up to 1Mbps
  - 64-transmission/reception message buffering
- FlexRay controller

CY91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ/
F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ:
1 unit (ch.A/ch.B)

  - FlexRay Specifications Version 2.1 supported
  - Up to 128 message buffers
  - 8K bytes of message RAM
  - Variable length of message buffers
  - Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO memory
  - Host access to the message buffer via input and output buffers
  - Filtering for slot counter, cycle counter and channels
  - Maskable interrupts are supported
- PPG: 16 bits × 6 channels
- Reload timer: 16 bits × 4 channels
- A/D converter (successive approximation type)
  - 12-bit resolution
    CY91F583AM/F584AM/F585AM: 3 units (23 channels)
    CY91F583AS/F584AS/F585AS: 3 units (17 channels)
  - Conversion time: 1 μs
- Free-run timer

16 bits × 6 channels (1 channel can be selected for input capture, and 1 channel for output compare.)

- Input capture: 16 bits × 4 channels (linked to the free-run timer)
- Output compare: 16 bits × 7 channels (linked to the free-run timer)
- Waveform generator: 2 units (7 channels)
- 10-bit D/A converter: 1 channel
- Calibration: The hardware watchdog for CR oscillation drive

The CR oscillation frequency can be trimmed.

- Clock Supervisor
  - Anomaly supervisory feature (by damaged quartz, etc.) of external main oscillation (4MHz)
  - When anomaly is detected, clock is switched to CR.
- Up/ down counter: 2 channels
  - 8/16-bit Up/ down counter
- Base timer: 2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used.
  - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.

- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read

Multiple interrupts from peripherals can be read by a series of registers.

- I/O relocation (CY91F583AM/F584AM/F585AM)

Change of pin position of peripheral functions

- Low-power consumption mode
  - Sleep/Stop/Watch
  - Stop (Power shutdown)/Watch (Power shutdown)
- Power-on reset
- Low-voltage detection reset (external low-voltage detection)
- Low-voltage detection reset (internal low-voltage detection)
- Package

CY91F583AM/F584AM/F585AM: LQFP-100
CY91F583AS/F584AS/F585AS: LQFP-64

- CMOS 90 nm technology
- Power supplies
  - Single 5V power supply
  - The voltage step-down circuit brings the 5.0V down to generate 1.2V internally
  - I/O 5.0V

Contents

1. Product Lineup

CY91580AM Series Product Lineup Comparison

■ Memory size

Items	CY91F583AMG CY91F583AMH CY91F583AMJ CY91F583AMK	CY91F584AMG CY91F584AMH CY91F584AMJ CY91F584AMK	CY91F585AMG CY91F585AMH CY91F585AMJ CY91F585AMK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

Items	CY91F583AMG CY91F584AMG CY91F585AMG	CY91F583AMH CY91F584AMH CY91F585AMH	CY91F583AMJ CY91F584AMJ CY91F585AMJ	CY91F583AMK CY91F584AMK CY91F585AMK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 units (7 channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	8 channels			
A/D converter	3 units (23 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	4 channels			
CAN	64msb × 2 channels (ch.0/ch.1)			
FlexRay	128msb × 1 unit (ch.A / ch.B)	Not provided	128msb × 1 unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (internal low-voltage detection)	Provided			

Items	CY91F583AMG CY91F584AMG CY91F585AMG	CY91F583AMH CY91F584AMH CY91F585AMH	CY91F583AMJ CY91F584AMJ CY91F585AMJ	CY91F583AMK CY91F584AMK CY91F585AMK
Low-voltage detection reset (external low-voltage detection)	Provided			
Device package	LQFP-100			
Debug interface	Built-in OCD (On Chip Debug Unit)			

CY91580AS Series Product Lineup Comparison

■ Memory size

Items	CY91F583ASG CY91F583ASH CY91F583ASJ CY91F583ASK	CY91F584ASG CY91F584ASH CY91F584ASJ CY91F584ASK	CY91F585ASG CY91F585ASH CY91F585ASJ CY91F585ASK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

Items	CY91F583ASG CY91F584ASG CY91F585ASG	CY91F583ASH CY91F584ASH CY91F585ASH	CY91F583ASJ CY91F584ASJ CY91F585ASJ	CY91F583ASK CY91F584ASK CY91F585ASK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 units (7 channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	7 channels			
A/D converter	3 units (17 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	2 channels			
CAN	64msb × 1 channel (ch.0)			
FlexRay	128msb × 1unit (ch.A / ch.B)	Not provided	128msb × 1unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (internal low-voltage detection)	Provided			

Items	CY91F583ASG CY91F584ASG CY91F585ASG	CY91F583ASH CY91F584ASH CY91F585ASH	CY91F583ASJ CY91F584ASJ CY91F585ASJ	CY91F583ASK CY91F584ASK CY91F585ASK
Low-voltage detection reset (external low-voltage detection)	Provided			
Device package	LQFP-64			
Debug interface	Built-in OCD (On Chip Debug Unit)			

CY91580L Series Product Lineup Comparison

■ Memory size

Items	CY91F585LA CY91F585LB CY91F585LC CY91F585LD	CY91F586LA CY91F586LB CY91F586LC CY91F586LD	CY91F587LA CY91F587LB CY91F587LC CY91F587LD
Flash memory capacity (program)	512+64 Kbytes	768+64 Kbytes	1024+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	48 Kbytes	64 Kbytes	96 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

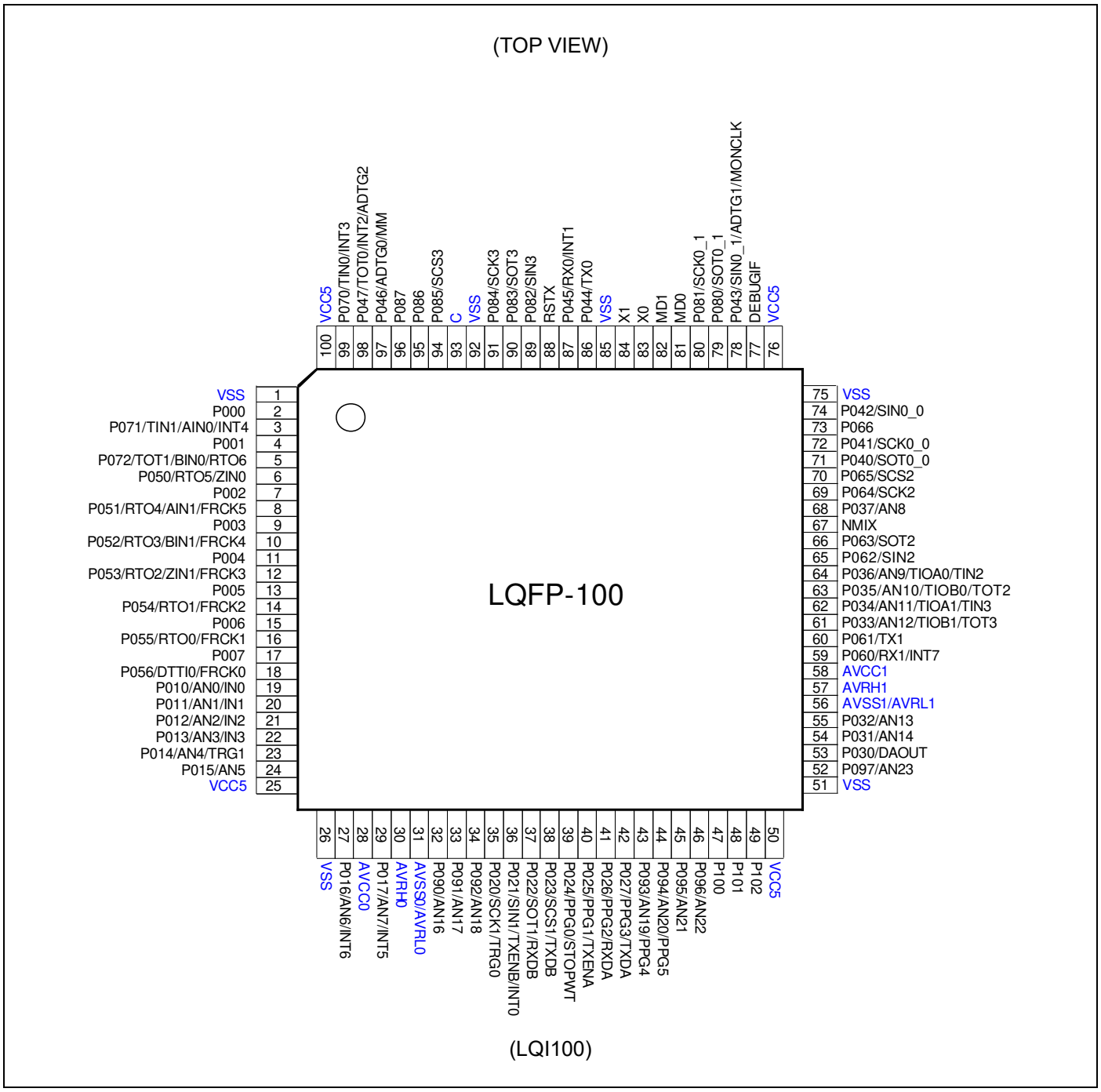
Items	CY91F585LA CY91F586LA CY91F587LA	CY91F585LB CY91F586LB CY91F587LB	CY91F585LC CY91F586LC CY91F587LC	CY91F585LD CY91F586LD CY91F587LD
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided	Address: 22 bits Data: 16 bits	Not provided	Address: 22 bits Data: 16 bits
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	8 channels			
Output compare	12 channels			
Waveform generator	2 units (12 channels)			
16-bit reload timer	4 channels			
PPG	24 channels			
External interrupt	8 channels			
A/D converter	3 units (24 channels)			
R/D converter	Provided	Not provided	Provided	Not provided
D/A converter	Not provided	Provided	Not provided	Provided
Up/ down counter	2 channels			
Multi-function serial interface	5 channels			
CAN	64 msb × 3 channels (ch.0/ch.1/ch.2)			
FlexRay	128 msb × 1 unit (ch.A / ch.B)			
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	1 channel			
Low-voltage detection reset (internal low-voltage detection)	Provided			
Low-voltage detection reset (external low-voltage detection)	Provided			

Items	CY91F585LA CY91F586LA CY91F587LA	CY91F585LB CY91F586LB CY91F587LB	CY91F585LC CY91F586LC CY91F587LC	CY91F585LD CY91F586LD CY91F587LD
Device package	LQFP-144			
Debug interface	Built-in OCD (On Chip Debug Unit)			

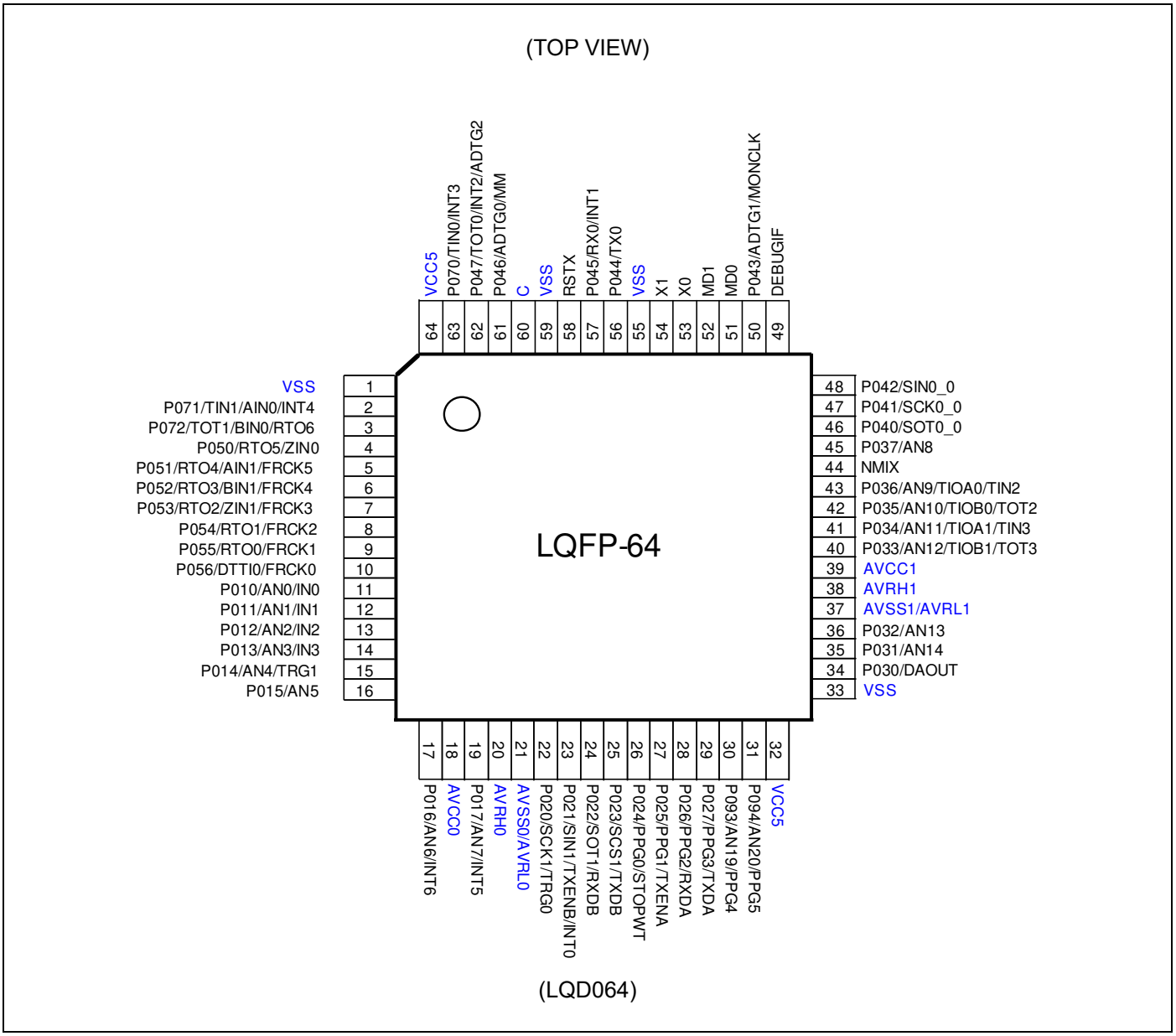
Note: For details on the CY91580L series, see the "CY91580L Series HARDWARE MANUAL".

2. Pin Assignment

LQFP-100 Pin Assignment CY91F583AM/F584AM/F585AM



LQFP-64 Pin Assignment CY91F583AS/F584AS/F585AS



3. Pin Description

CY91F583AM/F584AM/F585AM

Pin No.	Pin name	I/O circuit type*	Function
83	X0	A	Main clock oscillation input pin
84	X1		Main clock oscillation output pin
67	NMIX	B	Interrupt input pin without mask
88	RSTX	B	External reset input pin
81	MD0	C	Mode pin 0 (with high-voltage control)
82	MD1	C	Mode pin 1 (with high-voltage control)
2	P000	D	General-purpose I/O port
4	P001	D	General-purpose I/O port
7	P002	D	General-purpose I/O port
9	P003	D	General-purpose I/O port
11	P004	D	General-purpose I/O port
13	P005	D	General-purpose I/O port
15	P006	D	General-purpose I/O port
17	P007	D	General-purpose I/O port
19	P010	F	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
	AN0		ADC analog 0 input pin
20	P011	F	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
	AN1		ADC analog 1 input pin
21	P012	F	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
	AN2		ADC analog 2 input pin
22	P013	F	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
	AN3		ADC analog 3 input pin
23	P014	F	General-purpose I/O port
	TRG1		PPG ch.4, ch.5 external trigger
	AN4		ADC analog 4 input pin
24	P015	F	General-purpose I/O port
	AN5		ADC analog 5 input pin
27	P016	G	General-purpose I/O port
	AN6		ADC analog 6 input pin
	INT6		INT6 external interrupt input pin

Pin No.	Pin name	I/O circuit type*	Function
29	P017	G	General-purpose I/O port
	AN7		ADC analog 7 input pin
	INT5		INT5 external interrupt input pin
35	P020	D	General-purpose I/O port
	SCK1		Multi-function serial ch.1 clock I/O pin
	TRG0		PPG ch.0 to ch.3 external trigger
36	P021	L	General-purpose I/O port
	SIN1		Multi-function serial ch.1 serial data input pin
	TXENB		FlexRay ch.B operation enable output pin
	INT0		INT0 external interrupt input pin
37	P022	K	General-purpose I/O port
	SOT1		Multi-function serial ch.1 serial data output pin
	RXDB		FlexRay ch.B data input pin
38	P023	K	General-purpose I/O port
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
	TXDB		FlexRay ch.A operation enable output pin
39	P024	D	General-purpose I/O port
	PPG0		PPG ch.0 output pin
	STOPWT		FlexRay Stopwatch input pin
40	P025	K	General-purpose I/O port
	PPG1		PPG ch.1 output pin
	TXENA		FlexRay ch.A operation enable output pin
41	P026	K	General-purpose I/O port
	PPG2		PPG ch.2 output pin
	RXDA		FlexRay ch.A data input pin
42	P027	K	General-purpose I/O port
	PPG3		PPG ch.3 output pin
	TXDA		FlexRay ch.A data output pin
53	P030	M	General-purpose I/O port
	DAOUT		DAC analog output pin
54	P031	F	General-purpose I/O port
	AN14		ADC analog 14 input pin

Pin No.	Pin name	I/O circuit type*	Function
55	P032	F	General-purpose I/O port
	AN13		ADC analog 13 input pin
61	P033	F	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB input pin
	TOT3		Reload timer ch.3 output pin
	AN12		ADC analog 12 input pin
62	P034	F	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA I/O pin
	TIN3		Reload timer ch.3 event input pin
	AN11		ADC analog 11 input pin
63	P035	F	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB input pin
	TOT2		Reload timer ch.2 output pin
	AN10		ADC analog 10 input pin
64	P036	F	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA output pin
	TIN2		Reload timer ch.2 event input pin
	AN9		ADC analog 9 input pin
68	P037	F	General-purpose I/O port
	AN8		ADC analog 8 input pin
71	P040	H	General-purpose I/O port
	SOT0_0		Multi-function serial ch.0 serial data output pin (0)/ I^2C ch.0 serial data I/O pin (SDA)
72	P041	H	General-purpose I/O port
	SCK0_0		Multi-function serial ch.0 clock I/O pin (0)/ I^2C ch.0 clock I/O pin (SCL)
74	P042	D	General-purpose I/O port
	SIN0_0		Multi-function serial ch.0 serial data input pin (0)
78	P043	D	General-purpose I/O port
	SIN0_1		Multi-function serial ch.0 serial data input pin (1)
	ADTG1		A/D converter ch.8 to ch.14 external trigger input pin
	MONCLK		Clock monitor output pin
86	P044	D	General-purpose I/O port
	TX0		CAN transmission data 0 output pin

Pin No.	Pin name	I/O circuit type*	Function
87	P045	E	General-purpose I/O port
	RX0		CAN reception data 0 input pin
	INT1		INT1 external interrupt input pin
97	P046	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
	MM		Clock supervisor main clock stop detection output pin
98	P047	E	General-purpose I/O port
	TOT0		Reload timer ch.0 output pin
	INT2		INT2 external interrupt input pin
	ADTG2		A/D converter ch.16-ch.23 external trigger input pin
6	P050	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	ZIN0		Up/down counter ch.0 ZIN input pin
8	P051	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	AIN1		Up/down counter ch.1 AIN input pin
	FRCK5		Free-run timer ch.5 external clock input pin
10	P052	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	BIN1		Up/down counter ch.1 BIN input pin
	FRCK4		Free-run timer ch.4 external clock input pin
12	P053	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	ZIN1		Up/down counter ch.1 ZIN input pin
	FRCK3		Free-run timer ch.3 external clock input pin
14	P054	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	FRCK2		Free-run timer ch.2 external clock input pin
16	P055	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	FRCK1		Free-run timer ch.1 external clock input pin
18	P056	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	FRCK0		Free-run timer ch.0 external clock input pin
59	P060	E	General-purpose I/O port
	RX1		CAN reception data 1 input pin
	INT7		INT7 external interrupt input pin
60	P061	D	General-purpose I/O port
	TX1		CAN transmission data 1 output pin

Pin No.	Pin name	I/O circuit type*	Function
65	P062	D	General-purpose I/O port
	SIN2		Multi-function serial ch.2 serial data input pin
66	P063	H	General-purpose I/O port
	SOT2		Multi-function serial ch.2 serial data output pin/ I^2C ch.2 serial data I/O pin (SDA)
69	P064	H	General-purpose I/O port
	SCK2		Multi-function serial ch.2 clock I/O pin/ I^2C ch.2 clock I/O pin (SCL)
70	P065	D	General-purpose I/O port
	SCS2		Multi-function serial ch.2 serial chip select I/O pin
73	P066	D	General-purpose I/O port
99	P070	E	General-purpose I/O port
	TIN0		Reload timer ch.0 event input pin
	INT3		INT3 external interrupt input pin
3	P071	E	General-purpose I/O port
	TIN1		Reload timer ch.1 event input pin
	AIN0		Up/down counter ch.0 AIN input pin
	INT4		INT4 external interrupt input pin
5	P072	D	General-purpose I/O port
	TOT1		Reload timer ch.1 output pin
	BIN0		Up/down counter ch.0 BIN input pin
	RTO6		Waveform generator ch.6 output pin
79	P080	H	General-purpose I/O port
	SOT0_1		Multi-function serial ch.0 serial data output pin (1)/ I^2C ch.0 serial data I/O pin (1) (SDA)
80	P081	H	General-purpose I/O port
	SCK0_1		Multi-function serial ch.0 clock I/O pin (1)/ I^2C ch.0 clock I/O pin (1) (SCL)
89	P082	D	General-purpose I/O port
	SIN3		Multi-function serial ch.3 serial data input pin
90	P083	H	General-purpose I/O port
	SOT3		Multi-function serial ch.3 serial data output pin/ I^2C ch.3 serial data I/O pin (SDA)
91	P084	H	General-purpose I/O port
	SCK3		Multi-function serial ch.3 clock I/O pin/ I^2C ch.3 clock I/O pin (SCL)
94	P085	D	General-purpose I/O port
	SCS3		Multi-function serial ch.3 serial chip select I/O pin
95	P086	D	General-purpose I/O port
96	P087	D	General-purpose I/O port

Pin No.	Pin name	I/O circuit type*	Function
32	P090	F	General-purpose I/O port
	AN16		ADC analog 16 input pin
33	P091	F	General-purpose I/O port
	AN17		ADC analog 17 input pin
34	P092	F	General-purpose I/O port
	AN18		ADC analog 18 input pin
43	P093	F	General-purpose I/O port
	PPG4		PPG ch.4 output pin
	AN19		ADC analog 19 input pin
44	P094	F	General-purpose I/O port
	PPG5		PPG ch.5 output pin
	AN20		ADC analog 20 input pin
45	P095	F	General-purpose I/O port
	AN21		ADC analog 21 input pin
46	P096	F	General-purpose I/O port
	AN22		ADC analog 22 input pin
52	P097	F	General-purpose I/O port
	AN23		ADC analog 23 input pin
47	P100	D	General-purpose I/O port
48	P101	D	General-purpose I/O port
49	P102	D	General-purpose I/O port
77	DEBUGIF	I	DEBUG I/F pin
28	AVCC0	-	A/D converter analog power supply
58	AVCC1	-	A/D converter analog power supply
30	AVRH0	-	A/D converter upper limit reference voltage
57	AVRH1	-	A/D converter upper limit reference voltage
31	AVSS0	-	A/D converter GND
	AVRL0		A/D converter lower limit reference voltage
56	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
93	C	-	External capacity connection output pin
25, 50, 76, 100	VCC5	-	+5.0V power supply
1, 26, 51, 75, 85, 92	VSS	-	GND

* For I/O circuit types, see 4 I/O Circuit Type

CY91F583AS/F584AS/F585AS

Pin No.	Pin name	I/O circuit type*	Function
53	X0	A	Main clock oscillation input pin
54	X1		Main clock oscillation output pin
44	NMIX	B	Interrupt input pin without mask
58	RSTX	B	External reset input pin
51	MD0	C	Mode pin 0 (with high-voltage control)
52	MD1	C	Mode pin 1 (with high-voltage control)
11	P010	F	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
	AN0		ADC analog 0 input pin
12	P011	F	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
	AN1		ADC analog 1 input pin
13	P012	F	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
	AN2		ADC analog 2 input pin
14	P013	F	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
	AN3		ADC analog 3 input pin
15	P014	F	General-purpose I/O port
	TRG1		PPG ch.4, ch.5 external trigger
	AN4		ADC analog 4 input pin
16	P015	F	General-purpose I/O port
	AN5		ADC analog 5 input pin
17	P016	G	General-purpose I/O port
	AN6		ADC analog 6 input pin
	INT6		INT6 external interrupt input pin
19	P017	G	General-purpose I/O port
	AN7		ADC analog 7 input pin
	INT5		INT5 external interrupt input pin
22	P020	D	General-purpose I/O port
	SCK1		Multi-function serial ch.1 clock I/O pin
	TRG0		PPG ch.0 to ch.3 external trigger
23	P021	L	General-purpose I/O port
	SIN1		Multi-function serial ch.1 serial data input pin
	TXENB		FlexRay ch.B operation enable output pin
	INT0		INT0 external interrupt input pin

Pin No.	Pin name	I/O circuit type*	Function
24	P022	K	General-purpose I/O port
	SOT1		Multi-function serial ch.1 serial data output pin
	RXDB		FlexRay ch.B data input pin
25	P023	K	General-purpose I/O port
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
	TXDB		FlexRay ch.B data output pin
26	P024	D	General-purpose I/O port
	PPG0		PPG ch.0 output pin
	STOPWT		FlexRay Stopwatch input pin
27	P025	K	General-purpose I/O port
	PPG1		PPG ch.1 output pin
	TXENA		FlexRay ch.A operation enable output pin
28	P026	K	General-purpose I/O port
	PPG2		PPG ch.2 output pin
	RXDA		FlexRay ch.A data input pin
29	P027	K	General-purpose I/O port
	PPG3		PPG ch.3 output pin
	TXDA		FlexRay ch.A data output pin
34	P030	M	General-purpose I/O port
	DAOUT		DAC analog output pin
35	P031	F	General-purpose I/O port
	AN14		ADC analog 14 input pin
36	P032	F	General-purpose I/O port
	AN13		ADC analog 13 input pin
40	P033	F	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB input pin
	TOT3		Reload timer ch.3 output pin
	AN12		ADC analog 12 input pin
41	P034	F	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA I/O pin
	TIN3		Reload timer ch.3 event input pin
	AN11		ADC analog 11 input pin
42	P035	F	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB input pin
	TOT2		Reload timer ch.2 output pin
	AN10		ADC analog 10 input pin

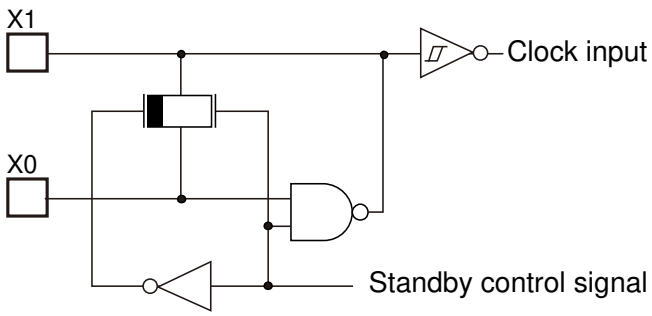
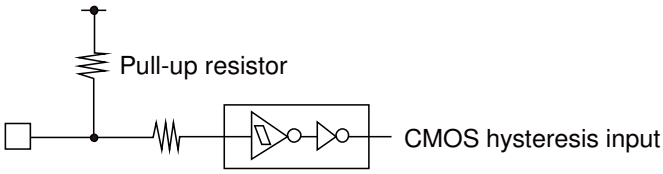
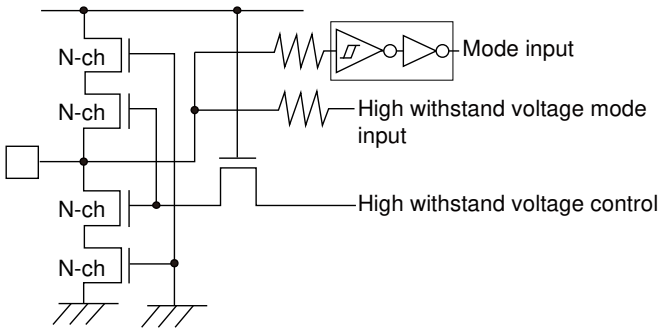
Pin No.	Pin name	I/O circuit type*	Function
43	P036	F	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA output pin
	TIN2		Reload timer ch.2 event input pin
	AN9		ADC analog 9 input pin
45	P037	F	General-purpose I/O port
	AN8		ADC analog 8 input pin
46	P040	H	General-purpose I/O port
	SOT0_0		Multi-function serial ch.0 serial data output pin(0)/ I^2C ch.0 serial data I/O pin (0) (SDA)
47	P041	H	General-purpose I/O port
	SCK0_0		Multi-function serial ch.0 clock I/O pin (0)/ I^2C ch.0 clock I/O pin (0) (SCL)
48	P042	D	General-purpose I/O port
	SIN0_0		Multi-function serial ch.0 serial data input pin (0)
50	P043	D	General-purpose I/O port
	ADTG1		A/D converter ch.8 to ch.14 external trigger input pin
	MONCLK		Clock monitor output pin
56	P044	D	General-purpose I/O port
	TX0		CAN transmission data 0 output pin
57	P045	E	General-purpose I/O port
	RX0		CAN reception data 0 input pin
	INT1		INT1 external interrupt input pin
61	P046	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
	MM		Clock supervisor main clock stop detection output pin
62	P047	E	General-purpose I/O port
	TOT0		Reload timer ch.0 output pin
	INT2		INT2 external interrupt input pin
	ADTG2		A/D converter ch.19 to ch.20 external trigger input pin
4	P050	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	ZIN0		Up/down counter ch.0 ZIN input pin
5	P051	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	AIN1		Up/down counter ch.1 AIN input pin
	FRCK5		Free-run timer ch.5 external clock input pin

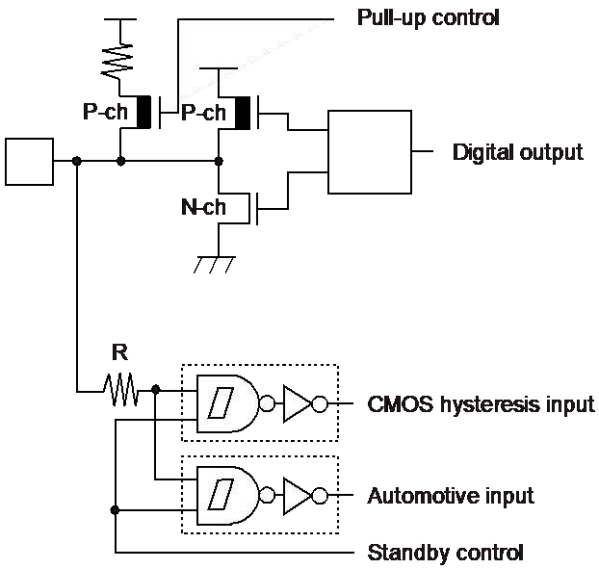
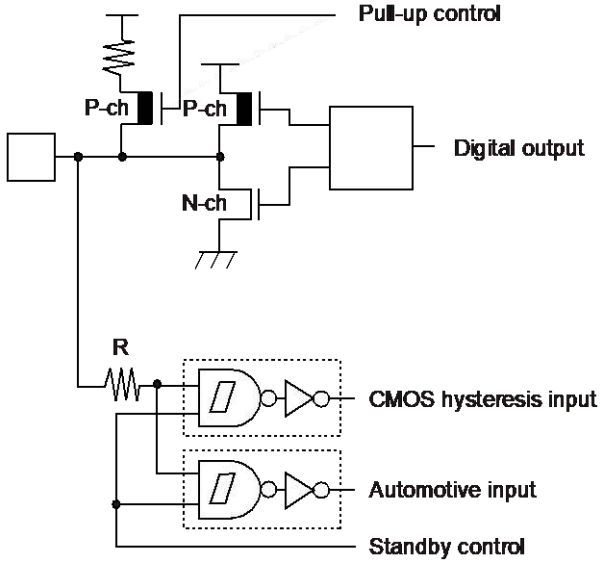
Pin No.	Pin name	I/O circuit type*	Function
6	P052	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	BIN1		Up/down counter ch.1 BIN input pin
	FRCK4		Free-run timer ch.4 external clock input pin
7	P053	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	ZIN1		Up/down counter ch.1 ZIN input pin
	FRCK3		Free-run timer ch.3 external clock input pin
8	P054	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	FRCK2		Free-run timer ch.2 external clock input pin
9	P055	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	FRCK1		Free-run timer ch.1 external clock input pin
10	P056	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	FRCK0		Free-run timer ch.0 external clock input pin
63	P070	E	General-purpose I/O port
	TIN0		Reload timer ch.0 event input pin
	INT3		INT3 external interrupt input pin
2	P071	E	General-purpose I/O port
	TIN1		Reload timer ch.1 event input pin
	AIN0		Up/down counter ch.0 AIN input pin
	INT4		INT4 external interrupt input pin
3	P072	D	General-purpose I/O port
	TOT1		Reload timer ch.1 output pin
	BIN0		Up/down counter ch.0 BIN input pin
	RTO6		Waveform generator ch.6 output pin
30	P093	F	General-purpose I/O port
	PPG4		PPG ch.4 output pin
	AN19		ADC analog 19 input pin
31	P094	F	General-purpose I/O port
	PPG5		PPG ch.5 output pin
	AN20		ADC analog 20 input pin
49	DEBUGIF	I	DEBUG I/F pin
18	AVCC0	-	A/D converter analog power supply
39	AVCC1	-	A/D converter analog power supply
20	AVRH0	-	A/D converter upper limit reference voltage
38	AVRH1	-	A/D converter upper limit reference voltage

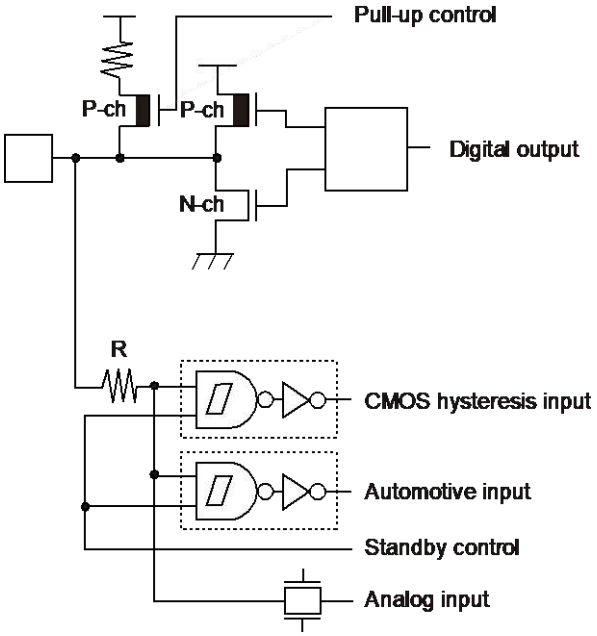
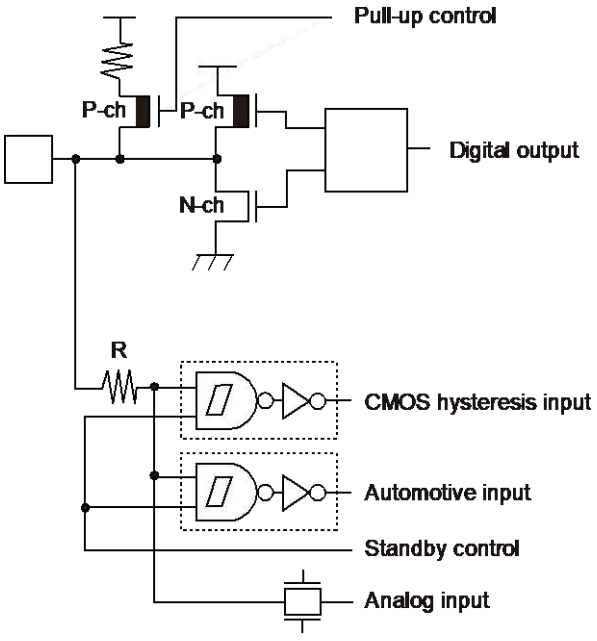
Pin No.	Pin name	I/O circuit type*	Function
21	AVSS0	-	A/D converter GND
	AVRL0		A/D converter lower limit reference voltage
37	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
60	C	-	External capacity connection output pin
32, 64	VCC5	-	+5.0V power supply
1, 33, 55, 59	VSS	-	GND

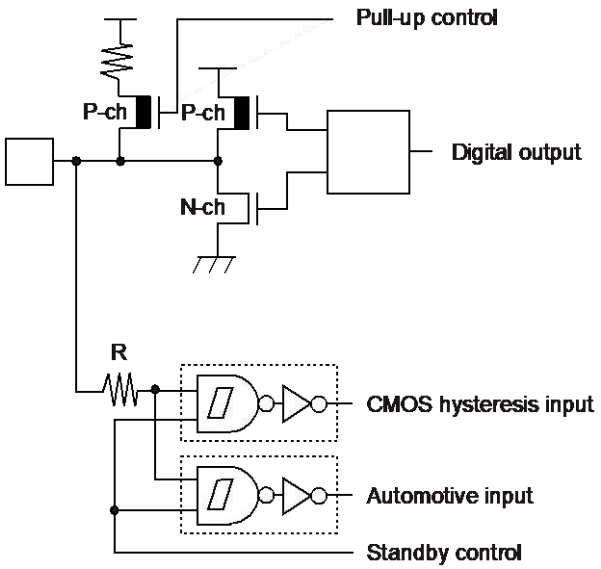
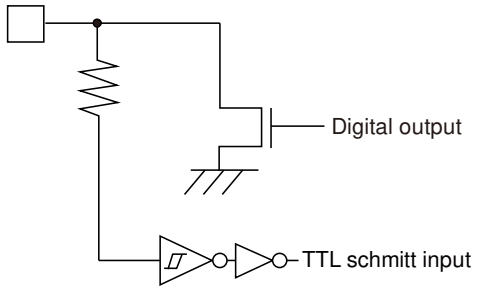
* For I/O circuit types, see 4 I/O Circuit Type

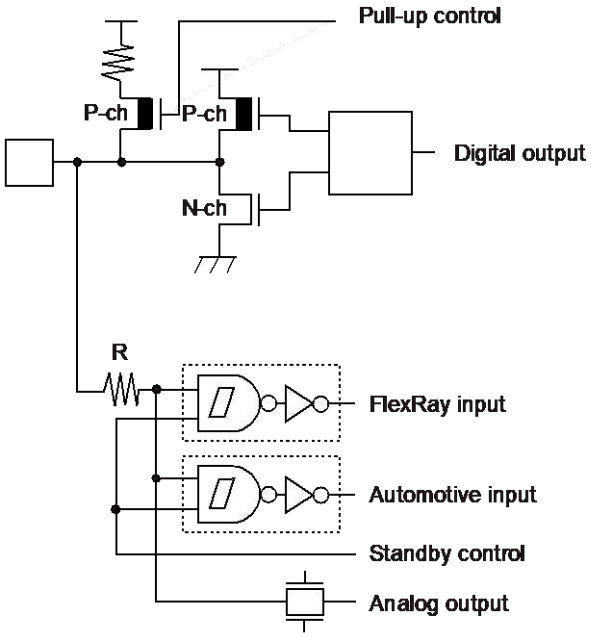
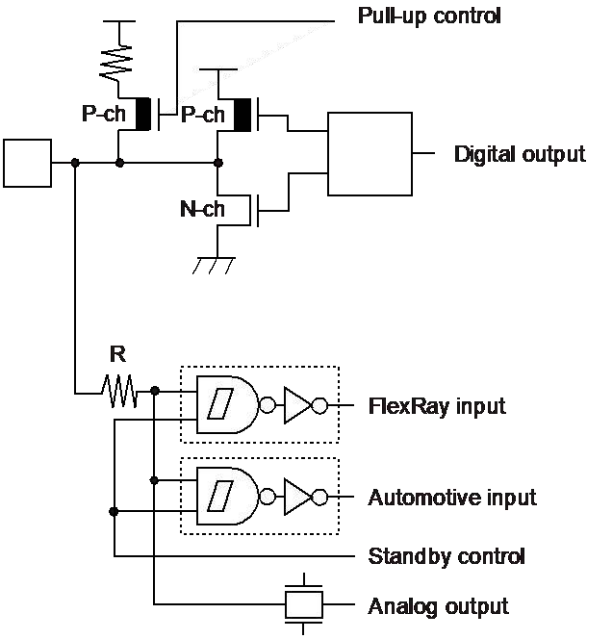
4. I/O Circuit Type

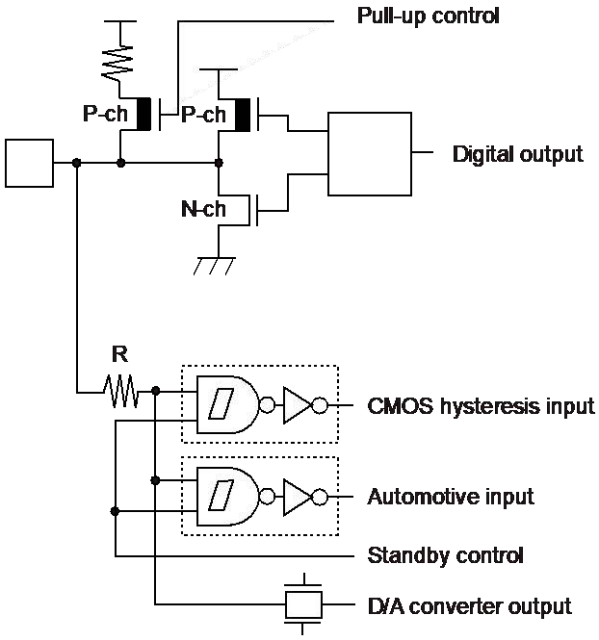
Type	Circuit	Remarks
A		Oscillation feedback resistor: Approx. 1 MΩ
B		■ CMOS hysteresis input ■ With 50 kΩ pull-up resistor
C		■ Schmitt input ■ With high withstand voltage control

Type	Circuit	Remarks
D		■ General-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
E		■ General-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Type	Circuit	Remarks
F		■ With analog input, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
G		■ With analog input, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Type	Circuit	Remarks
H		■ With I²C, general-purpose I/O port ■ CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I²C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
I		Open drain I/O

Type	Circuit	Remarks
K		■ With analog output, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA ■ With 50 kΩ pull-up resistor control ■ FlexRay input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vccc)
L		■ With analog output, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA ■ With 50 kΩ pull-up resistor control ■ FlexRay input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Type	Circuit	Remarks
M		■ With D/A converter output, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

2. Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

The latch-up prevention and pin processing are explained below.

■ For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supplies (AVCC0, AVCC1, AVRH0, AVRH1) and analog input must not exceed the digital power supply (VCC5) when the power supply to the analog system is turned on or off.

In the correct power-on sequence, turn on the digital power supply voltage (VCC5) and analog power supply voltages (AVCC0, AVCC1, AVRH0, AVRH1) simultaneously. Alternatively, turn on the digital power supply voltage (VCC5) first, and then turn on the analog power supplies (AVCC0, AVCC1, AVRH0, AVRH1).

■ Treatment of unused pins

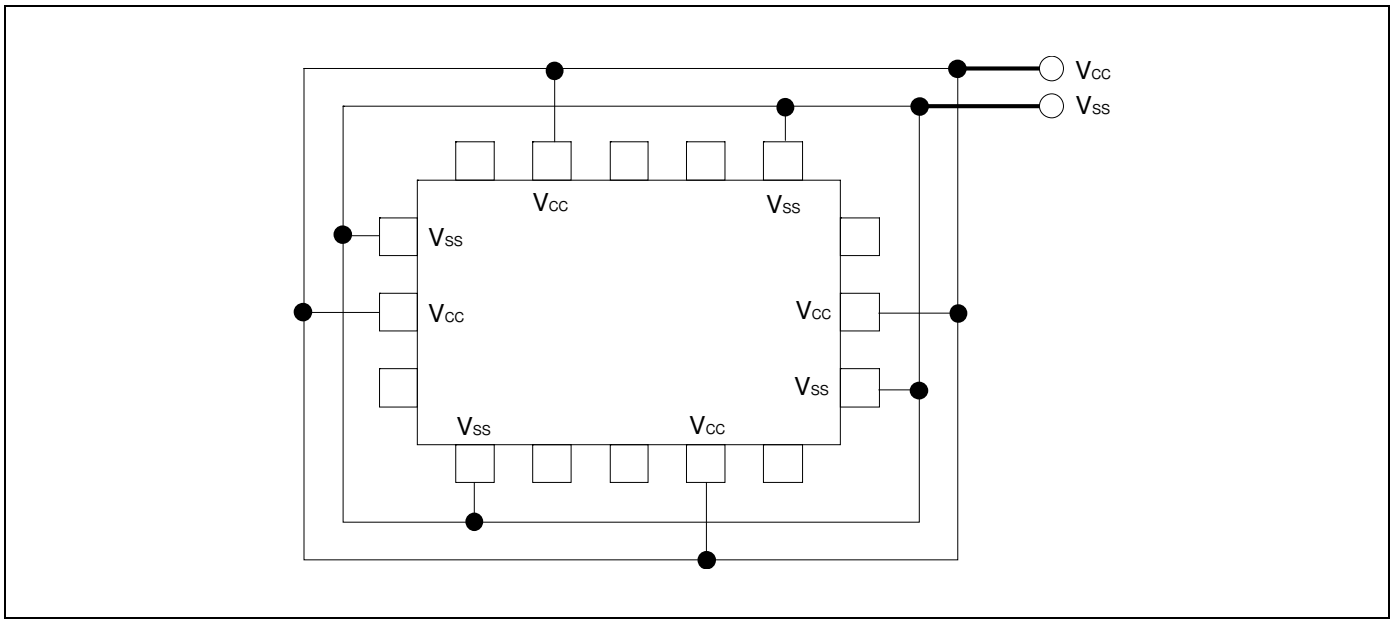
If unused input pins are left open, they may cause a permanent damage to the device due to device malfunction or latch-up. Connect a 2kΩ or higher resistor to each of unused input pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

■ Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in following figure, all VSS power supply pins must be treated in the similar way. If multiple VCC or VSS systems are connected, the device cannot operate correctly even within the guaranteed operating range.

■ Power Supply Input Pins



The power supply pins should be connected to VCC and VSS of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

■ Crystal oscillation circuit

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

■ Mode pin (MD[1:0])

Connect the MD[1:0] mode pin to the VCC or VSS pin directly.

To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■ During power-on

To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

■ Notes during PLL clock operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self oscillator circuit built in the PLL. This operation is not guaranteed.

■ Treatment of A/D converter power supply pins

Connect the pins to have AVCC0 = AVCC1 = AVRH0 = AVRH1 = VCC,

AVSS0/AVRL0 = AVSS1/AVRL1 = VSS even if the A/D converter is not used.

■ Note on using external clock

The external clock is unsupported.

External direct clock input cannot use.

■ Power-on sequence of A/D converter power supply analog inputs

Be sure to turn on the digital power supply (VCC5) first, and then turn on the A/D converter power supplies (AVCC0, AVCC1, AVRH0, AVRH1, AVRL0, AVRL1) and analog inputs (AN0 to AN14, AN16 to AN23). Also, turn off the A/D converter power supplies (AVCC0, AVCC1, AVRH0, AVRH1, AVRL0, AVRL1) and analog inputs (AN0 to AN14, AN16 to AN23) first, and then turn off the digital power supply (VCC5). When the AVRH0 and AVRH1 pin voltages are turned on or off, they must not exceed AVCC0 and AVCC1. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVCC0 or AVCC1. (However, the analog power supply voltage and digital power supply voltage can be turned on or off simultaneously.)

■ Treatment of C pin

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

■ Function Switching of a Multiplexed Port

To switch between the port function and the multiplexed pin function, use the PFR (port function register). For details, see "I/O PORTS" in Hardware Manual.

■ Low-power Consumption Mode

To set Sleep mode / Watch mode / Stop mode, or Watch mode (power-off) / Stop mode (power-off), see the section "Launching Sleep mode / Watch mode / Stop mode" or "Launching Watch mode (power-off) / Stop mode (power-off)" of "POWER CONSUMPTION CONTROL" in Hardware Manual, and follow the procedures.

Do not perform the following when using a monitor debugger.

•Do not set a break point for the low-power consumption transition program.

•Do not execute an operation step for the low-power consumption transition program.

■ Notes When Writing Data in a Register Having the Status Flag

When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, take care not to clear its status flag erroneously.

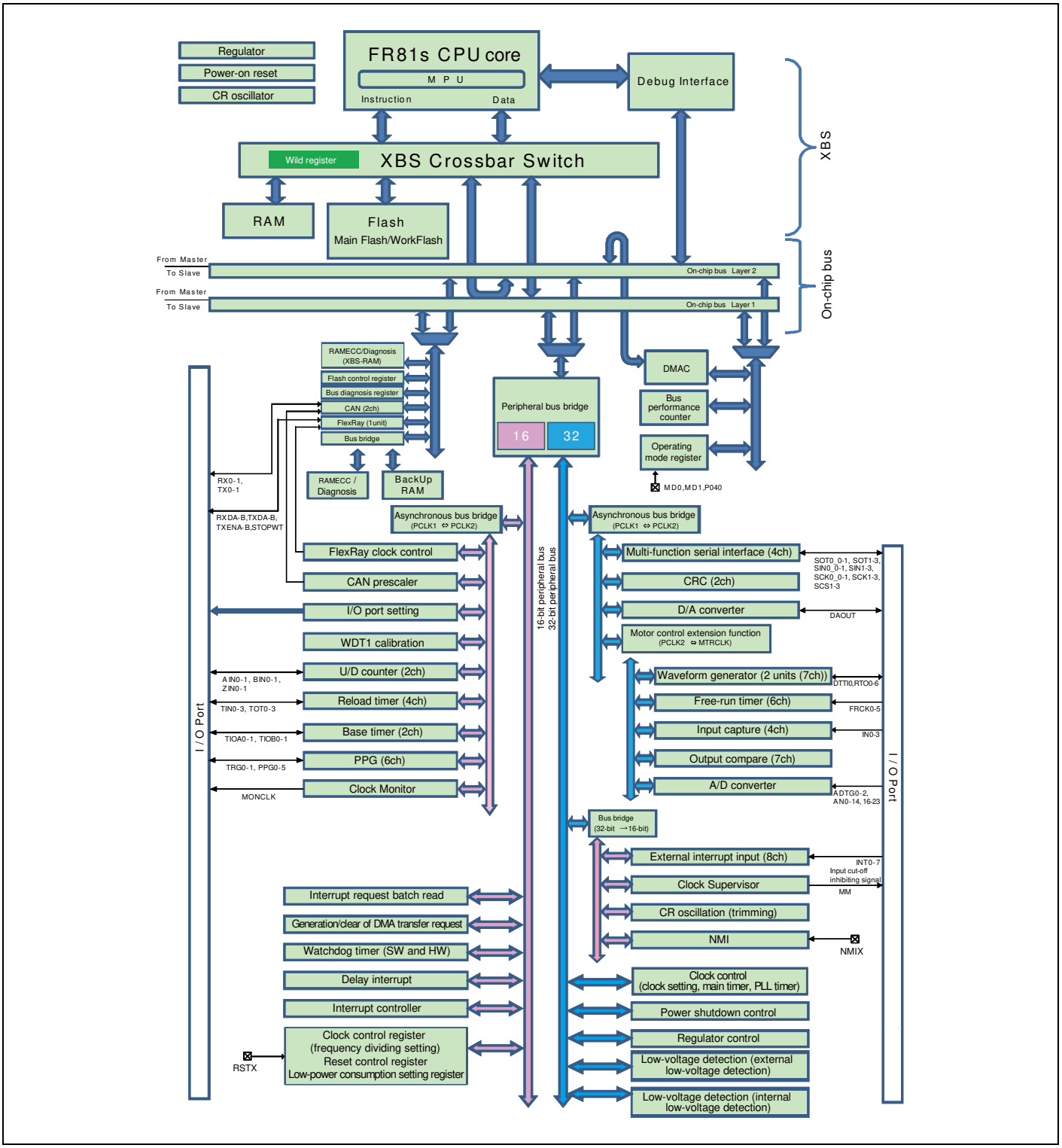
The program must be written not to clear the flag to the status bit, and to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) The Byte, Half-word, or Word access must be used to write data in the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

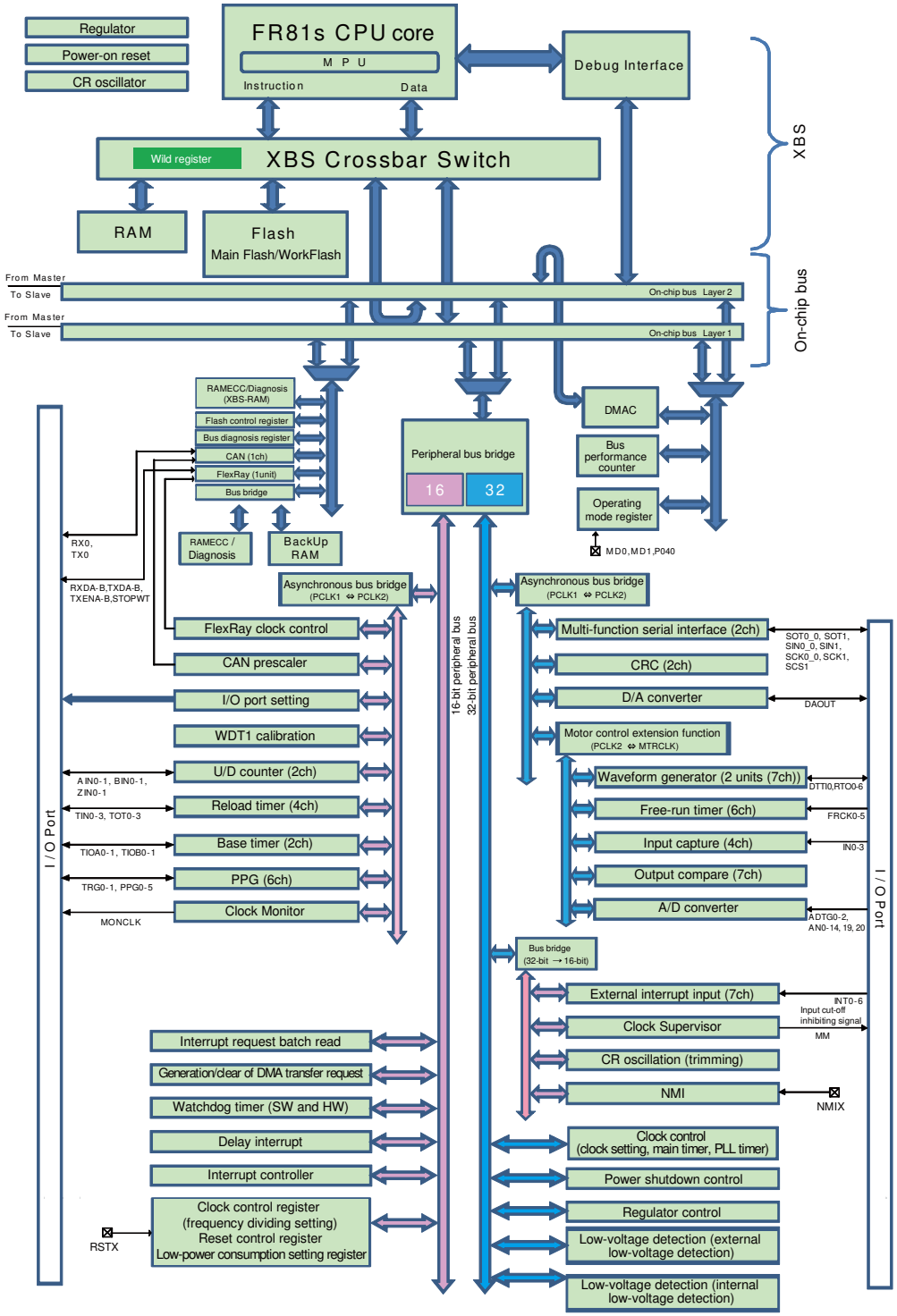
Note: These points can be ignored because the bit instructions already take the points into consideration for registers that support read-modify-write (RMW) operations. These points must be considered when using the bit instructions for registers that do not support RMW operations.

7. Block Diagram

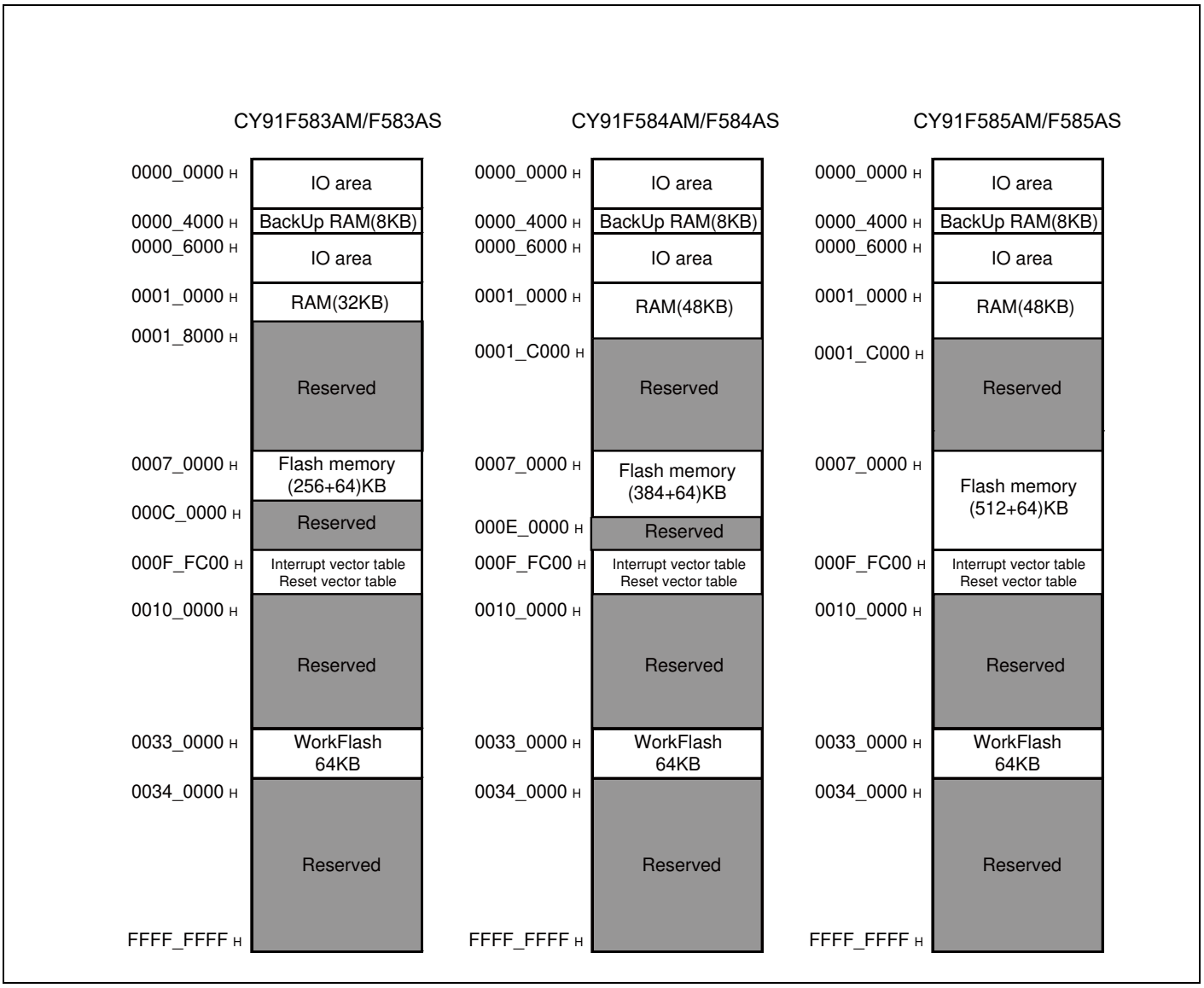
■ CY91F583AM/F584AM/F585AM



■ CY91F583AS/F584AS/F585AS



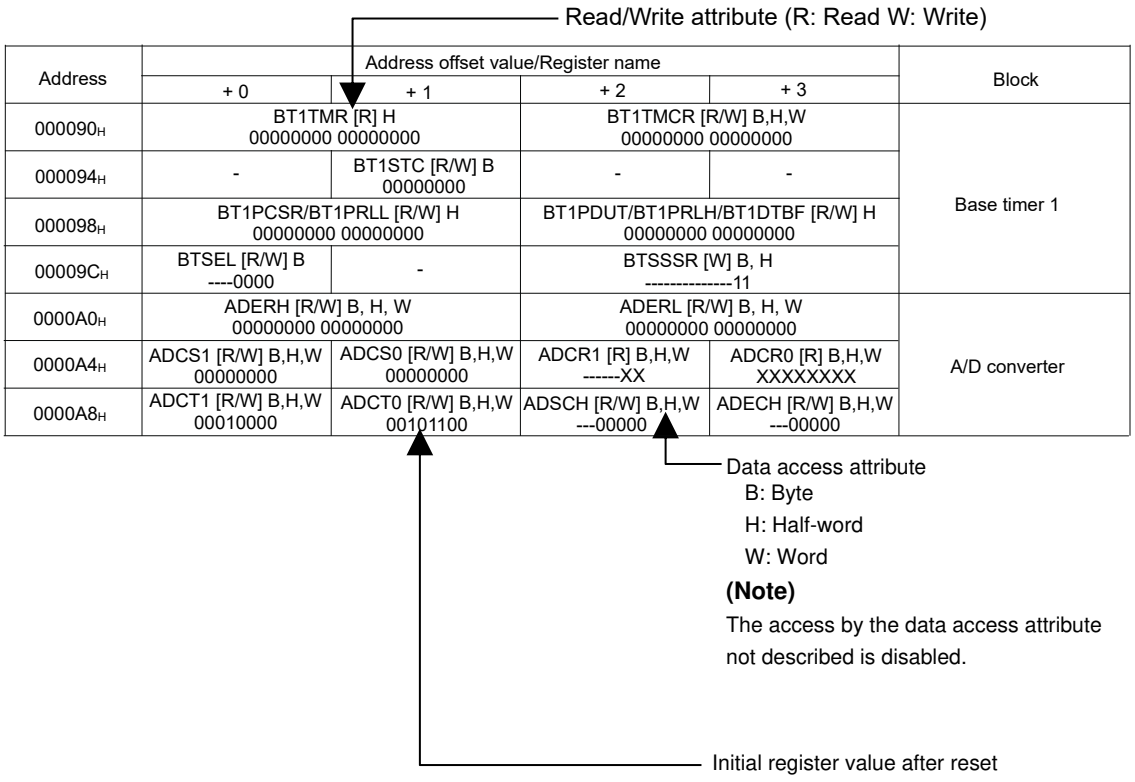
8. Memory Map


CY91F583AM/F583AS
0000_0000 H
IO area
0000_4000 H
BackUp RAM(8KB)
0000_6000 H
IO area
0001_0000 H
RAM(32KB)
0001_8000 H
Reserved
0007_0000 H
Flash memory (256+64)KB
000C_0000 H
Reserved
000F_FC00 H
Interrupt vector table
Reset vector table
0010_0000 H
Reserved
0033_0000 H
WorkFlash 64KB
0034_0000 H
Reserved
FFFF_FFFF H
CY91F584AM/F584AS
0000_0000 H
IO area
0000_4000 H
BackUp RAM(8KB)
0000_6000 H
IO area
0001_0000 H
RAM(48KB)
0001_C000 H
Reserved
0007_0000 H
Flash memory (384+64)KB
000E_0000 H
Reserved
000F_FC00 H
Interrupt vector table
Reset vector table
0010_0000 H
Reserved
0033_0000 H
WorkFlash 64KB
0034_0000 H
Reserved
FFFF_FFFF H
CY91F585AM/F585AS
0000_0000 H
IO area
0000_4000 H
BackUp RAM(8KB)
0000_6000 H
IO area
0001_0000 H
RAM(48KB)
0001_C000 H
Reserved
0007_0000 H
Flash memory (512+64)KB
000F_FC00 H
Interrupt vector table
Reset vector table
0010_0000 H
Reserved
0033_0000 H
WorkFlash 64KB
0034_0000 H
Reserved
FFFF_FFFF H

9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/Register name				Block
	+ 0	+ 1	+ 2	+ 3	
000090H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] B,H,W 00000000 00000000		Base timer 1
000094H	-	BT1STC [R/W] B 00000000	-	-	
000098H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009CH	BTSEL [R/W] B ----0000	-	BTSSSR [W] B, H ----------11		
0000A0H	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
0000A4H	ADCS1 [R/W] B,H,W 00000000	ADCS0 [R/W] B,H,W 00000000	ADCR1 [R] B,H,W ------XX	ADCR0 [R] B,H,W XXXXXXXX	
0000A8H	ADCT1 [R/W] B,H,W 00010000	ADCT0 [R/W] B,H,W 00101100	ADSCH [R/W] B,H,W ---00000	ADECH [R/W] B,H,W ---00000	

The initial register values after reset are indicated as follows:

"1": Initial value "1"

"0": Initial value "0"

"X": Initial value undefined

"-": Reserved bit/Undefined bit

"*": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

■ CY91F583AM/F584AM/F585AM

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W -XXXXXXX	PDR06[R/W] B,H,W -XXXXXXX	PDR07[R/W] B,H,W -----XXX	
000008_H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W -----XXX	-	
$00000C_H$	-	-	-	-	
000010_H | 000038_H	-	-	-	-	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	-	-	-		Reserved
000044_H	DICR[R/W] B -------0	-	-	-	Delay interrupt
000048_H | $00005C_H$	-		-		Reserved
000060_H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068_H | $00007C_H$	-	-	-	-	Reserved
000080_H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084_H	BT0TMCR2[R/W] B -------0	BT0STC[R/W] B -0-0-0-0	-	-	
000088_H	BT0PCSR/BT0PRLL[R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	-	-	-	-	
000090_H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094_H	BT1TMCR2[R/W] B -------0	BT1STC[R/W] B -0-0-0-0	-	-	
000098_H	BT1PCSR/BT1PRLL[R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		
$00009C_H$	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -------- ------11		Base timer 0,1
$0000A0_H$ | $0000FC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000100_H	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104_H	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108_H	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
$00010C_H$	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114_H	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118_H | $00011C_H$	-	-	-	-	Reserved
000120_H	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124_H	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W *5 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128_H	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
$00012C_H$	IRPR6H[R] B,H,W 0000----	IRPR6L[R] B,H,W 00------	IRPR7H[R] B,H,W 00------	IRPR7L[R] B,H,W --------	
000130_H	IRPR8H[R] B,H,W --------	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134_H	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138_H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 0000000-	IRPR13L[R] B,H,W 00000000	
$00013C_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 0000----	
000140_H	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W 00------	IRPR17H[R] B,H,W 00------	IRPR17L[R]B,H,W --------	
000144_H	IRPR18H[R] B,H,W --------	IRPR18L[R] B,H,W 000000--	-	-	
000148_H | $0001FC_H$	-	-	-	-	Reserved
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00020C$_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210$_H$	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214$_H$	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		
000218$_H$	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
00021C$_H$	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		
000220$_H$	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		PPG4
000224$_H$	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		
000228$_H$	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		PPG5
00022C$_H$	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		
000230$_H$ | 0002BC$_H$	-		-		Reserved
0002C0$_H$	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
0002C4$_H$	GTRS2[R/W] B,H,W -0000000 -0000000		-		
0002C8$_H$	-		-		
0002CC$_H$	-		-		
0002D0$_H$	-		-		
0002D4$_H$	-		-		
0002D8$_H$	GTREN0[R/W] H,W -------- --000000		-		
0002DC$_H$	-		-		Reserved
0002E0$_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
0002E4$_H$	-	GATEC4[R/W] B,H,W ------00	-	-	
0002E8$_H$	-	-	-	-	
0002EC$_H$	-	-	-	-	Reserved
0002F0$_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
0002F4$_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
0002F8$_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
0002FC$_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003CC_H$	-	-	-	-	Reserved [S]
$0003D0_H$	-				Reserved [S]
$0003D4_H$	-				
$0003D8_H$	-				
$0003DC_H$	-				
$0003E0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clear of DMA transfer request
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W ------00	ICSEL11[R/W] B,H,W -------0	
$00040C_H$	ICSEL12[R/W] B,H,W -------0	ICSEL13[R/W] B,H,W -------0	ICSEL14[R/W] B,H,W -------0	ICSEL15[R/W] B,H,W -------0	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	Generation and clear of DMA transfer request
000414_H	ICSEL20[R/W] B,H,W -------0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	
000418_H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -------0	ICSEL27[R/W] B,H,W -------0	
$00041C_H$	-	-	-	-	
000420_H	-	-	-	-	
000424_H | $00043C_H$	-	-	-	-	Reserved
000440_H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444_H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448_H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
$00044C_H$	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450_H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454_H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458_H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
$00045C_H$	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460_H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464_H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468_H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
$00046C_H$	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470_H | $00047C_H$	-	-	-	-	Reserved [S]
000480_H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W 000---11*	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484_H	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000488_H	DIVR0[R/W] B,H,W 000-----	-	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
$00048C_H$	-	-	-	-	Reserved [S]
000490_H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498_H	-	-	-	-	
$00049C_H$	-	-	-	-	
$0004A0_H$	-	-	-	-	Reserved
$0004A4_H$	CANPRE[R/W] B,H,W ---00000	-	-	-	CAN prescaler
$0004A8_H$ | $0004AC_H$	-	-	-	-	Reserved
$0004B0_H$	-	-	-	-	Reserved
$0004B4_H$ | $0004C0_H$	-	-	-	-	Reserved
$0004C4_H$	CUCR1[R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
$0004C8_H$	CUTR1[R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ | $0004DC_H$	-	-	-	-	Reserved
$0004E0_H$	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
$0004E4_H$	-	-	-	-	
$0004E8_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control [*5]
$0004EC_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
$0004F0_H$ | $0004FC_H$	-	-	-	-	Reserved
000500_H	-				Reserved
000504_H	-				Reserved
000508_H | $00050C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000510_H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514_H	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00------	
000518_H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
$00051C_H$	-		-	-	Reserved [S]
000520_H	CCPSSELR[R/W] B,H,W -------0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524_H	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528_H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] B,H,W 000----- --------		
$00052C_H$	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530_H	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534_H	-	-	-	-	
000538_H	-	-	-	-	
$00053C_H$	-	-	-	-	
000540_H | $00054C_H$	-	-	-	-	Reserved
000550_H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt (INT0 to 7)
000554_H | 000568_H	-	-	-	-	Reserved
$00056C_H$	-	CSVCR[R/W] B -0--1--0	-	-	CSV
000570_H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574_H | $00057C_H$	-	-	-	-	Reserved
000580_H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control
000584_H	LVD5R[R/W] B,H,W -------1	LVD5F[R/W] B,H,W 001100-1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H | $00060C_H$	-	-	-	-	Reserved [S]
000610_H | $00063C_H$	-	-	-	-	Reserved [S]
000640_H | $00064C_H$	-	-	-	-	Reserved [S]
000650_H | $00067C_H$	-	-	-	-	Reserved [S]
000680_H | $00068C_H$	-	-	-	-	Reserved [S]
000690_H | $0006BC_H$	-	-	-	-	Reserved [S]
$0006C0_H$ | $0006CC_H$	-	-	-	-	Reserved [S]
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720_H | $0007F8_H$	-	-	-	-	Reserved
$0007FC_H$	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800_H | $00083C_H$	-	-	-	-	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844_H	-	-	-	-	Reserved [S]
000848_H | 000854_H	-	-	-	-	Reserved [S]
000858_H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ | $00087C_H$	-	-	-	-	Reserved [S]
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0008A4_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
$0008A8_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008F4_H$	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F8_H$	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008FC_H$	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000900_H | $000BF8_H$	-	-	-	-	Reserved
$000BFC_H$	-		UER[W] B,H,W -------- -------X		OCDU
$000C00_H$	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
$000C04_H$	DCSR0[R/W] H 0------- -----000		DTCR0[R/W] H 00000000 00000000		
$000C08_H$	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1[R/W] H 0------- -----000		DTCR1[R/W] H 00000000 00000000		
$000C18_H$	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2[R/W] H 0------- -----000		DTCR2[R/W] H 00000000 00000000		
$000C28_H$	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
$000C38_H$	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		
$000C48_H$	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ | $000DF0_H$	-	-	-	-	
$000DF4_H$	-	-	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	-	-	-	-	Reserved [S]
$000E00_H$	DDR00[R/W] B,H 00000000	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H 00000000	DDR05[R/W] B,H -0000000	DDR06[R/W] B,H -0000000	DDR07[R/W] B,H -----000	
$000E08_H$	DDR08[R/W] B,H 00000000	DDR09[R/W] B,H 00000000	DDR10[R/W] B,H -----000	-	
$000E0C_H$	-	-	-	-	
$000E10_H$ | $000E1C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E20_H$	PFR00[R/W] B,H 00000000	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H 00000000	PFR05[R/W] B,H -0000000	PFR06[R/W] B,H -0000000	PFR07[R/W] B,H -----000	
$000E28_H$	PFR08[R/W] B,H 00000000	PFR09[R/W] B,H 00000000	PFR10[R/W] B,H -----000	-	
$000E2C_H$	-	-	-	-	
$000E30_H$ | $000E3C_H$	-	-	-	-	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W -XXXXXXX	PDDR06[R] B,H,W -XXXXXXX	PDDR07[R] B,H,W -----XXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W -----XXX	-	
$000E4C_H$	-	-	-	-	
$000E50_H$ | $000E5C_H$	-	-	-	-	Reserved
$000E60_H$	EPFR00[R/W] B,H ------00	EPFR01[R/W] B,H ---00000	EPFR02[R/W] B,H --000000	EPFR03[R/W] B,H --000000	Extended port function register
$000E64_H$	-	-	EPFR06[R/W] B,H ------00	EPFR07[R/W] B,H ----0000	
$000E68_H$	EPFR08[R/W] B,H [*5] ----0000	EPFR09[R/W] B,H -------0	EPFR10[R/W] B,H -0000000	-	
$000E6C_H$	-	-	EPFR14[R/W] B,H --0-0-0-	-	
$000E70_H$	-	-	-	-	
$000E74_H$	-	-	-	-	
$000E78_H$	-	-	-	-	
$000E7C_H$	-	-	-	-	
$000E80_H$	-	-	-	-	
$000E84_H$ | $000EBC_H$	-	-	-	-	Reserved
$000EC0_H$	PPER00[R/W] B,H 00000000	PPER01[R/W] B,H 00000000	PPER02[R/W] B,H 00000000	PPER03[R/W] B,H 00000000	Port pull-up/down enable register
$000EC4_H$	PPER04[R/W] B,H 00000000	PPER05[R/W] B,H -0000000	PPER06[R/W] B,H -0000000	PPER07[R/W] B,H -----000	
$000EC8_H$	PPER08[R/W] B,H 00000000	PPER09[R/W] B,H 00000000	PPER10[R/W] B,H -----000	-	
$000ECC_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000ED0_H$ | $000EDC_H$	-	-	-	-	Reserved
$000EE0_H$	PILR00[R/W] B,H 11111111	PILR01[R/W] B,H 11111111	PILR02[R/W] B,H 11111111	PILR03[R/W] B,H 11111111	Port input level selection register
$000EE4_H$	PILR04[R/W] B,H 11111111	PILR05[R/W] B,H -1111111	PILR06[R/W] B,H -1111111	PILR07[R/W] B,H -----111	
$000EE8_H$	PILR08[R/W] B,H 11111111	PILR09[R/W] B,H 11111111	PILR10[R/W] B,H -----111	-	
$000EEC_H$	-	-	-	-	
$000EF0_H$ | $000EFC_H$	-	-	-	-	Reserved
$000F00_H$ | $000F1C_H$	-	-	-	-	Reserved
$000F20_H$	PODR00[R/W] B,H 00000000	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
$000F24_H$	PODR04[R/W] B,H 00000000	PODR05[R/W] B,H -0000000	PODR06[R/W] B,H -0000000	PODR07[R/W] B,H -----000	
$000F28_H$	PODR08[R/W] B,H 00000000	PODR09[R/W] B,H 00000000	PODR10[R/W] B,H -----000	-	
$000F2C_H$	-	-	-	-	
$000F30_H$ | $000F3C_H$	-	-	-	-	Reserved
$000F40_H$	PORTEN[R/W] B,H,W ------00	-	-	-	Port input enable register
$000F44_H$	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
$000F48_H$	ADERH[R/W] B,H -------- 11111111		ADERL[R/W] B,H -1111111 11111111		Analog input enable register
$000F4C_H$	DAER[R/W] B,H -------0	-	-	-	Analog output enable register
$000F50_H$ | $000FFC_H$	-	-	-	-	Reserved
001000_H	SACR[R/W] B,H,W -------0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asynchronous switch control
001004_H | $0010BC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0010C0H	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation 0
0010C4H	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010C8H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010CCH	CRCR[R] B,H,W 11111111 11111111 11111111 11111111				
0010D0H	-	-	-	CRCCR1[R/W] B,H,W -0000000	CRC arithmetic operation 1
0010D4H	CRCINIT1[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010D8H	CRCIN1[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010DCH	CRCR1[R] B,H,W 11111111 11111111 11111111 11111111				
0010E0H | 0010FCH	-	-	-	-	Reserved
001100H	TCGS[R/W] B,H,W ------00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104H	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108H	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 --------				
00110CH	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 --------				
001114H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 --------				
00111CH	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 --------				
001124H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 --------				
00112CH	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 --------				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001134_H	FRS0[R/W] B,H,W -------- -000-000 -000-000 -000-000				Free-run timer selection
001138_H	FRS1[R/W] B,H,W -------- -------- -000-000 -000-000				
$00113C_H$	FRS2[R/W] B,H,W -------- -000-000 -000-000 -000-000				
001140_H	-				
001144_H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148_H	FRS5[R/W] B,H,W -----000 -000-000 -000-000 -000-000				
$00114C_H$	FRS6[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001150_H	-				
001154_H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158_H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W ------00	
$00115C_H$	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160_H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W ------00	
001164_H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168_H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W ------00	
$00116C_H$	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170_H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W ------00	
001174_H	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178_H	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W ------00	
$00117C_H$	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180_H	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W ------00	
001184_H	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188_H	ICS01[R/W] B,H,W ------00 00000000		-	LSYNS[R/W] B,H,W ----0000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00118C$_H$	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190$_H$	ICS23[R/W] B,H,W ------00 00000000		-	-	
001194$_H$	-		-		Reserved
001198$_H$	-		-	-	
00119C$_H$	-		-		Reserved
0011A0$_H$	-		-	-	
0011A4$_H$	DTSR[R/W] B,H,W ------10	-	-	-	DTTI selection
0011A8$_H$	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0011AC$_H$	TMRR2[R/W] H,W 00000000 00000001		-	-	
0011B0$_H$	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
0011B4$_H$	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
0011B8$_H$	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
0011BC$_H$	PICS0[R/W] B,H,W 000000-- -------- -------- --------				
0011C0$_H$	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
0011C4$_H$	TMRR5[R/W] H,W 00000000 00000001		-	-	
0011C8$_H$	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
0011CC$_H$	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00---000	Waveform generator 3/4/5
0011D0$_H$	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W -------1	
0011D4$_H$	-				
0011D8$_H$	-	-	-	-	12-bit A/D converter
0011DC$_H$	ADTSS[R/W] B,H,W -------0	-	-	-	
0011E0$_H$	ADTSE[R/W] B,H,W -------- 00000000 -0000000 00000000				
0011E4$_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
0011E8$_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
0011EC$_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
0011F0$_H$	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0011F4$_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		12-bit A/D converter
0011F8$_H$	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
0011FC$_H$	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001200$_H$	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		-		
001204$_H$	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001208$_H$	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
00120C$_H$	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001210$_H$	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
001214$_H$	-	-	-	-	
001218$_H$	-	-	-	-	
00121C$_H$	-	-	-	-	
001220$_H$	-	-	-	-	
001224$_H$	ADTCS0[R/W] B,H,W 00000000 0010-000		ADTCS1[R/W] B,H,W 00000000 0010-000		
001228$_H$	ADTCS2[R/W] B,H,W 00000000 0010-000		ADTCS3[R/W] B,H,W 00000000 0010-000		
00122C$_H$	ADTCS4[R/W] B,H,W 00000000 0010-000		ADTCS5[R/W] B,H,W 00000000 0010-000		
001230$_H$	ADTCS6[R/W] B,H,W 00000000 0010-000		ADTCS7[R/W] B,H,W 00000000 0010-000		
001234$_H$	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		
001238$_H$	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
00123C$_H$	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240$_H$	ADTCS14[R/W] B,H,W 00000000 0010-000		-		
001244$_H$	ADTCS16[R/W] B,H,W 00000000 00100000		ADTCS17[R/W] B,H,W 00000000 00100000		
001248$_H$	ADTCS18[R/W] B,H,W 00000000 00100000		ADTCS19[R/W] B,H,W 00000000 00100000		
00124C$_H$	ADTCS20[R/W] B,H,W 00000000 00100000		ADTCS21[R/W] B,H,W 00000000 00100000		
001250$_H$	ADTCS22[R/W] B,H,W 00000000 00100000		ADTCS23[R/W] B,H,W 00000000 00100000		
001254$_H$	-	-	-	-	
001258$_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00125C$_H$	-	-	-	-	12-bit A/D converter
001260$_H$	-	-	-	-	
001264$_H$	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268$_H$	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
00126C$_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270$_H$	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274$_H$	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278$_H$	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
00127C$_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280$_H$	ADTCD14[R] B,H,W 10--0000 00000000		-		
001284$_H$	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
001288$_H$	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
00128C$_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
001290$_H$	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
001294$_H$	-	-	-	-	
001298$_H$	-	-	-	-	
00129C$_H$	-	-	-	-	
0012A0$_H$	-	-	-	-	
0012A4$_H$	ADCS0[R/W] B,H,W 0------- --------		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	
0012A8$_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	
0012AC$_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
0012B0$_H$	MTRCSR[R/W] B,H,W -------0	-	-	-	Motor control extension function
0012B4$_H$	RTOSEL0[R/W] B,H,W --000000	RTOSEL1[R/W] B,H,W -------0	-	-	
0012B8$_H$ | 0012FC$_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001300_H	-	-	-	-	Reserved
001304_H	-	-	-	-	
001308_H	-	-	-	-	
$00130C_H$	-	-	-	-	
001310_H	-	-	-	-	
001314_H	-	-	-	-	
001318_H	-	-	-	-	
$00131C_H$	-	-	-	-	
001320_H	-	-	-	-	
001324_H	-		-		
001328_H | $00132C_H$	-	-	-	-	Reserved
001330_H	-		-		
001334_H | $0013FC_H$	-	-	-	-	Reserved
001400_H	DACR[R/W] B,H,W -------0	-	DADR[R/W] H,W ------XX XXXXXXXX		DAC
001404_H | $0014FC_H$	-	-	-	-	Reserved
001500_H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000000-0	SSR0[R/W] B,H,W 0--00011	ESCR0/(IBSR0) [R/W] B,H,W 00000000	Multi Function Serial I/F 0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001504_H	-/(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001508_H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
$00150C_H$	STMCR0[R/W] B,H,W 00000000 00000000		-/(SFUR0) [R/W] B,H,W -------- -------- *4		
001510_H	-	-	-/(SFLR10) [R/W] B,H,W -------- *4	-/(SFLR00) [R/W] B,H,W -------- *4	
001514_H	-	-	-	-	
001518_H	-	-	-	-	
$00151C_H$	BGR0[R/W] H,W 00000000 00000000		-/(ISMK0)[R/W] B,H,W -------- *2	-/(ISBA0)[R/W] B,H,W -------- *2	
001520_H	FCR10[R/W] B,H,W 00-00100	FCR00[R/W] B,H,W -0000000	FBYTE20[R/W] B,H,W 00000000	FBYTE10[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001524_H	SCR1[R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1[R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528_H	-/(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
$00152C_H$	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530_H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W -------- -------- *3 *4		
001534_H	-/(SCSTR31) [R/W] B,H,W -------- *3	-/(SCSTR21) [R/W] B,H,W -------- *3	-/(SCSTR11/ SFLR11) [R/W] B,H,W -------- *3 *4	-/(SCSTR01/ SFLR01) [R/W] B,H,W -------- *3 *4	
001538_H	-	-	-	-	
$00153C_H$	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540_H	BGR1[R/W] H,W 00000000 00000000		-	-	
001544_H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
001548_H	SCR2/(IBCR2) [R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000000-0	SSR2[R/W] B,H,W 0--00011	ESCR2/(IBSR2) [R/W] B,H,W 00000000	Multi Function Serial I/F 2 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
$00154C_H$	-/(RDR12/(TDR12))[R/W] B,H,W -------- -------- *3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1		
001550_H	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
001554_H	STMCR2[R/W] B,H,W 00000000 00000000		-/(SCSCR2/SFUR2) [R/W] B,H,W -------- -------- *3 *4		
001558_H	-/(SCSTR32) [R/W] B,H,W -------- *3	-/(SCSTR22) [R/W] B,H,W -------- *3	-/(SCSTR12/ SFLR12) [R/W] B,H,W -------- *3 *4	-/(SCSTR02/ SFLR02) [R/W] B,H,W -------- *3 *4	
$00155C_H$	-	-	-	-	
001560_H	-	-	-	TBYTE02[R/W] B,H,W 00000000	
001564_H	BGR2[R/W] H,W 00000000 00000000		-/(ISMK2)[R/W] B,H,W -------- *2	-/(ISBA2)[R/W] B,H,W -------- *2	
001568_H	FCR12[R/W] B,H,W 00-00100	FCR02[R/W] B,H,W -0000000	FBYTE22[R/W] B,H,W 00000000	FBYTE12[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00156C$_H$	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000000-0	SSR3[R/W] B,H,W 0--00011	ESCR3/(IBSR3) [R/W] B,H,W 00000000	Multi Function Serial I/F 3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001570$_H$	-/(RDR13/(TDR13))[R/W] B,H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
001574$_H$	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
001578$_H$	STMCR3[R/W] B,H,W 00000000 00000000		-/(SCSCR3/SFUR3) [R/W] B,H,W -------- -------- *3 *4		
00157C$_H$	-/(SCSTR33) [R/W] B,H,W -------- *3	-/(SCSTR23) [R/W] B,H,W -------- *3	-/(SCSTR13/ SFLR13) [R/W] B,H,W -------- *3 *4	-/(SCSTR03/ SFLR03) [R/W] B,H,W -------- *3 *4	
001580$_H$	-	-	-	-	
001584$_H$	-	-	-	TBYTE03[R/W] B,H,W 00000000	
001588$_H$	BGR3[R/W] H,W 00000000 00000000		-/(ISMK3)[R/W] B,H,W -------- *2	-/(ISBA3)[R/W] B,H,W -------- *2	
00158C$_H$	FCR13[R/W] B,H,W 00-00100	FCR03[R/W] B,H,W -0000000	FBYTE23[R/W] B,H,W 00000000	FBYTE13[R/W] B,H,W 00000000	
001590$_H$ | 001FFC$_H$	-	-	-	-	Reserved
002000$_H$	CTRLR0[R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN 0 64msb
002004$_H$	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008$_H$	INTR0[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
00200C$_H$	BRPER0[R/W] B,H,W -------- ----0000		-		
002010$_H$	IF1CREQ0[R/W] B,H,W 0------- 00000001		IF1CMSK0[R/W] B,H,W -------- 00000000		
002014$_H$	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018$_H$	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
00201C$_H$	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020$_H$	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024$_H$	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002028_{H,}$ $00202C_{H}$	-		-		CAN 0 64msb
$002030_{H,}$ 002034_{H}	Reserved (IF1 data mirror)				
$002038_{H,}$ $00203C_{H}$	-		-		
002040_{H}	IF2CREQ0[R/W] B,H,W 0------- 00000001		IF2CMSK0[R/W] B,H,W -------- 00000000		
002044_{H}	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048_{H}	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_{H}$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_{H}	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_{H}	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
$002058_{H,}$ $00205C_{H}$	-		-		
$002060_{H,}$ 002064_{H}	Reserved (IF2 data mirror)				
002068_{H} | $00207C_{H}$	-		-		
002080_{H}	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_{H}	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_{H}	-		-		
$00208C_{H}$	-		-		
002090_{H}	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_{H}	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098_{H}	-		-		
$00209C_{H}$	-		-		
$0020A0_{H}$	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
$0020A4_{H}$	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
$0020A8_{H}$	-		-		
$0020AC_{H}$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0020B0_H$	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		CAN 0 64msb
$0020B4_H$	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
$0020B8_H$	-		-		
$0020BC_H$	-		-		
$0020C0_H$ | $0020FC_H$	-		-		
002100_H	CTRLR1[R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN 1 64msb
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108_H	INTR1[R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1[R/W] B,H,W -------- ----0000		-		
002110_H	IF1CREQ1[R/W] B,H,W 0------- 00000001		IF1CMSK1[R/W] B,H,W -------- 00000000		
002114_H	IF1MSK21[R/W] B,H,W 11-11111 11111111		IF1MSK11[R/W] B,H,W 11111111 11111111		
002118_H	IF1ARB21[R/W] B,H,W 00000000 00000000		IF1ARB11[R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1[R/W] B,H,W 00000000 0---0000		-		
002120_H	IF1DTA11[R/W] B,H,W 00000000 00000000		IF1DTA21[R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11[R/W] B,H,W 00000000 00000000		IF1DTB21[R/W] B,H,W 00000000 00000000		
002128_H, $00212C_H$	-		-		
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H, $00213C_H$	-		-		
002140_H	IF2CREQ1[R/W] B,H,W 0------- 00000001		IF2CMSK1[R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21[R/W] B,H,W 11-11111 11111111		IF2MSK11[R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21[R/W] B,H,W 00000000 00000000		IF2ARB11[R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1[R/W] B,H,W 00000000 0---0000		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002150_H	IF2DTA11[R/W] B,H,W 00000000 00000000		IF2DTA21[R/W] B,H,W 00000000 00000000		CAN 1 64msb
002154_H	IF2DTB11[R/W] B,H,W 00000000 00000000		IF2DTB21[R/W] B,H,W 00000000 00000000		
002158_H, $00215C_H$	-		-		
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H | $00217C_H$	-		-		
002180_H	TREQR21[R] B,H,W 00000000 00000000		TREQR11[R] B,H,W 00000000 00000000		
002184_H	TREQR41[R] B,H,W 00000000 00000000		TREQR31[R] B,H,W 00000000 00000000		
002188_H	-		-		
$00218C_H$	-		-		
002190_H	NEWDT21[R] B,H,W 00000000 00000000		NEWDT11[R] B,H,W 00000000 00000000		
002194_H	NEWDT41[R] B,H,W 00000000 00000000		NEWDT31[R] B,H,W 00000000 00000000		
002198_H	-		-		
$00219C_H$	-		-		
$0021A0_H$	INTPND21[R] B,H,W 00000000 00000000		INTPND11[R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41[R] B,H,W 00000000 00000000		INTPND31[R] B,H,W 00000000 00000000		
$0021A8_H$	-		-		
$0021AC_H$	-		-		
$0021B0_H$	MSGVAL21[R] B,H,W 00000000 00000000		MSGVAL11[R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		
$0021B8_H$	-		-		
$0021BC_H$	-		-		
$0021C0_H$ | $0021FC_H$	-		-		
002200_H | $0022FC_H$	-		-		Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002300_H	DFCTLR[R/W] B,H,W -0------ --------		-	DFSTR[R/W] B,H,W -----001	WorkFlash
002304_H	-	-	-	-	
002308_H	FLIFCTLR[R/W] B,H,W ---0--00	-	FLIFFER1[R/W] B,H,W --------	FLIFFER2[R/W] B,H,W --------	
$00230C_H$ | $002FFC_H$	-	-	-	-	Reserved
003000_H	SEEARX[R] B,H,W --000000 00000000		DEEARX[R] B,H,W --000000 00000000		XBS RAM ECC control register
003004_H	EECSRX[R/W] B,H,W ----00-0	-	EFEARX[R/W] B,H,W --000000 00000000		
003008_H	-	EFECRX[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- --000000 00000000				XBS RAM diagnosis register
003010_H	TEAR1X[R] B,H,W 000----- -------- --000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- --000000 00000000				
003018_H	TAEARX[R/W] B,H,W --101111 11111111		TASARX[R/W] B,H,W --000000 00000000		
$00301C_H$	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W ------00 00001100		
003020_H	TSRCRX[R/W] B,H,W 0-------	-	-	TKCCRX[R/W] B,H,W 00----00	
003024_H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028_H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
$00302C_H$	-	EFECRA[R/W] B,H,W -------0 00000000 00000000			
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				Backup RAM diagnosis register
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W ------00 00001100		
003044_H	TSRCRA[R/W] B,H,W 0-------	-	-	TKCCRA[R/W] B,H,W 00----00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003048_H | $0030FC_H$	-	-	-	-	Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				Bus diagnosis
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF [*5]
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF [*5]
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT *5
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ | $00D07C_H$	-	-	-	-	Reserved
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC *5
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM *5
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT *5
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 --001110				
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD *5
$00D09C_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU *5
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 --000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				
$00D0CC_H$ | $00D0FC_H$	-				Reserved
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC *5
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$ $00D10C_H$	-				Reserved
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU *5
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W -------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				FlexRay GTU [*5]
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	-				
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				FlexRay GTU [*5]
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM [*5]
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD [*5]
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				FlexRay MHD [*5]
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				
$00D33C_H$	NDAT4[R] W 00000000 00000000 00000000 00000000				
$00D340_H$	MBSC1[R] W 00000000 00000000 00000000 00000000				
$00D344_H$	MBSC2[R] W 00000000 00000000 00000000 00000000				
$00D348_H$	MBSC3[R] W 00000000 00000000 00000000 00000000				
$00D34C_H$	MBSC4[R] W 00000000 00000000 00000000 00000000				
$00D350_H$ | $00D3EC_H$	-				Reserved
$00D3F0_H$	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF [*5]
$00D3F4_H$	ENDN[R] W 10000111 01100101 01000011 00100001				
$00D3F8_H$ | $00D3FC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D400_H$ | $00D4FC_H$	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF *5
$00D500_H$	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
$00D504_H$	WRHS2[R/W] W -------- -0000000 -----000 00000000				
$00D508_H$	WRHS3[R/W] W -------- -------- -----000 00000000				
$00D50C_H$	-				
$00D510_H$	IBCM[R/W] W -------- ------00 -------- -----000				
$00D514_H$	IBCR[R/W] W 0------- -0000000 0------- -0000000				
$00D518_H$ | $00D5FC_H$	-				Reserved
$00D600_H$ | $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF *5
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ | $00D7FC_H$	-				Reserved
$00D800_H$ | $00EFFC_H$	-				Reserved
$00F000_H$ | $00FEFC_H$	-				Reserved [S]
$00FF00_H$	DSUCR[R/W] B,H,W -------- -------0		-	-	OCDU [S]
$00FF04_H$ | $00FF0C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00FF10_H$	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ | $00FFF4_H$	-	-	-	-	Reserved [S]
$00FFF8_H$	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

*5: For FlexRay, the CY91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ has corresponding functions. The following registers are reserved registers for models without the FlexRay function.
000125_H IRPR2L[5:4], $000E68_H$, $0004E8_H$-$0004EF_H$, $00D000_H$-$00D717_H$

■ I/O Map (CY91F583AS/F584AS/F585AS)

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000_H	-	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W -XXXXXXX	-	PDR07[R/W] B,H,W -----XXX	
000008_H	-	PDR09[R/W] B,H,W ---XX---	-	-	
$00000C_H$	-	-	-	-	
000010_H | 000038_H	-	-	-	-	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	-	-	-		Reserved
000044_H	DICR[R/W] B -------0	-	-	-	Delay interrupt
000048_H | $00005C_H$	-		-		Reserved
000060_H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068_H | $00007C_H$	-	-	-	-	Reserved
000080_H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	-	-	
000088_H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	-	-	-	-	
000090_H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094_H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	-	-	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -------- ------11		Base timer 0, 1

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0000A0$_H$ | 0000FC$_H$	-	-	-	-	Reserved
000100$_H$	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104$_H$	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108$_H$	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
00010C$_H$	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110$_H$	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114$_H$	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118$_H$ | 00011C$_H$	-	-	-	-	Reserved
000120$_H$	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124$_H$	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W [*5] 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128$_H$	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
00012C$_H$	IRPR6H[R] B,H,W 0000----	IRPR6L[R] B,H,W 00------	IRPR7H[R] B,H,W 00------	IRPR7L[R] B,H,W --------	
000130$_H$	IRPR8H[R] B,H,W --------	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134$_H$	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138$_H$	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 0000000-	IRPR13L[R] B,H,W ---00---	
00013C$_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 0000----	
000140 $_H$	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W --------	IRPR17H[R] B,H,W --------	IRPR17L[R] B,H,W --------	
000144 $_H$	IRPR18H[R]B,H,W --------	IRPR18L[R]B,H,W 000000--	-	-	
000148$_H$ | 0001FC$_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
$00020C_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210_H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214_H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		
000218_H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
$00021C_H$	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		
000220_H	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		PPG4
000224_H	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		
000228_H	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		PPG5
$00022C_H$	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		
000230_H | $0002BC_H$	-		-		Reserved
$0002C0_H$	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
$0002C4_H$	GTRS2[R/W] B,H,W -0000000 -0000000		-		
$0002C8_H$	-		-		
$0002CC_H$	-		-		
$0002D0_H$	-		-		
$0002D4_H$	-		-		
$0002D8_H$	GTREN0[R/W] H,W -------- --000000		-		
$0002DC_H$	-		-		Reserved
$0002E0_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
$0002E4_H$	-	GATEC4[R/W] B,H,W ------00	-	-	
$0002E8_H$	-	-	-	-	
$0002EC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002F0_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
$0002F4_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
$0002F8_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
$0002FC_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003CC_H$	-	-	-	-	Reserved [S]
$0003D0_H$	-				Reserved [S]
$0003D4_H$	-				
$0003D8_H$	-				
$0003DC_H$	-				
$0003E0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clear of DMA transfer request
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W ------00	ICSEL11[R/W] B,H,W -------0	
$00040C_H$	ICSEL12[R/W] B,H,W -------0	ICSEL13[R/W] B,H,W -------0	ICSEL14[R/W] B,H,W -------0	ICSEL15[R/W] B,H,W -------0	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	
000414_H	ICSEL20[R/W] B,H,W -------0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	
000418_H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -------0	ICSEL27[R/W] B,H,W -------0	
$00041C_H$	-	-	-	-	
000420_H	-	-	-	-	
000424_H | $00043C_H$	-	-	-	-	Reserved
000440_H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444_H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448_H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
$00044C_H$	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450_H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454_H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458_H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
$00045C_H$	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460_H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464_H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468_H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
$00046C_H$	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470_H | $00047C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000480$_H$	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W 000---11 *	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484$_H$	-	-	-	-	Reserved [S]
000488$_H$	DIVR0[R/W] B,H,W 000-----	-	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
00048C$_H$	-	-	-	-	Reserved [S]
000490$_H$	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494$_H$	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498$_H$	-	-	-	-	
00049C$_H$	-	-	-	-	
0004A0$_H$	-	-	-	-	Reserved
0004A4$_H$	CANPRE[R/W] B,H,W ---00000	-	-	-	CAN prescaler
0004A8$_H$ | 0004AC$_H$	-	-	-	-	Reserved
0004B0$_H$	-	-	-	-	Reserved
0004B4$_H$ | 0004C0$_H$	-	-	-	-	Reserved
0004C4$_H$	CUCR1[R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
0004C8$_H$	CUTR1[R] B,H,W -------- 00000000 00000000 00000000				
0004CC$_H$ | 0004DC$_H$	-	-	-	-	Reserved
0004E0$_H$	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
0004E4$_H$	-	-	-	-	
0004E8$_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control *5
0004EC$_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
0004F0$_H$ | 0004FC$_H$	-	-	-	-	Reserved
000500$_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000504_H	-				Reserved
000508_H | $00050C_H$	-	-	-	-	Reserved
000510_H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514_H	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00------	
000518_H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
$00051C_H$	-		-	-	Reserved [S]
000520_H	CCPSSELR[R/W] B,H,W -------0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524_H	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528_H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] B,H,W 000----- --------		
$00052C_H$	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530_H	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534_H	-	-	-	-	
000538_H	-	-	-	-	
$00053C_H$	-	-	-	-	
000540_H | $00054C_H$	-	-	-	-	Reserved
000550_H	EIRR0[R/W] B,H,W -XXXXXXX	ENIR0[R/W] B,H,W -0000000	ELVR0[R/W] B,H,W --000000 00000000		External interrupt (INT0 to 6)
000554_H | 000568_H	-	-	-	-	Reserved
$00056C_H$	-	CSVCR[R/W] B -0--1--0	-	-	CSV
000570_H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574_H | $00057C_H$	-	-	-	-	Reserved
000580_H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000584_H	LVD5R[R/W] B,H,W -------1	LVD5F[R/W] B,H,W 001100-1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H | $00060C_H$	-				Reserved [S]
000610_H | $00063C_H$	-	-	-	-	Reserved [S]
000640_H | $00064C_H$	-				Reserved [S]
000650_H | $00067C_H$	-	-	-	-	Reserved [S]
000680_H | $00068C_H$	-				Reserved [S]
000690_H | $0006BC_H$	-	-	-	-	Reserved [S]
$0006C0_H$ | $0006CC_H$	-				Reserved [S]
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000704_H | $00070C_H$	-	-	-	-	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720_H | $0007F8_H$	-	-	-	-	Reserved
$0007FC_H$	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800_H | $00083C_H$	-	-	-	-	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844_H	-	-	-	-	Reserved [S]
000848_H | 000854_H	-	-	-	-	Reserved [S]
000858_H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ | $00087C_H$	-	-	-	-	Reserved [S]
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0008A0$_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
0008A4$_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A8$_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008AC$_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0$_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008B4$_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8$_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008BC$_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0$_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008C4$_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8$_H$	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008CC$_H$	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0$_H$	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008D4$_H$	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8$_H$	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008DC$_H$	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0$_H$	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008E4$_H$	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8$_H$	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008EC$_H$	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0$_H$	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008F4$_H$	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8$_H$	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0008FC$_H$	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
000900$_H$ | 000BF8$_H$	-	-	-	-	Reserved
000BFC$_H$	-		UER[W] B,H,W -------- -------X		OCDU
000C00$_H$	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C04$_H$	DCSR0[R/W] H 0------- -----000		DTCR0[R/W] H 00000000 00000000		
000C08$_H$	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0C$_H$	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10$_H$	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
000C14$_H$	DCSR1[R/W] H 0------- -----000		DTCR1[R/W] H 00000000 00000000		
000C18$_H$	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1C$_H$	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20$_H$	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
000C24$_H$	DCSR2[R/W] H 0------- -----000		DTCR2[R/W] H 00000000 00000000		
000C28$_H$	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2C$_H$	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30$_H$	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
000C34$_H$	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
000C38$_H$	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3C$_H$	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40$_H$	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
000C44$_H$	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C48_H$	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
$000C4C_H$	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ | $000DF0_H$	-	-	-	-	
$000DF4_H$	-	-	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	-	-	-	-	Reserved [S]
$000E00_H$	-	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H 00000000	DDR05[R/W] B,H -0000000	-	DDR07[R/W] B,H -----000	
$000E08_H$	-	DDR09[R/W] B,H ---00---	-	-	
$000E0C_H$	-	-	-	-	
$000E10_H$ | $000E1C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E20_H$	-	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H 00000000	PFR05[R/W] B,H -0000000	-	PFR07[R/W] B,H -----000	
$000E28_H$	-	PFR09[R/W] B,H ---00---	-	-	
$000E2C_H$	-	-	-	-	
$000E30_H$ | $000E3C_H$	-	-	-	-	Reserved
$000E40_H$	-	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W -XXXXXXX	-	PDDR07[R] B,H,W -----XXX	
$000E48_H$	-	PDDR09[R] B,H,W ---XX---	-	-	
$000E4C_H$	-	-	-	-	
$000E50_H$ | $000E5C_H$	-	-	-	-	Reserved
$000E60_H$	EPFR00[R/W] B,H -------0	EPFR01[R/W] B,H ------00	EPFR02[R/W] B,H -----000	EPFR03[R/W] B,H --000000	Extended port function register
$000E64_H$	-	-	EPFR06[R/W] B,H ------00	EPFR07[R/W] B,H ----0000	
$000E68_H$	EPFR08[R/W] B,H [*5] ----0000	EPFR09[R/W] B,H -------0	EPFR10[R/W] B,H -0000000	-	
$000E6C_H$	-	-	-	-	
$000E70_H$	-	-	-	-	
$000E74_H$	-	-	-	-	
$000E78_H$	-	-	-	-	
$000E7C_H$	-	-	-	-	
$000E80_H$	-	-	-	-	
$000E84_H$ | $000EBC_H$	-	-	-	-	Reserved
$000EC0_H$	-	PPER01[R/W] B,H 00000000	PPER02[R/W] B,H 00000000	PPER03[R/W] B,H 00000000	Port pull-up/down enable register
$000EC4_H$	PPER04[R/W] B,H 00000000	PPER05[R/W] B,H -0000000	-	PPER07[R/W] B,H -----000	
$000EC8_H$	-	PPER09[R/W] B,H ---00---	-	-	
$000ECC_H$	-	-	-	-	
$000ED0_H$ | $000EDC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000EE0_H$	-	PILR01[R/W] B,H 11111111	PILR02[R/W] B,H 11111111	PILR03[R/W] B,H 11111111	Port input level selection register
$000EE4_H$	PILR04[R/W] B,H 11111111	PILR05[R/W] B,H -1111111	-	PILR07[R/W] B,H -----111	
$000EE8_H$	-	PILR09[R/W] B,H ---11---	-	-	
$000EEC_H$	-	-	-	-	
$000EF0_H$ | $000EFC_H$	-	-	-	-	Reserved
$000F00_H$ | $000F1C_H$	-	-	-	-	Reserved
$000F20_H$	-	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
$000F24_H$	PODR04[R/W] B,H 00000000	PODR05[R/W] B,H -0000000	-	PODR07[R/W] B,H -----000	
$000F28_H$	-	PODR09[R/W] B,H ---00---	-	-	
$000F2C_H$	-	-	-	-	
$000F30_H$ | $000F3C_H$	-	-	-	-	Reserved
$000F40_H$	PORTEN[R/W] B,H,W ------00	-	-	-	Port input enable register
$000F44_H$	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
$000F48_H$	ADERH[R/W] B,H -------- ---11---		ADERL[R/W] B,H -1111111 11111111		Analog input enable register
$000F4C_H$	DAER[R/W] B,H -------0	-	-	-	Analog output enable register
$000F50_H$ | $000FFC_H$	-	-	-	-	Reserved
001000_H	SACR[R/W] B,H,W -------0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asynchronous switch control
001004_H | $0010BC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0010C0$_H$	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation 0
0010C4$_H$	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010C8$_H$	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010CC$_H$	CRCR[R] B,H,W 11111111 11111111 11111111 11111111				
0010D0$_H$	-	-	-	CRCCR1[R/W] B,H,W -0000000	CRC arithmetic operation 1
0010D4$_H$	CRCINIT1[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010D8$_H$	CRCIN1[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010DC$_H$	CRCR1[R] B,H,W 11111111 11111111 11111111 11111111				
0010E0$_H$ | 0010FC$_H$	-	-	-	-	Reserved
001100$_H$	TCGS[R/W] B,H,W ------00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104$_H$	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108$_H$	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 --------				
00110C$_H$	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110$_H$	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 --------				
001114$_H$	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118$_H$	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 --------				
00111C$_H$	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120$_H$	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 --------				
001124$_H$	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128$_H$	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 --------				
00112C$_H$	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130$_H$	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 --------				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001134$_H$	FRS0[R/W] B,H,W -------- -000-000 -000-000 -000-000				Free-run timer selection
001138$_H$	FRS1[R/W] B,H,W -------- -------- -000-000 -000-000				
00113C$_H$	FRS2[R/W] B,H,W -------- -000-000 -000-000 -000-000				
001140$_H$	-				
001144$_H$	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148$_H$	FRS5[R/W] B,H,W -----000 -000-000 -000-000 -000-000				
00114C$_H$	FRS6[R/W] B,H,W -------- -----000 -000---- --------				
001150$_H$	-				
001154$_H$	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158$_H$	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W ------00	
00115C$_H$	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160$_H$	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W ------00	
001164$_H$	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168$_H$	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W ------00	
00116C$_H$	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170$_H$	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W ------00	
001174$_H$	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178$_H$	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W ------00	
00117C$_H$	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180$_H$	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W ------00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001184$_H$	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188$_H$	ICS01[R/W] B,H,W ------00 00000000		-	LSYNS[R/W] B,H,W ------00	
00118C$_H$	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190$_H$	ICS23[R/W] B,H,W ------00 00000000		-	-	
001194$_H$	-		-		Reserved
001198$_H$	-		-	-	
00119C$_H$	-		-		Reserved
0011A0$_H$	-		-	-	
0011A4$_H$	DTSR[R/W] B,H,W ------10	-	-	-	DTTI selection
0011A8$_H$	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0011AC$_H$	TMRR2[R/W] H,W 00000000 00000001		-	-	
0011B0$_H$	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
0011B4$_H$	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
0011B8$_H$	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
0011BC$_H$	PICS0[R/W] B,H,W 000000-- -------- -------- --------				
0011C0$_H$	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
0011C4$_H$	TMRR5[R/W] H,W 00000000 00000001		-	-	
0011C8$_H$	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
0011CC$_H$	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00---000	
0011D0$_H$	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W -------1	
0011D4$_H$	-				
0011D8$_H$	-	-	-	-	12-bit A/D converter
0011DC$_H$	ADTSS[R/W] B,H,W -------0	-	-	-	
0011E0$_H$	ADTSE[R/W] B,H,W -------- ---00--- -0000000 00000000				
0011E4$_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0011E8$_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		12-bit A/D converter
0011EC$_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
0011F0$_H$	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
0011F4$_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
0011F8$_H$	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
0011FC$_H$	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001200$_H$	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		-		
001204$_H$	-		-		
001208$_H$	-		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
00120C$_H$	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		-		
001210$_H$	-		-		
001214$_H$	-	-	-	-	
001218$_H$	-	-	-	-	
00121C$_H$	-	-	-	-	
001220$_H$	-	-	-	-	
001224$_H$	ADTCS0[R/W] B,H,W 00000000 0010-000		ADTCS1[R/W] B,H,W 00000000 0010-000		
001228$_H$	ADTCS2[R/W] B,H,W 00000000 0010-000		ADTCS3[R/W] B,H,W 00000000 0010-000		
00122C$_H$	ADTCS4[R/W] B,H,W 00000000 0010-000		ADTCS5[R/W] B,H,W 00000000 0010-000		
001230$_H$	ADTCS6[R/W] B,H,W 00000000 0010-000		ADTCS7[R/W] B,H,W 00000000 0010-000		
001234$_H$	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		
001238$_H$	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
00123C$_H$	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240$_H$	ADTCS14[R/W] B,H,W 00000000 0010-000		-		
001244$_H$	-		-		
001248$_H$	-		ADTCS19[R/W] B,H,W 00000000 00100000		
00124C$_H$	ADTCS20[R/W] B,H,W 00000000 00100000		-		
001250$_H$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001254_H	-	-	-	-	12-bit A/D converter
001258_H	-	-	-	-	
$00125C_H$	-	-	-	-	
001260_H	-	-	-	-	
001264_H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268_H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
$00126C_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274_H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278_H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$00127C_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280_H	ADTCD14[R] B,H,W 10--0000 00000000		-		
001284_H	-		-		
001288_H	-		ADTCD19[R] B,H,W 10--0000 00000000		
$00128C_H$	ADTCD20[R] B,H,W 10--0000 00000000		-		
001290_H	-		-		
001294_H	-	-	-	-	
001298_H	-	-	-	-	
$00129C_H$	-	-	-	-	
$0012A0_H$	-	-	-	-	
$0012A4_H$	ADCS0[R/W] B,H,W 0------- --------		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	
$0012A8_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	
$0012AC_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
$0012B0_H$	MTRCSR[R/W] B,H,W -------0	-	-	-	Motor control extension function
$0012B4_H$	RTOSEL0[R/W] B,H,W --000000	RTOSEL1[R/W] B,H,W -------0	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0012B8_H$ | $0012FC_H$	-	-	-	-	Reserved
001300_H	-	-	-	-	Reserved
001304_H	-	-	-	-	
001308_H	-	-	-	-	
$00130C_H$	-	-	-	-	
001310_H	-	-	-	-	
001314_H	-	-	-	-	
001318_H	-	-	-	-	
$00131C_H$	-	-	-	-	
001320_H	-	-	-	-	
001324_H	-		-		
001328_H | $00132C_H$	-	-	-	-	
001330_H	-		-		
001334_H | $0013FC_H$	-	-	-	-	Reserved
001400_H	DACR[R/W] B,H,W -------0	-	DADR[R/W] H,W ------XX XXXXXXXX		DAC
001404_H | $0014FC_H$	-	-	-	-	Reserved
001500_H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000000-0	SSR0 [R/W] B,H,W 0--00011	ESCR0/(IBSR0) [R/W] B,H,W 00000000	Multi Function Serial I/F 0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001504_H	-/(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001508_H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
$00150C_H$	STMCR0[R/W] B,H,W 00000000 00000000		-/(SFUR0) [R/W] B,H,W -------- -------- *4		
001510_H	-	-	-/(SFLR10) [R/W] B,H,W -------- *4	-/(SFLR00) [R/W] B,H,W -------- *4	
001514_H	-	-	-	-	
001518_H	-	-	-	-	
$00151C_H$	BGR0[R/W] H,W 00000000 00000000		-/(ISMK0)[R/W] B,H,W -------- *2	-/(ISBA0)[R/W] B,H,W -------- *2	
001520_H	FCR10[R/W] B,H,W 00-00100	FCR00[R/W] B,H,W -0000000	FBYTE20[R/W] B,H,W 00000000	FBYTE10[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001524$_H$	SCR1[R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1[R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528$_H$	-/(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
00152C$_H$	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530$_H$	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W -------- -------- *3 *4		
001534$_H$	-/(SCSTR31) [R/W] B,H,W -------- *3	-/(SCSTR21) [R/W] B,H,W -------- *3	-/(SCSTR11/ SFLR11) [R/W] B,H,W -------- *3 *4	-/(SCSTR01/ SFLR01) [R/W] B,H,W -------- *3 *4	
001538$_H$	-	-	-	-	
00153C$_H$	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540$_H$	BGR1[R/W] H,W 00000000 00000000		-	-	
001544$_H$	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
001548$_H$ | 001FFC$_H$	-	-	-	-	Reserved
002000$_H$	CTRLR0[R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN 0 64msb
002004$_H$	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008$_H$	INTR0[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
00200C$_H$	BRPER0[R/W] B,H,W -------- ----0000		-		
002010$_H$	IF1CREQ0[R/W] B,H,W 0------- 00000001		IF1CMSK0[R/W] B,H,W -------- 00000000		
002014$_H$	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018$_H$	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
00201C$_H$	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020$_H$	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024$_H$	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		
002028$_H$, 00202C$_H$	-		-		
002030$_H$, 002034$_H$	Reserved (IF1 data mirror)				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002038_{H,}$ $00203C_{H}$	-		-		CAN 0 64msb
002040_{H}	IF2CREQ0[R/W] B,H,W 0------- 00000001		IF2CMSK0[R/W] B,H,W -------- 00000000		
002044_{H}	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048_{H}	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_{H}$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_{H}	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_{H}	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
$002058_{H,}$ $00205C_{H}$	-		-		
$002060_{H,}$ 002064_{H}	Reserved (IF2 data mirror)				
002068_{H} | $00207C_{H}$	-		-		
002080_{H}	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_{H}	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_{H}	-		-		
$00208C_{H}$	-		-		
002090_{H}	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_{H}	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098_{H}	-		-		
$00209C_{H}$	-		-		
$0020A0_{H}$	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
$0020A4_{H}$	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
$0020A8_{H}$	-		-		
$0020AC_{H}$	-		-		
$0020B0_{H}$	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		
$0020B4_{H}$	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
$0020B8_{H}$	-		-		
$0020BC_{H}$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0020C0_H$ | $0020FC_H$	-		-		CAN 0 64msb
002100_H | $0022FC_H$	-		-		Reserved
002300_H	DFCTLR[R/W] B,H,W -0------ --------		-	DFSTR[R/W] B,H,W -----001	WorkFlash
002304_H	-	-	-	-	
002308_H	FLIFCTLR[R/W] B,H,W ---0--00	-	FLIFFER1[R/W] B,H,W --------	FLIFFER2[R/W] B,H,W --------	
$00230C_H$ | $002FFC_H$	-	-	-	-	Reserved
003000_H	SEEARX[R] B,H,W --000000 00000000		DEEARX[R] B,H,W --000000 00000000		XBS RAM ECC control register
003004_H	EECSRX[R/W] B,H,W ----00-0	-	EFEARX[R/W] B,H,W --000000 00000000		
003008_H	-	EFECRX[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- --000000 00000000				XBS RAM diagnosis register
003010_H	TEAR1X[R] B,H,W 000----- -------- --000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- --000000 00000000				
003018_H	TAEARX[R/W] B,H,W --101111 11111111		TASARX[R/W] B,H,W --000000 00000000		
$00301C_H$	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W ------00 00001100		
003020_H	TSRCRX[R/W] B,H,W 0-------	-	-	TKCCRX[R/W] B,H,W 00----00	
003024_H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028_H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
$00302C_H$	-	EFECRA[R/W] B,H,W -------0 00000000 00000000			

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				Backup RAM diagnosis register
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W ------00 00001100		
003044_H	TSRCRA[R/W] B,H,W 0-------	-	-	TKCCRA[R/W] B,H,W 00----00	
003048_H | $0030FC_H$	-	-	-	-	Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF *5
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF *5
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT *5
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ | $00D07C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC *5
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM *5
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT *5
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 --001110				
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD *5
$00D09C_H$	-				Reserved
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU *5
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 --000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				
$00D0CC_H$ | $00D0FC_H$	-				Reserved
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC *5
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$ $00D10C_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU [*5]
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W -------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	-				
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				FlexRay GTU [*5]
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM [*5]
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD *5
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				
$00D33C_H$	NDAT4[R] W 00000000 00000000 00000000 00000000				
$00D340_H$	MBSC1[R] W 00000000 00000000 00000000 00000000				
$00D344_H$	MBSC2[R] W 00000000 00000000 00000000 00000000				
$00D348_H$	MBSC3[R] W 00000000 00000000 00000000 00000000				
$00D34C_H$	MBSC4[R] W 00000000 00000000 00000000 00000000				
$00D350_H$ | $00D3EC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D3F0_H$	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF *5
$00D3F4_H$	ENDN[R] W 10000111 01100101 01000011 00100001				
$00D3F8_H$ | $00D3FC_H$	-				Reserved
$00D400_H$ | $00D4FC_H$	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF *5
$00D500_H$	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
$00D504_H$	WRHS2[R/W] W -------- -0000000 -----000 00000000				
$00D508_H$	WRHS3[R/W] W -------- -------- -----000 00000000				
$00D50C_H$	-				
$00D510_H$	IBCM[R/W] W -------- ------00 -------- -----000				
$00D514_H$	IBCR[R/W] W 0------- -0000000 0------- -0000000				
$00D518_H$ | $00D5FC_H$	-				Reserved
$00D600_H$ | $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF *5
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ | $00D7FC_H$	-				Reserved
$00D800_H$ | $00EFFC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00F000_H$ | $00FEFC_H$	-				Reserved [S]
$00FF00_H$	DSUCR[R/W] B,H,W -------- -------0		-	-	OCDU [S]
$00FF04_H$ | $00FF0C_H$	-	-	-	-	Reserved [S]
$00FF10_H$	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ | $00FFF4_H$	-	-	-	-	Reserved [S]
$00FFF8_H$	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

*5: For FlexRay, the CY91F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ has corresponding functions. The following registers are reserved registers for models without the FlexRay function.
000125_H IRPR2L[5:4], $000E68_H$, $0004E8_H$-$0004EF_H$, $00D000_H$-$00D717_H$

10. Interrupt Vector Table

■ CY91F583AM/F584AM/F585AM

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-	-
Instruction access protection violation exception	6	06	-	$3E4_H$	$000FFFE4_H$	-	-
Data access protection violation exception	7	07	-	$3E0_H$	$000FFFE0_H$	-	-
Data access error interrupts	8	08	-	$3DC_H$	$000FFFDC_H$	-	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-	-
NMI request Error generation at internal bus diagnosis RAM double-bit error Backup RAM double-bit error	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-	○
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0	-
Reload timer 0 / 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1	○
Reload timer 2 / 3	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2	○
Multifunction serial interface ch.0 (reception completed)/ Multifunction serial interface ch.0 (status)	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2	○
Multifunction serial interface ch.0 (transmission completed)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4	-
Multifunction serial interface ch.1 (reception completed)/ Multifunction serial interface ch.1 (status)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*2	○
Multifunction serial interface ch.1 (transmission completed)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6	-
Multifunction serial interface ch.2 (reception completed)/ Multifunction serial interface ch.2 (status)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*2	○
Multifunction serial interface ch.2 (transmission completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8	-
Multifunction serial interface ch.3 (reception completed)/ Multifunction serial interface ch.3 (status)	25	19	ICR09	398_H	$000FFF98_H$	9*2	○
Multifunction serial interface ch.3 (transmission completed)	26	1A	ICR10	394_H	$000FFF94_H$	10	-
*4	27	1B	ICR11	390_H	$000FFF90_H$	-	-
*4	28	1C	ICR12	$38C_H$	$000FFF8C_H$	-	-
CAN 0	29	1D	ICR13	388_H	$000FFF88_H$	-	-
CAN 1	30	1E	ICR14	384_H	$000FFF84_H$	-	-
FlexRay 0 *5	31	1F	ICR15	380_H	$000FFF80_H$	-	-
FlexRay 1 *5	32	20	ICR16	$37C_H$	$000FFF7C_H$	-	-
FlexRay timer 0 *5	33	21	ICR17	378_H	$000FFF78_H$	-	-
FlexRay timer 1 *5	34	22	ICR18	374_H	$000FFF74_H$	-	-
RAM diagnosis completed RAM initialization completed Error generation at RAM diagnosis Backup RAM diagnosis completed Backup RAM initialization completed Error generation at Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-	○

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
Main timer/PLL timer/ PLL gear for FlexRay*5/ PLL alarm for FlexRay*5	36	24	ICR20	$36C_H$	$000FFF6C_H$	20*3	O
Clock calibration unit (CR oscillation)	37	25	ICR21	368_H	$000FFF68_H$	-	-
U/D counter 0 / 1	38	26	ICR22	364_H	$000FFF64_H$	22	O
Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23	O
Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24	O
Free-run timer 2 (0 detection) / (compare clear) PPG 0 / 1 / 2 / 3	41	29	ICR25	358_H	$000FFF58_H$	25	O
Free-run timer 3 (0 detection) / (compare clear)	42	2A	ICR26	354_H	$000FFF54_H$	26	O
Free-run timer 4 (0 detection) / (compare clear)	43	2B	ICR27	350_H	$000FFF50_H$	27	O
Free-run timer 5 (0 detection) / (compare clear) PPG 4 / 5	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28	O
ICU 0 (fetching) / ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29	O
ICU 2 (fetching) / ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30	O
*4	47	2F	ICR31	340_H	$000FFF40_H$	-	-
*4	48	30	ICR32	$33C_H$	$000FFF3C_H$	-	-
OCU 0 (match) / OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33	O
OCU 2 (match) / OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34	O
OCU 4 (match) / OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35	O
OCU 6 (match) / OCU 7 (match)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36	O
OCU 8 (match) / OCU 9 (match)	53	35	ICR37	328_H	$000FFF28_H$	37	O
OCU 10 (match) / OCU 11 (match)	54	36	ICR38	324_H	$000FFF24_H$	38	O
WG dead timer underflow 0 / 1 / 2 WG dead timer reload 0 / 1 / 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39	O
WG dead timer underflow 3 / 4 / 5 WG dead timer reload 3 / 4 / 5 WG DTTI 1	56	38	ICR40	$31C_H$	$000FFF1C_H$	40	O
AD converter 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	57	39	ICR41	318_H	$000FFF18_H$	41	O
AD converter 8 / 9 / 10 / 11 / 12 / 13 / 14	58	3A	ICR42	314_H	$000FFF14_H$	42	O
AD converter 16 / 17 / 18 / 19 / 20 / 21 / 22 / 23	59	3B	ICR43	310_H	$000FFF10_H$	43	O
Base timer 0 IRQ 0/ base timer 0 IRQ 1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44	O
Base timer 1 IRQ 0/ base timer 1 IRQ 1	61	3D	ICR45	308_H	$000FFF08_H$	45	O
DMAC 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	62	3E	ICR46	304_H	$000FFF04_H$	-	O
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-	-
System reserved	64	40	-	$2FC_H$	$000FFEFC_H$	-	-
System reserved	65	41	-	$2F8_H$	$000FFEF8_H$	-	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-	-

*1 :Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (resource number) is assigned.

*2 :The multi-function serial interface status does not support DMA transfer caused by I^2C reception.

*3 :"PLL gear for FlexRay" and "PLL alarm for FlexRay" do not support DMA transfer.

*4 :For CY91F583AM/F584AM/F585AM, the interrupt vectors are unused.

*5 :For FlexRay, the CY91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ have corresponding functions.

■ CY91F583AS/F584AS/F585AS

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-	-
Instruction access protection violation exception	6	06	-	$3E4_H$	$000FFFE4_H$	-	-
Data access protection violation exception	7	07	-	$3E0_H$	$000FFFE0_H$	-	-
Data access error interrupts	8	08	-	$3DC_H$	$000FFFDC_H$	-	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-	-
NMI request Error generation at internal bus diagnosis RAM double-bit error Backup RAM double-bit error	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-	○
External interrupt 0-6	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0	-
Reload timer 0 / 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1	○
Reload timer 2 / 3	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2	○
Multifunction serial interface ch.0 (reception completed)/ Multifunction serial interface ch.0 (status)	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2	○
Multifunction serial interface ch.0 (transmission completed)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4	-
Multifunction serial interface ch.1 (reception completed)/ Multifunction serial interface ch.1 (status)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*2	○
Multifunction serial interface ch.1 (transmission completed)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6	-
*4	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-	-
*4	24	18	ICR08	$39C_H$	$000FFF9C_H$	-	-
*4	25	19	ICR09	398_H	$000FFF98_H$	-	-
*4	26	1A	ICR10	394_H	$000FFF94_H$	-	-
*4	27	1B	ICR11	390_H	$000FFF90_H$	-	-
*4	28	1C	ICR12	$38C_H$	$000FFF8C_H$	-	-
CAN 0	29	1D	ICR13	388_H	$000FFF88_H$	-	-
*4	30	1E	ICR14	384_H	$000FFF84_H$	-	-
FlexRay 0 *5	31	1F	ICR15	380_H	$000FFF80_H$	-	-
FlexRay 1 *5	32	20	ICR16	$37C_H$	$000FFF7C_H$	-	-
FlexRay timer 0 *5	33	21	ICR17	378_H	$000FFF78_H$	-	-
FlexRay timer 1 *5	34	22	ICR18	374_H	$000FFF74_H$	-	-

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
RAM diagnosis completed RAM initialization completed Error generation at RAM diagnosis Backup RAM diagnosis completed Backup RAM initialization completed Error generation at Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-	○
Main timer/PLL timer/ PLL gear for FlexRay*5/ PLL alarm for FlexRay*5	36	24	ICR20	$36C_H$	$000FFF6C_H$	20*3	○
Clock calibration unit (CR oscillation)	37	25	ICR21	368_H	$000FFF68_H$	-	-
U/D counter 0 / 1	38	26	ICR22	364_H	$000FFF64_H$	22	○
Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23	○
Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24	○
Free-run timer 2 (0 detection) / (compare clear) PPG 0 / 1 / 2 / 3	41	29	ICR25	358_H	$000FFF58_H$	25	○
Free-run timer 3 (0 detection) / (compare clear)	42	2A	ICR26	354_H	$000FFF54_H$	26	○
Free-run timer 4 (0 detection) / (compare clear)	43	2B	ICR27	350_H	$000FFF50_H$	27	○
Free-run timer 5 (0 detection) / (compare clear) PPG 4 / 5	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28	○
ICU 0 (fetching) / ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29	○
ICU 2 (fetching) / ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30	○
*4	47	2F	ICR31	340_H	$000FFF40_H$	-	-
*4	48	30	ICR32	$33C_H$	$000FFF3C_H$	-	-
OCU 0 (match) / OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33	○
OCU 2 (match) / OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34	○
OCU 4 (match) / OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35	○
OCU 6 (match) / OCU 7 (match)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36	○
OCU 8 (match) / OCU 9 (match)	53	35	ICR37	328_H	$000FFF28_H$	37	○
OCU 10 (match) / OCU 11 (match)	54	36	ICR38	324_H	$000FFF24_H$	38	○
WG dead timer underflow 0 / 1 / 2 WG dead timer reload 0 / 1 / 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39	○
WG dead timer underflow 3 / 4 / 5 WG dead timer reload 3 / 4 / 5 WG DTTI 1	56	38	ICR40	$31C_H$	$000FFF1C_H$	40	○
AD converter 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	57	39	ICR41	318_H	$000FFF18_H$	41	○
AD converter 8 / 9 / 10 / 11 / 12 / 13 / 14	58	3A	ICR42	314_H	$000FFF14_H$	42	○
AD converter 19 / 20	59	3B	ICR43	310_H	$000FFF10_H$	43	○
Base timer 0 IRQ 0/ base timer 0 IRQ 1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44	○
Base timer 1 IRQ 0/ base timer 1 IRQ 1	61	3D	ICR45	308_H	$000FFF08_H$	45	○
DMAC 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	62	3E	ICR46	304_H	$000FFF04_H$	-	○

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-	-
System reserved	64	40	-	$2FC_H$	$000FFEFC_H$	-	-
System reserved	65	41	-	$2F8_H$	$000FFEF8_H$	-	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-	-

*1 :Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (resource number) is assigned.

*2 :The multi-function serial interface status does not support DMA transfer caused by I^2C reception.

*3 :"PLL gear for FlexRay" and "PLL alarm for FlexRay" do not support DMA transfer.

*4 :For CY91F583AS/F584AS/F585AS, the interrupt vectors are unused.

*5 :For FlexRay, the CY91F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ have corresponding functions

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage*1 ,*2	AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	Avcc ≤ Vcc
Analog reference voltage*1	AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage*1	V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage*1	V_O	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current	I_{CLAMP}	-	4	mA	*9
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*9
"L" level maximum output current*3	I_{OL1}	-	7	mA	When setting to 2mA*6
	I_{OL2}	-	14	mA	When setting to 4mA *7
	I_{OL3}	-	17.5	mA	When setting to 5mA *8
"L" level average output current*4	I_{OLAV1}	-	2	mA	When setting to 2mA *6
	I_{OLAV2}	-	4	mA	When setting to 4mA *7
	I_{OLAV3}	-	5	mA	When setting to 5mA *8
"L" level total output current*5	ΣI_{OL}	-	50	mA	*6
"H" level maximum output current*3	I_{OH1}	-	-7	mA	When setting to 2mA *6
	I_{OH2}	-	-14	mA	When setting to 4mA *7
	I_{OH3}	-	-17.5	mA	When setting to 5mA *8
"H" level average output current*4	I_{OHAV1}	-	-2	mA	When setting to 2mA *6
	I_{OHAV2}	-	-4	mA	When setting to 4mA *7
	I_{OHAV3}	-	-5	mA	When setting to 5mA *8
"H" level total output current*5	ΣI_{OH}	-	-50	mA	*6
Power consumption	P_D	-	690	mW	
Operating temperature	T_A	-40	+125	°C	*10, *11
Storage temperature	Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS} =0.0V.

*2: Caution must be taken that AV_{CC} does not exceed V_{CC}.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Corresponding pins: General-purpose ports

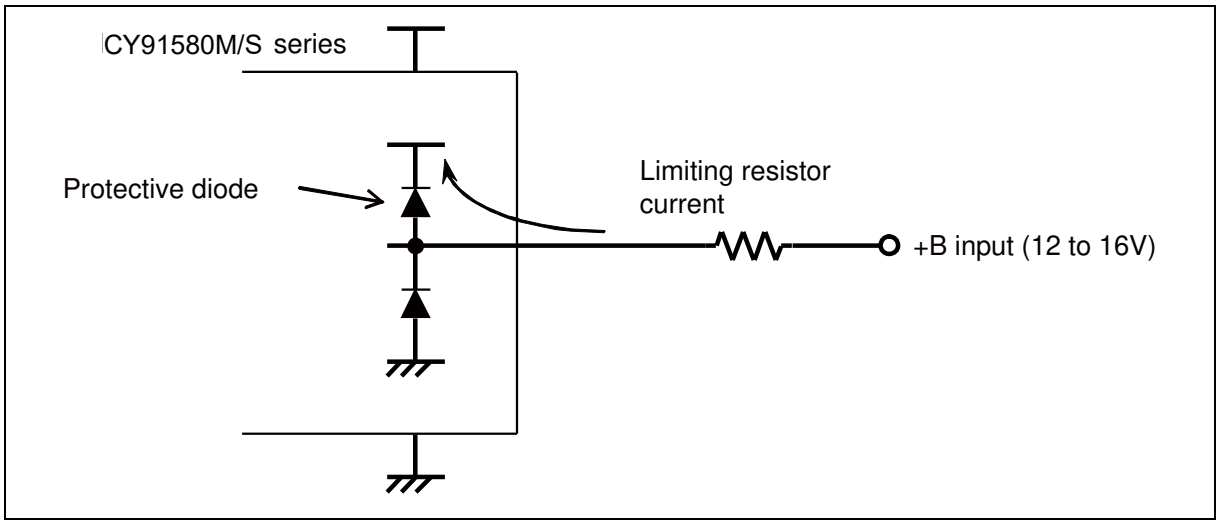
*7: Corresponding pins: General-purpose ports of P021 to P023, P025 to P027

*8: Corresponding pins: General-purpose ports other than those of P021 to P023, P025 to P027

*9:
- Corresponding pins: General-purpose ports
- Use the devices within recommended operating conditions.
- Use the devices with direct voltage (current).

- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the Vcc pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Sample recommended circuit



*10: To use this product at T_A=125°C, equip this on a multilayer board with four or more layers.
To equip this on a single-layer board, change the operating conditions (operating frequency, power supply voltage, etc) to use this at the power consumption P_D=415mW or lower, or use this at T_A=105°C or lower.

*11: When it is used exceeding T_A=125°C, contact your sales representative.

WARNING

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

11.2 Recommended Operating Conditions

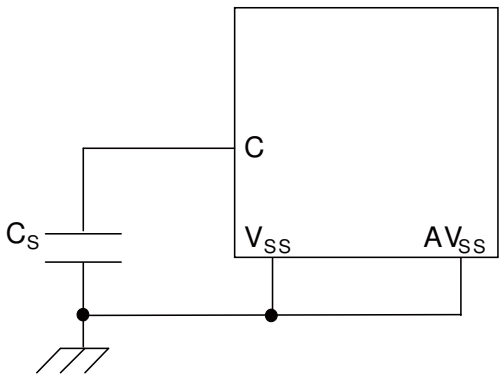
(V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.5	5.5	V	Recommended operation guarantee range
	AV_{CC}	4.5	5.5	V	
	V_{CC}	3.7	5.5	V	Operation guarantee range
	AV_{CC}	3.7	5.5	V	
Smoothing capacitor*1	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+125	°C	*2

*1: For connection of smoothing capacitor C_S, see the figure below.

*2: When it is used exceeding T_A=125°C, contact your sales representative.

C Pin Connection Diagram



WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

11.3 DC Characteristics

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When CMOS schmitt input level is selected	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When Automotive input level is selected	0.8 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH3}	P021 to P023, P025 to P027	When FlexRay input level is selected	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH4}	RSTX, NMIX	-	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH5}	MD0, MD1	-	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH6}	DEBUGIF	-	2.0	-	V_{CC}+0.3	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When CMOS schmitt input level is selected	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When Automotive input level is selected	Vss-0.3	-	0.5 × V_{CC}	V	
	V_{IL3}	P021 to P023, P025 to P027	When FlexRay input level is selected	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL4}	RSTX, NMIX	-	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL5}	MD0, MD1	-	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL6}	DEBUGIF	-	Vss-0.3	-	0.8	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, Vcc=5.0V±10%,V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I_{OH}=-2.0mA	Vcc-0.5	-	Vcc	V	
	V_{OH2}	P021 to P023, P025 to P027	Vcc=4.5V I_{OH}=-4.0mA	Vcc-0.5	-	Vcc	V	When FlexRay is selected
	V_{OH3}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I_{OH}=-5.0mA	Vcc-0.5	-	Vcc	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I_{OL}=2.0mA	0	-	0.4	V	
	V_{OL2}	P021 to P023, P025 to P027	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	When FlexRay is selected
	V_{OL3}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I_{OL}=5.0mA	0	-	0.4	V	
	V_{OL4}	P040, P041, P063*, P064*, P080*, P081*, P083*,P084*	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C shared pin (when I^2C is selected)
	V_{OL5}	DEBUGIF	Vcc=2.7V I_{OL}=25.0mA	0	-	0.25	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input Leak Current	I_{IL}	All input pins	Vcc= AV_{CC}=5.5V V_{SS} < V_I < V_{CC}	-5	-	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When pull-up resistance is selected	25	-	100	kΩ	
Input Capacitor	C_{IN}	Other thanVCC, VSS, AVCC, AVSS, C	-	-	5	15	pF	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	VCC5	Normal operations F_{CP}=128MHz, F_{CPM}=128MHz, F_{CPP}=32MHz	-	80	110	mA	FlexRay =ON
				-	73	103	mA	FlexRay =OFF
			Normal operations F_{CP}=128MHz, F_{CPM}=32MHz, F_{CPP}=32MHz	-	77	107	mA	FlexRay =ON
				-	70	100	mA	FlexRay =OFF
			Normal operations F_{CP}=80MHz, F_{CPM}=80MHz, F_{CPP}=40MHz	-	62	89	mA	FlexRay =ON
				-	57	85	mA	FlexRay =OFF
			Normal operations F_{CP}=80MHz, F_{CPM}=40MHz, F_{CPP}=40MHz	-	61	88	mA	FlexRay =ON
				-	56	84	mA	FlexRay =OFF
			Flash write F_{CP}=128MHz, F_{CPM}=128MHz, F_{CPP}=32MHz	-	95	125	mA	*
			Flash erase F_{CP}=128MHz, F_{CPM}=128MHz, F_{CPP}=32MHz	-	95	125	mA	*

*: This series has 2 types of flash; main flash and WorkFlash; however, this is the specification when only one of those is written/erased.

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS}	VCC5	CPU sleep F_{CP}=128MHz, F_{CPm}=128MHz, F_{CPP}=32MHz	-	41	66	mA	*1, *2 ,*3, *4
	I_{CCBS}		Bus sleep F_{CP}=128MHz, F_{CPm}=128MHz, F_{CPP}=32MHz	-	19	45	mA	*1, *2 ,*3 ,*4
	I_{CCT}		Clock mode 4MHz source oscillation	-	1.2	1.8	mA	When using external clock*5 T_A=25°C, *1, *2 ,*3 ,*4
				-	2.7	3.3	mA	When using crystal T_A=25°C, *1, *2, *3, *4
	I_{CCTS}		Clock mode shutdown 4MHz source oscillation	-	0.3	0.4	mA	When using external clock*5 T_A=25°C, *1, *2
				-	1.8	1.9	mA	When using crystal T_A=25°C, *1, *2
				-	0.7	0.8	mA	When using external clock*5 T_A=25°C, *3, *4
				-	2.2	2.3	mA	When using crystal T_A=25°C, *3 ,*4
	I_{CCH}		STOP mode	-	0.6	1.1	mA	T_A=25°C, *1 ,*2
				-	1.0	1.6	mA	T_A=25°C, *3 ,*4
	I_{CCHS}		STOP mode shutdown	-	0.1	0.2	mA	T_A=25°C, *1, *2
				-	0.5	0.6	mA	T_A=25°C, *3, *4

*1:CY91F583AMG/F584AMG/F585AMG/F583AMH/F584AMH/F585AMH

*2:CY91F583ASG/F584ASG/F585ASG/F583ASH/F584ASH/F585ASH

*3:CY91F583AMJ/F584AMJ/F585AMJ/F583AMK/F584AMK/F585AMK

*4:CY91F583ASJ/F584ASJ/F585ASJ/F583ASK/F584ASK/F585ASK

*5: The power supply current is the current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

11.4 AC Characteristics

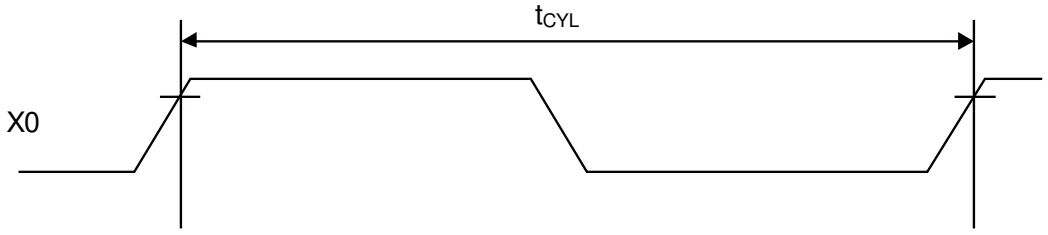
11.4.1 Main Clock Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	4	-	20	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	50	-	250	ns	
Internal operating clock frequency*	F_{CP}	-	-	-	-	128	MHz	CPU clock
	F_{CPP}	-	-	-	-	40	MHz	Peripheral bus clock
	F_{CPM}	-	-	-	-	128	MHz	Motor clock
Internal operating clock cycle time*	t_{CP}	-	-	7.82	-	-	ns	CPU clock
	t_{CPP}	-	-	25	-	-	ns	Peripheral bus clock
	t_{CPM}	-	-	7.82	-	-	ns	Motor clock
CAN PLL jitter (during lock)	t_{PJ}	-	-	-10	-	+10	ns	
Built-in CR oscillation frequency	F_{CCR}	-	-	50	100	150	kHz	

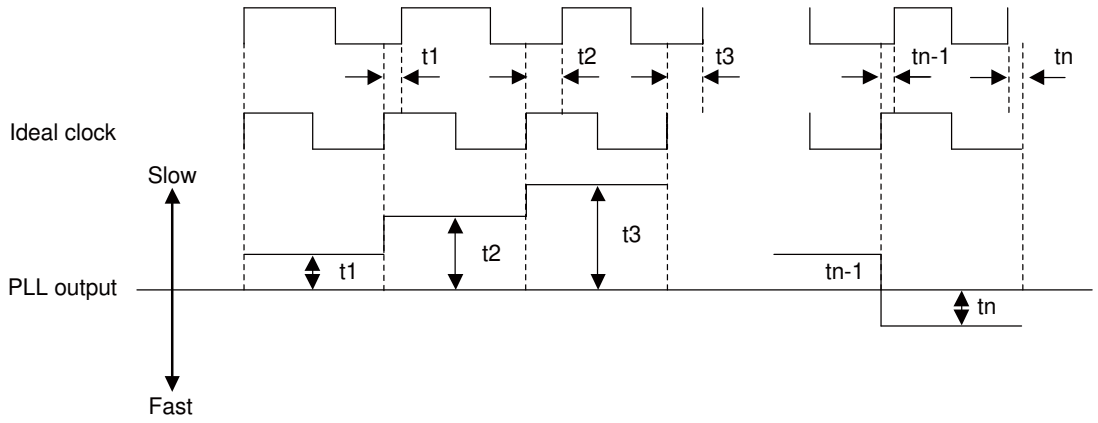
*: The maximum/minimum value is defined when using the main clock and PLL clock.

■ X0,X1 clock timing



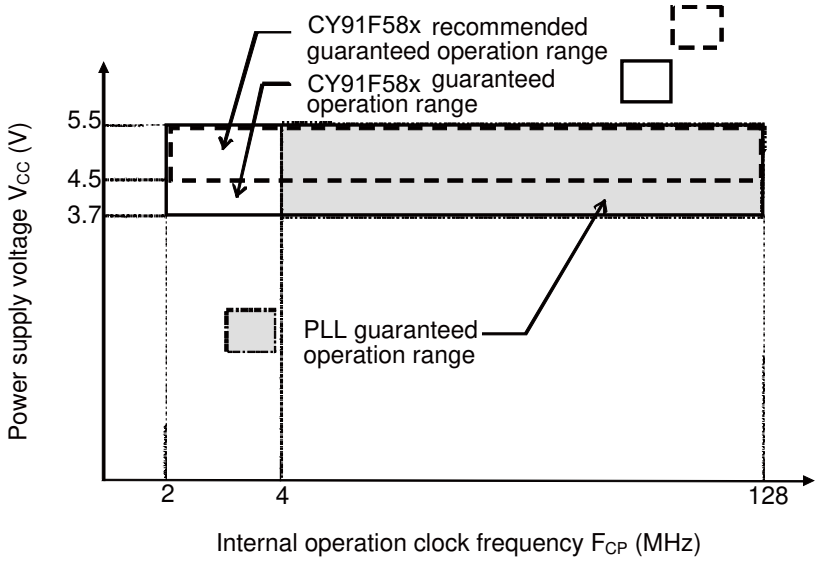
■ CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



■ Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

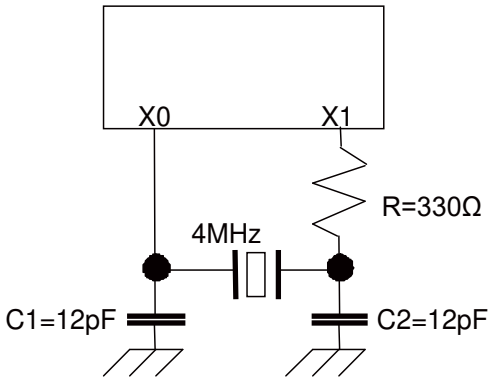


Note: The CPU will be reset at the power supply voltage of the low-voltage detection setting voltage or less.

Oscillation clock frequency vs. Internal operation clock frequency

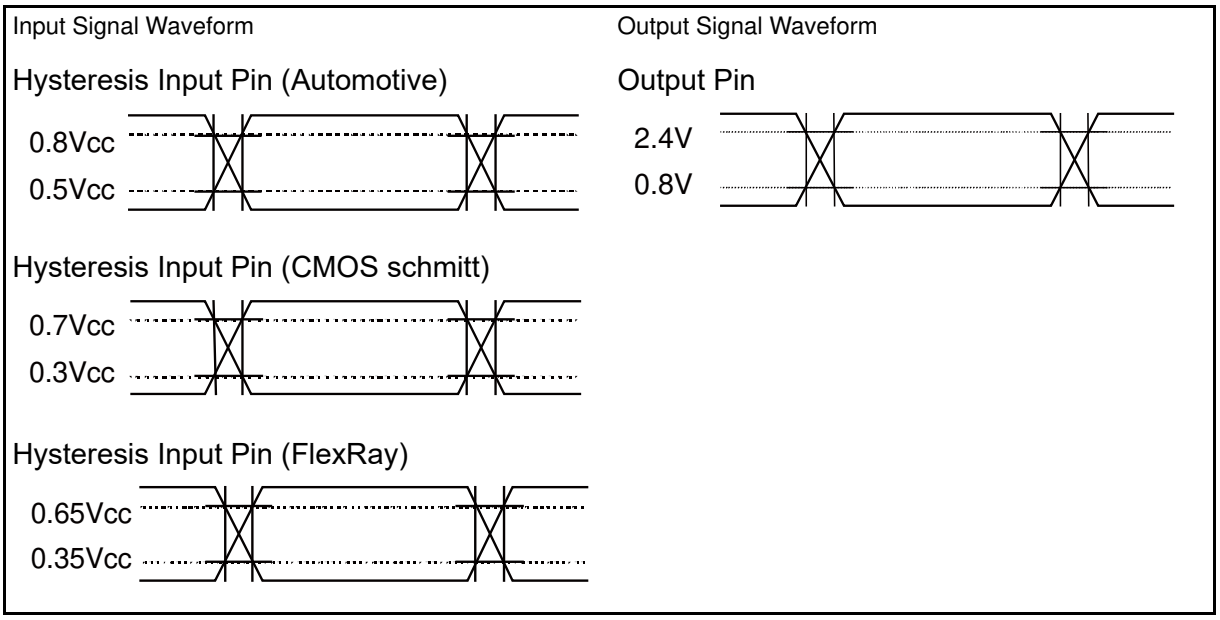
		Internal operation clock frequency								
		Main clock	PLL clock							
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	...	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	80MHz	...	128MHz

- Example of oscillation circuit



Note: If it is impossible to start the oscillation within or equal to 20ms when starting from the oscillation stop state, the clock supervisor performs a detection of oscillation stop and moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms.
In addition, when configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.

AC characteristics are specified by the following measurement reference voltage values.

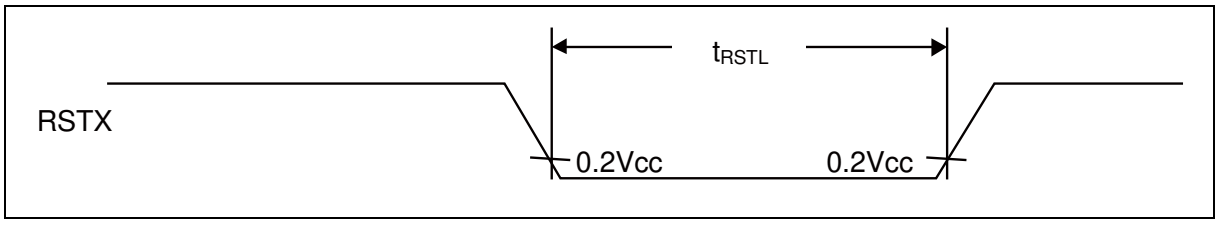


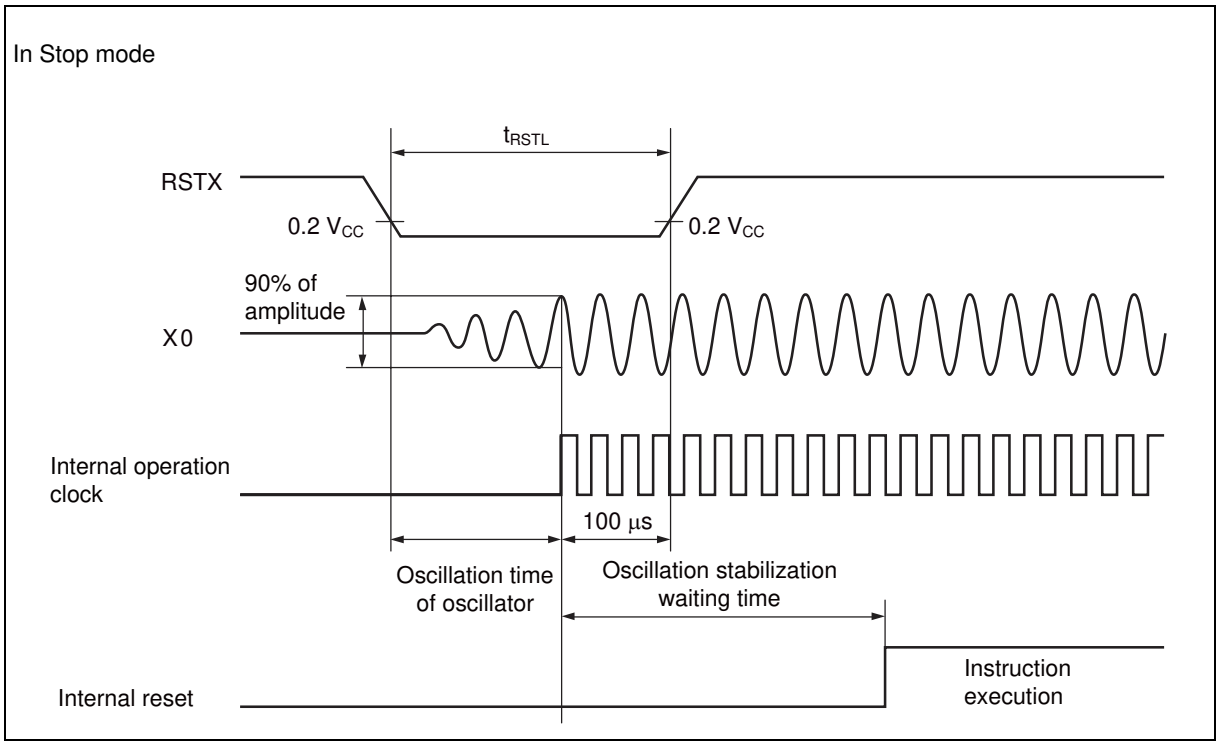
11.4.2 Reset input

(T_A: Recommended operating conditions, Vcc =5.0V±10%, Vss=AVss=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	During normal operation
				Oscillation time of oscillator* +0.1	-	ms	At Stop mode
				100	-	µs	At Clock mode
Reset input removal width				1	-	µs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.





11.4.3 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.024	2.200	2.376	V	When turning on power
Level detection hysteresis width	-	VCC5	-	-	100	-	mV	During voltage drop
Level detection time	-	-	-	-	-	30	µs	*1
Slope detection undetected standard	-	VCC5	V_{CC}=level detection release level	-	-	4	mV/µs	*2
Power off time	t_{OFF}	VCC5	-	50	-	-	ms	*3

*1: If the fluctuation of the power supply is faster than the low-voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss.

11.4.4 Multi-function Serial

CSIO timing (SMR:MD2-0="010"b)

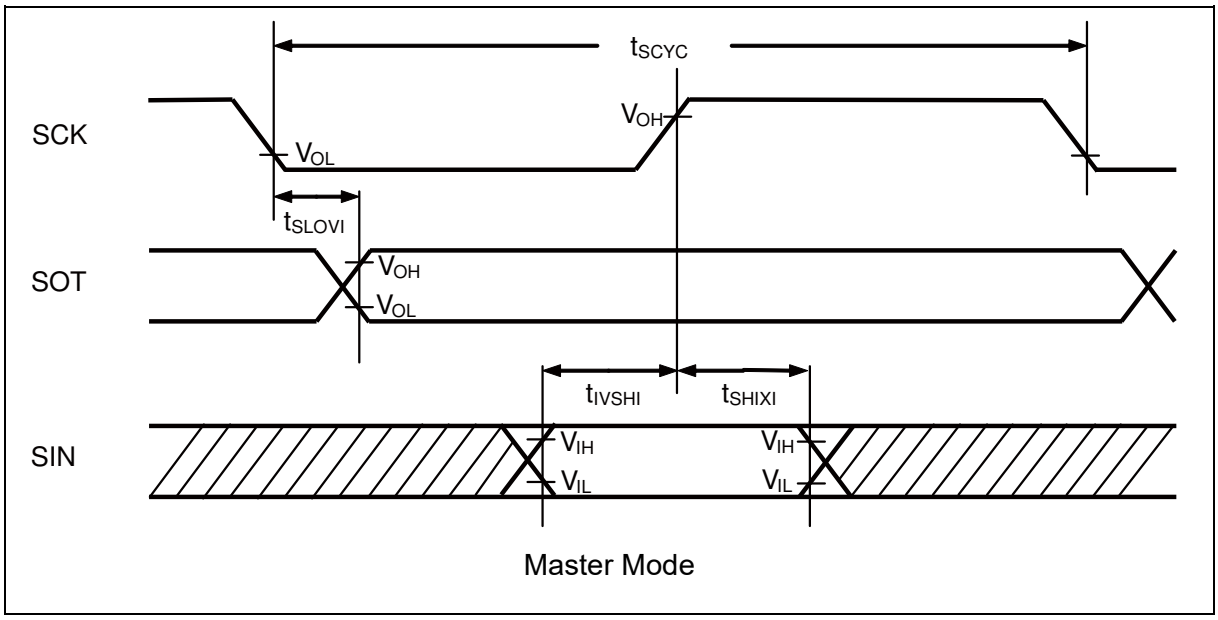
Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "H" (SMR:SCINV=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

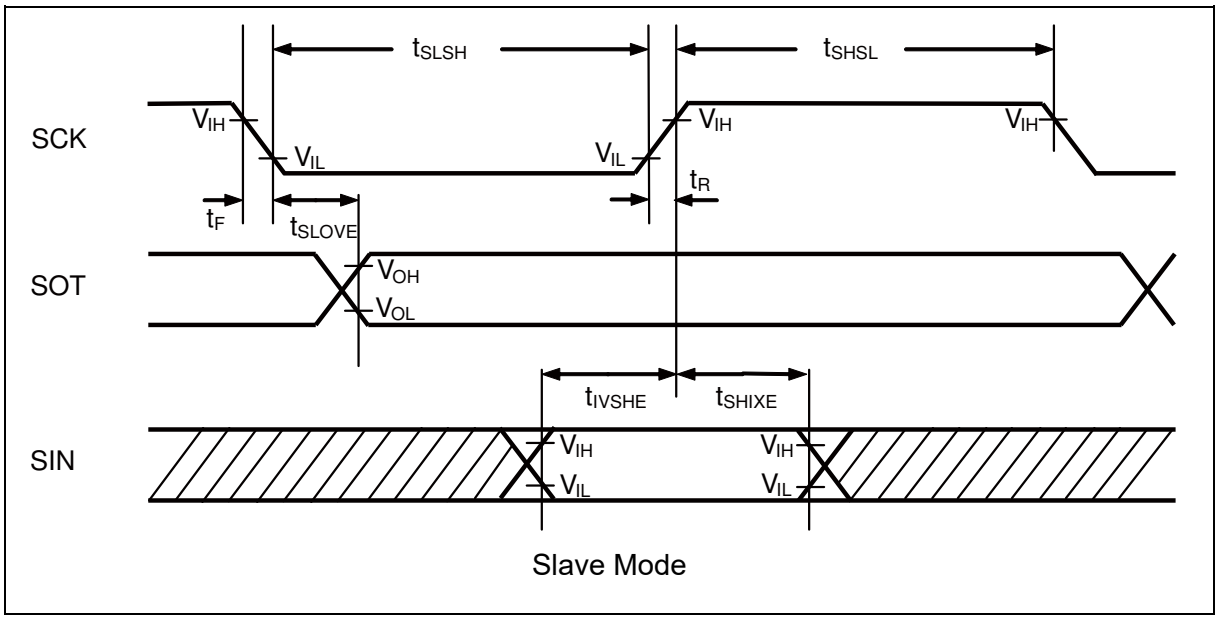
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXI}			0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L"pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t_R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode

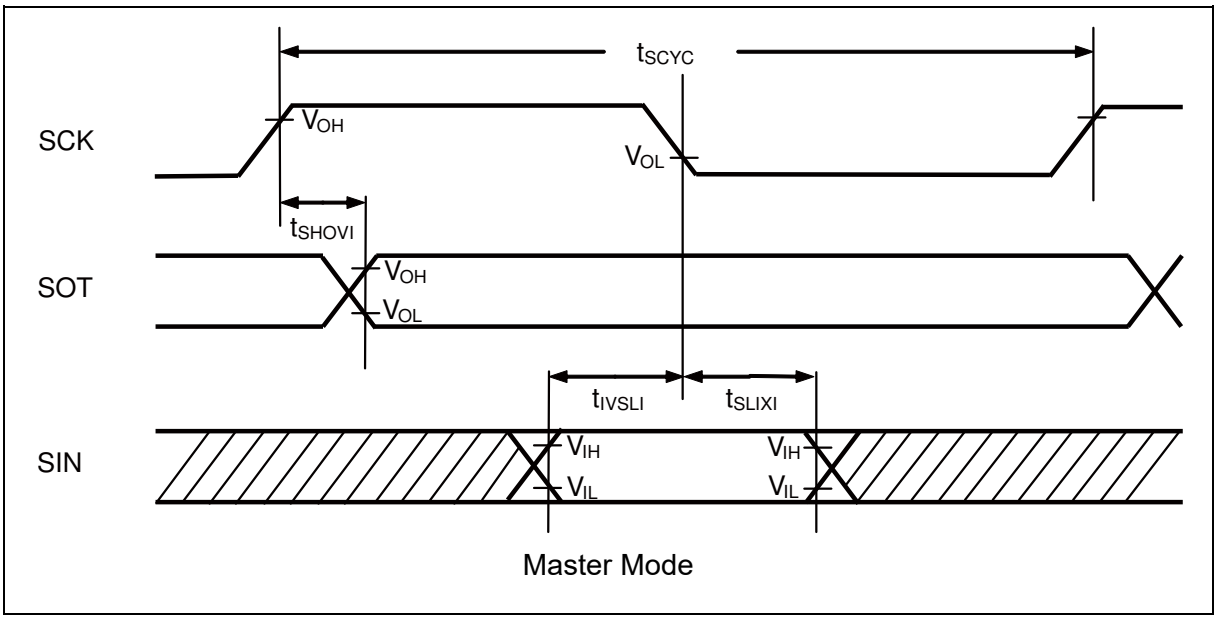
Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "L" (SMR:SCINV=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

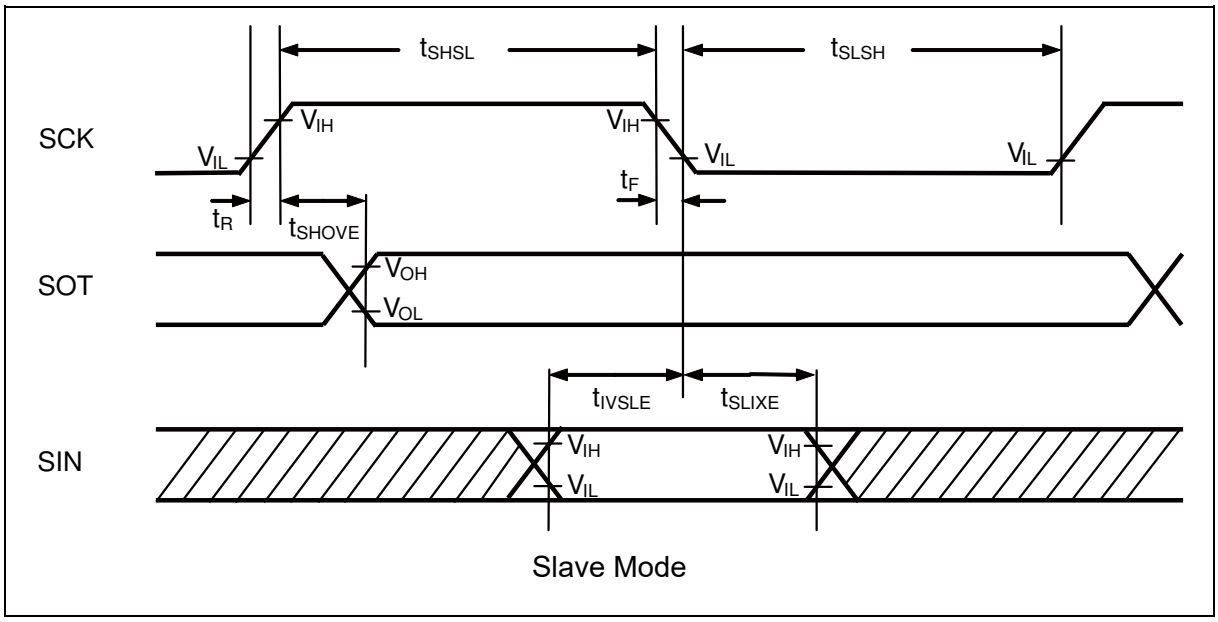
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L"pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t_R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode

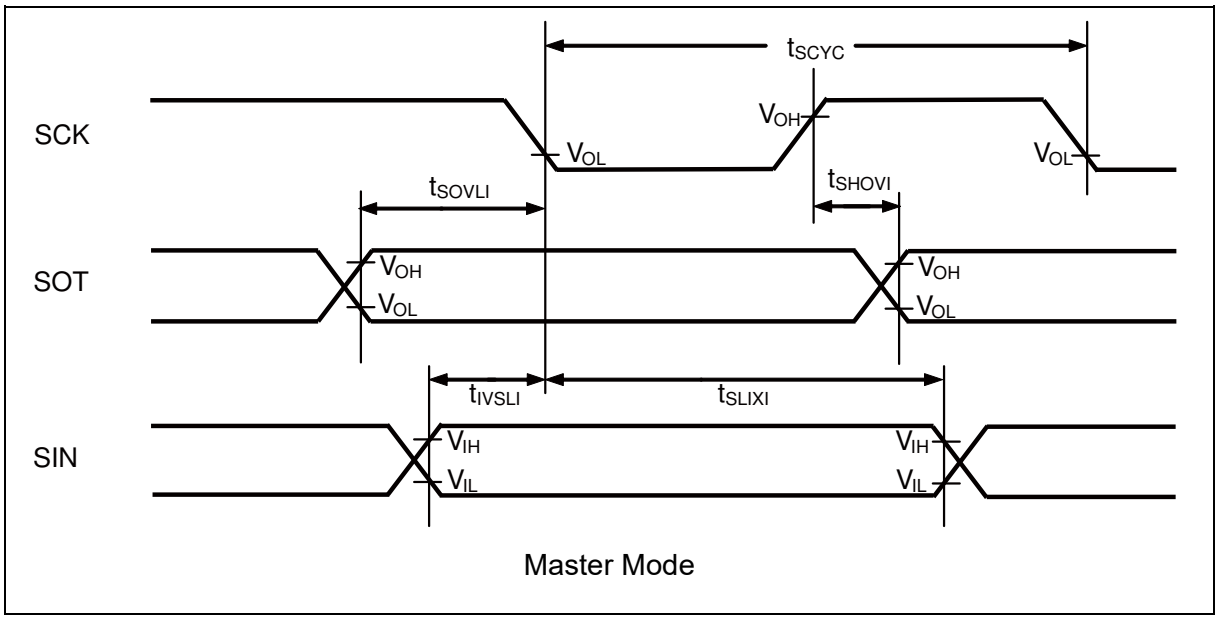
SPI compatible (SCR:SPI=1) and serial clock output signal detect level "H" (SMR:SCINV=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10% , V_{SS}=AV_{SS}=0.0V)

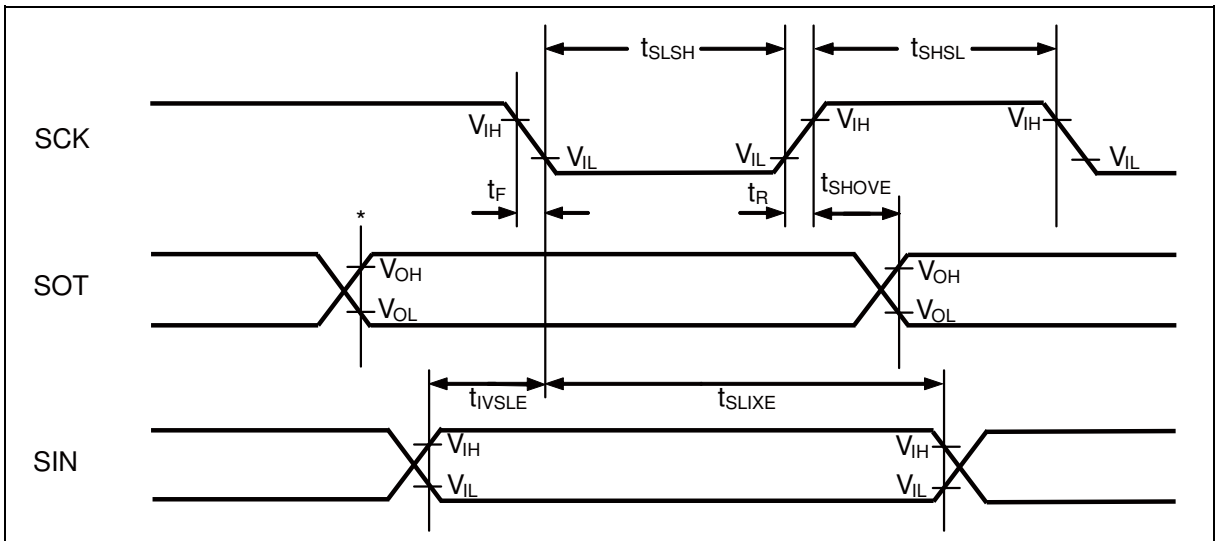
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT ⇒ SCK ↓ delay time	t_{SOVLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L"pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t_R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



*: Changes when writing to TDR register

Slave Mode

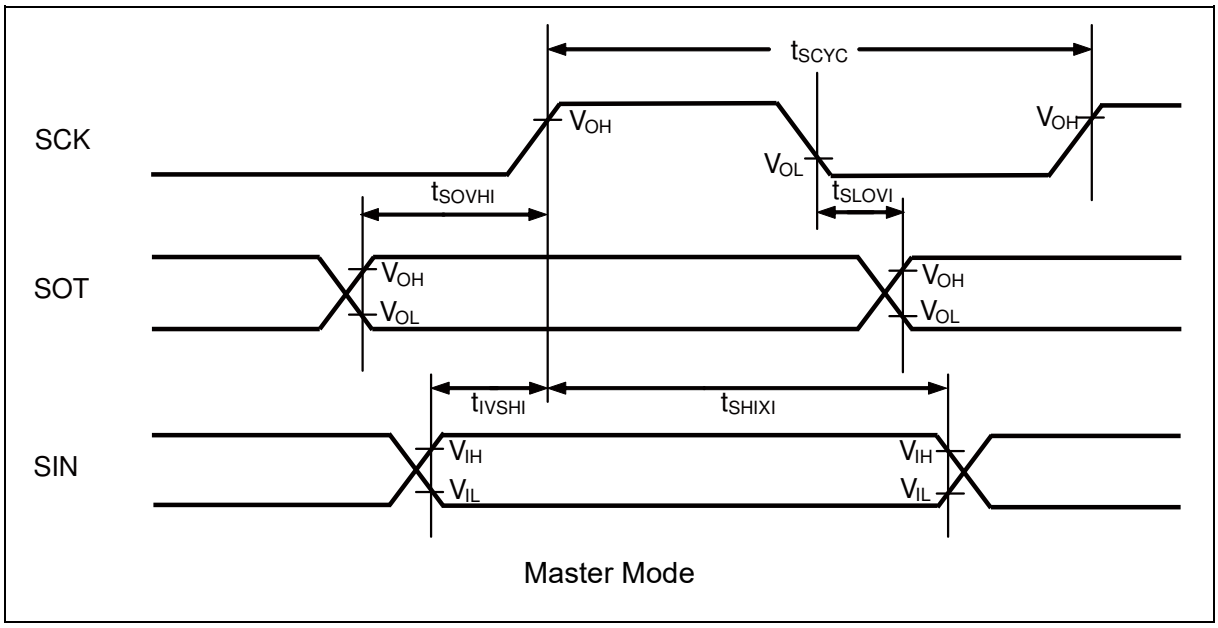
SPI compatible (SCR:SPI=1) and serial clock output signal detect level "L" (SMR:SCINV=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

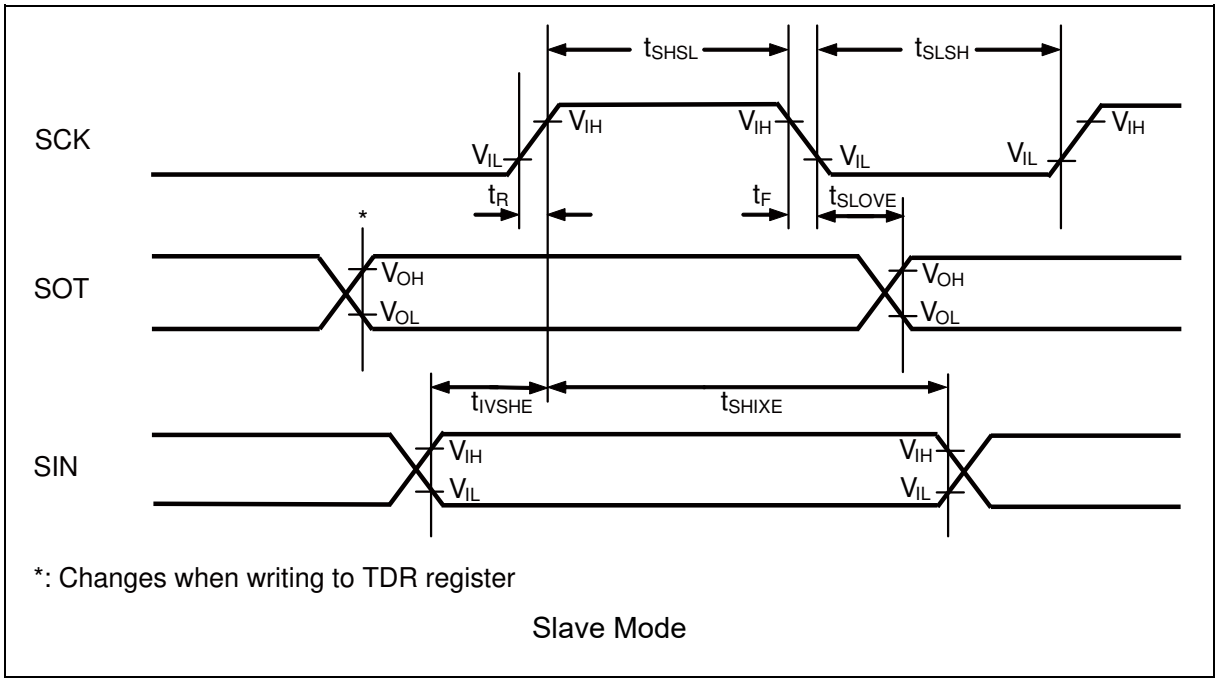
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT ⇒ SCK ↑ delay time	t_{SOVHI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		$2t_{CPP}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t_R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



*: Changes when writing to TDR register

Slave Mode

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H" (SMR:SCINV=0)
- Serial chip select inactive level "H" (SCSCR:CSLVL=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ ⇒ SCK ↓ setup time	t_{CSSI}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Master mode C_L=50pF	t_{CSSU}*1+0	t_{CSSU}*1+50	ns	
SCK ↑ ⇒ SCS ↑ hold time	t_{CSHI}			t_{CSHD}*2-50	t_{CSHD}*2+0	ns	
SCS deselect time	t_{CSDI}	SCS1, SCS2*4, SCS3*4		-50+5t_{CPP} +t_{CSDS}*3	+50+5t_{CPP} +t_{CSDS}*3	ns	
SCS ↓ ⇒ SCK ↓ setup time	t_{CSSE}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↑ ⇒ SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS1, SCS2*4, SCS3*4		3t_{CPP}+30	-	ns	
SCS ↓ ⇒ SOT delay time	t_{DSE}	SCS1, SCS2*4, SCS3*4, SOT1, SOT2*4, SOT3*4		-	40	ns	
SCS ↑ ⇒ SOT delay time	t_{DEE}			0	-	ns	

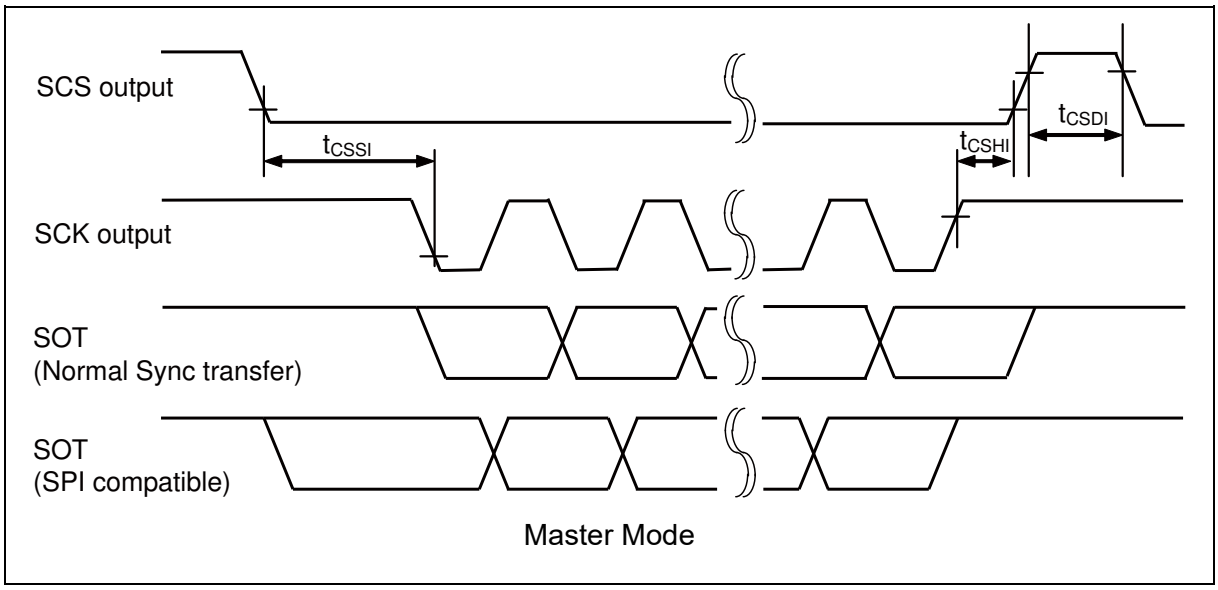
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

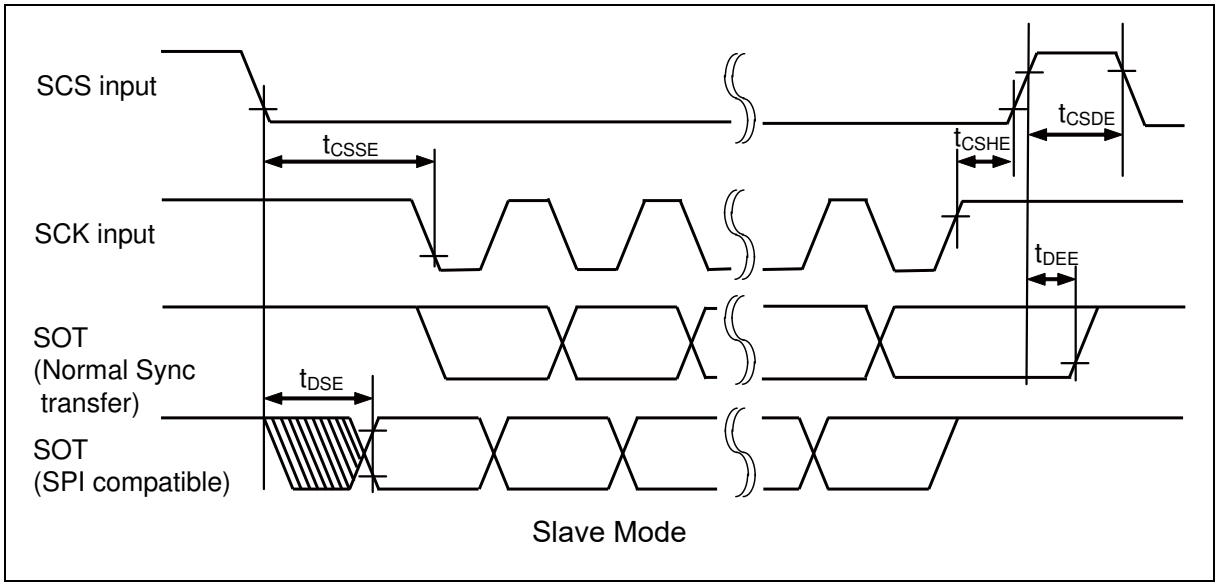
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L" (SMR:SCINV=1)
- Serial chip select inactive level "H" (SCSCR:CSLVL=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, VSS=AVSS=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Master mode C_L=50pF	t_{CSSU}*1+0	t_{CSSU}*1+50	ns	
SCK ↓ ⇒ SCS ↑ hold time	t_{CSHI}			t_{CSHD}*2-50	t_{CSHD}*2+0	ns	
SCS deselect time	t_{CSDI}	SCS1, SCS2*4, SCS3*4		-50+5t_{CPP} +t_{CSDS}*3	+50+5t_{CPP} +t_{CSDS}*3	ns	
SCS ↓ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↓ ⇒ SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS1, SCS2*4, SCS3*4		3t_{CPP}+30	-	ns	
SCS ↓ ⇒ SOT delay time	t_{DSE}	SCS1, SCS2*4, SCS3*4, SOT1, SOT2*4, SOT3*4		-	40	ns	
SCS ↑ ⇒ SOT delay time	t_{DEE}			0	-	ns	

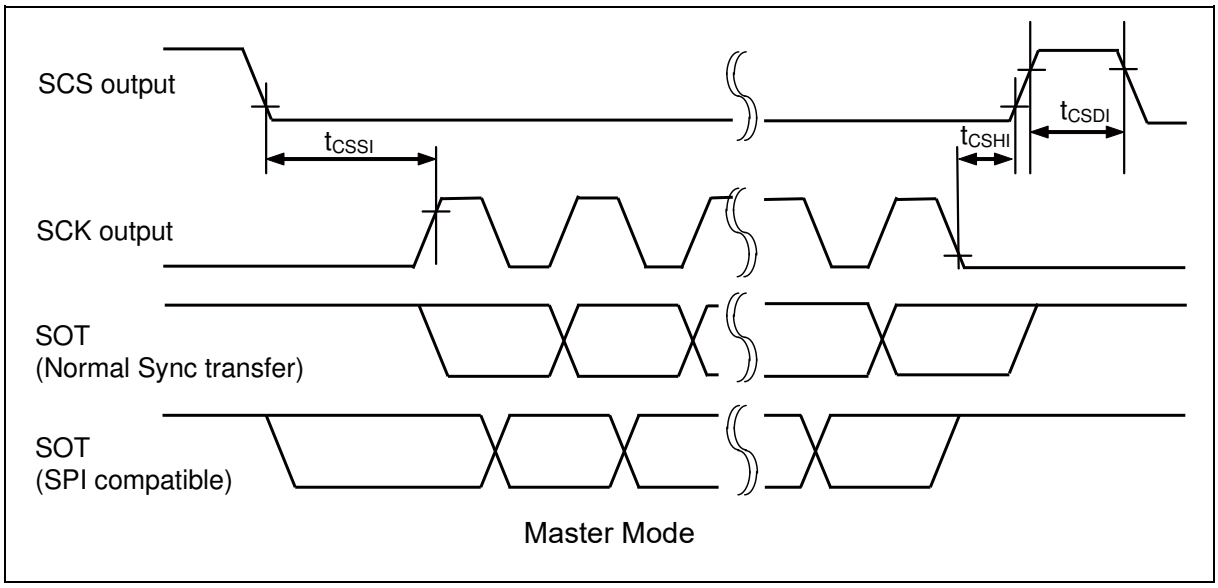
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

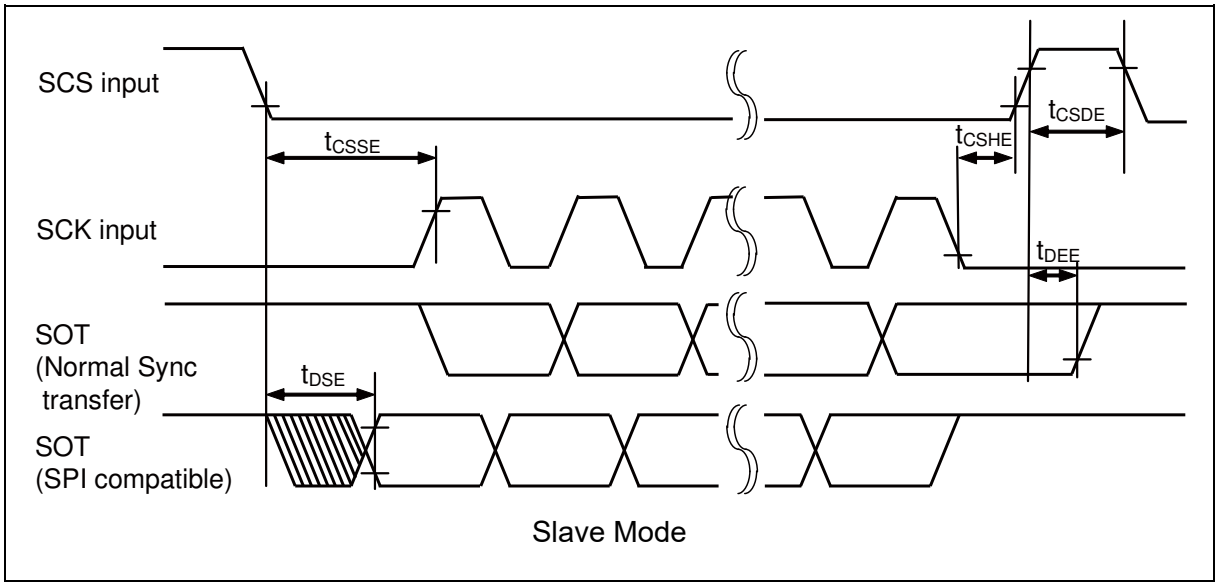
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H" (SMR:SCINV=0)
- Serial chip select inactive level "L" (SCSCR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↓ setup time	t_{CSSI}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Master mode C_L=50pF	t_{CSSU}*1+0	t_{CSSU}*1+50	ns	
SCK ↑ ⇒ SCS ↓ hold time	t_{CSHI}			t_{CSHD}*2-50	t_{CSHD}*2+0	ns	
SCS deselect time	t_{CSDI}	SCS1, SCS2*4, SCS3*4		-50+5t_{CPP} +t_{CSDS}*3	+50+5t_{CPP} +t_{CSDS}*3	ns	
SCS ↑ ⇒ SCK ↓ setup time	t_{CSSE}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↑ ⇒ SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS1, SCS2*4, SCS3*4		3t_{CPP}+30	-	ns	
SCS ↑ ⇒ SOT delay time	t_{DSE}	SCS1, SCS2*4, SCS3*4, SOT1, SOT2*4, SOT3*4		-	40	ns	
SCS ↓ ⇒ SOT delay time	t_{DEE}			0	-	ns	

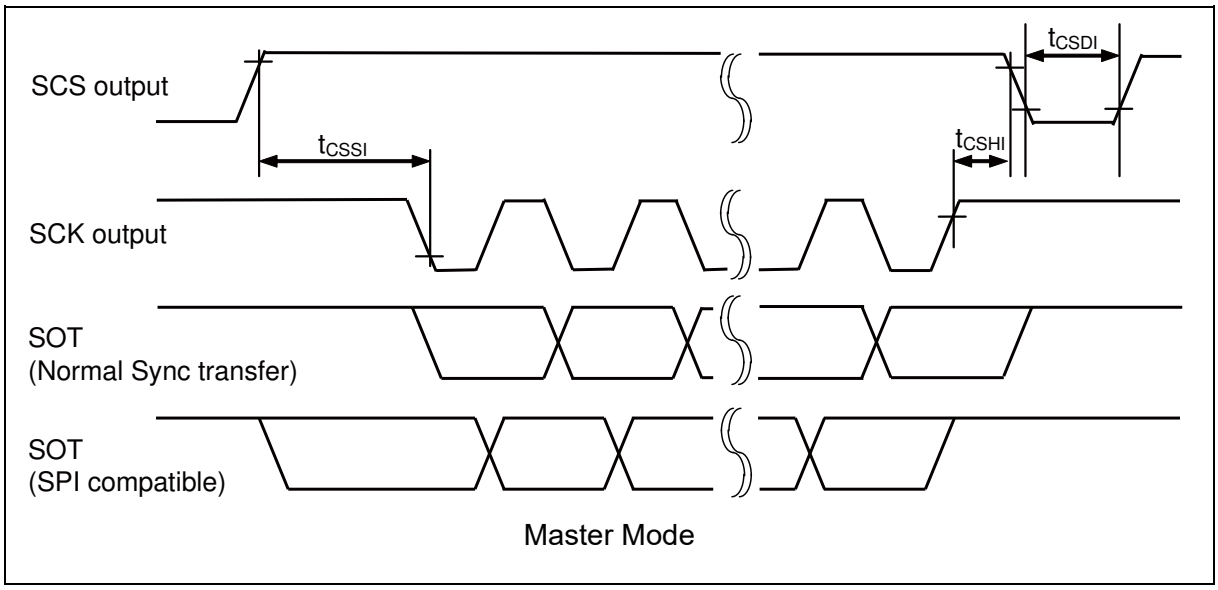
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

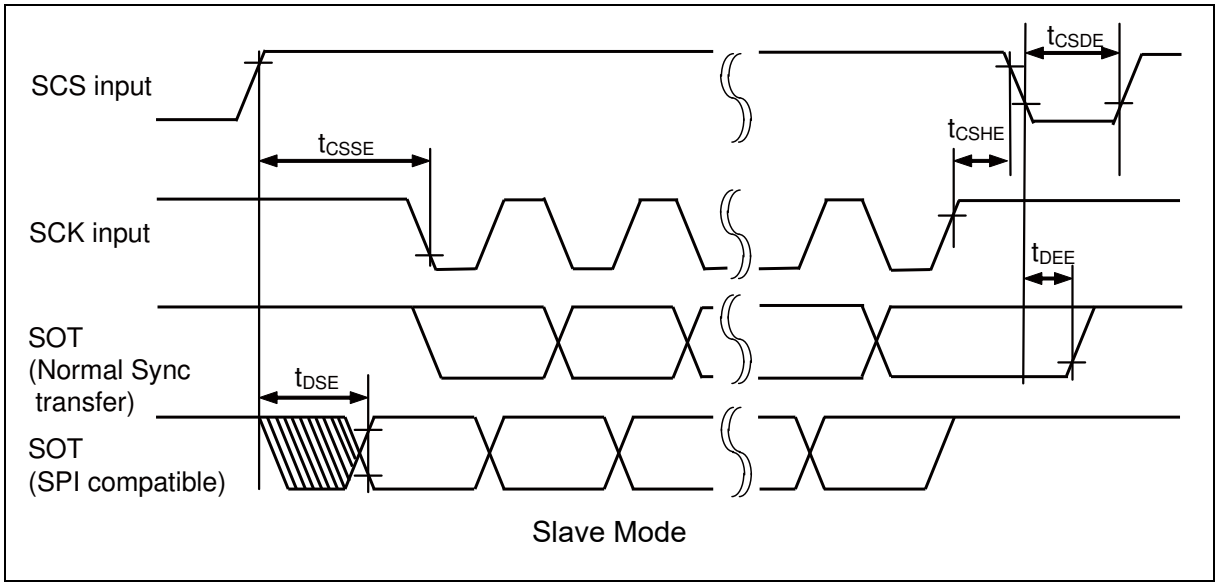
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.


SCS output
SCK output
SOT
(Normal Sync transfer)
SOT
(SPI compatible)
tCSSI
tCSHI
tCSDI
Master Mode


SCS input
SCK input
SOT
(Normal Sync
transfer)
SOT
(SPI compatible)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
Slave Mode

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L" (SMR:SCINV=1)
- Serial chip select inactive level "L" (SCSCR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Master mode C_L=50pF	t_{CSSU}*1+0	t_{CSSU}*1+50	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHI}			t_{CSHD}*2-50	t_{CSHD}*2+0	ns	
SCS deselect time	t_{CSDI}	SCS1, SCS2*4, SCS3*4		-50+5t_{CPP} +t_{CSDS}*3	+50+5t_{CPP} +t_{CSDS}*3	ns	
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1, SCK2*4, SCK3*4, SCS1, SCS2*4, SCS3*4	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS1, SCS2*4, SCS3*4		3t_{CPP}+30	-	ns	
SCS ↑ ⇒ SOT delay time	t_{DSE}	SCS1, SCS2*4, SCS3*4, SOT1, SOT2*4, SOT3*4		-	40	ns	
SCS ↓ ⇒ SOT delay time	t_{DEE}			0	-	ns	

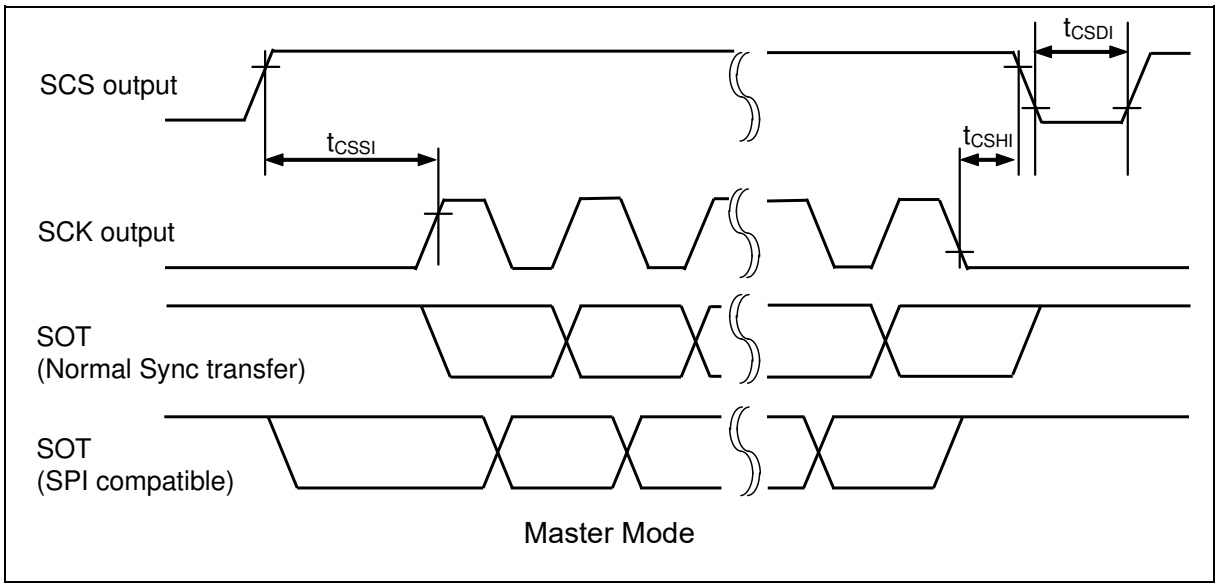
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

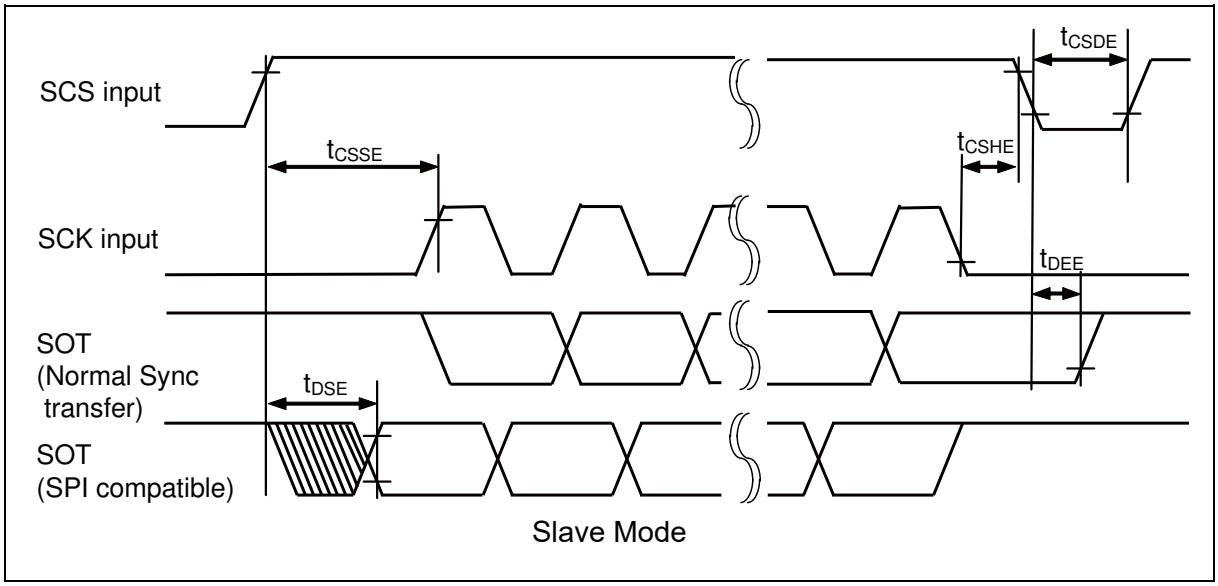
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode

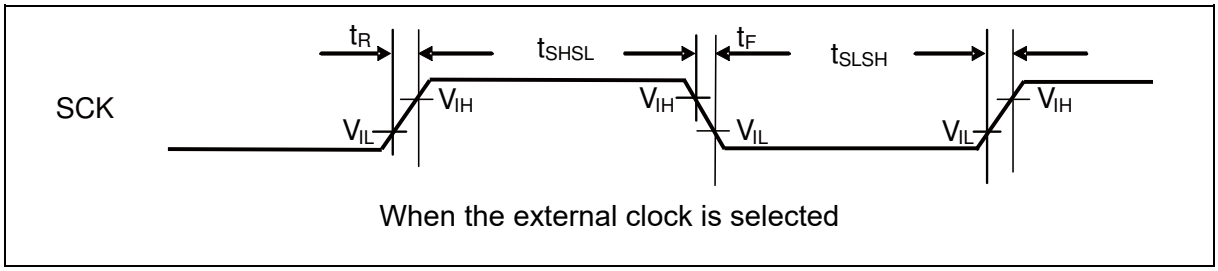
UART (Async Serial Interface) timing (SMR:MD2-0="000"b, "001"b)

When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM



When the external clock is selected

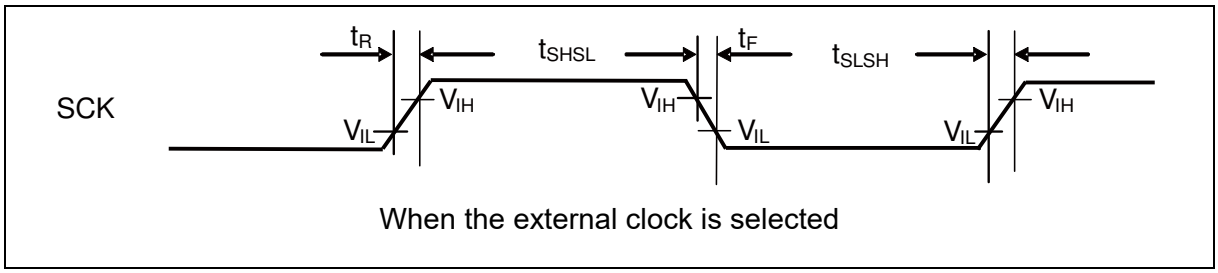
LIN interface (v2.1)(LIN Communication Control Interface (v2.1)) timing (SMR:MD2-0="011"b)

When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM



When the external clock is selected

I²C timing (SMR:MD2-0="100"b)

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Standard mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0_0, SCK0_1*5, SCK2*5, SCK3*5 (SCL)	C_L=50pF R=(V_P/I_{OL}) *1	0	100	0	400	kHz	
"Repeat START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}	SCK0_0, SCK0_1*5, SCK2*5, SCK3*5 (SCL) SOT0_0, SOT0_1*5, SOT2*5, SOT3*5 (SDA)		4.0	-	0.6	-	µs	
"L" width for SCL clock	t_{LOW}	SCK0_0, SCK0_1*5, SCK2*5, SCK3*5 (SCL)		4.7	-	1.3	-	µs	
"H" width for SCL clock	t_{HIGH}			4.0	-	0.6	-	µs	
"Repeat START condition" setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0_0, SCK0_1*5, SCK2*5, SCK3*5 (SCL) SOT0_0, SOT0_1*5, SOT2*5, SOT3*5 (SDA)		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}			0	3.45 *2	0	0.90 *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}			250	-	100	-	ns	
"STOP condition" setup time SCL ↑ → SDA ↑	t_{SUSTO}			4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}	-		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-		$2t_{CPP}$ *4	-	$2t_{CPP}$ *4	-	ns	

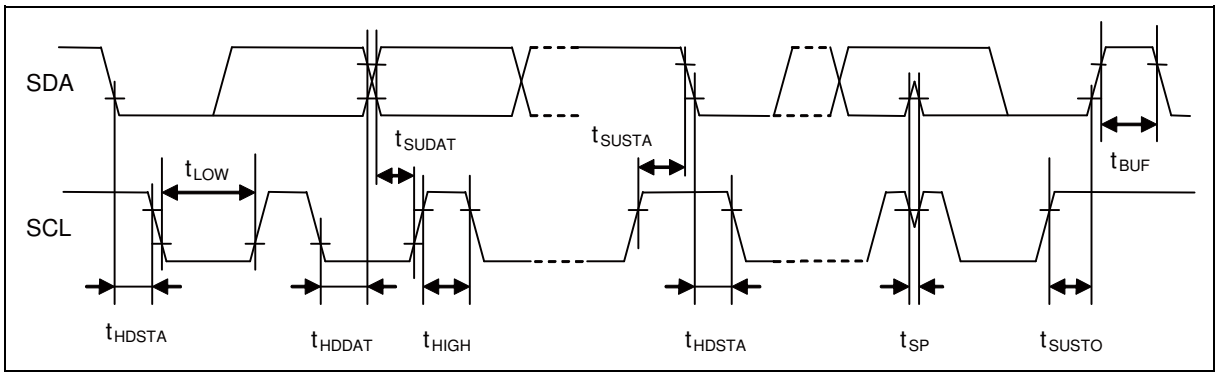
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. V_P shows that the power supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the peripheral bus to 8MHz or more when using I²C.

*5: Only available with CY91F583AM/F584AM/F585AM

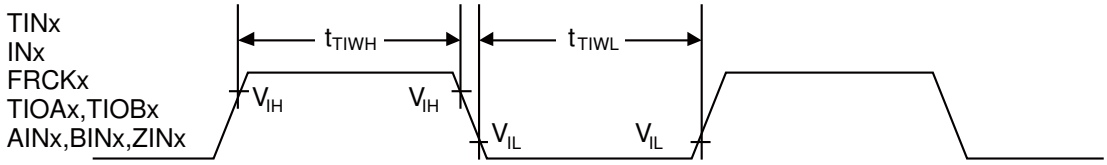


11.4.5 Timer Input Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN3, IN0 to IN3, FRCK0 to FRCK5, TIOA1, TIOB0, TIOB1	-	$4t_{CPP}$	-	ns	
		AIN0,AIN1, BIN0,BIN1, ZIN0,ZIN1	-	$2t_{CPP}$	-	ns	

■ Timer input timing



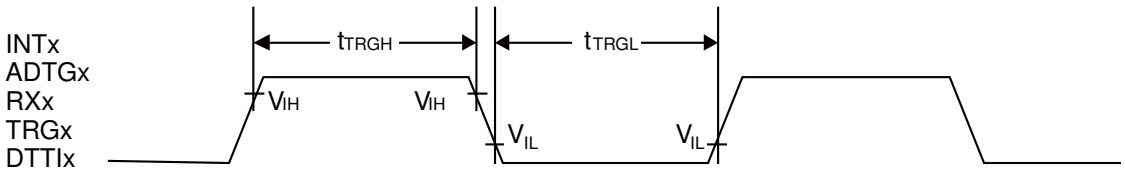
11.4.6 Trigger Input Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10% V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT6, INT7*, ADTG0 to ADTG2, RX0, RX1*, TRG0, TRG1,	-	$5t_{CPP}$	-	ns	
				1	-	µs	At Stop mode

*: Only available with CY91F583AM/F584AM/F585AM

■ Trigger input timing

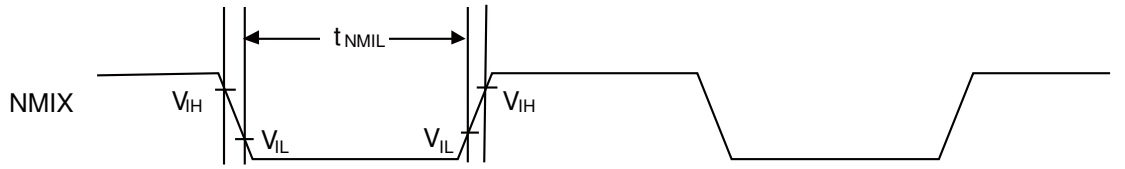


11.4.7 NMI Input Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	$4t_{CPP}$	-	ns	

■ NMIX input timing



11.4.8 Low-voltage Detection (External Low-voltage Detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC5	-	3.7	-	5.5	V	
Detection voltage	V_{DL}	VCC5	*1	-8%	3.9	+8%	V	When power supply voltage falls and detection level is set initially
Hysteresis width	V_{HYS}	VCC5	-	-	0.1	-	V	When power supply voltage rises
Low-voltage detection time	Td	-	-	-	-	30	µs	
Power supply voltage fluctuation rate	-	VCC5	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (Td), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply within the limits of the power supply voltage fluctuation rate.

11.4.9 Low-voltage Detection (Internal Low-voltage Detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	1.1	-	1.3	V	
Detection voltage	V_{RDL}	-	*	0.8	0.9	1.0	V	When power supply voltage falls
Hysteresis width	V_{RHYS}	-	-	-	0.1	-	V	When power supply voltage rises
Low-voltage detection time	-	-	-	-	-	30	µs	

*: If the fluctuation of the power supply is faster than the low-voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.5 A/D Converter

11.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	-4.0	-	+4.0	LSB	
Differential linearity error	-	-	-1.9	-	+1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN14, AN16 to AN18*3, AN19, AN20, AN21 to AN23*3	AVRL+ 0.5LSB-20	-	AVRL+ 0.5LSB+20	mV	1LSB= (VFST-VOT)/4094
Full-scale transition voltage	V_{FST}	AN0 to AN14, AN16 to AN18*3, AN19, AN20, AN21 to AN23*3	AVRH-1.5LSB-20	-	AVRH-1.5LSB+20	mV	
Sampling time	t_{SMP}	-	0.3	-	12	µs	*1
Compare time	t_{CMP}	-	0.7	-	28	µs	*1
A/D conversion time	t_{CNV}	-	1.0	-	40	µs	*1
Analog port input current	I_{AIN}	AN0 to AN14, AN16 to AN18*3, AN19, AN20, AN21 to AN23*3	-1.0	-	1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN14, AN16 to AN18*3, AN19, AN20, AN21 to AN23*3	AV_{SS}	-	AVRH	V	
Reference voltage	AVRH	AVRH0, AVRH1	4.5	-	5.5	V	Avcc ≥ AVRH
	AVRL	AVRL0, AVRL1,	-	0.0	-	V	
Power supply current	I_A	AVCC0, AVCC1	-	1.5	2.1	mA	3 units operating
	I_{AH}		-	-	25	µA	3 units operating*2
	I_R	AVRH0, AVRH1	-	3	6	mA	3 units operating
	I_{RH}		-	-	4.8	µA	3 units operating*2
Variation between channels	-	AN0 to AN14, AN16 to AN18*3, AN19, AN20, AN21 to AN23*3	-	-	4	LSB	Every 1 unit*4

*1: Time for each channel.

*2: The Power supply current (Vcc=AVcc=5.0V) is specified if the A/D converter is not operating and CPU is stopped.

*3: Only available with CY91F583AM/F584AM/F585AM

*4: Unit0 AN0 to AN7

Unit1 AN8 to AN14

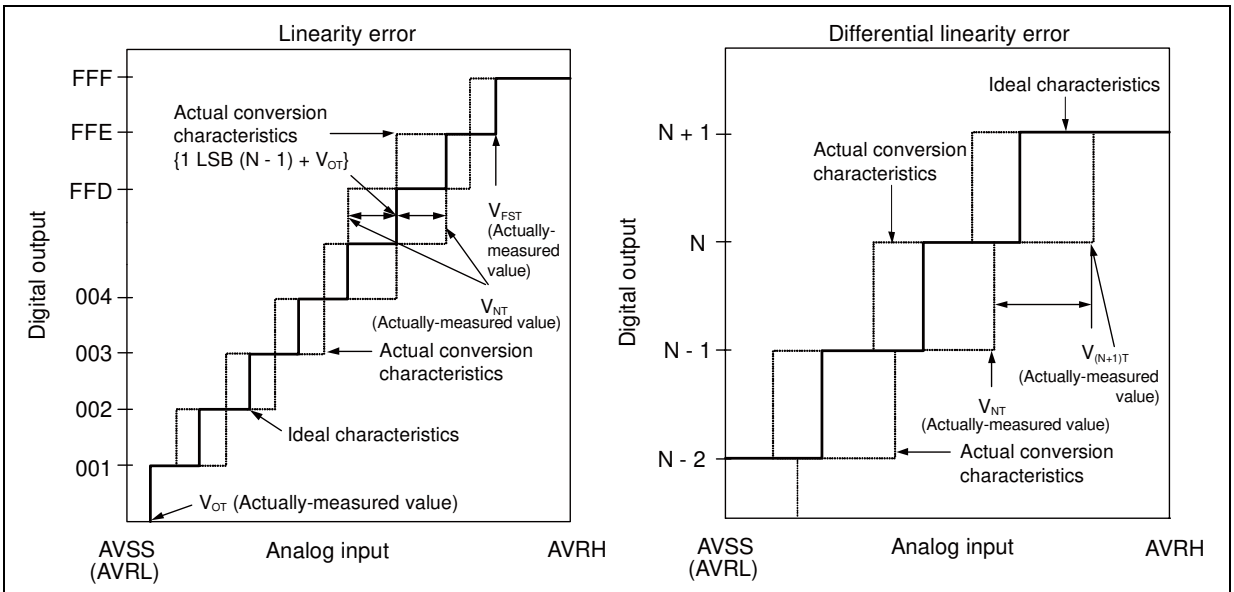
Unit2 AN16 to AN23

11.5.2 Definition of Terms

Resolution: Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"←→"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"←→"1111 1111 1111").

Differential linearity error: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\}}{1LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1\ LSB \quad [LSB]$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \quad [V]$$

V_{OT}: Voltage at which the digital output changes from "000_H" to "001_H".

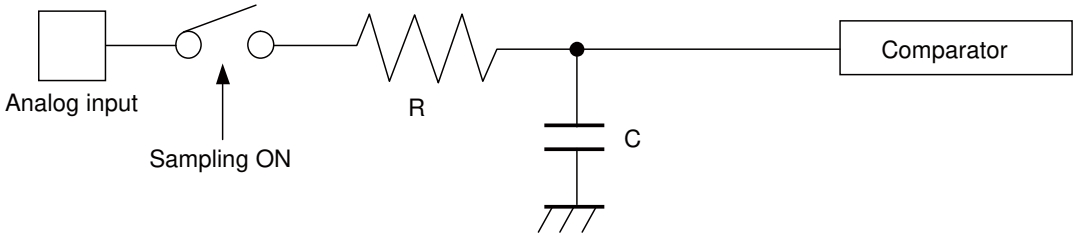
V_{FST}: Voltage at which the digital output changes from "FFE_H" to "FFF_H".

11.5.3 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

● Analog input circuit model



	R	C
12bit A/D	1.9kΩ (max)	8.3pF (max) (4.5V≦Avcc≦5.5V)

Note: Listed values must be considered as reference values.

11.6 D/A Converter

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Differential linearity error	-	-	-4.0	-	+4.0	LSB	When the analog output voltage is 0.5V to 4.5V

11.7 Flash memory

11.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	200	800	ms	8 Kbyte sector*1 excluding internal preprogramming time
	-	300	1100	ms	8 Kbyte sector*1 including internal preprogramming time
	-	400	2000	ms	64 Kbyte sector*1 excluding internal preprogramming time
	-	700	3700	ms	64 Kbyte sector*1 including internal preprogramming time
8-bit writing time	-	9	288	µs	Excluding overhead time at system level*1
16-bit writing time	-	12	384	µs	Excluding overhead time at system level*1
ECC writing time	-	9	288	µs	Excluding overhead time at system level*1
Erase cycle*2/ Data retention time	1,000 cycles/20 years, 10,000 cycles/10 years, 100,000 cycles/5 years	-	-	-	Average temperature T_A=+85°C *3

*1: The guaranteed value for erase up to 100,000 cycles

*2: Number of erase cycles for each sector

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

11.7.2 Notes

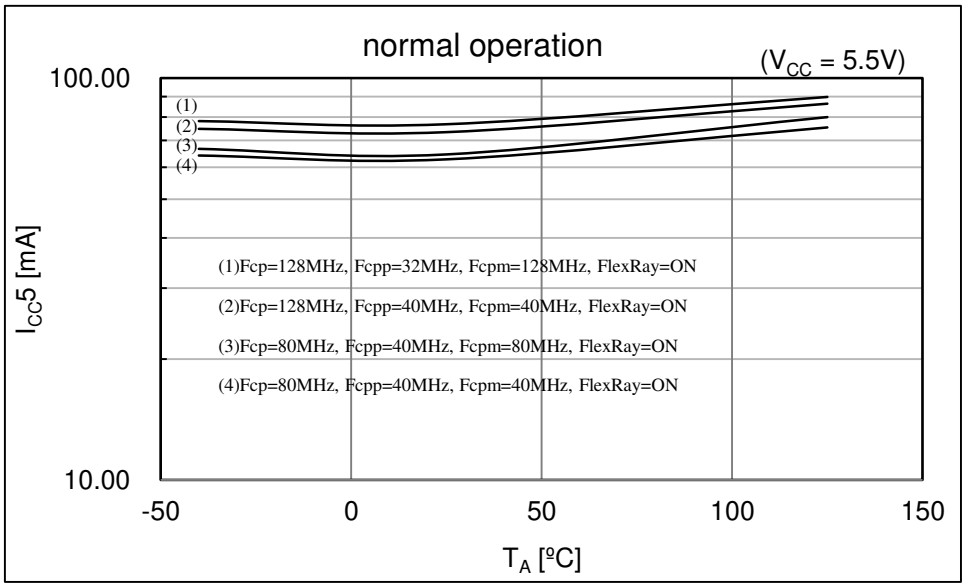
While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.
In the application system where Vcc might disappear while writing or erasing, be sure to turn the power off by using an external low-voltage detection function.
To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

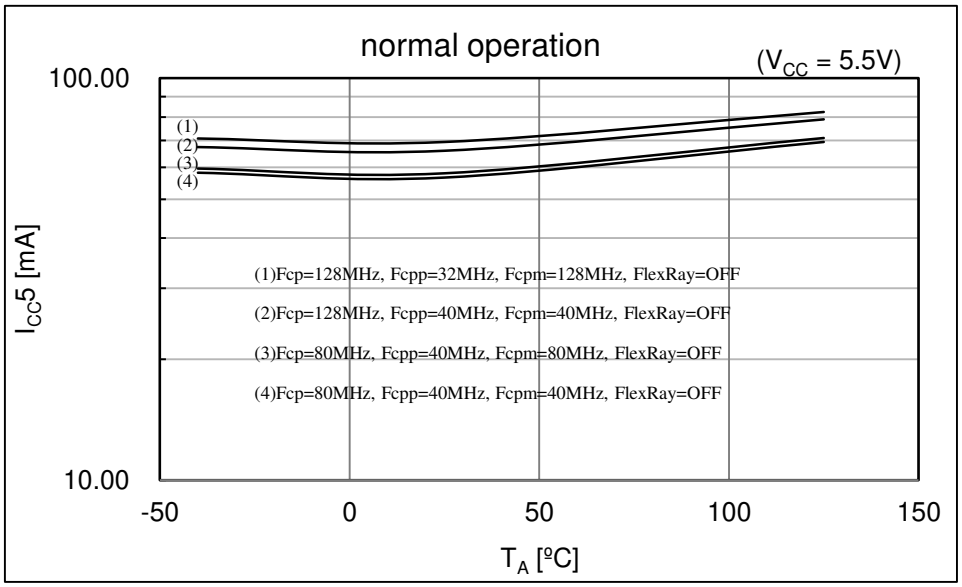
Td*[µs] + (PCLK cycle[µs] × 257) + 50[µs]

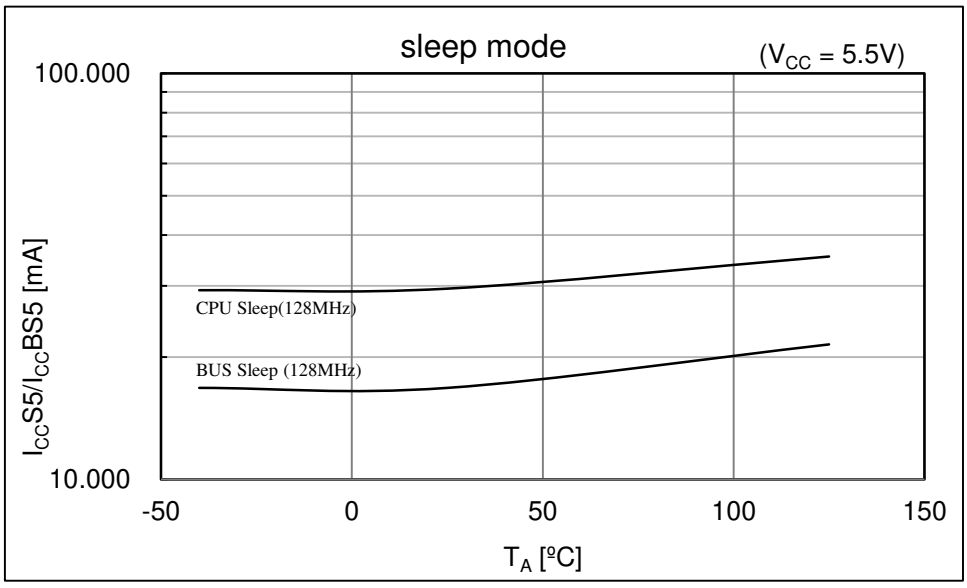
*: See "4. AC characteristics (8) Low-voltage detection (External low-voltage detection)."

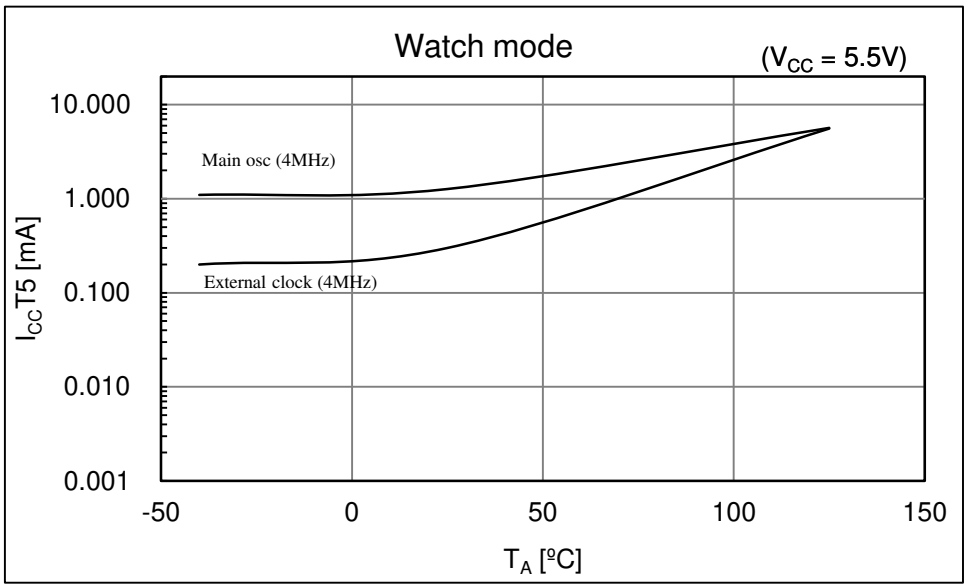
12. Example Characteristics

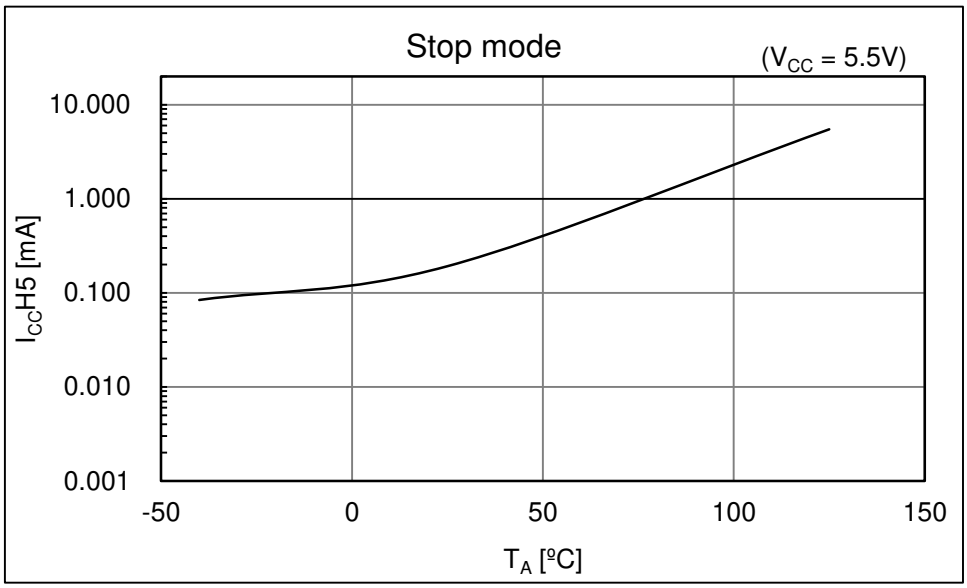
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

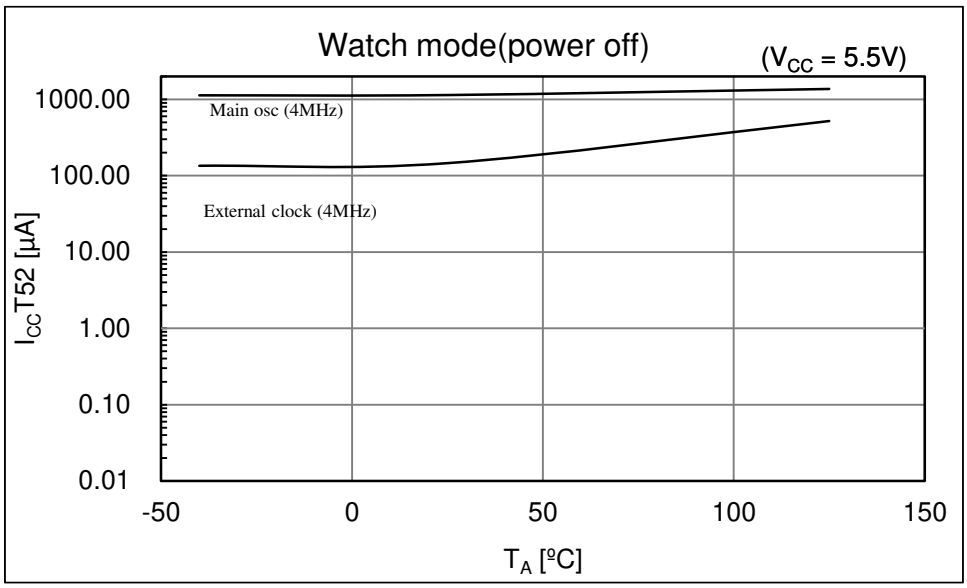


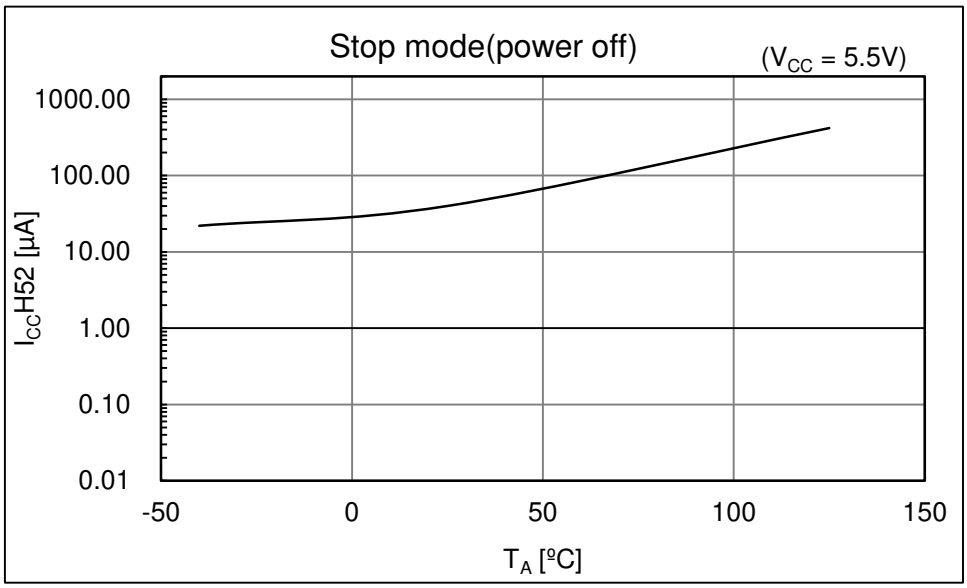



sleep mode
(V_{CC} = 5.5V)
100.000
10.000
$I_{CC}S5/I_{CC}BS5$ [mA]
CPU Sleep(128MHz)
BUS Sleep (128MHz)
-50
0
50
100
150
T_A [ºC]


Watch mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
Main osc (4MHz)
External clock (4MHz)
I_{CC}T5 [mA]
-50
0
50
100
150
T_A [ºC]


Stop mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}H5 [mA]
-50
0
50
100
150
T_A [ºC]


Watch mode(power off)
(VCC = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
Main osc (4MHz)
External clock (4MHz)
ICCT52 [µA]
-50
0
50
100
150
TA [ºC]


Stop mode(power off)
(VCC = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
ICCH52 [µA]
-50
0
50
100
150
TA [ºC]

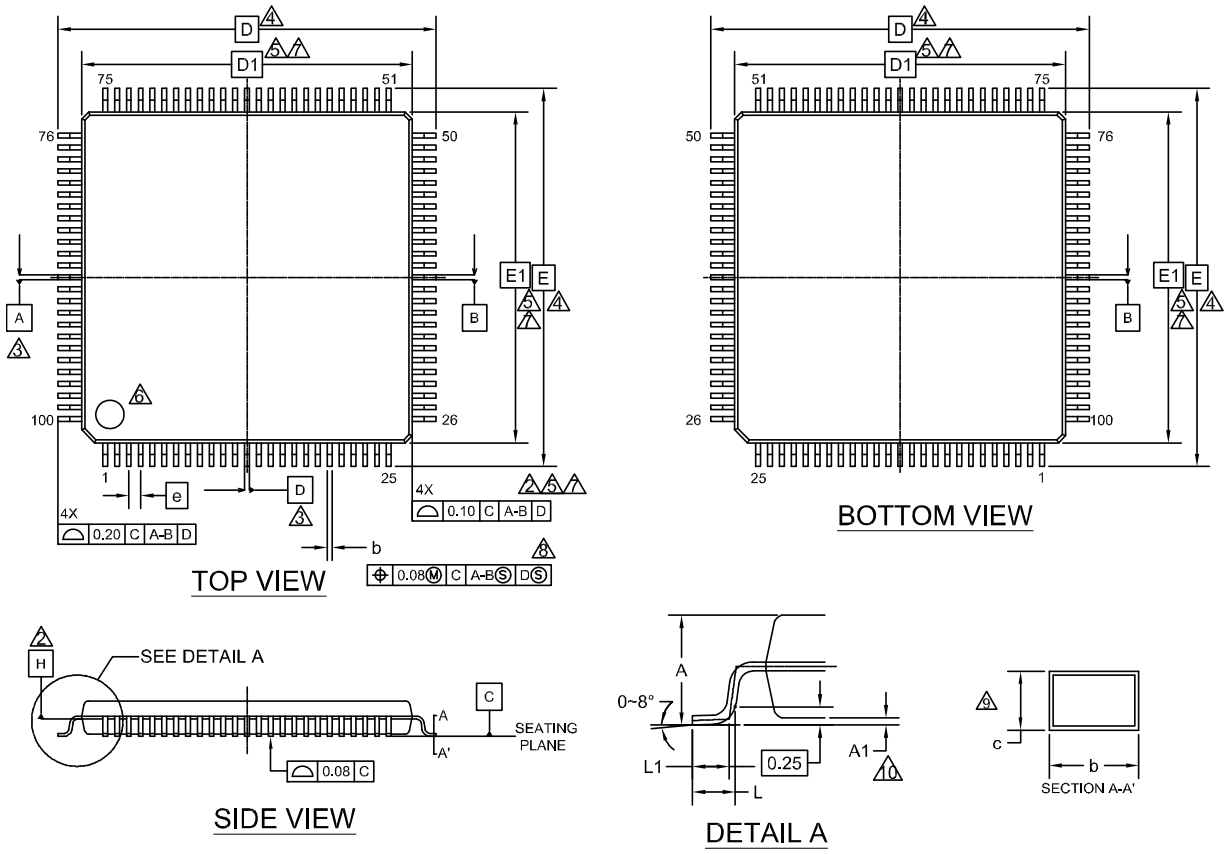
13. Ordering Information

Part number	Package*
CY91F583AMGPMC-GTE1 CY91F584AMGPMC-GTE1 CY91F585AMGPMC-GTE1 CY91F583AMHPMC-GTE1 CY91F584AMHPMC-GTE1 CY91F585AMHPMC-GTE1 CY91F583AMJPMC-GTE1 CY91F584AMJPMC-GTE1 CY91F585AMJPMC-GTE1 CY91F583AMKPMC-GTE1 CY91F584AMKPMC-GTE1 CY91F585AMKPMC-GTE1	100-pin plastic LQFP (LQI100)
CY91F583ASGPMC1-GTE1 CY91F584ASGPMC1-GTE1 CY91F585ASGPMC1-GTE1 CY91F583ASHPMC1-GTE1 CY91F584ASHPMC1-GTE1 CY91F585ASHPMC1-GTE1 CY91F583ASJPMC1-GTE1 CY91F584ASJPMC1-GTE1 CY91F585ASJPMC1-GTE1 CY91F583ASKPMC1-GTE1 CY91F584ASKPMC1-GTE1 CY91F585ASKPMC1-GTE1	64-pin plastic LQFP (LQD064)

*: For details of the package, see Package Dimensions

14. Package Dimensions

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.25
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

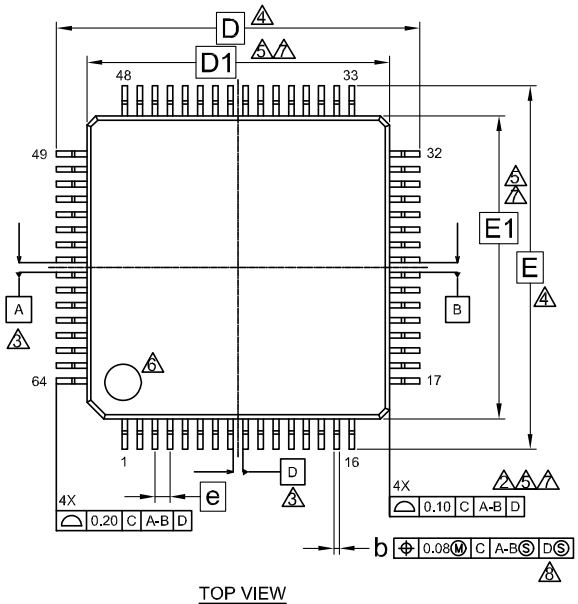
NOTES :

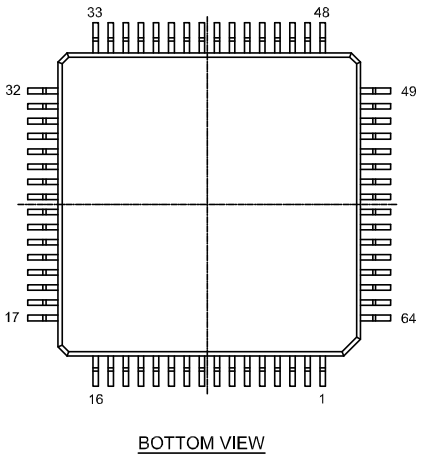
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

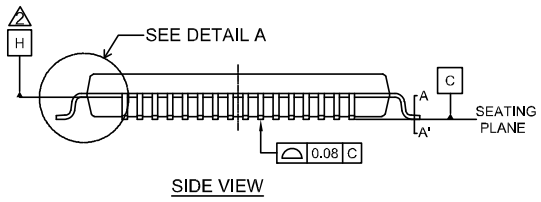
002-25980 **

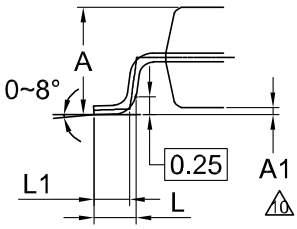
PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 for legacy MB product

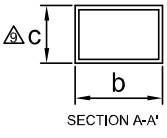
Package Type	Package Code
LQFP 64	LQD064











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.25
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-25982 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 for legacy MB product

15. Major Changes

Spansion Publication Number: MB91F585AMG_DS705-00013

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
-	-	The product series name should be corrected. MB91F585MG → MB91F585AMG MB91F585MH → MB91F585AMH MB91F585MJ → MB91F585AMJ MB91F585MK → MB91F585AMK MB91F584MG → MB91F584AMG MB91F584MH → MB91F584AMH MB91F584MJ → MB91F584AMJ MB91F584MK → MB91F584AMK MB91F583MG → MB91F583AMG MB91F583MH → MB91F583AMH MB91F583MJ → MB91F583AMJ MB91F583MK → MB91F583AMK MB91F585SG → MB91F585ASG MB91F585SH → MB91F585ASH MB91F585SJ → MB91F585ASJ MB91F585SK → MB91F585ASK MB91F584SG → MB91F584ASG MB91F584SH → MB91F584ASH MB91F584SJ → MB91F584ASJ MB91F584SK → MB91F584ASK MB91F583SG → MB91F583ASG MB91F583SH → MB91F583ASH MB91F583SJ → MB91F583ASJ MB91F583SK → MB91F583ASK
2	Features	The features of CR oscillation should be corrected. Oscillation frequency: 100kHz, with frequency accuracy ± 10% ↓ Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)
22	I/O Circuit Type	The specification of "H" level input voltage and "L" level input voltage of FlexRay should be corrected. FlexRay input (0.65Vcc/0.35Vcc) ↓ FlexRay input (0.7Vcc/0.3Vcc)
33	Memory Map	The memory map should be corrected. The address of "Reset vector table" and "Interrupt vector table" should be added
54,85	I/O Map Address:00150C$_H$	The register name should be corrected. STMCR00 → STMCR0

Page	Section	Change Results
54,55,85	I/O Map Address: 00150 $E_{H,}$ $001510_{H,}$ $001511_{H,}$ $001512_{H,}$ 001513_{H}	The registers should be deleted. SCS CR0,SCSTR30,SCSTR20,SCSTR10,SCSTR00
63,92	I/O Map Address:$00D310_{H}$	The initial values of MHDS should be corrected. -0000000 -0000000 -0000000 10000000 ↓ -0000000 -0000000 -0000000 00000000
104	Electrical Characteristics DC Caharacteristics	The specification of "H" level input voltage of P021-P023,P025-P027 should be corrected. Min:0.65 ×Vcc ↓ Min: 0.7 × Vcc
105	Electrical Characteristics DC Caharacteristics	The specification of "L" level input voltage of P021-P023,P025-P027 should be corrected. Max: 0.35 × Vcc ↓ Max: 0.3 × Vcc
111	Electrical Characteristics AC Characteristics Main Clock Timing	The remarks of "CAN PLL jitter" should be deleted.
111	Electrical Characteristics AC Characteristics Main Clock Timing	The specifications of "The Built-in CR oscillation frequency" should be corrected. Min: 90kHz, Max: 110kHz ↓ Min:50kHz Max:150kHz,
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY91F583AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK, CY91F584AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK, CY91F585AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK, CY91580M/S Series FR81S, 32-bit Microcontroller Datasheet
Document Number: 002-04665

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KOJM	04/18/2014	Migrated to Cypress and assigned document number 002-04665. No change to document contents or format.
*A	5139690	KOJM	03/29/2016	Updated to Cypress template
*B	6508924	KOJM	03/20/2019	Marketing Part Numbers changed from prefix MB to prefix CY. Updated the 100-pin, 64-pin Package Dimensions.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support