

## **DAC9881 Evaluation Module**

This user's guide describes the characteristics, operation, and the use of the DAC9881 Evaluation Module (EVM). It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

### **Contents**

1	EVM Overview .....	2
	1.1 Features .....	2
	1.2 Power Requirements .....	2
	1.3 EVM Basic Functions .....	3
2	PCB Design and Performance .....	4
	2.1 PCB Layout .....	4
3	EVM Performance .....	7
4	Bill of Materials .....	9
5	EVM Operation .....	10
	5.1 Factory Default Setting .....	10
	5.2 Host Processor Interface .....	11
	5.3 Digital Control Interface .....	11
	5.4 Analog Output .....	12
	5.5 Jumper Setting .....	14
	5.6 DAC9881EVM Schematic .....	16
6	Using the DAC9881EVM with DXP .....	16
	6.1 Hardware .....	16
	6.2 MMB0 Power Supplies .....	17
	6.3 Software – Running DXP .....	18
7	Related Documentation From Texas Instruments .....	19

### **List of Figures**

1	Block Diagram .....	4
2	Top Silkscreen.....	5
3	Layer 1, Top Signal Plane .....	6
4	Layer 2, Ground Plane .....	6
5	Layer 3, Power Plane .....	7
6	Layer 4, Bottom Signal Plane .....	7
7	Bottom Silkscreen.....	7
8	INL and DNL Characteristic Plot .....	8
9	DAC9881 EVM Default Jumper Configuration.....	10
10	MMB0 with DAC9881EVM Installed .....	17
11	Loading the DAC9881EVM INI File .....	18
12	DAC9881 – Frequency/Amplitude and GPIO Control Options .....	19

### **List of Tables**

1	Parts Lists .....	9
2	Factory Default Jumper Setting.....	10
3	Digital Control Interface Signal Mapping for J2/P2 Connectors .....	11

4	Bipolar Output Operation Jumper Settings.....	13
5	Gain of Two Output Jumper Settings .....	13
6	Capacitive Load Drive Output Jumper Settings .....	13
7	Jumper Setting Function.....	14

## 1 EVM Overview

This section gives a general overview of the DAC9881 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

### 1.1 Features

This EVM features the DAC9881 digital-to-analog converter (DAC). The DAC9881EVM is a simple evaluation module designed for quick and easy evaluation of the functionality and performance of the 18-bit, high-resolution, voltage-output, single-channel, and serial input DAC. This EVM features a high-speed serial interface of up to 50 MHz to communicate with any host microprocessor or DSP-based system.

The DAC9881 is designed to work by default for unipolar output range, but it can also be configured for bipolar output range with the addition of an external amplifier and some resistors. The option for bipolar mode of operation is included in the EVM with some minor jumper configuration.

A +5-V precision voltage reference is provided on the board via U3 (REF5050) to supply the necessary external reference voltage to set the DAC9881 output range. The footprint of U3 is compatible with many SO-8 package type reference devices. The user has the flexibility to select the reference supply to set the output range of the DAC9881 differently than what is provided on the board. The family of REF50xx precision reference sources work well with this EVM. In addition, the provision of test points TP1 and TP8, allow users to use their own external reference supply. Typically, TP1 ( $V_{REFL}$ ) must be connected to ground, but it can accept up to  $\pm 0.2$  V, if necessary. The test point, TP8 ( $V_{REFH}$ ), is typically set to +5 V, but can accept a minimum of +1.25 V and up to a maximum of +5.5 V.

The voltage reference configuration implemented on this EVM uses the Kelvin connection feature of the DAC9881 device. This connection helps minimize the internal errors caused by the changing reference current and its associated circuit impedances.

### 1.2 Power Requirements

The following sections describe the power requirements of this EVM.

#### 1.2.1 Supply Voltage

The dc power supply requirement for this DAC9881EVM ( $AV_{DD}$  and  $DV_{DD}$ ) is selectable between +3.3 VA and +5 VA via W1 jumper header. The +3.3 VA comes from J6-8, and the +5 VA comes from J6-3. These power supply voltages are referenced to analog ground through J6-5 and J6-6.

The logic voltage,  $IOV_{DD}$ , is selectable between +1.8 VD, +3.3 VD and +5 VD via the J3 jumper.

The  $V_{CC}$  and  $V_{SS}$  that ranges from +15-V to -15-V maximum connect through J6-1 and J6-2 terminals, respectively. All the analog power supplies are referenced to analog ground through J3-6.

#### CAUTION

To avoid potential damage to the EVM board, ensure that the proper voltages are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

### 1.2.2 Reference Voltage

The DAC9881 requires an external reference source to set the DAC's operating voltage output range. Applying the desired voltage between the ranges of 1.25 V to  $AV_{DD}$  into the  $V_{REFH}$  pin sets the positive range of the DAC9881 output. Also, applying the desired voltage between the range of -0.2 V to +0.2 V into the  $V_{REFL}$  pin sets the negative range of the DAC9881 output, although the  $V_{REFL}$  pin must nominally be set to zero volts. The voltages applied into the  $V_{REFH}$  and  $V_{REFL}$  pins set the DAC9881's full output voltage swing.

For optimum performance, the DAC9881 supports a set Kelvin connection to the external reference via  $V_{REFHF}$  and  $V_{REFHS}$  pins, as well as  $V_{REFLF}$  and  $V_{REFLS}$  pins. This option for reference configuration minimizes the internal errors caused by the changing reference current and its associated circuit impedances.

A +5-V precision voltage reference is provided for the external reference source of the DAC through REF5050, U3. The power supply for the reference device, U3, is selectable between  $V_{CC}$  and +5 VA via W11 to ensure that the correct voltage range of U3 can be set. As mentioned earlier, the family of REF50xx reference devices may be used and the installed device on the EVM changed to provide the desired voltage range required.

The reference voltages,  $V_{REFH}$  and  $V_{REFL}$  are selectable via jumpers W8 and W4. When shorting pins 1 and 2 of both jumpers, the onboard +5-V reference via REF5050 is selected. Shorting pins 2 and 3 of both jumpers selects the reference voltages that are applied via J4 pins 18 and 20, respectively. These voltages normally come from the host platform that is used to interface with the DAC9881EVM.

The test points TP1 and TP8 are also provided to allow the user to connect other external reference sources if the onboard reference circuit is not desired. The external voltage reference must not exceed the applied power supplies,  $AV_{DD}$  and  $DV_{DD}$  of the DAC.

#### CAUTION

When applying an external voltage reference through TP8 or J4-20, ensure that it does not exceed the applied  $AV_{DD}$ . This can permanently damage the DAC9881, U1.

### 1.3 EVM Basic Functions

This EVM is designed as a functional evaluation platform to test certain characteristics of the DAC9881 digital-to-analog converter. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, DSP, or a signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC9881 EVM. All signals are routed through except SDI because of daisy-chain capability. SDI to the DAC9881 enters the P2 connector (located on the bottom side of the board) at pin 11 and is viewable on TP7. SDO from the DAC9881 exits the board at J1 pin 11 and is viewable on TP6.

An adapter interface card (5–6K Interface Board) is also available to fit and mate with TI's C5000™ and C6000™ DSP Starter Kit (DSK). This alleviates the building of a custom cable. In addition, the Precision Analog Application group of Texas Instruments has other interface boards that are designed to connect to and interface with this EVM as well. For more details or information regarding the 5-6K Interface Board, call Texas Instruments Incorporated or visit the product folder for the tool here: [5-6K Interface Board](#).

The DAC output can be monitored through pins 2 and 6 of the J4 connector. The DAC output can be switched through W2 for stacking the EVM for daisy-chaining purposes.

A block diagram of the EVM is shown in [Figure 1](#).



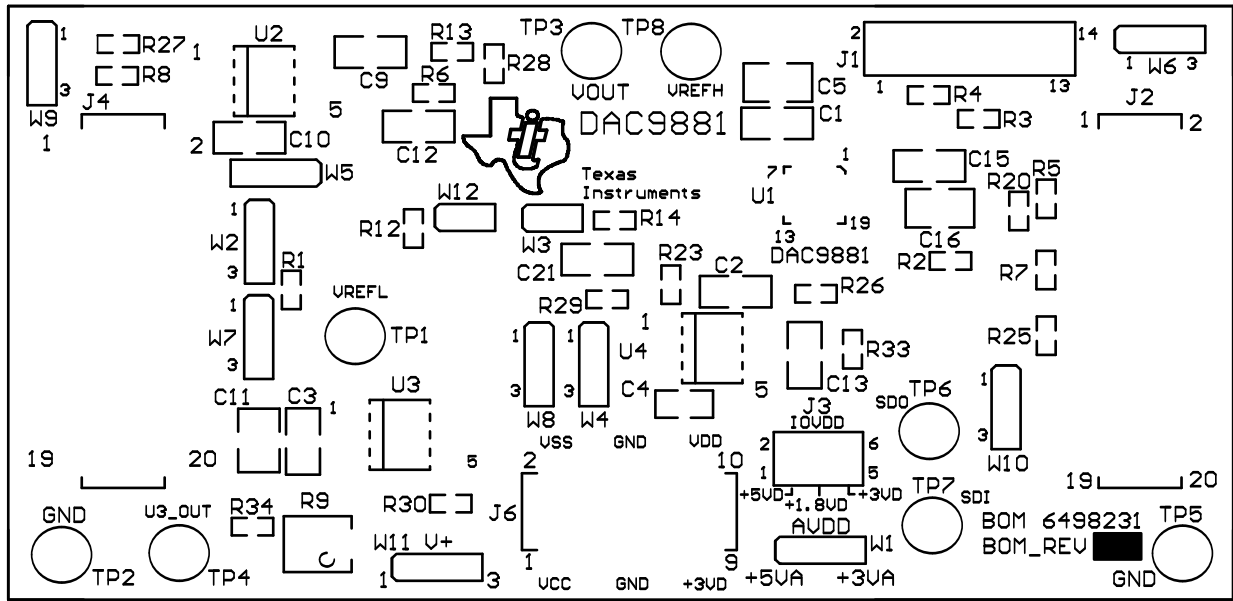


Figure 2. Top Silkscreen

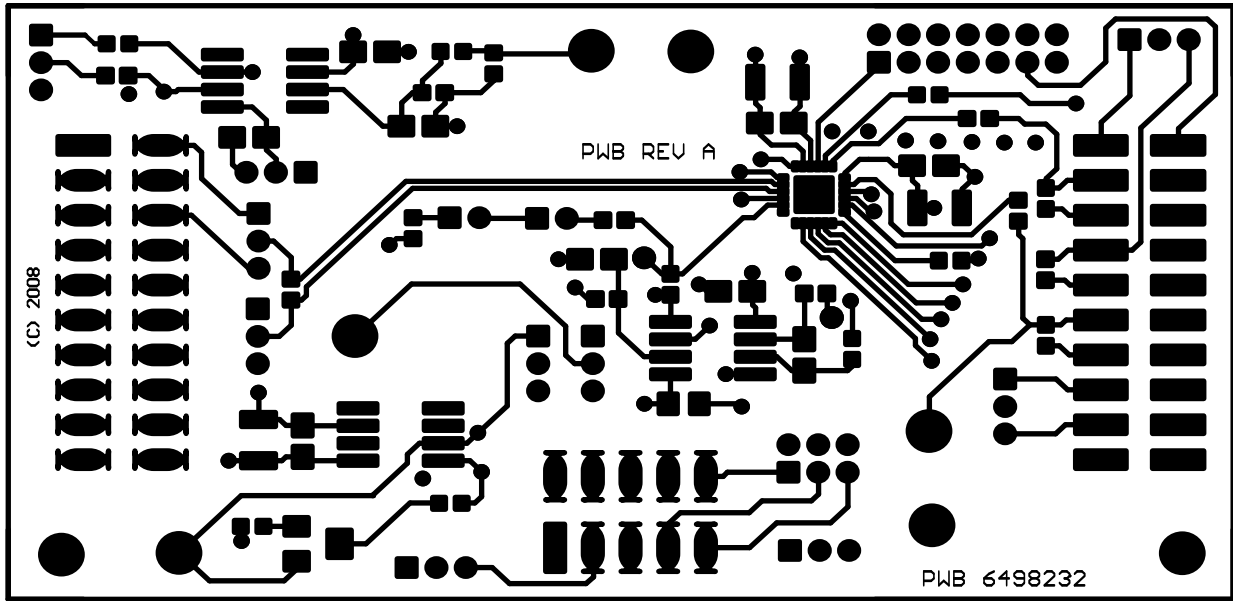


Figure 3. Layer 1, Top Signal Plane

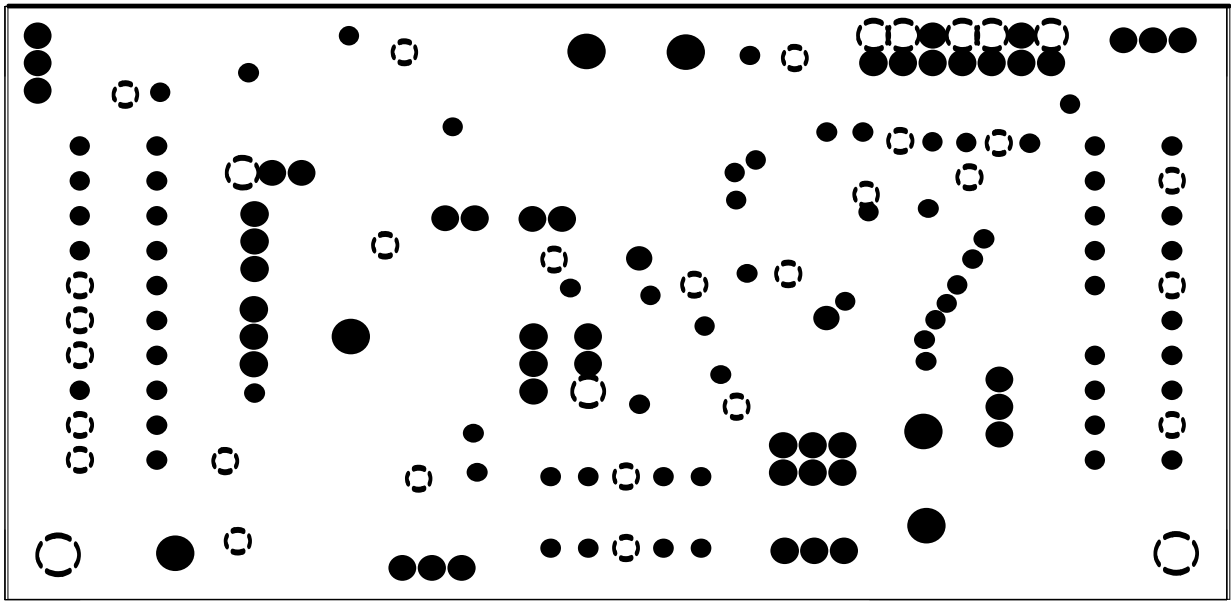


Figure 4. Layer 2, Ground Plane

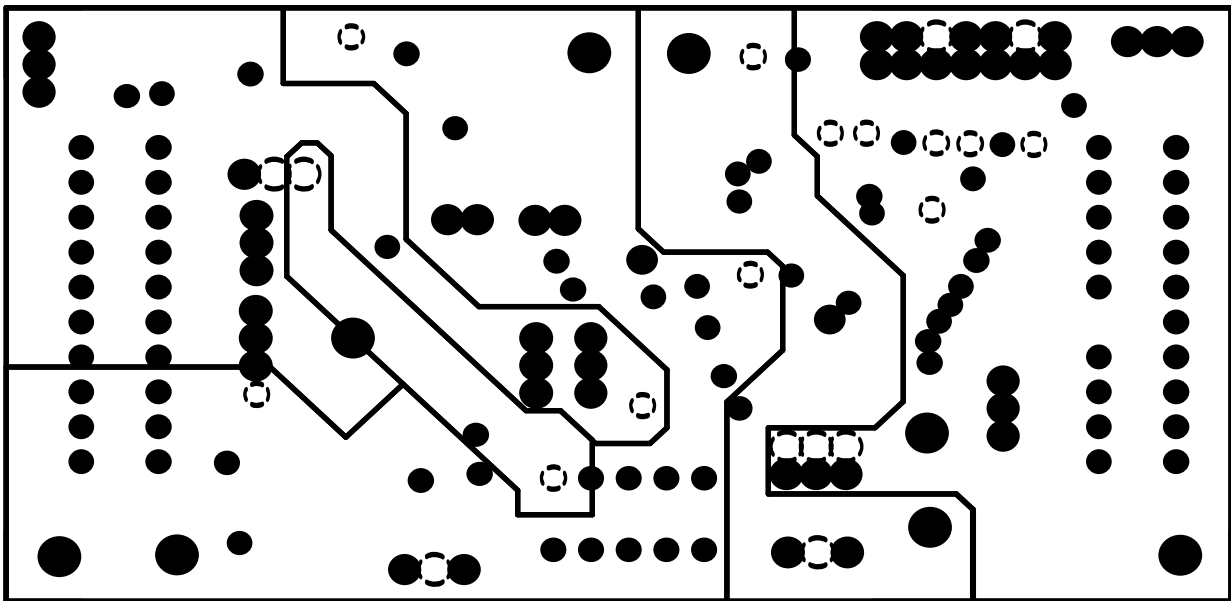


Figure 5. Layer 3, Power Plane

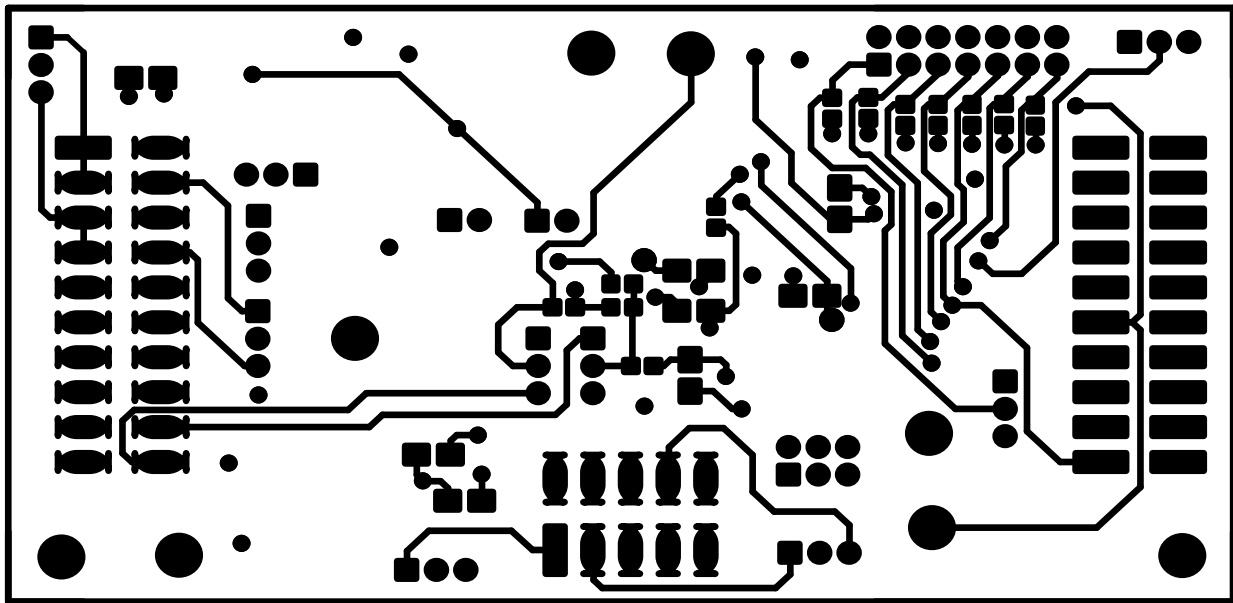


Figure 6. Layer 4, Bottom Signal Plane

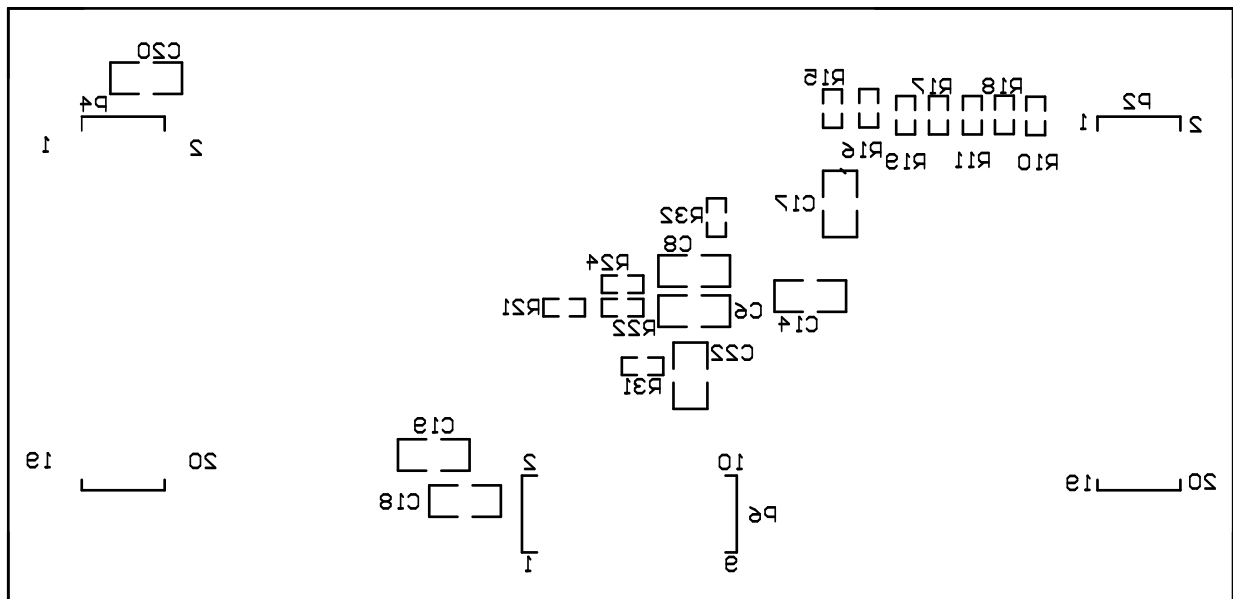


Figure 7. Bottom Silkscreen

### 3 EVM Performance

The DAC9881 is optimized for DC performance; total harmonic distortion (THD) is typically at -80 dB. The EVM INL and DNL testing is performed using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a personal computer (PC) running LabVIEW™ software. The EVM board is tested for all codes of 262,144 × 8 bits organization and the DAC is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 8 shows the INL and DNL characteristic plots.

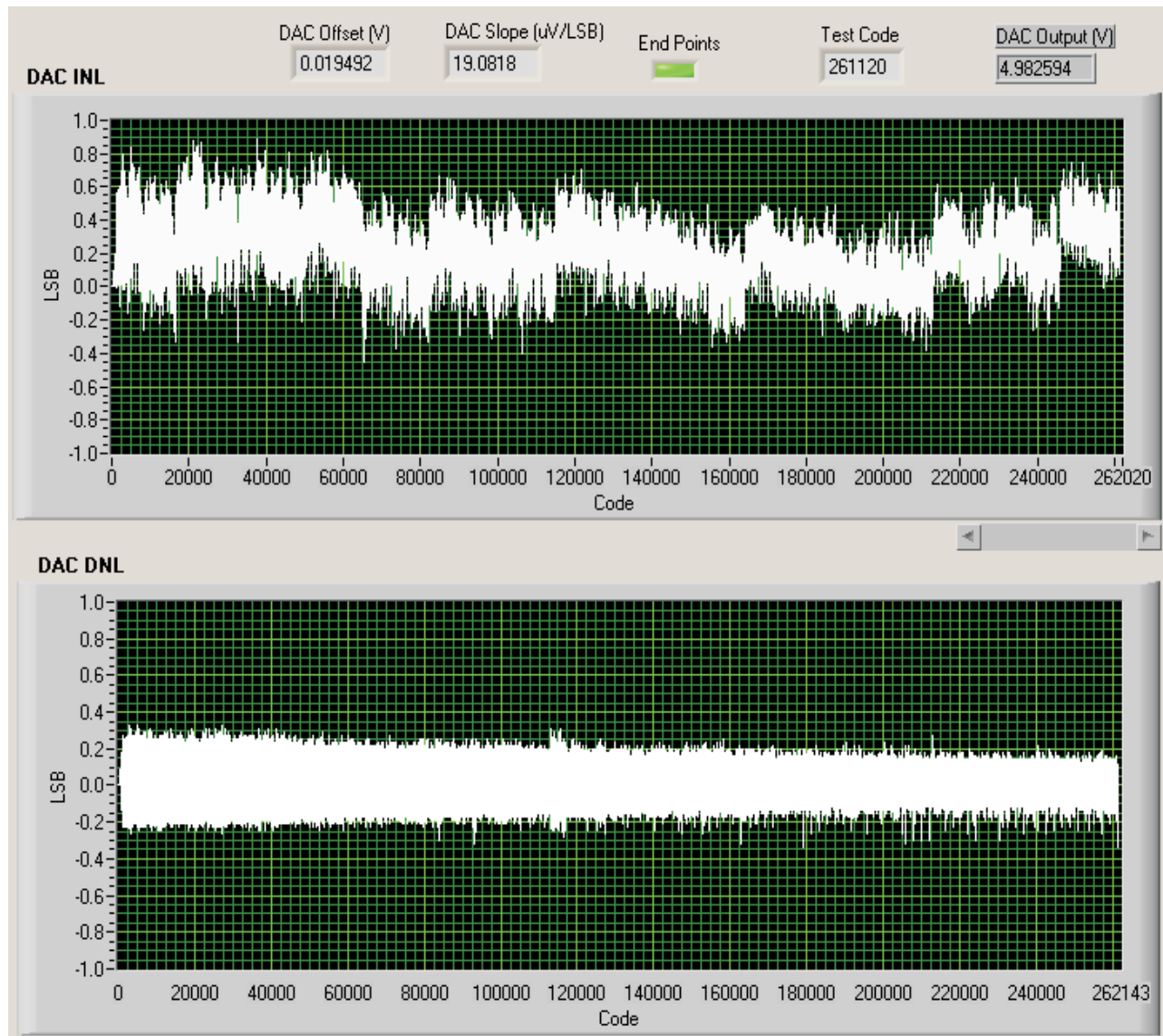


Figure 8. INL and DNL Characteristic Plot



## 4 Bill of Materials

**Table 1. Parts Lists**

Qty.	Designators	Description	Manufacturer	Mfg. Part Number
1	N/A	Printed Wiring Board	TI	6498232
6	C1–C4, C15, C17	0.1 $\mu$ F, 0805, Ceramic, X7R, 50V, 10%	TDK	C2012X7R1H104K
3	C5, C11, C16	10 $\mu$ F, 1210, Ceramic, X7R, 25V, 20%	TDK	C3225X7R1E106M
2	C6, C13	2200 pF, 0805, Ceramic, C0G, 50V, 5%	TDK	C2012C0G1H222J
3	C8, C12, C14	1000 pF, 0805, Ceramic, C0G, 50V, 5%	TDK	C2012C0G1H102J
4	C9, C10, C18, C19	1 $\mu$ F, 0805, Ceramic, X7R, 25V, 10%	TDK	C2012X7R1E105K
0	C20	DNP		
2	C21, C22	2.2 $\mu$ F, 0805, Ceramic, X7R, 16V, 10%	TDK	C2012X7R1C225K
1	J1	7 $\times$ 2 $\times$ 2 mm Terminal Strip	Samtec	TMM-107-01-T-D
2	J2, J4 (top side)	10 Pin, Dual Row, TH Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
1	J3	3 $\times$ 2 $\times$ 2mm Terminal Strip	Samtec	TMM-103-01-T-D
1	J6 (top side)	5 Pin, Dual Row, TH Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
2	P2, P4 (bottom side)	10 Pin, Dual Row, TH Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
1	P6 (bottom side)	5 Pin, Dual Row, TH Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
6	R1–R4, R8, R20	0.0 $\Omega$ 1/10W, 5%, 0603, SMD	Yageo	RC0603JR-070RL
0	R5, R7, R25, R27, R28	DNP		
2	R6, R12	6.04 k $\Omega$ , 1/10W, 0.1%, 0603, SMD	BCC	2312-201-76042
1	R9	10 k $\Omega$ 4MM TOP ADJ SMD	Bourns	3214W-1-103E
7	R10, R11, R15–R19	10.0 k $\Omega$ , 1/10W, 1%, 0603, SMD	Yageo	RC0603FR-0710KL
1	R13	100 $\Omega$ , 1/10W, 0.1%, 0603, SMD	BCC	2312-201-71001
1	R14	3.01 k $\Omega$ , 1/10W, 0.1%, 0603, SMD	BCC	2312-201-73012
2	R21, R24	2.00 k $\Omega$ , 1/10W, 0.1%, 0603, SMD	BCC	2312-201-72002
1	R22	95.3 k $\Omega$ , 1/10W, 0.1%, 0603, SMD	KOA	RN731JTSDK9532B25
2	R23, R26	49.9 $\Omega$ , 1/10W, 0.1%, 0603,	SMD KOA	RN731JTSDK49R9B25
4	R29, R31, R32, R33	10.0 k $\Omega$ , 1/10W, 0.1%, 0603,	SMD KOA	RN731JTSDK1002B25
1	R30	470 k $\Omega$ , 1/10W, 1%, 0603,	SMD Yageo	RC0603FR-07470KL
1	R34	1.00 k $\Omega$ , 1/10W, 1%, 0603,	SMD Yageo	RC0603FR-071KL
8	TP1–TP8	Test Point Turret	Mill-Max	2348-2-00-44-00-00-07-0
1	U1	18-Bit, Buffered Voltage Output DAC	TI	DAC9881SBRGET
1	U2	High Precision Op-Amp	TI	OPA211AIDR
1	U3	5V Precision Voltage Reference	TI	REF5050AID
1	U4	High Precision Dual Operational Amplifier	TI	OPA2277UA
10	W1, W2, W4–W11	3 Pin Mini Header	Samtec	TMM-103-01-T-T
2	W3, W12	2 Pin Mini Header Components	Samtec	TMM-102-01-T-T
<b>ADDITIONAL COMPONENTS</b>				
9	Shunt for items 33 and 34	2mm Shunt – Black	Samtec	2SN-BK-G
1	Shunt for J4	0.100 Shunt – Black (J4 Pins 1 and 2)	Samtec	SNT-100-BK-T
Notes: 1. P2, P4 and P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.				

## 5 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

For information about the serial interface and other related topics, see the DAC9881 data sheet ([SBAS438](#)).

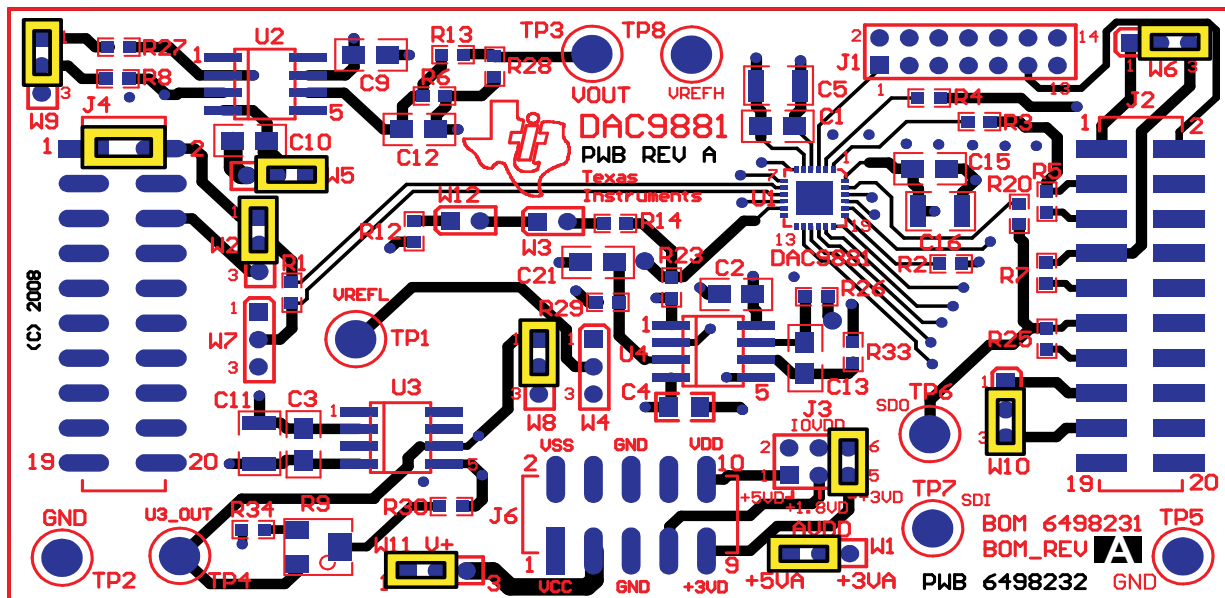
The EVM board is factory tested and configured to operate in the unipolar output mode.

### 5.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in the [Table 2](#) to operate in unipolar +5V mode of operation. [Figure 9](#) shows the default jumper configuration as described in table 2.

**Table 2. Factory Default Jumper Setting**

Reference	Jumper Position	Function
W1	1-2	The +5VA is used for AV <sub>DD</sub> and DV <sub>DD</sub> to power the analog and digital supplies of the DAC9881.
W2	1-2	Routes V <sub>OUT</sub> of the DAC9881 to J4-2 for analog output monitoring.
W3	OPEN	Disconnects V <sub>REFH</sub> from the inverting input of U2 to allow other output mode of configuration.
W4	2-3	Connects the V <sub>REFL</sub> pin of the DAC9881 to ground.
W5	1-2	Negative supply rail of the output operational amplifier, U2, is powered by V <sub>SS</sub> for bipolar operation.
W6	2-3	FS signal from J2-7 is routed to drive the $\overline{CS}$ signal of the DAC9881.
W7	OPEN	Leave this jumper open because R1 is installed. This is the default mode of the EVM when it leaves the factory.
W8	1-2	Routes the onboard +5-V voltage reference, V <sub>REFH</sub> for the DAC.
W9	1-2	Routes V <sub>OUT</sub> and R <sub>FB</sub> from J4-2 and J4-4 (if they are shunted) to the noninverting input of U2 operational amplifier.
W10	OPEN	The $\overline{LDAC}$ signal of the DAC9881 is tied to ground for synchronous update of the DAC9881 output.
W11	1-2	Routes V <sub>CC</sub> to power the analog supply of the U3 reference device.
W12	OPEN	Disconnects the inverting input of U2 from R12 gain resistor to allow other output mode of configuration.
J1	1-2	The $\overline{LDAC}$ signal of the DAC9881 is tied to ground for synchronous DAC update operation.
J3	5-6	The DAC9881's IOV <sub>DD</sub> is powered with +3.3 VD.



**Figure 9. DAC9881 EVM Default Jumper Configuration**

## 5.2 Host Processor Interface

The DAC9881 supports high-speed serial peripheral interface (SPI) to communicate with gate arrays, microprocessors or DSP devices. The user supplied host processor drives the serial communication to the DAC9881EVM. The DAC9881EVM provides the necessary connections to the host processor through connector P2 (located on the bottom side of the board). Proper operation of the DAC9881 depends on the successful communication between the host processor and the EVM. Communication is based on an SPI where CPOL = 0 and CPHA = 0. This means the serial clock dwells low in its inactive state and the input data considered valid on the rising edge of the serial clock.

The following sections describe the basic operation of the digital control inputs to the DAC9881. For more detailed information regarding the DAC9881 digital interface, see the data sheet ([SBAS438](#)).

## 5.3 Digital Control Interface

The DAC9881 can be considered a 3-wire SPI slave device. The host processor must provide a chip select ( $\overline{CS}$ ), the serial data input (SDI) and the serial clock (SCLK) necessary to control the operation of the DAC9881. A fourth control line called load dac ( $\overline{LDAC}$ ) can be used to control the point in time at which the DAC output data is updated. This is useful in applications where multiple DAC9881's need to be updated simultaneously. With the exception of the serial data input (SDI) and the serial data output (SDO) to and from the DAC9881, the EVM incorporates a pass-through connector arrangement to accommodate the digital control interface of the DAC9881 device via J2 (top side) or P2 (bottom side) connectors. The signals on these pass-through connectors are listed as shown in [Table 3](#).

**Table 3. Digital Control Interface Signal Mapping for J2/P2 Connectors**

Pin Number	Signal	Function
J2.1/P2.1	$\overline{CS}$	Primary synchronization and device enable input for the DAC9881. Host microcontroller's STE signal for SPI interface.
J2.3/P2.3	SCLK	Serial interface clock.
J2.5/P2.5	CLKR	Unused.
J2.7/P2.7	FS	Secondary synchronization and device enable input for the DAC9881. Host microcontroller's STE signal for SPI interface or FS signal from DSP host system.
J2.9/P2.9	FSR	Unused.
J2.11	SDO	Serial Data Output.
P2.11	SDI	Serial Data Input.
J2.13/P2.13	DR	Unused.
J2.15/P2.15	$\overline{LDAC}1$	GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.17/P2.17	$\overline{LDAC}2$	Alternate GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.19/P2.19	$\overline{RST}$	GPIO signal to control $\overline{RST}$ for DAC reset function.
J2.2/P2.2	PDN	GPIO signal to control PDN for hardware power down.
J2.4/P2.4 J2.10/P2.10 J2.18/P2.18	GND	Signal Ground
J2.6/P2.6 J2.8/P2.8 J2.12/P2.12 J2.14/P2.14 J2.16/P2.16 J2.20/P2.20	GPIOs	Unused

### 5.3.1 $\overline{CS}$ Signal

The signals found on J2 pins 1 and 7 of the EVM are used to control the chip select input of the DAC9881. These signals are configurable via wire jumper W6. Either signal can be chosen to drive the DAC9881  $\overline{CS}$  pin. The basic function of the  $\overline{CS}$  input signal is to enable serial communication with the DAC9881. This signal must be held low while the host processor is accessing the DAC serial shift register. The low-to-high transition of this signal transfers the content of the serial shift register to the DAC input register. The  $\overline{CS}$  input can also be used to update the DAC output if the  $\overline{LDAC}$  is tied to ground.

### 5.3.2 SDI Signal

The SDI signal is the serial data input that is loaded into the DAC's input register. The data frame sent to the DAC9881 is 24-bits wide. The first 6 bits are 'don't care', the seventh bit is the most-significant bit (MSB) of the DAC data and the 24th bit is the least significant bit (LSB) of the 18-bit DAC data. The serial data input is driven from the SPI master on the falling SCLK edge and sampled by the DAC9881 on the rising edge of the serial clock.

### 5.3.3 SCLK Signal

The host processor must provide an SCLK signal which is used to advance serial data through the DAC's serial shift register. The serial clock rate can operate at speeds up to 50 MHz. The 6 don't care bits plus 18-bit data is shifted out of the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the DAC's serial shift register. After 24-bits are transferred or 24 SCLK cycles are generated, the bus master must take the  $\overline{CS}$  signal high. If the  $\overline{CS}$  signal is held low and more than 24 SCLK cycles are applied, the last SCLK cycle is considered the least significant bit (LSB) of the 18-bit data stream loaded into the DAC's serial shift register.

### 5.3.4 $\overline{LDAC}$ Signal

The  $\overline{LDAC}$  signal is a control input signal that can be used to update the DAC output at a specific point in time. This signal is active low and can be triggered synchronously or asynchronously. If  $\overline{LDAC}$  is held low, the DAC9881 output updates with the rising edge of the  $\overline{CS}$  input. If multiple DAC9881 devices share the databus in daisy-chain fashion, a common  $\overline{LDAC}$  signal can be used to update multiple DAC outputs simultaneously.

### 5.3.5 $\overline{RST}$ Signal

The  $\overline{RST}$  signal is the control input used to reset the DAC output to a known state which is determined by the logic level of the RSTSEL pin when the  $\overline{RST}$  pin is asserted. If RSTSEL is tied to DGND, the DAC output latch is cleared (0 V) and  $V_{OUT}$  is minimum scale (i.e.,  $V_{REFL}$ ). If RSTSEL is tied to VDD, the DAC output latch is set to midscale and  $V_{OUT}$  is equal to  $(V_{REFH} - V_{REFL})/2$ . This pin is an active low input.

### 5.3.6 PDN Signal

The PDN signal is the control input provided for hardware power-down function of the device. This signal is active high, so when the PDN pin is driven high, the device goes into power-down mode, which reduces its power consumption. The DAC9881 voltage output pin is connected to ground through an internal 10-k $\Omega$  resistor while in power-down mode.

## 5.4 Analog Output

The DAC9881 voltage output is buffered internally and offers a force and sense output configuration to allow the loop around the output amplifier to be closed as near to the load as possible. The EVM closes this loop by default with R1 installed, so if the loop at the load needs to be closed, R1 must be removed and jumpers W2 and W7 used to connect  $V_{OUT}$  and  $R_{FB}$  to the connector J4. The selected pins of the J4 connector, as dictated by the jumper positions of W2 and W7 jumpers, can then be connected to the load to close the loop.

The EVM includes an external operational amplifier, U2, as an option for other output signal-conditioning circuitry for the DAC output. Although the buffered output of the DAC9881 can be monitored through J4 pin 2, the optional external buffer output (if the DAC output is connected to it) can be monitored through the TP3 test point.

The external operational amplifier, U2, is set to unity gain configuration by default to maintain the DAC9881 unipolar output mode of operation. But it can be modified by simple jumper settings to achieve other modes of operation. The following sections describe the different configurations of the output amplifier, U2.

### 5.4.1 Bipolar Output Operation

Using the external  $V_{REFH}$  to offset the DAC output and extend the range of operation to achieve a bipolar mode of operation is possible by properly configuring the output operational amplifier, U2. This configuration is described in [Table 4](#).

**Table 4. Bipolar Output Operation Jumper Settings**

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ( $V_{OUT1}$ ) to the noninverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ( $V_{OUT2}$ ) to the noninverting input of the output operational amplifier, U2.
W3	CLOSE	Connect $V_{REFH}$ to the inverting input of the operational amplifier, U2.
W5	1-2	Supplies power, $V_{SS}$ , to the negative rail of operational amplifier, U2, for wider range of operation.
W12	OPEN	Disconnect negative input of the operational amplifier from the gain resistor, R12.

### 5.4.2 Output Gain of Two Operation

The configuration as described on [Table 5](#) yields a voltage output mode of operation that is gained by two.

**Table 5. Gain of Two Output Jumper Settings**

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ( $V_{OUT1}$ ) to the noninverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ( $V_{OUT2}$ ) to the noninverting input of the output operational amplifier, U2.
W3	OPEN	Disconnect $V_{REFH}$ from the inverting input of the operational amplifier, U2.
W5	1-2	Supplies power, $V_{SS}$ , to the negative rail of operational amplifier, U2, for wider range of operation.
W12	CLOSE	Connect the negative input of the operational amplifier, U2, to the gain resistor, R12.

### 5.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all operational amplifiers under certain conditions may become unstable depending on the operational amplifier configuration, gain, and load value. These are just a few factors that can affect operational amplifiers stability performance and must be considered when implementing.

In unity gain, the OPA211 operational amplifier, U2, performs well with large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and adding a load resistor even improves the capacitive load drive capability.

[Table 6](#) shows the jumper setting configuration for a capacitive load drive.

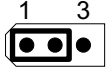
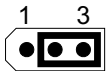
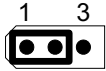
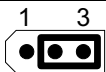


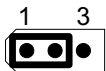
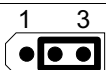
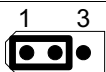
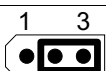
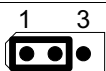
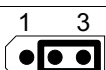

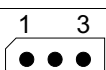
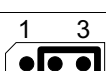
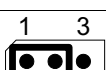
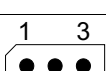
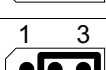
**Table 6. Capacitive Load Drive Output Jumper Settings**

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ( $V_{OUT1}$ ) to the noninverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ( $V_{OUT2}$ ) to the noninverting input of the output operational amplifier, U2.
W3	OPEN	Disconnect $V_{REFH}$ to the inverting input of the operational amplifier, U2.
W5	1-2	Supplies power, $V_{SS}$ , to the negative rail of operational amplifier, U2, for wider range of operation.
W12	CLOSE	Connect the negative input of the operational amplifier, U2, to the gain resistor, R12.

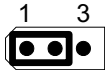
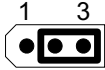
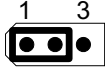
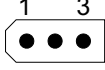
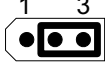
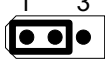
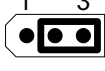


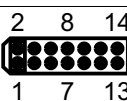
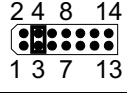
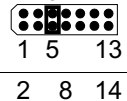
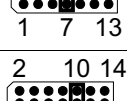
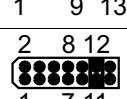
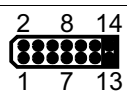

## 5.5 Jumper Setting

Table 7 shows the function of each specific jumper setting of the EVM.

**Table 7. Jumper Setting Function**

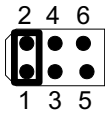
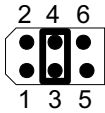
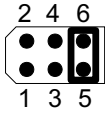

Reference	Jumper Setting	Function
W1		Routes +5VA for AV <sub>DD</sub> and DV <sub>DD</sub> to power the analog and digital supplies of the DAC9881.
		Routes +3.3VA for AV <sub>DD</sub> and DV <sub>DD</sub> to power the analog and digital supplies of the DAC9881.
W2		Routes V <sub>OUT</sub> to J4-2.
		Routes V <sub>OUT</sub> to J4-6.
W3		Connect V <sub>REFH</sub> to the inverting input of U2 for DAC9881's bipolar mode of operation.
		Disconnects V <sub>REFH</sub> from the inverting input of U2 to allow other output mode of configuration.
W4		Routes the reference voltage from J4 pin 18 for the V <sub>REFL</sub> pin of the DAC9881.
		Connects the V <sub>REFL</sub> pin of the DAC9881 to ground.
W5		Negative supply rail of the output operational amplifier, U2, is powered by V <sub>SS</sub> for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
W6		$\overline{CS}$ signal from J2-1 is routed to drive the $\overline{CS}$ signal of the DAC9881.
		FS signal from J2-7 is routed to drive the $\overline{CS}$ signal of the DAC9881.
W7		Routes the reference feedback, R <sub>FB</sub> , pin of the DAC9881 to J4 pin 4 to provide the option to close the output operational amplifier, U2, loop as close as possible to the load.
		Leave this jumper open if R1 is installed. This is the default mode of the EVM when it comes out of the factory.
		Routes the reference feedback, R <sub>FB</sub> , pin of the DAC9881 to J4 pin 8 to provide the option to close the output operational amplifier, U2, loop as close as possible to the load.
W8		Routes the onboard +5-V voltage reference, V <sub>REFH</sub> for the DAC.
		Disconnect onboard or external positive voltage reference, V <sub>REFH</sub> for the DAC via U5A or J1 pin 20. Allows user reference voltage to connect via TP1.
		Routes the external positive voltage reference, V <sub>REFH</sub> for the DAC via J1 pin 20.

**Table 7. Jumper Setting Function (continued)**

Reference	Jumper Setting	Function
W9		Routes $V_{OUT}$ and $R_{FB}$ from J4-2 and J4-4 to the noninverting input of U2 operational amplifier.
		Routes $V_{OUT}$ and $R_{FB}$ from J4-6 and J4-8 to the noninverting input of U2 operational amplifier.
W10		$\overline{LDAC}1$ signal from J2-15 is routed to drive the $\overline{LDAC}$ signal of the DAC9881.
		The $\overline{LDAC}$ signal of the DAC9881 is tied to ground for synchronous update of the DAC9881 output.
		$\overline{LDAC}2$ signal from J2-17 is routed to drive the $\overline{LDAC}$ signal of the DAC9881.
W11		Routes $V_{CC}$ to power the analog supply of the U3 reference device.
		Routes +5VA to power the analog supply of the U3 reference device.
W12		Connect the inverting input of U2 to R12 gain resistor for DAC9881's 2x gain of operation.
		Disconnects the inverting input of U2 from R12 gain resistor to allow other output mode of configuration.
J1		If jumper is installed on pins 1 and 2, the $\overline{LDAC}$ signal of the DAC9881 is tied to ground for synchronous DAC update operation.
		If jumper is installed on pins 3 and 4, the $\overline{RSTSEL}$ pin of the DAC9881 is tied to ground so that the DAC output is at 0 V on power up or reset to the device is issued.
		If jumper is installed on pins 5 and 6, the $\overline{GAIN}$ pin of the DAC9881 is tied to $IOV_{DD}$ so that the DAC output is set with a gain of two output.
		If jumper is installed on pins 7 and 8, the $\overline{USB/BTC}$ pin of the DAC9881 is tied to ground so that the DAC's input data format is set for 2s complement format.
		If jumper is installed on pins 9 and 10, the $\overline{RST}$ pin of the DAC9881 is tied to ground so that the DAC is forced into hardware reset mode.
		If jumper is installed on pins 11 and 12, the $\overline{PDN}$ pin of the DAC9881 is tied to $IOV_{DD}$ so that the DAC is forced into power-down status.
		If jumper is installed on pins 13 and 14, the $\overline{SDOSEL}$ pin of the DAC9881 is tied to ground so that the DAC device can be operated in daisy-chain mode.



**Table 7. Jumper Setting Function (continued)**

Reference	Jumper Setting	Function
J3		The DAC9881's IOV <sub>DD</sub> is powered with +5VD.
		The DAC9881's IOV <sub>DD</sub> is powered with +1.8VD.
		The DAC9881's IOV <sub>DD</sub> is powered with +3.3VD.
<b>Legend:</b>  Indicates the corresponding pins that are shorted or closed.		

## 5.6 DAC9881EVM Schematic

The DAC9881EVM schematic appears as the last page of this manual.

## 6 Using the DAC9881EVM with DXP

The DAC9881EVM is compatible with the DAC eXerciser Program (DXP) from Texas Instruments. DXP is a tool that can generate the necessary code required to output various signals and waveforms from the DAC9881EVM. The DAC9881EVM-DXP kit combines the DAC9881EVM board with the TMS320VC5509 DSP-based modular motherboard (MMB0), and includes DXP software for evaluation using any available USB port.

DXP is a program for controlling the digital input signals such as the clock, LDAC,  $\overline{CS}$ , and SDI. Wave tables are built into the DSP software to allow Sine, Ramp, Triangle, and Square wave signals to be generated by the DAC9881. Straight DC outputs also can be obtained.

The DAC9881EVM-PDK is controlled by loading a DAC EVM configuration into the MMB0. For complete information about installing and configuring DXP, see the *DXP User's Guide*, available for download from the TI Web site.

This section covers the specific operation of the DAC9881EVM-PDK. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DAC9881EVM.

### 6.1 Hardware

The hardware consists of two main components, the first is the DAC9881EVM itself and the other is a modular motherboard called the MMB0. The MMB0 board houses a TMS320VC5507DSP which controls the DAC9881 serial interface.

The hardware needs to be configured such that the DAC9881EVM is plugged onto the board onto the MMB0 aligning female connectors P4, P2, and P6 (bottom side of the DAC9881EVM) with male connectors J4, J7, and J5 on the MMB0. Exercise caution when assembling the boards as it is possible to misalign the connectors. Do not connect the MMB0 to your PC before installing the DXP software. Installing the software ensures that the necessary drivers are properly loaded to run the hardware.



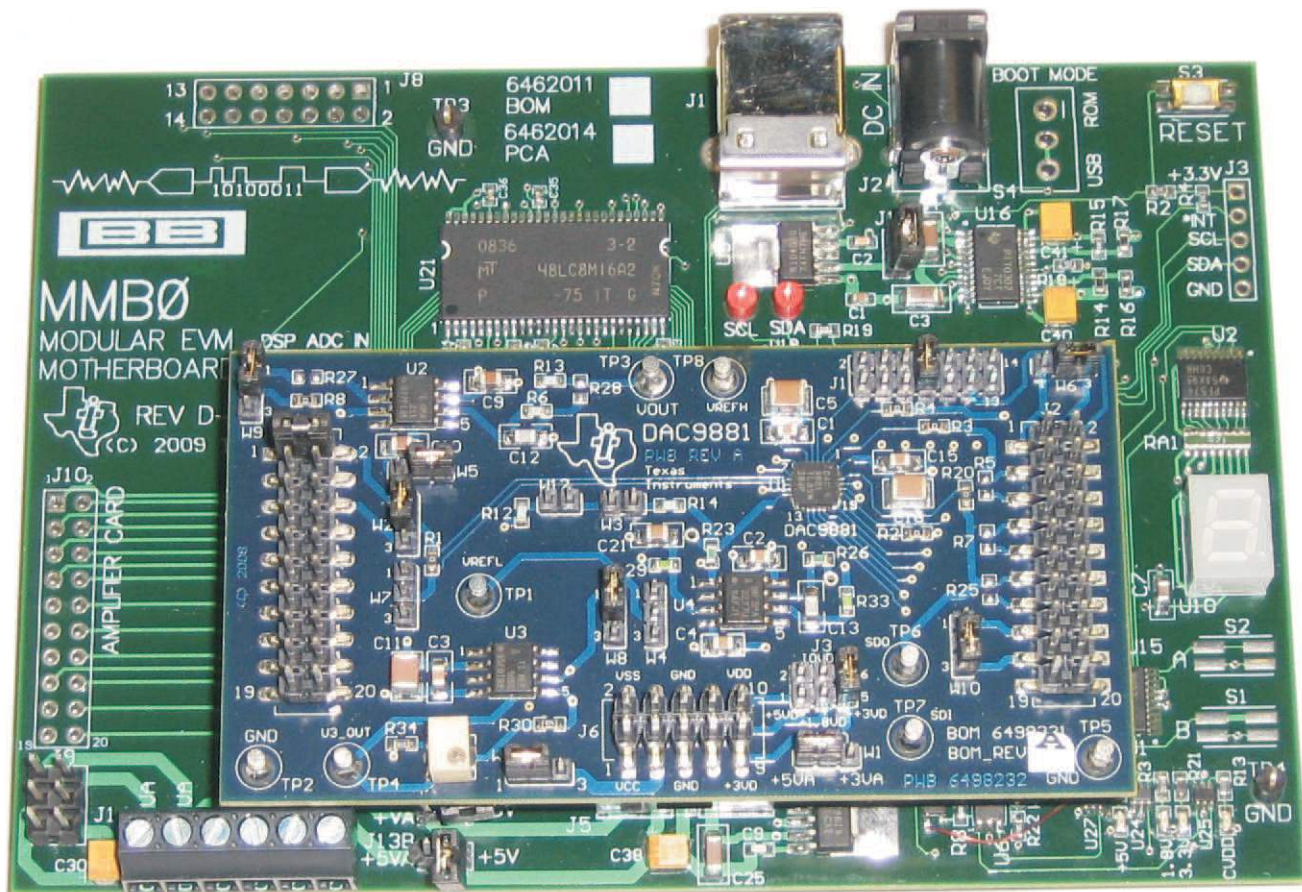


Figure 10. MMB0 with DAC9881EVM Installed

## 6.2 MMB0 Power Supplies

Several power connections are required for the hardware to work properly. For the MMB0, the supplied 6-V AC/DC converter is all that is necessary. Ensure that J12 on the MMB0 board is closed before connecting the AC/DC adapter to the DC In connector of the MMB0. This supply provides all power to the digital portion of the DAC9881EVM as well as all necessary power for the DSP. Analog power for the DAC9881EVM must be supplied externally via J14 – a 6-position screw terminal mounted in the lower left corner of the MMB0 board.

### CAUTION

When using external power supplies applied to J14 on the MMB0, ensure that all shorting blocks from J13 are completely removed. Permanent damage to the MMB0 may occur otherwise.

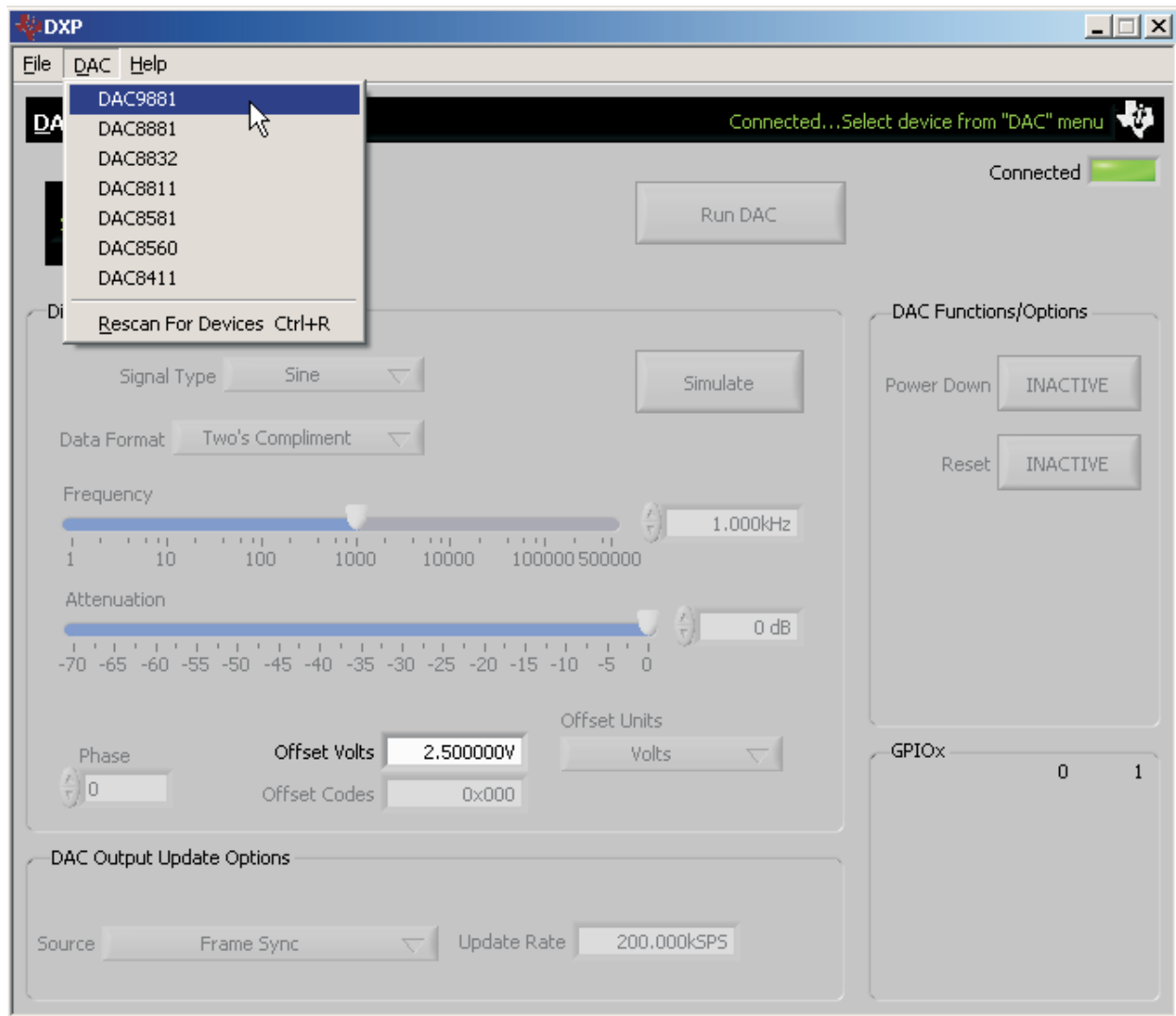
From left to right, the screw terminal connections of J14 are  $-VA$ ,  $+VA$ ,  $+5VA$ ,  $-5VA$ ,  $+5VD$ , and GND. The DAC9881 board has power requirements as described in [Section 1.2](#). The analog power for  $V_{cc}$  ( $+VA$ ),  $V_{ss}$  ( $-VA$ ), and  $+5VA$  may be applied directly to the screw terminals at J14 on the MMB0 (referenced to the GND terminal).

Connect the MMB0 power supply to DC IN connector (J2) on the MMB0. Connect all other analog supplies as necessary to J14 on the MMB0 (referenced to the ground terminal).

### 6.3 Software – Running DXP

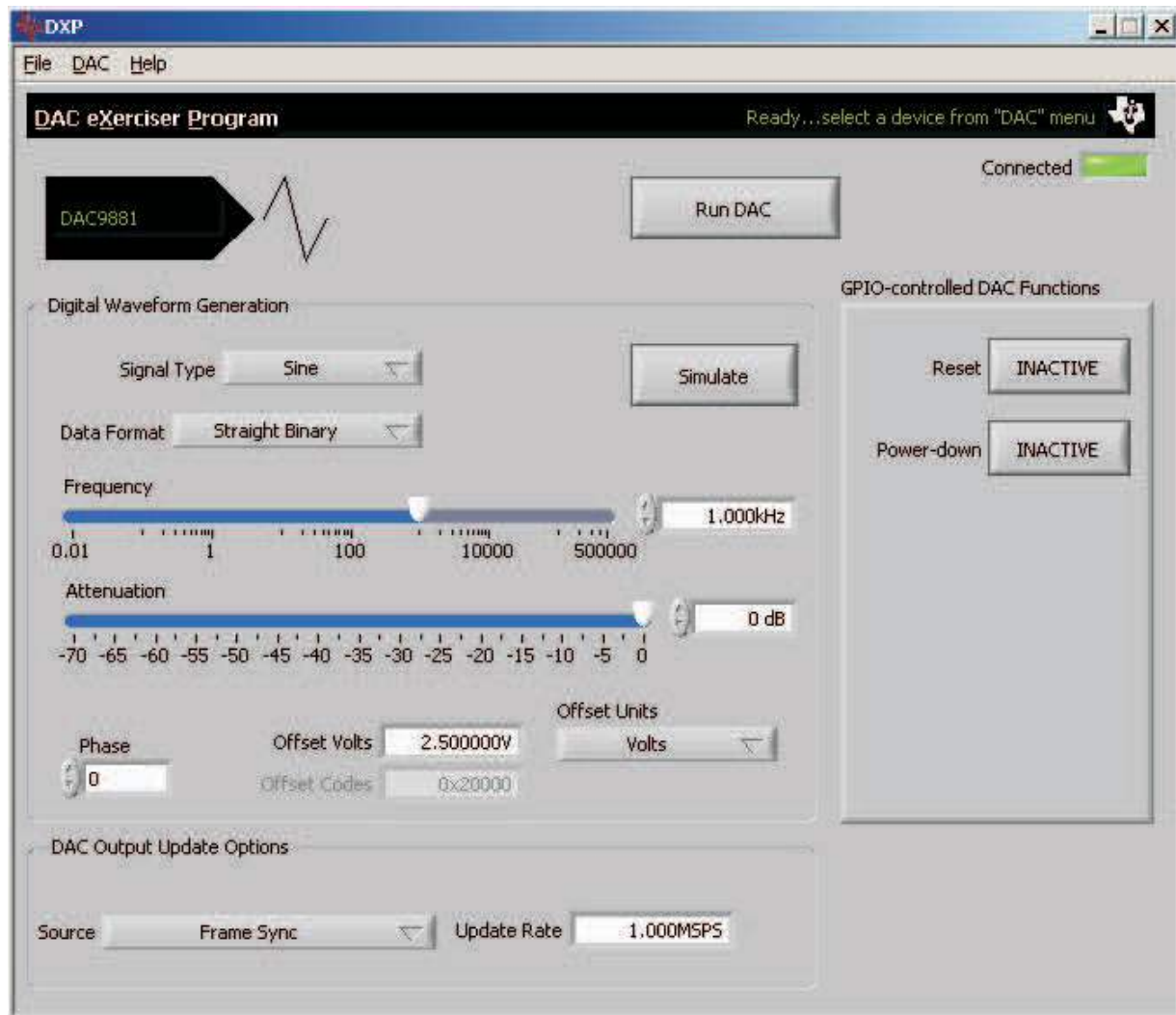
Install DXP on a laptop or personal computer running Windows XP as per the detailed instruction in the DXP User's Guide ([SBAU146](#)). Run the DXP program by clicking on the DXP icon on your desktop or by browsing to your installation directory.

Before you can use DXP, a DAC EVM configuration file must be loaded. To load a configuration file, select the desired DAC from the configuration list under the **DAC** menu. Choose the DAC configuration file for the DAC9881 EVM as shown in [Figure 11](#).



**Figure 11. Loading the DAC9881EVM INI File**

The DXP software defaults to output a 1-kHz sine wave from the DAC, other waveform options include Square, Saw tooth, Triangle, and DC output options as described in the DXP User's Guide. GPIO options are available on the DAC9881EVM which active either the RESET or power-down functions of the DAC9881. These are shown in [Figure 12](#) on the right side of the screen labeled GPIO-controlled DAC Functions. Pressing the Reset button resets the DAC9881 outputs as described in the device data sheet. Pressing the Power-Down button places the DAC9881 in low-power mode.



**Figure 12. DAC9881 – Frequency/Amplitude and GPIO Control Options**

## 7 Related Documentation From Texas Instruments

1. *DAC9881, 18-Bit, Single-Channel, Low-Noise, Voltage-Output Digital-to-Analog Converter* data sheet ([SBAS438](#))
2. *REF02, +5V Precision Voltage Reference* data sheet ([SBVS003](#))
3. *REF5050, Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet ([SBOS410](#))
4. *OPA211, 1.1nV/√Hz Noise, Low Power, Precision Operational Amplifier in Small DFN-8 Package* data sheet ([SBOS377](#))
5. *OPA827, Low-Noise, High-Precision, JFET-Input Operational Amplifier* data sheet ([SBOS376](#))
6. *OPA277, OPA2277, OPA4277, High Precision Operational Amplifiers* data sheet ([SBOS079](#))
7. *OPA227, High Precision, Low Noise Operational Amplifiers* data sheet ([SBOS110](#))

If you have questions about this or other Texas Instruments Data Converter evaluation modules, send an e-mail to the Data Converter Application Team at [dataconvapps@list.ti.com](mailto:dataconvapps@list.ti.com). Include in the subject heading the product with which you have questions or concerns.





## EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

**EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.**

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit [www.ti.com/esh](http://www.ti.com/esh).

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

### FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

### EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -15 V to +15 V and the output voltage range of -15 V to +15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated