Features

- Incorporates the ARM7TDMI™ ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-circuit Emulation)
- 8K Bytes On-chip SRAM
  - 32-bit Data Bus, Single-clock Cycle Access
- 1M Words 16-bit Flash Memory (16 Mbits)
  - Single Voltage Read/Write, 110 ns Access Time
  - Sector Erase Architecture
  - Fast Word Program Time of 20 µs; Fast Sector Erase Time of 200 ms
  - Dual-plane Organization Allows Concurrent Read and Program/Erase
  - Erase Suspend Capability
  - Low-power Operation: 25 mA Active - 10 µA Standby
  - Data Polling, Toggle Bit and Ready/Busy End of Program Cycle Detection
  - Reset Input for Device Initialization
  - Sector Program Unlock Command
  - Factory-programmed AT91 Flash Uploader Software
- Fully-programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - 8 Chip Selects, Software-programmable 8/16-bit External Data Bus
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 4 External Interrupts, Including a High-priority Low-latency Interrupt Request
- 32 Programmable I/O Lines
- 3-channel 16-bit Timer/Counter
  - 3 External Clock Inputs
  - 2 Multi-purpose I/O Pins per Channel
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Programmable Watchdog Timer
- Advanced Power-saving Features
  - CPU and Peripherals Can Be Deactivated Individually
- Fully Static Operation:
  - 0 Hz to 40 MHz Internal Frequency Range at 3.0V, 85°C
- 2.7V to 3.6V Operating Range
- -40°C to 85°C Temperature Range
- Available in a 120-ball BGA Package

Description

The AT91F40816 is a member of the Atmel AT91 16/32-bit microcontroller family, which is based on the ARM7TDMI processor core. The processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The eight-level priority-vectored interrupt controller, together with the Peripheral Data Controller, significantly enhance real-time device performance.

By combining the microcontroller, featuring on-chip SRAM and a wide range of peripheral functions, with 16 Mbits of Flash memory in a single compact 120-ball BGA package, the Atmel AT91F40816 provides a powerful, flexible and cost-effective solution to many compute-intensive embedded control applications and offers significant board size reductions.

The Flash memory may be programmed via the JTAG/ICE interface or the factory-programmed Flash Uploader using a single device supply, making the AT91F40816 ideal for in-system programmable applications.

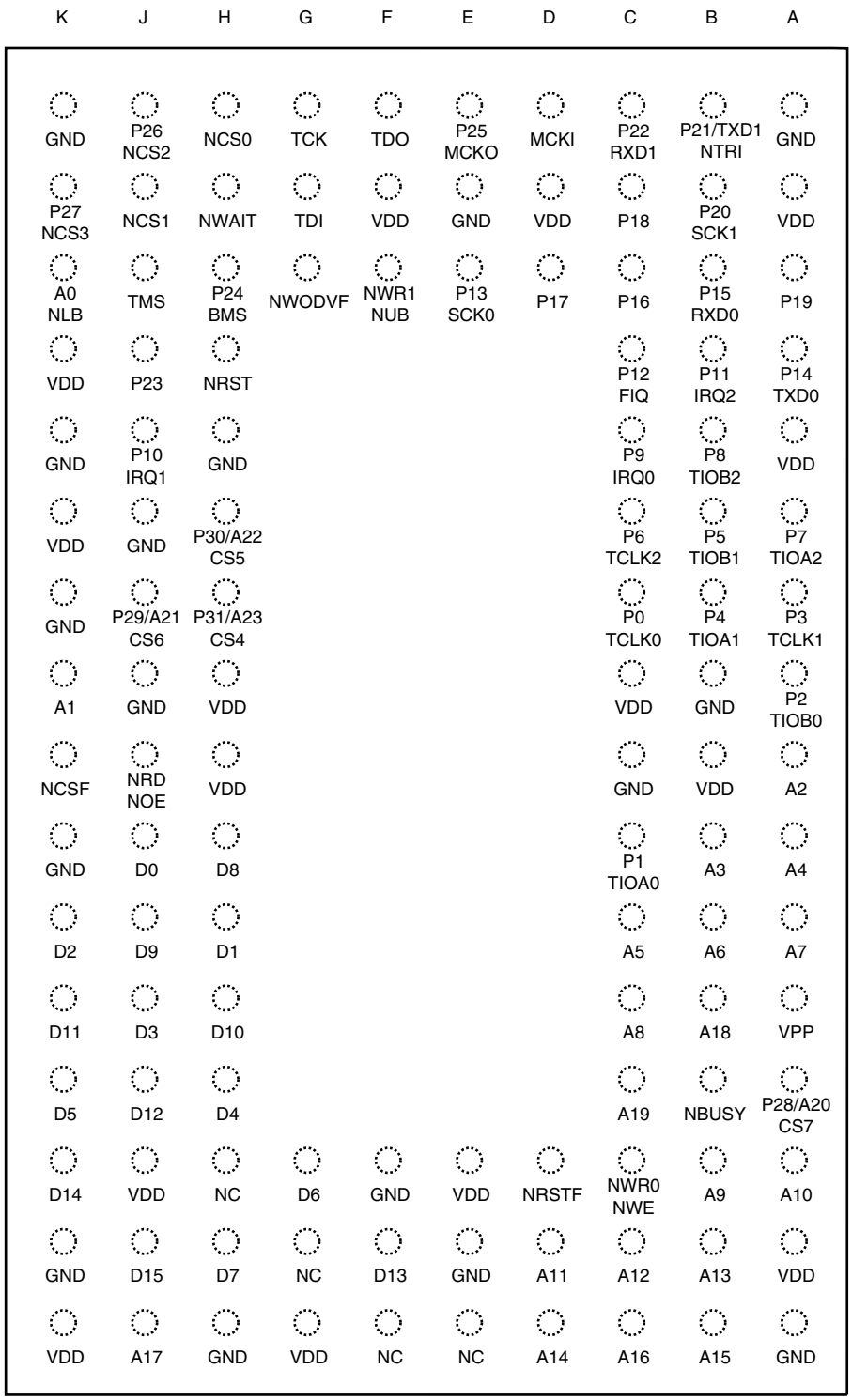
AT91 ARM® Thumb® Microcontrollers

AT91F40816

Rev. 1384C–ATARM–02/02

Pin Configuration

Figure 1. AT91F40816 Pinout (Top View)



Pin Description

Table 1. AT91F40816 Pin Description

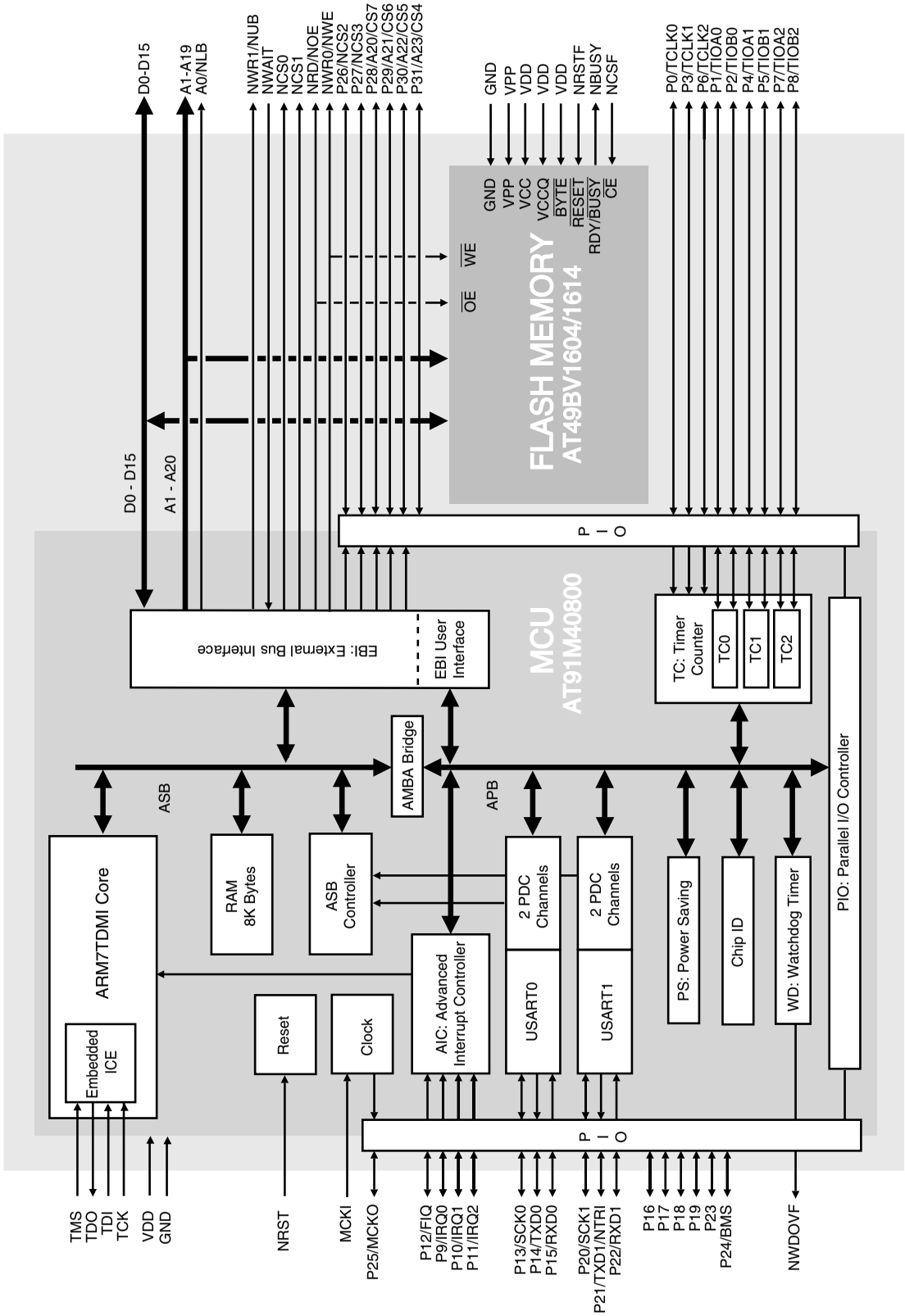
Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address Bus	Output	–	Valid after reset; do not reprogram A20 to I/O, as it is MSB of Flash address
	D0 - D15	Data Bus	I/O	–	
	NCS0 - NCS3	External Chip Select	Output	Low	Used to select external devices
	CS4 - CS7	External Chip Select	Output	High	A23 - A20 after reset
	NWR0	Lower Byte 0 Write Signal	Output	Low	Used in Byte Write option
	NWR1	Upper Byte 1 Write Signal	Output	Low	Used in Byte Write option
	NRD	Read Signal	Output	Low	Used in Byte Write option
	NWE	Write Enable	Output	Low	Used in Byte Select option
	NOE	Output Enable	Output	Low	Used in Byte Select option
	NUB	Upper Byte Select	Output	Low	Used in Byte Select option
	NLB	Lower Byte Select	Output	Low	Used in Byte Select option
	NWAIT	Wait Input	Input	Low	
	BMS	Boot Mode Select	Input	–	Sampled during reset; must be driven low during reset for Flash to be used as boot memory
AIC	FIQ	Fast Interrupt Request	Input	–	PIO-controlled after reset
	IRQ0 - IRQ2	External Interrupt Request	Input	–	PIO-controlled after reset
Timer	TCLK0 - TCLK2	Timer External Clock	Input	–	PIO-controlled after reset
	TIOA0 - TIOA2	Multi-purpose Timer I/O Pin A	I/O	–	PIO-controlled after reset
	TIOB0 - TIOB2	Multi-purpose Timer I/O Pin B	I/O	–	PIO-controlled after reset
USART	SCK0 - SCK1	External Serial Clock	I/O	–	PIO-controlled after reset
	TXD0 - TXD1	Transmit Data Output	Output	–	PIO-controlled after reset
	RXD0 - RXD1	Receive Data Input	Input	–	PIO-controlled after reset
PIO	P0 - P31	Parallel IO Line	I/O	–	
WD	NWDOVF	Watchdog Overflow	Output	Low	Open drain
Clock	MCKI	Master Clock Input	Input	–	Schmidt trigger
	MCKO	Master Clock Output	Output	–	
Reset	NRST	Hardware Reset Input	Input	Low	Schmidt trigger
	NTRI	Tri-state Mode Select	Input	Low	Sampled during reset
ICE	TMS	Test Mode Select	Input	–	Schmidt trigger, internal pull-up
	TDI	Test Data Input	Input	–	Schmidt trigger, internal pull-up
	TDO	Test Data Output	Output	–	
	TCK	Test Clock	Input	–	Schmidt trigger, internal pull-up

Table 1. AT91F40816 Pin Description (Continued)

Module	Name	Function	Type	Active Level	Comments
Flash Memory	NCSF	Flash Memory Select	Input	Low	Enables Flash Memory when pulled low
	NBUSY	Flash Memory Busy Output	Output	Low	Flash RDY/$\overline{\text{BUSY}}$ signal; open-drain
	NRSTF	Flash Memory Reset Input	Input	Low	Resets Flash to standard operating mode
Power	VDD	Power	Power	–	All V_{DD} and all GND pins **MUST** be connected to their respective supplies by the shortest route
	GND	Ground	Ground	–	
	VPP	Faster Program/Erase Voltage	Power	–	See AT49BV/LV1604(T) 16-megabit (1M x 16/2M x 8) 3-volt Only Flash Memory Datasheet

Block Diagram

Figure 2. AT91F40816



Architectural Overview

The AT91F40816 integrates Atmel's AT91M40800 ARM Thumb Microcontroller and an AT49BV1604/1614 16 Mbits, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash memory die in a single compact 120-ball BGA device. The address, data and control signals, except the Flash memory enable, are internally interconnected.

The architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). Designed for maximum performance and controlled by the memory controller, the ASB interfaces the ARM7TDMI processor with the on-chip 32-bit memories, the External Bus Interface (EBI) and the AMBA™ Bridge. The AMBA Bridge drives the APB, which is designed for accesses to on-chip peripherals and optimized for low power consumption.

The AT91F40816 implements the ICE port of the ARM7TDMI processor on dedicated pins, offering a complete, low-cost and easy-to-use debug solution for target debugging.

Memories

The AT91F40816 embeds 8K bytes of internal SRAM. The internal memory is directly connected to the 32-bit data bus and is single-cycle accessible.

The AT91F40816 features an External Bus Interface (EBI), which enables connection of external memories and application-specific peripherals. The EBI supports 8- or 16-bit devices and can use two 8-bit devices to emulate a single 16-bit device. The EBI implements the early read protocol, enabling faster memory accesses than standard memory interfaces.

The AT91F40816 embeds a Flash memory organized as 1M 16-bit words, accessed via the EBI. Its main function is as a program memory. A 16-bit Thumb instruction can be loaded from Flash memory in a single access. Separate MCU and Flash memory Reset inputs (NRST and NRSTF) are provided for maximum flexibility. The user is thus free to conform the reset operation to the application.

The AT91F40816 integrates resident boot software called AT91 Flash Uploader software. The AT91 Flash Uploader software is able to upload program application software into its Flash memory.

Peripherals

The AT91F40816 integrates several peripherals, which are classified as system or user peripherals. All on-chip peripherals are 32-bit accessible by the AMBA Bridge, and can be programmed with a minimum number of instructions. The peripheral register set is composed of control, mode, data, status and enable/disable/status registers.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs and on- and off-chip memories address space without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead, making it possible to transfer up to 64K continuous bytes without reprogramming the start address, thus increasing the performance of the microcontroller, and reducing the power consumption.

System Peripherals

The External Bus Interface (EBI) controls the external memory or peripheral devices via an 8- or 16-bit databus and is programmed through the APB. Each chip-select line has its own programming register.

The Power-saving (PS) module implements the Idle mode (ARM7TDMI core clock stopped until the next interrupt) and enables the user to adapt the power consumption of the microcontroller to application requirements (independent peripheral clock control).

The Advanced Interrupt Controller (AIC) controls the internal sources from the internal peripherals and the four external interrupt lines (including the FIQ) to provide an interrupt and/or fast interrupt request to the ARM7TDMI. It integrates an 8-level priority controller, and using the Auto-vectoring feature, reduces the interrupt latency time.

The Parallel Input/Output Controller (PIO) controls up to 32 I/O lines. It enables the user to select specific pins for on-chip peripheral input/output functions, and general-purpose input/output signal pins. The PIO controller can be programmed to detect an interrupt on a signal change from each line.

The Watchdog (WD) can be used to prevent system lock-up if the software becomes trapped in a deadlock.

The Special Function (SF) module integrates the Chip ID, the Reset Status and the Protect registers.

User Peripherals

Two USARTs, independently configurable, enable communication at a high baud rate in synchronous or asynchronous mode. The format includes start, stop and parity bits and up to 8 data bits. Each USART also features a Time-out and a Time-guard register, facilitating the use of the two dedicated Peripheral Data Controller (PDC) channels.

The 3-channel, 16-bit Timer Counter (TC) is highly-programmable and supports capture or waveform modes. Each TC channel can be programmed to measure or generate different kinds of waves, and can detect and control two input/output signals. The TC has also 3 external clock signals.

Associated Documentation

Table 2. Associated Documentation

Product	Information	Document Title
AT91F40816	Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI (Thumb) Datasheet
	External memory interface mapping Peripheral operations Peripheral user interfaces	AT91x40 Series Datasheet
	DC characteristics Power consumption Thermal and reliability considerations AC characteristics	AT91M40800 Electrical Characteristics
	Product overview Ordering information Packaging information Soldering profile	AT91F40816 Summary Datasheet (this document)

Product Overview

Power Supply

The AT91F40816 has a single type of power supply pin, VDD. The VDD pin supplies the I/O pads and the core. The supported voltage range on V_{DD} is 2.7V to 3.6V.

Input/Output Considerations

The AT91F40816 I/O pads are 5V-tolerant except for the EBI Data Bus (D0 - D15). This enables the PIO pads to interface with external 5V devices without any additional components.

After the reset, the microcontroller peripheral I/Os are initialized as inputs to provide the user with maximum flexibility. It is recommended that in any application phase, the inputs to the microcontroller be held at valid logic levels to minimize the power consumption.

Master Clock

The AT91F40816 has a fully static design and works on the Master Clock (MCK), provided on the MCKI pin from an external source.

The Master Clock is also provided as an output of the device on the pin MCKO, which is multiplexed with a general-purpose I/O line. While NRST is active, MCKO remains low. After the reset, the MCKO is valid and outputs an image of the MCK signal. The PIO Controller must be programmed to use this pin as standard I/O line.

Reset

Reset restores the default states of the user interface registers (defined in the user interface of each peripheral), and forces the ARM7TDMI to perform the next instruction fetch from address zero. Except for the program counter the ARM7TDMI registers do not have defined reset states.

NRST Pin

NRST is active low-level input. It is asserted asynchronously, but exit from reset is synchronized internally to the MCK. The signal presented on MCKI must be active within the specification for a minimum of 10 clock cycles up to the rising edge of NRST, to ensure correct operation.

The first processor fetch occurs 80 clock cycles after the rising edge of NRST.

Watchdog Reset

The watchdog can be programmed to generate an internal reset. In this case, the reset has the same effect as the NRST pin assertion, but the pins BMS and NTRI are not sampled. Boot mode and Tri-state mode are not updated. If the NRST pin is asserted and the watchdog triggers the internal reset, the NRST pin has priority.

Emulation Functions

Tri-state Mode

The AT91F40816 provides a Tri-state mode, which is used for debug purposes in order to connect an emulator probe to an application board. In Tri-state mode, all the output pin drivers of the microcontroller are disabled.

This feature can also be used to program the embedded Flash within a standard NVM programmer.

To enter Tri-state mode, the pin NTRI must be held low during the last 10 clock cycles before the rising edge of NRST.

For normal operation, the pin NTRI must be held high during reset, by a resistor of up to 400K Ohm. NTRI is multiplexed with I/O line P21 and USART1 serial data transmit line TXD1.

Standard RS232 drivers generally contain internal 400K Ohm pull-up resistors. If TXD1 is connected to a device not including this pull-up, the user must make sure that a high level is tied on NTRI while NRST is asserted.

JTAG/ICE Debug

ARM standard embedded In-circuit emulation is supported via the JTAG/ICE port. The pins TDI, TDO, TCK and TMS are dedicated to this debug function and can be connected to a host computer via the external ICE interface.

In ICE Debug mode, the ARM7TDMI core responds with a non-JTAG chip ID that identifies the microcontroller. This is not fully IEEE1149.1 compliant.

Memory Controller

The ARM7TDMI processor address space is 4G bytes. The memory controller decodes the internal 32-bit address bus and defines three address spaces:

- Internal memories in the four lowest megabytes
- Middle space reserved for the external devices (memory or peripherals) controlled by the EBI
- Internal peripherals in the four highest megabytes

In any of these address spaces, the ARM7TDMI operates in Little-Endian mode only.

Internal Memories

The AT91F40816 integrates 8K bytes of primary internal SRAM that is 32 bits wide and single-clock cycle accessible. This SRAM is mapped at address 0x0 (after the remap command), allowing ARM7TDMI exception vectors between 0x0 and 0x20 to be modified by the software. The rest of the SRAM can be used for stack allocation (to speed up context saving and restoring), or as data and program storage for critical algorithms. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one cycle. Fetching Thumb or ARM instructions is supported and internal memory can store twice as many Thumb instructions as ARM ones.

The AT91F40816 also integrates a 2-Mbyte Flash memory that is accessed via the External Bus Interface. All data, address and control lines, except for the Chip Select signal, are connected within the device. Byte and half-word accesses are supported.

Boot Mode Select

The ARM reset vector is at address 0x0. After the NRST line is released, the ARM7TDMI executes the instruction stored at this address. This means that this address must be mapped in nonvolatile memory after the reset.

The input level on the BMS pin during the last 10 clock cycles before the rising edge of the NRST selects the type of boot memory (see Table 3). If the embedded Flash memory is to be used as boot memory, the BMS input must be pulled down externally.

The pin BMS is multiplexed with the I/O line P24 that can be programmed after reset like any standard PIO line.

Table 3. Boot Mode Select

BMS	Boot Memory
1	External 8-bit memory on NCS0
0	External 16-bit memory on NCS0

Remap Command

The ARM vectors (Reset, Abort, Data Abort, Prefetch Abort, Undefined Instruction, Interrupt, Fast Interrupt) are mapped from address 0x0 to address 0x20. In order to allow these vectors to be redefined dynamically by the software, the AT91F40816 uses a remap command that enables switching between the boot memory and the internal primary SRAM addresses. The remap command is accessible through the EBI User Interface by writing one in RCB of

EBI_RCR (Remap Control Register). Performing a remap command is mandatory if access to the other external devices (connected to chip-selects 1 to 7) is required. The remap operation can only be changed back by an internal reset or an NRST assertion.

Abort Control

The abort signal providing a Data Abort or a Prefetch Abort exception to the ARM7TDMI is asserted when accessing an undefined address in the EBI address space.

No abort is generated when reading the internal memory or by accessing the internal peripherals, whether the address is defined or not.

External Bus Interface

The External Bus Interface handles the accesses between addresses 0x0040 0000 and 0xFFC0 0000. It generates the signals that control access to the external devices, and can be configured from eight 1-Mbyte banks up to four 16-Mbyte banks. It supports byte, half-word and word aligned accesses.

For each of these banks, the user can program:

- Number of wait states
- Number of data float times (wait time after the access is finished to prevent any bus contention in case the device is too long in releasing the bus)
- Data bus-width (8-bit or 16-bit).
- With a 16-bit wide data bus, the user can program the EBI to control one 16-bit device (Byte Access Select mode) or two 8-bit devices in parallel that emulate a 16-bit memory (Byte Write Access Mode).

The External Bus Interface features also the Early Read Protocol, configurable for all the devices, that significantly reduces access time requirements on an external device in the case of single-clock cycle access.

In the AT91F40816, the External Bus Interface connects internally to the Flash memory.

Flash Memory

The 16M-bit Flash memory is organized as 1,048,576 16-bit words. The Flash memory is addressed as 16-bit words via the EBI. It uses address lines A1 to A20. Address line A20 must not be reprogrammed as an I/O pin or as a chip select, as it is the most significant bit of the Flash memory address.

The address, data and control signals, except the Flash memory enable, are internally interconnected. The user should connect the Flash memory enable (NCSF) to one of the active-low chip selects on the EBI. NCS0 must be used if the Flash memory is to be the boot memory. In addition, if the Flash memory is to be used as boot memory, the BMS input must be pulled down externally in order for the processor to perform correct 16-bit fetches after reset.

During boot, the EBI must be configured with correct number of standard wait states. For example, five standard wait states are required when the microcontroller is running at 40 MHz.

The user must ensure that all VDD and all GND pins are connected to their respective supplies by the shortest route. The Flash memory powers-on in the read mode. Command sequences are used to place the device in other operating modes, such as program and erase.

A separate Flash memory reset input pin (NRSTF) is provided for maximum flexibility, enabling the reset operation to adapt to the application. When this input is at a logic high-level, the memory is in its standard operating mode; a low-level on this input halts the current memory operation and puts its outputs in a high impedance state.

The Flash memory features data polling to detect the end of a program cycle. While a program cycle is in progress, an attempted read of the last word written returns the complement of the written data on I/O7. An open-drain NBUSY output pin provides another method of detecting

the end of a program or erase cycle. This pin is pulled low while program and erase cycles are in progress, and it is released at the completion of the cycle. A toggle bit feature provides a third means of detecting the end of a program or erase cycle.

The Flash memory is segmented into two memory planes. Reads from one memory plane may be performed even while program or erase functions are being executed in the other memory plane. This feature enhances performance by not requiring the system to wait for a program or erase cycle to complete before a read may be performed.

The Flash memory is divided into 40 sectors for erase operations. To further enhance device flexibility, an Erase Suspend feature is offered. This feature puts the erase cycle on hold for an indefinite period and allows the user to read data from, or to write data to, any other sector within the same memory plane. There is no need to suspend an erase cycle if the data to be read is in the other memory plane. The device has the capability to protect data stored in any sector. Once the data protection for a sector is enabled, the data in that sector cannot be changed while input levels lie between ground and V_{DD}.

An optional VPP pin is available to enhance the program/erase times. See the AT49BV1604(T)/1614(T) “16 Mbits, 2.7-Volt Read and 2.7-Volt Byte-Write Sectored Flash” datasheet for further detail.

A 6-byte command sequence (Bypass Unlock) allows the device to be written to directly, using single pulses on the write control lines. This mode (Single Pulse Programming) is exited by powering down the device or by pulsing the NRSTF pin low for a minimum of 50 ns and then bringing it back to V_{DD}.

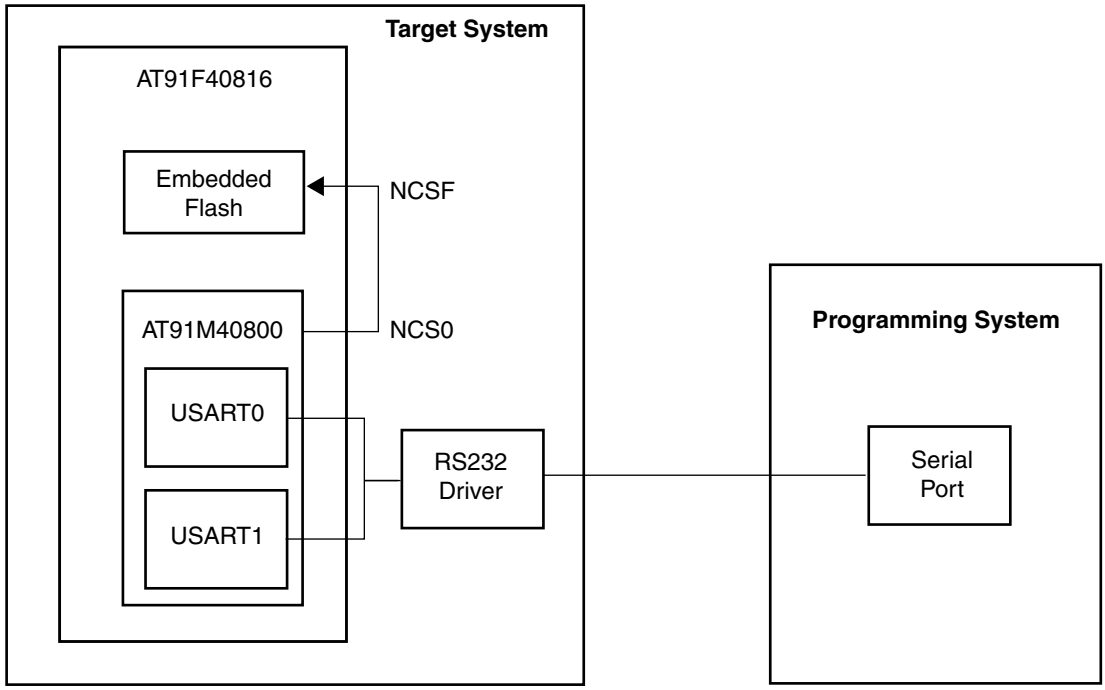
The following hardware features protect against inadvertent programming of the Flash memory.

- V_{DD} Sense – if V_{DD} is below 1.8V (typical), the program function is inhibited
- V_{DD} Power-on Delay – once V_{DD} has reached the V_{DD} sense level, the device automatically times out 10 ms (typically) before programming
- Program Inhibit – holding any one of OE low, CE high or WE high inhibits program cycles
- Noise Filter – pulses of less than 15 ns (typical) on the WE or CE inputs do not initiate a program cycle

AT91 Flash Uploader Software

All Flash-based AT91 devices are delivered with a factory-programmed software called the AT91 Flash Uploader, which resides in the first sector of the embedded Flash. The Flash Uploader allows programming to the embedded flash through a serial port. Either of the on-chip USARTs can be used by the Flash Uploader.

Figure 3. Flash Uploader



Flash Uploader Operations

The Flash Uploader requires NCS0 to be connected to NCSF and a valid clock to be applied to MCKI. The chip select line loop allows the ARM Core to boot from the embedded Flash when the reset is de-asserted. Next, the Flash Uploader immediately recopies itself in the internal SRAM and jumps into it. The following operation requires this memory resource only. External accesses are performed only to program the Flash.

When starting, PIO input change interrupts are initialized on the RXD lines of both USARTs. When an interrupt occurs, a Timer Counter channel is started. When the next input change is detected on the RXD line, the Timer Counter channel is stopped. This is how the first character length is measured and the USART can be initiated by taking into account the ratio between the device master clock speed and the actual communication baud rate speed.

The Programming System, then, can send commands and data following a proprietary protocol for the Flash device to be programmed. It is up to the Programming System to erase and program the first sector of the Flash lastly, in order to reduce, at a minimum, the risk that the Flash Uploader is erased and the power supply shuts down.

In the event that the Flash Uploader is erased from the first sector while the new final application is not yet programmed, and while the target system power supply is switched off, it would lead to a non-recoverable error and the AT91F40816 could not be re-programmed by using the Flash Uploader.

Programming System

Atmel provides a free Host Loader that runs on an IBM compatible PC under Windows®95 or Windows®98 operating system. It can be downloaded from the Atmel web site and requires only a serial cable to connect the Host to the Target.

Communications can be selected on either COM1 or COM2 and the serial link speed is limited to 115200 bauds. Because the serial link is the bottleneck in this configuration, the Flash programming lasts 110 seconds per Mbytes.

Programming time can be reached by using a faster programming system. An EB40 (AT91 Evaluation Board for the x40 Series Microcontroller) is capable of running a serial link at up to 500 Kbits/sec and can match the fastest programming allowed by the Flash, for example, about 40 seconds per Mbyte when the word programming becomes the bottleneck.

Peripherals

The AT91F40816 peripherals are connected to the 32-bit wide Advanced Peripheral Bus.

Peripheral registers are only word accessible. Byte and half-word accesses are not supported. If a byte or a half-word access is attempted, the memory controller automatically masks the lowest address bits and generates an word access.

Each peripheral has a 16-Kbyte address space allocated (the AIC only has a 4-Kbyte address space).

Peripheral Registers

The following registers are common to all peripherals:

- Control Register – write only register that triggers a command when a one is written to the corresponding position at the appropriate address. Writing a zero has no effect.
- Mode Register – read/write register that defines the configuration of the peripheral. Usually has a value of 0x0 after a reset.
- Data Registers – read and/or write register that enables the exchange of data between the processor and the peripheral.
- Status Register – read only register that returns the status of the peripheral.
- Enable/Disable/Status Registers – shadow command registers. Writing a one in the Enable Register sets the corresponding bit in the Status Register. Writing a one in the Disable Register resets the corresponding bit and the result can be read in the Status Register. Writing a bit to zero has no effect. This register access method maximizes the efficiency of bit manipulation, and enables modification of a register with a single non-interruptible instruction, replacing the costly read-modify-write operation.

Unused bits in the peripheral registers must be written at 0 for upward compatibility. These bits read 0.

Peripheral Interrupt Control

The Interrupt Control of each peripheral is controlled from the status register using the interrupt mask. The status register bits are ANDed to their corresponding interrupt mask bits and the result is then ORed to generate the Interrupt Source signal to the Advanced Interrupt Controller.

The interrupt mask is read in the Interrupt Mask Register and is modified with the Interrupt Enable Register and the Interrupt Disable Register. The enable/disable/status (or mask) makes it possible to enable or disable peripheral interrupt sources with a non-interruptible single instruction. This eliminates the need for interrupt masking at the AIC or Core level in real-time and multi-tasking systems.

Peripheral Data Controller

The AT91F40816 has a 4-channel PDC dedicated to the two on-chip USARTs. One PDC channel is dedicated to the receiver and one to the transmitter of each USART.

The user interface of a PDC channel is integrated in the memory space of each USART. It contains a 32-bit Address Pointer Register (RPR or TPR) and a 16-bit Transfer Counter Register (RCR or TCR). When the programmed number of transfers are performed, a status bit indicating the end of transfer is set in the USART Status Register and an interrupt can be generated.

System Peripherals

PS: Power-saving

The Power-saving feature optimizes power consumption, enabling the software to stop the ARM7TDMI clock (idle mode) and restarting it when the module receives an interrupt (or reset). It also enables on-chip peripheral clocks to be enabled and disabled individually, matching power consumption and application needs.

AIC: Advanced Interrupt Controller

The Advanced Interrupt Controller has an 8-level priority, individually maskable, vectored interrupt controller, and drives the NIRQ and NFIQ pins of the ARM7TDMI from:

- The external fast interrupt line (FIQ)
- The three external interrupt request lines (IRQ0-IRQ2)
- The interrupt signals from the on-chip peripherals

The AIC is extensively programmable, offering maximum flexibility, and its vectoring features reduce the real-time overhead in handling interrupts.

The AIC also features a spurious vector detection feature, which reduces spurious interrupt handling to a minimum, and a protect mode that facilitates the debug capabilities.

PIO: Parallel I/O Controller

The AT91F40816 has 32 programmable I/O lines. Six pins are dedicated as general-purpose I/O pins. Other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The PIO controller enables generation of an interrupt on input change and insertion of a simple input glitch filter on any of the PIO pins.

WD: Watchdog

The Watchdog is built around a 16-bit counter and is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or interrupt, or assert an active level on the dedicated pin NWDOVF. All programming registers are password-protected to prevent unintentional programming.

SF: Special Function

The AT91F40816 provides registers that implement the following special functions.

- Chip Identification
- RESET Status
- Protect Mode

User Peripherals

USART: Universal Synchronous/ Asynchronous Receiver Transmitter

The AT91F40816 provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters.

Each USART has its own baud rate generator, and two dedicated Peripheral Data Controller channels. The data format includes a start bit, up to 8 data bits, an optional programmable parity bit and up to 2 stop bits.

The USART also features a Receiver Time-out register, facilitating variable length frame support when it is working with the PDC, and a Time-guard register, used when interfacing with slow remote equipment.

TC: Timer Counter

The AT91F40816 features a Timer Counter block that includes three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions, including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

The Timer Counter can be used in Capture or Waveform mode, and all three counter channels can be started simultaneously and chained together.

Ordering Information

Table 4. Ordering Information

Ordering Code	Package	Temperature Operating Range
AT91F40816-33CI	BGA 120	Industrial (-40°C to 85°C)

Packaging Information

Figure 4. 120-ball Ball Grid Array Package Drawing

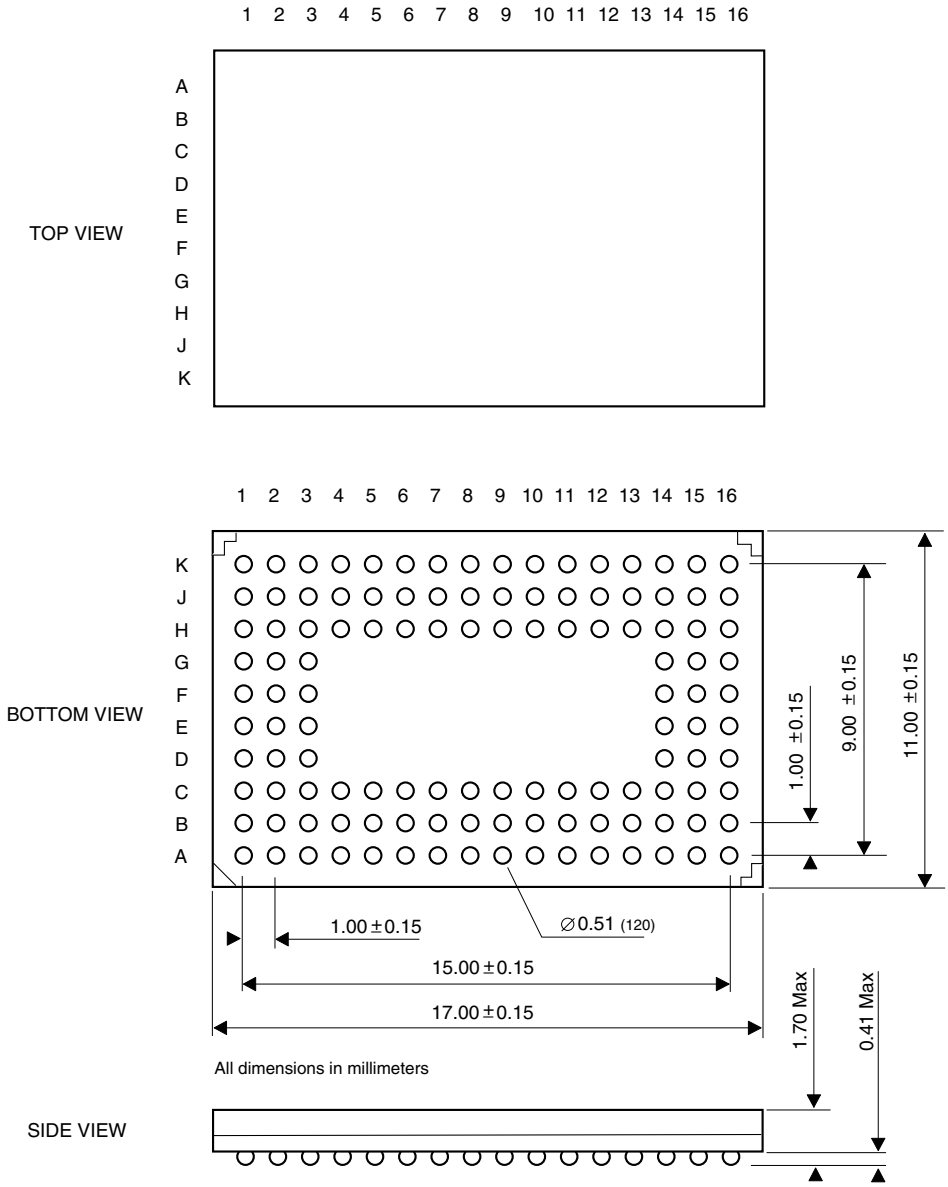


Table 5. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Units
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	120-BGA	36.6	°C/W
θ_{JC}	Junction-to-case thermal resistance		120-BGA	11	

Table 6. Device and 120-ball BGA Package Maximum Weight

605	mg

Soldering Profile

Table 7 gives the recommended soldering profile from J-STD-20.

Table 7. Soldering Profile

	Convection or IR/Convection	VPR
Average Ramp-up Rate (183°C to Peak)	3°C/sec. max.	10°C/sec.
Preheat Temperature 125°C ±25°C	120 sec. max	
Temperature Maintained Above 183°C	60 sec. to 150 sec.	
Time within 5°C of Actual Peak Temperature	10 sec. to 20 sec.	60 sec.
Peak Temperature Range	220 +5/-0°C or 235 +5/-0°C	215 to 219°C or 235 +5/-0°C
Ramp-down Rate	6°C/sec.	10°C/sec.
Time 25°C to Peak Temperature	6 min. max	

Small packages may be subject to higher temperatures if they are reflowed in boards with larger components. In this case, small packages may have to withstand temperatures of up to 235°C, not 220°C (IR reflow).

Recommended package reflow conditions depend on package thickness and volume. See Table 8.

Table 8. Recommended Package Reflow Conditions (1, 2, 3)

Parameter	Temperature
Convection	220 +5/-0°C
VPR	215 to 219°C
IR/Convection	220 +5/-0°C

Notes:
1. The packages are qualified by Atmel by using IR reflow conditions, not convection or VPR.
2. By default, the package level 1 is qualified at 220°C (unless 235°C is stipulated).
3. The body temperature is the most important parameter but other profile parameters such as total exposure time to hot temperature or heating rate may also influence component reliability.

A maximum of three reflow passes is allowed per component.

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Version A	**Publication Date:** Jul-00
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Revisions Since Previous Version

Page: 4	Change in Table 1
Page: 10	Added information to section Internal Memories
Page: 18	Added Table 6
Page: 19	Added section Soldering Profile

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