MP8720

26V,10A, High Efficiency, Fast Transient, Synchronous, Buck Converter with adjustable CLM

The Future of Analog IC Technology

DESCRIPTION

The MP8720 provides a complete power supply with the highest power density for system powers, such as DDR memory and USB type-C. The MP8720 integrates a high-frequency, synchronous, rectified, step-down, switch-mode converter (V_{OUT}) with an adjustable current limit (CLM).

The MP8720 operates at high efficiency over a wide output current load range based on MPS's proprietary switching loss reduction technology and internal low $R_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

By setting CLM, the current limit can be adjusted from 8.5A to 16.5A for different mode applications.

Full protection features include over-current limit (OCL), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP8720 requires a minimal number of external components and is available in a QFN-16 (3mmx3mm) package.

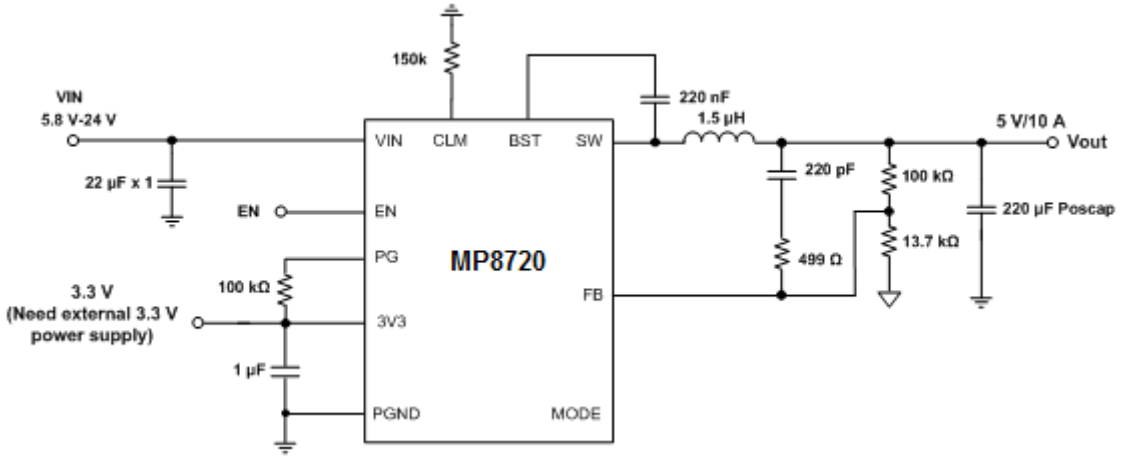
FEATURES

- Wide 4.5V to 26V Operating Input Range
- Compatible for USB Type-C
- 10A Continous Output Current
- Adjustable Current Limit from 8.5A to 16.5A
- Fixed 700KHz Switching Frequency
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Stable with POSCAP and Ceramic Output Capacitors
- Internal Soft Start (SS)
- Selectable Pulse Skip or Forced CCM
- Output Adjustable from 0.8V to 5.5V
- OCL, OVP, UVP, and Thermal Shutdown
- Latch-Off Reset via EN or Power Cycle
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Televisions
- Networking Systems
- Distributed Power System
- Set-Top-Box

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8720GQ	QFN-16 (3mmx3mm)	*See below*

* For Tape & Reel, add suffix –Z (e.g. MP8720GQ–Z)

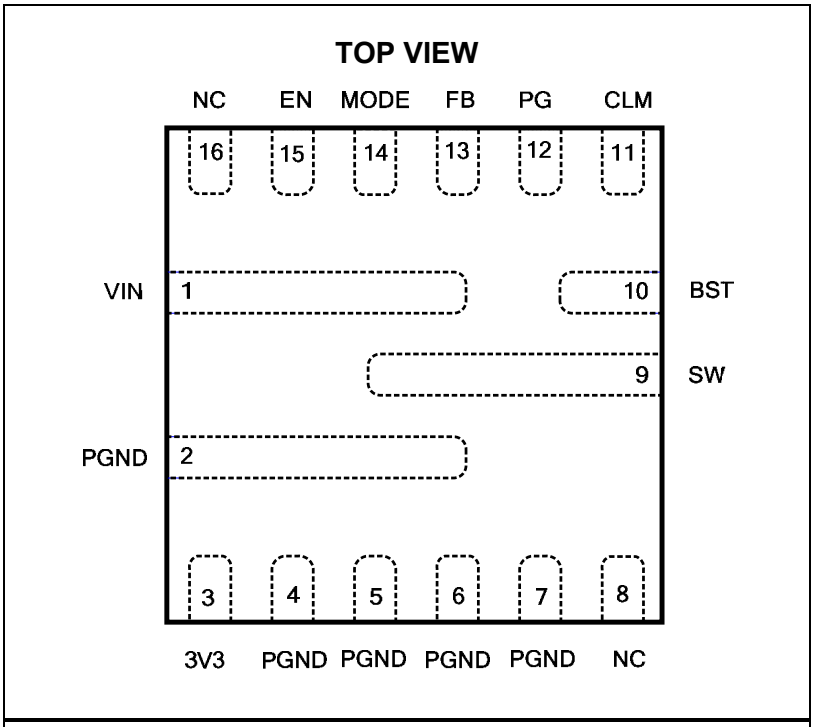
TOP MARKING

BCTY

LLL

BCT: product code of MP8720GQ;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 26V
V_{SW} (DC) ..... -1V to VIN + 0.3V
V_{SW} (25ns) ..... -3.6V to VIN + 4V (2)
V_{BST} ..... V_{SW} + 4.5V
All other pins ..... -0.3V to +4.5V
Continuous power dissipation (T_A = +25°C) (3)
QFN-16 (3mmx3mm) 2.3W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply voltage (VIN) ..... 4.5V to 24V
Supply voltage (V_{CC}) ..... 3.15V to 3.5V
Output voltage (V_{OUT}) ..... 0.8V to 5.5V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
QFN-16 (3mmx3mm)	55	13	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN = 12V, 3V3 = 3.3V, T_J = 25°C, R_{MODE} = 0Ω, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
3V3 supply current	I_{3V3}	V_{EN} = 3V, V_{FB} = 0.65V, no load		140	230	μA
3V3 shutdown current	$I_{3V3\ SDN}$	V_{EN} = 0V, no load			1	μA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}	T_J = 25°C		19		mΩ
Low-side switch on resistance	LS_{RDS-ON}	T_J = 25°C		7		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT}	CLM = 0Ω		8.5		A
		CLM = 90kΩ	9	10	11	A
		CLM = 150kΩ		13		A
		CLM = float		16.5		A
Switching Frequency and Minimum Off Time						
Switching frequency	Fs			700		kHz
Constant on timer	T_{ON}	VIN = 5V, V_{OUT} = 1.8V	430	515	600	ns
Minimum on time (6)	$T_{ON\ MIN}$			70		ns
Minimum off time (6)	$T_{OFF\ MIN}$			240		ns
Protection						
OVP threshold	V_{OVP}		125	130	135	$\%V_{REF}$
UVP-1 threshold	V_{UVP-1}		70	75	80	$\%V_{REF}$
UVP-1 foldback timer (6)	T_{UVP-1}			30		μs
UVP-2 threshold	V_{UVP-2}		45	50	55	$\%V_{REF}$
Reference and Soft Start, Soft Stop						
Reference voltage	V_{REF}		594	600	606	mV
Feedback current	I_{FB}	V_{FB} = 0.62V		10	50	nA
Soft-start time	T_{SStart}	EN to PG up	1.8	2.2	2.6	ms
MODE						
Mode source current	I_{MODE}		9	10	11.4	μA
Enable and UVLO						
En rising threshold	$V_{EN\ TH}$		1.12	1.22	1.32	V
En hysteresis	V_{EN-HYS}			125		mV
Enable input current	I_{EN}	V_{EN} = 2V			5	μA
		V_{EN} = 0V			1	
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.9	3.0	3.1	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			220		mV
VIN under-voltage lockout threshold rising	VIN_{VTH}			4.2	4.4	V
VIN under-voltage lockout threshold hysteresis	VIN_{HYS}			360		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, 3V3 = 3.3V, T_J = 25°C, R_{MODE} = 0Ω, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good						
PG when FB rising (good)	$PG_{\_Rising(GOOD)}$	V_{FB} rising, percentage of V_{FB}		95		%
PG when FB falling (fault)	$PG_{\_Falling(Fault)}$	V_{FB} falling, percentage of V_{FB}		90		
PG when FB rising (fault)	$PG_{\_Rising(Fault)}$	V_{FB} rising, percentage of V_{FB}		115		
PG when FB falling (good)	$PG_{\_Falling(GOOD)}$	V_{FB} falling, percentage of V_{FB}		105		
PG low to high delay	PG_{Td}			3		µs
EN low to PG low delay	$PG_{Td\ EN\ low}$				1	µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Thermal Protection						
Thermal shutdown (6)	T_{SD}			150		°C
Thermal shutdown hysteresis	$T_{SD\ HYS}$			25		°C

NOTE:

6) Guaranteed by design.

PIN FUNCTIONS

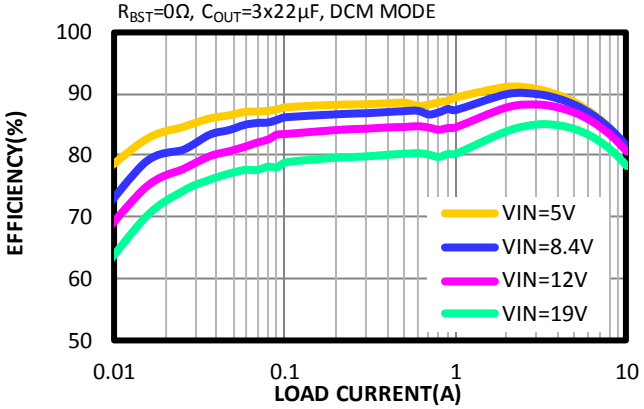
PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power for the internal MOSFET and regulator. The MP8720 operates from a +4.5V to +26V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2, 4, 5, 6, 7	PGND	**Power ground.** Use wide PCB traces and multiple vias to make the connection.
3	3V3	**External 3V3 VCC input for control and driver.** Place a 1μF decoupling capacitor close to 3V3 and PGND. It is recommended to form an R-C filter.
8, 16	NC	**No connection.** NC can either be connected to VIN, SW, or GND for easy layout.
9	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is connected to VIN when the HS-FET is on. SW is connected to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. SW is noisy, so keep sensitive traces away from SW.
10	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
11	CLM	**Current limit adjust.** There are four settings for the current, which can be set by connecting CLM to GND with different kinds of resistors.
12	PG	**Power good output.** PG is an open-drain signal. PG is high if the output voltage is within a proper range.
13	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces.
14	MODE	**Mode.** Select MODE for different output ranges and to select DCM or CCM.
15	EN	**Enable.** When EN = 1, the regulator turns on; when EN = 0, the regulator turns off.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, F_{SW} = 700kHz, DCM, CLM = 16A, T_J = +25°C, unless otherwise noted.

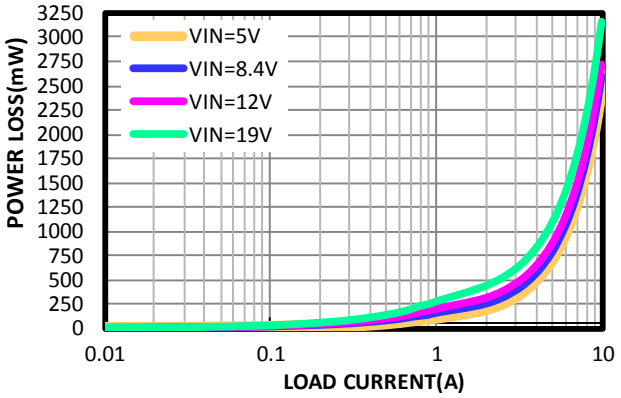
Efficiency

V_{OUT}=1.2V, F_{SW}=700kHz, L=0.68µH, DCR=3.1mΩ, R_{BST}=0Ω, C_{OUT}=3x22µF, DCM MODE



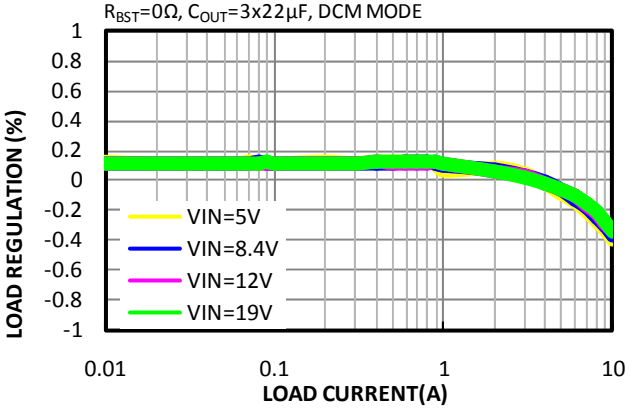
Power Loss

V_{OUT}=1.2V, F_{SW}=700kHz, L=0.68µH, DCR=3.1mΩ, R_{BST}=0Ω, C_{OUT}=3x22µF, DCM MODE



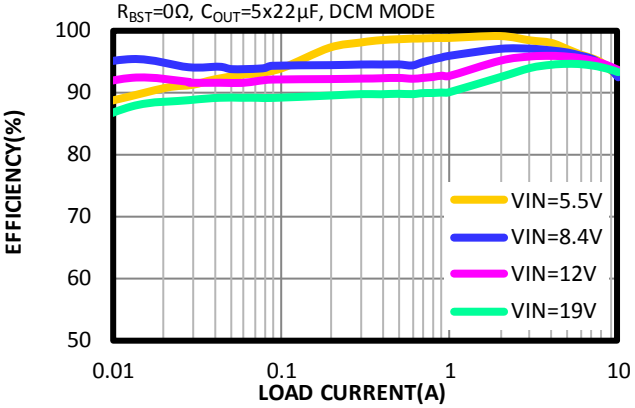
Load Regulation vs. Load Current

V_{OUT}=1.2V, F_{SW}=700kHz, L=0.68µH, DCR=3.1mΩ, R_{BST}=0Ω, C_{OUT}=3x22µF, DCM MODE



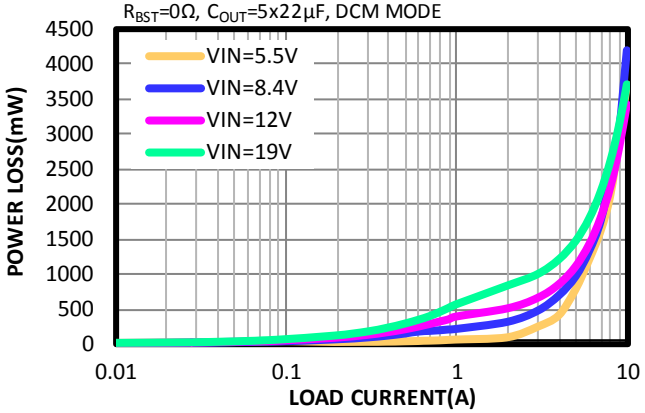
Efficiency

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, DCR=10mΩ, R_{BST}=0Ω, C_{OUT}=5x22µF, DCM MODE



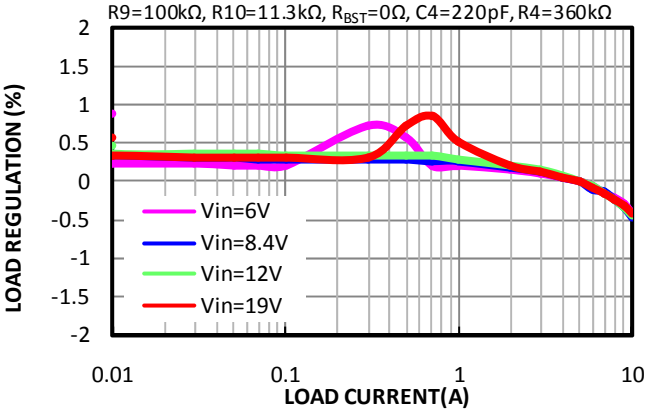
Power Loss

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, DCR=10mΩ, R_{BST}=0Ω, C_{OUT}=5x22µF, DCM MODE



Load Regulation

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, 744323150, C_{OUT}=3x47µF, R9=100kΩ, R10=11.3kΩ, R_{BST}=0Ω, C4=220pF, R4=360kΩ

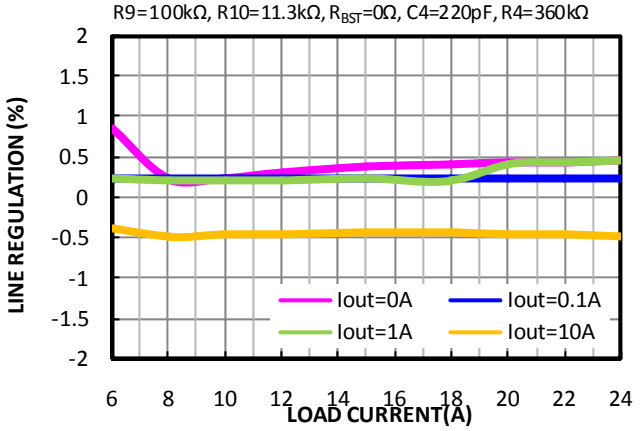


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, F_{SW} = 700kHz, DCM, CLM = 16A, T_J = +25°C, unless otherwise noted.

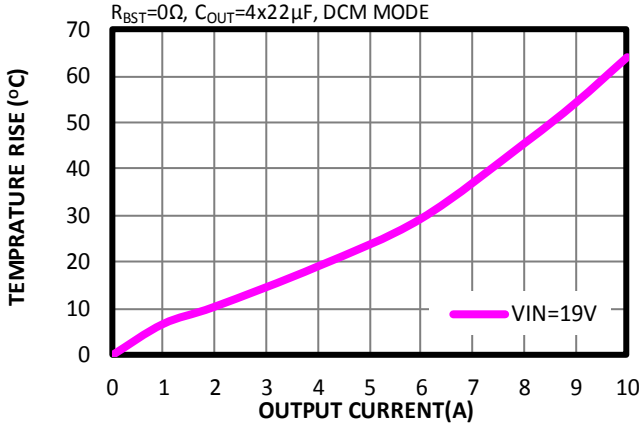
Line Regulation

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, 744323150, C_{OUT}=3x47µF, R9=100kΩ, R10=11.3kΩ, R_{BST}=0Ω, C4=220pF, R4=360kΩ



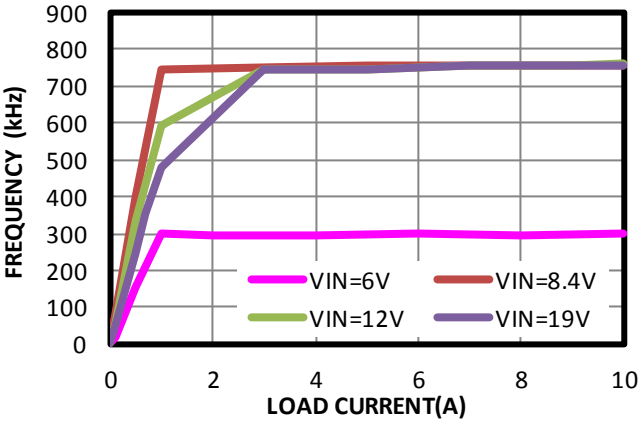
Temperature Rise with Load Current

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, DCR=4.3mΩ, R_{BST}=0Ω, C_{OUT}=4x22µF, DCM MODE



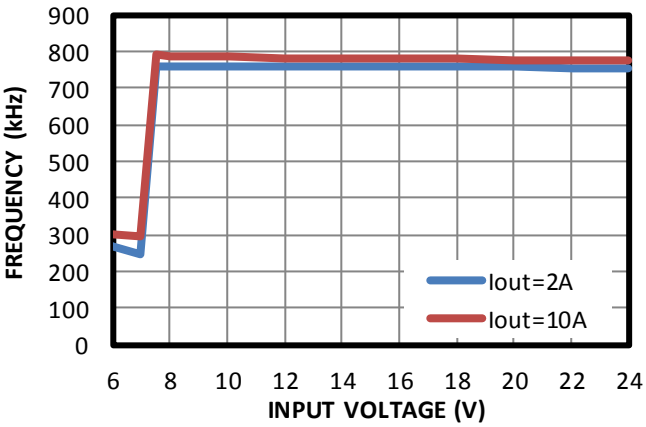
Frequency vs. Load Current

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, DCM MODE

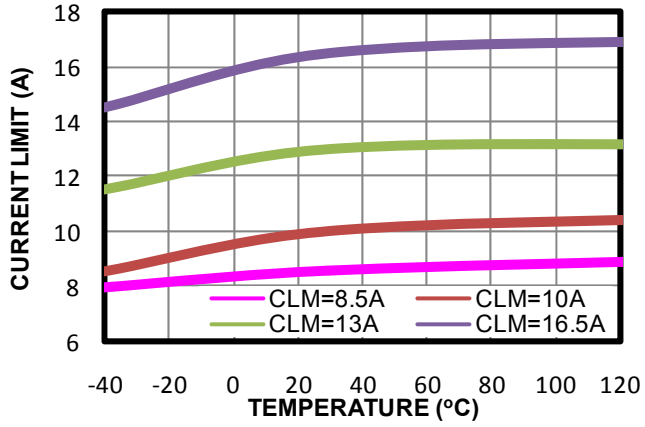


Frequency vs. Input Voltage

V_{OUT}=5V, F_{SW}=700kHz, L=1.5µH, DCM MODE



Current Limit vs. Temperature

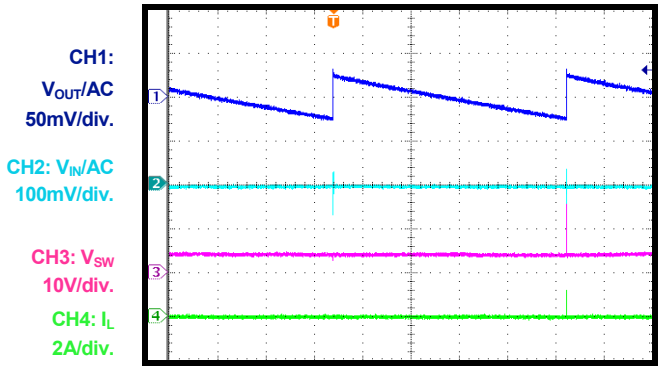


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, F_{SW} = 700kHz, DCM, CLM = 16A, T_J = +25°C, unless otherwise noted.

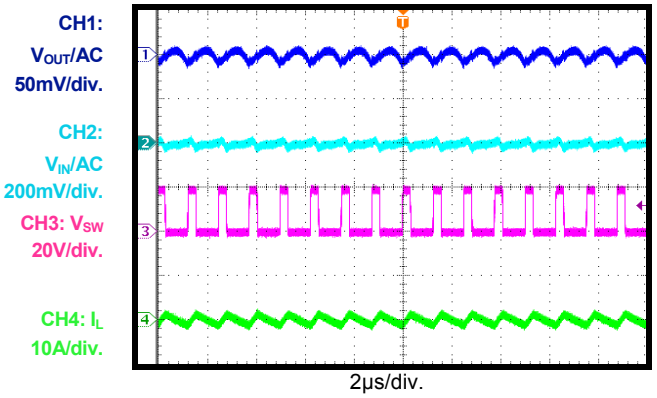
Input/Output Voltage Ripple

I_{OUT} = 0A, DCM



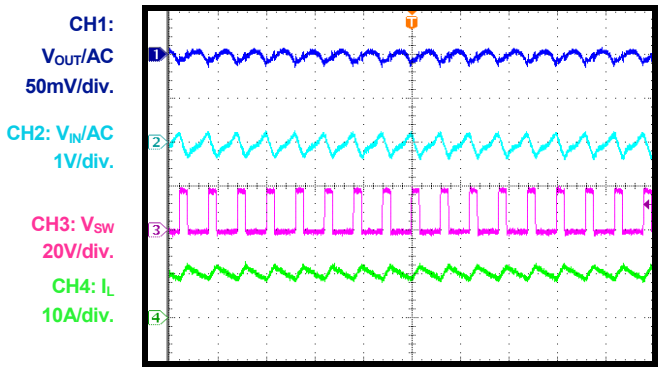
Input/Output Voltage Ripple

I_{OUT} = 0A, CCM



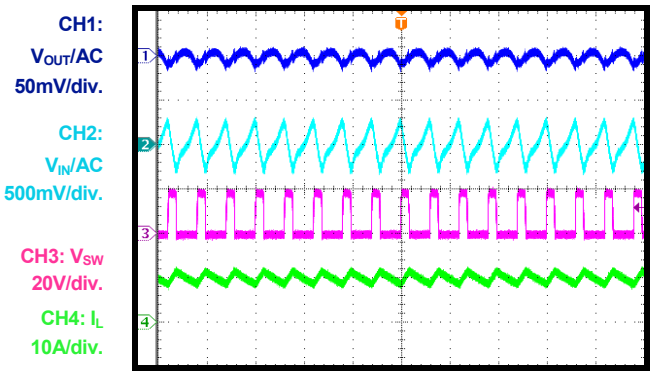
Input/Output Voltage Ripple

I_{OUT} = 10A, DCM



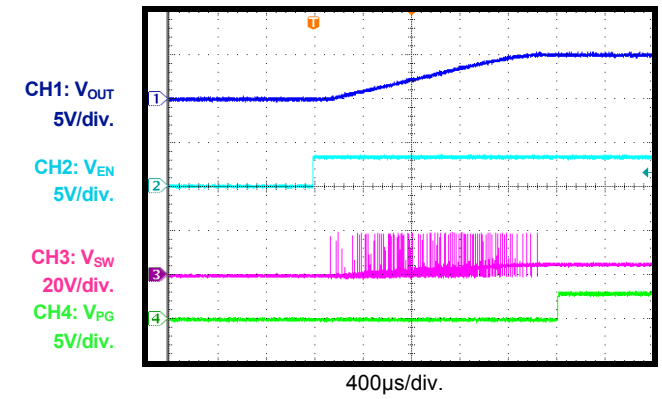
Input/Output Voltage Ripple

I_{OUT} = 10A, CCM



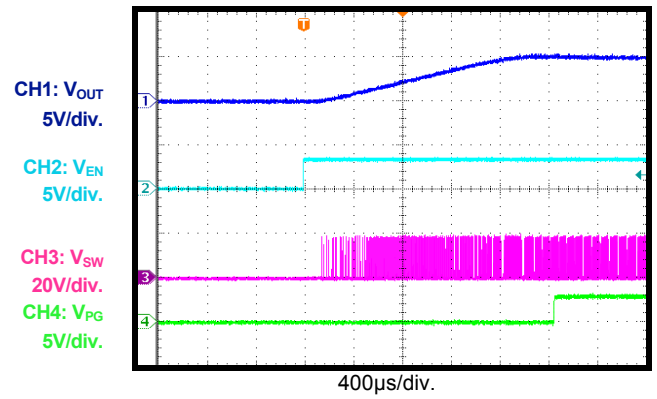
Power Good through EN Start-Up

I_{OUT} = 0A, DCM



Power Good through EN Start-Up

I_{OUT} = 10A, DCM

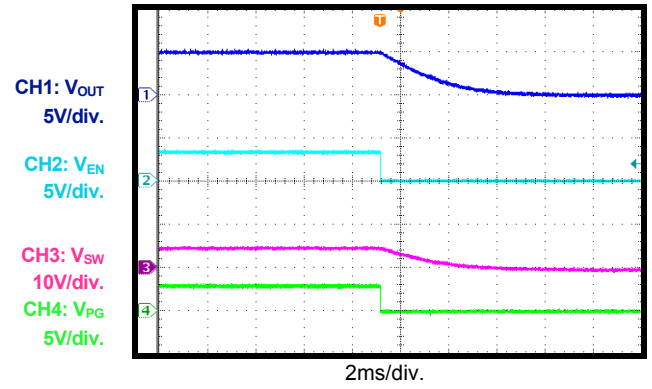


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, F_{SW} = 700kHz, DCM, CLM = 16A, T_J = +25°C, unless otherwise noted.

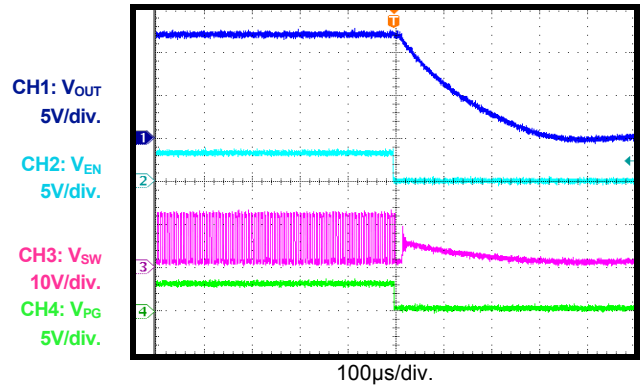
Power Good through EN Shutdown

I_{OUT} = 0A, DCM



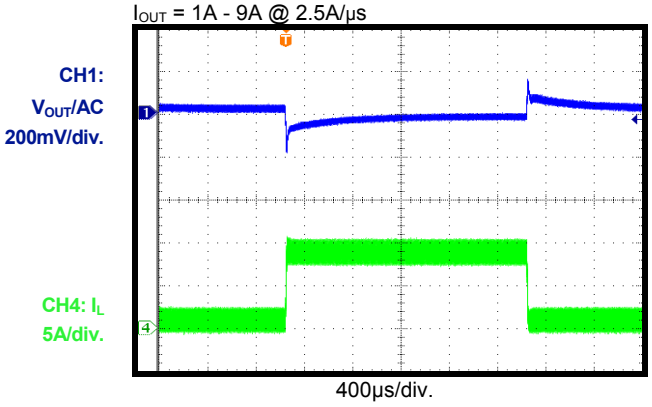
Power Good through EN Shutdown

I_{OUT} = 10A, DCM



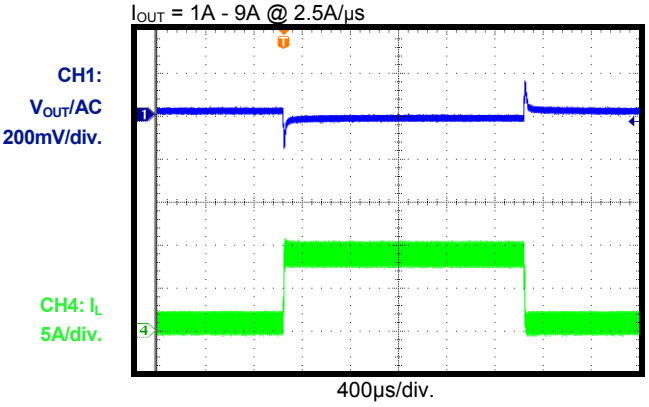
Transient

VIN = 19V, L = 1.5µH, C_{OUT} = 6 x 22µF, DCM,
I_{OUT} = 1A - 9A @ 2.5A/µs



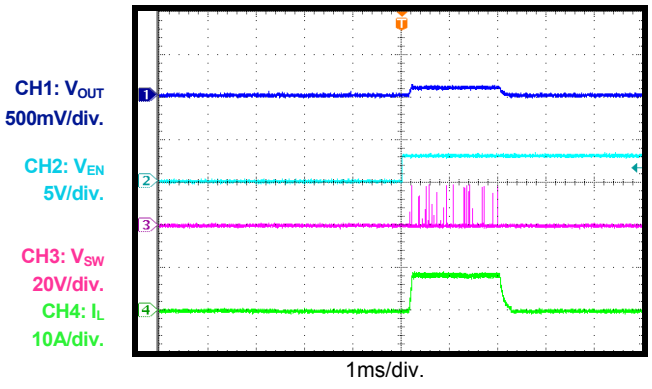
Transient

VIN = 19V, L = 1.5µH, C_{OUT} = 6 x 22µF , CCM,
I_{OUT} = 1A - 9A @ 2.5A/µs



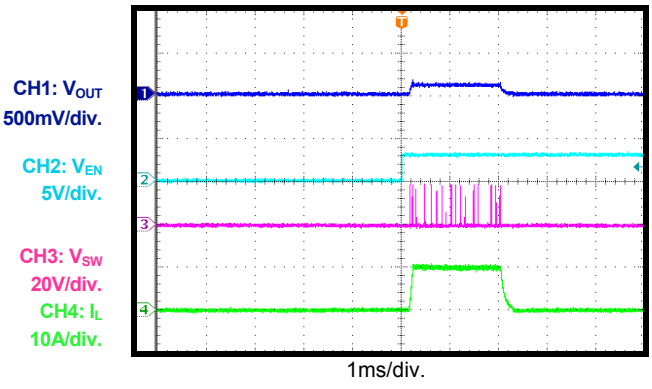
Short-Circuit Protection through EN Up

Set CLM = 8.5A, VIN = 19V



Short-Circuit Protection through EN Up

Set CLM = 10A, VIN = 19V

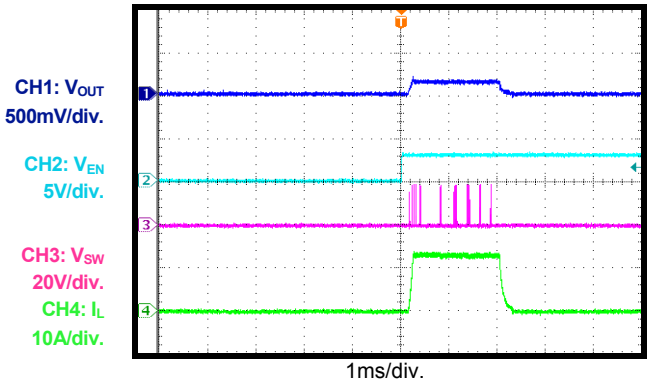


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, F_{SW} = 700kHz, DCM, CLM = 16A, T_J = +25°C, unless otherwise noted.

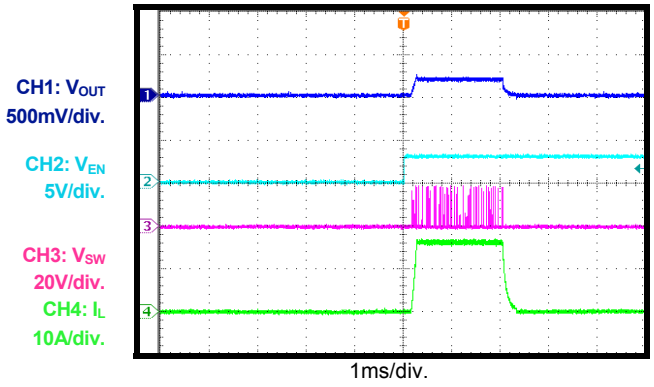
Short-Circuit Protection through EN Up

Set CLM = 13A, VIN = 19V



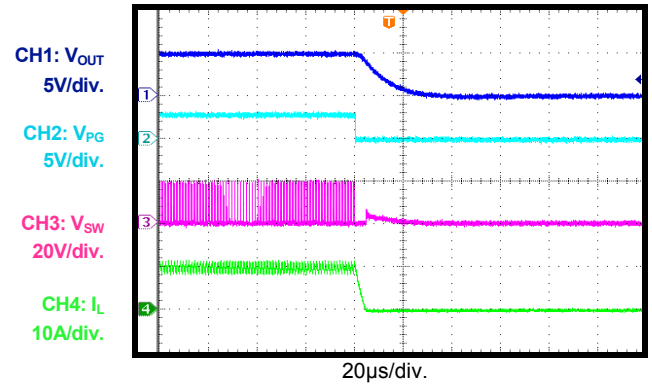
Short-Circuit Protection through EN Up

Set CLM = 16.5A, VIN = 19V



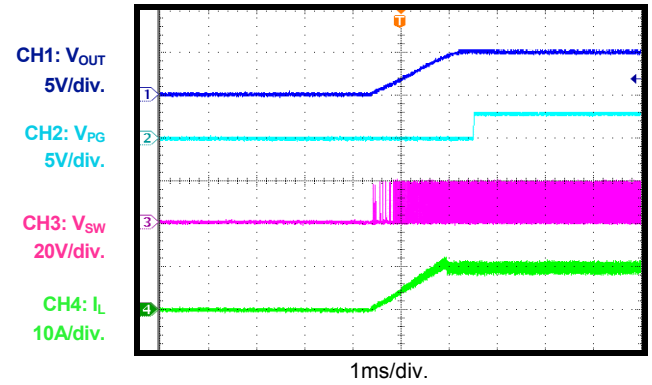
Thermal Shutdown

VIN = 19V, I_{OUT} = 10A



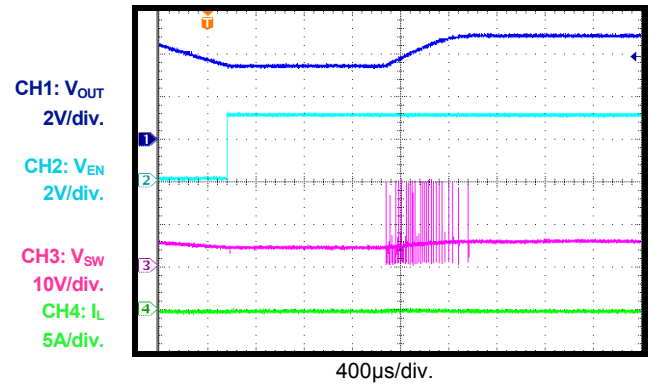
Thermal Recovery

VIN = 19V, I_{OUT} = 10A



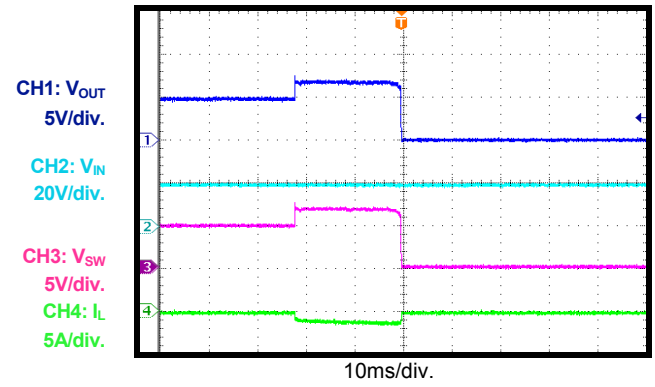
EN Pre-Bias Start-Up

VIN = 19V, I_{OUT} = 10A



OVP Circuit Protection

VIN = 19V, I_{OUT} = 10A, Force V_{OUT} = 6.8V



BLOCK DIAGRAM

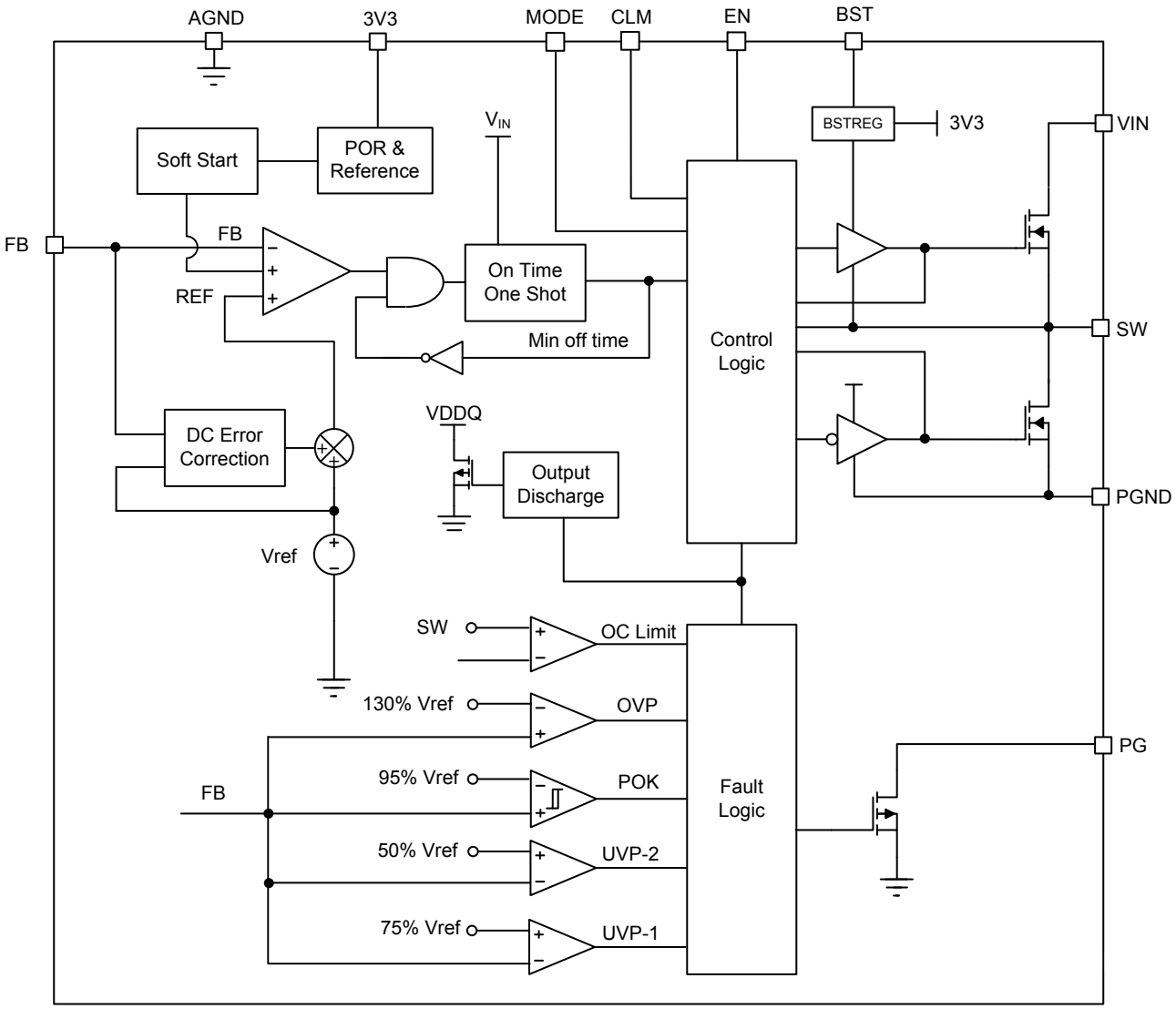


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MP8720 is a fully integrated, synchronous, rectified, step-down, switch-mode converter with an adjustable current limit (CLM). Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and the input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between the input and GND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control for stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on timer. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant (pulse-width modulation (PWM) mode).

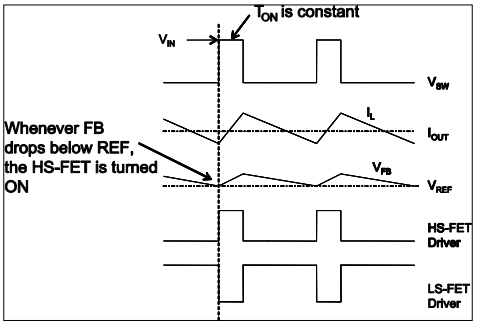


Figure 2: CCM Operation

Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MP8720 transitions from CCM to discontinuous conduction mode (DCM). DCM operation is shown in Figure 3.

When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (Hi-Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Therefore, the output capacitors discharge slowly to GND through the LS-FET. As a result, the efficiency during light-load condition improves greatly. The HS-FET does not turn on as frequently during a light-load condition as it does during a heavy-load condition (skip mode).

At a light-load or no-load condition, the output drops very slowly, and the MP8720 reduces the switching frequency naturally, achieving high efficiency at light load.

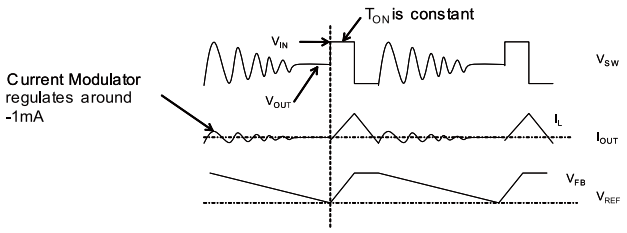


Figure 3: DCM Operation

As the output current increases from light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, making the switching frequency increases. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

The MP8720 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 4 and Figure 5). Jitter affects system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope, so the jitter in DCM is usually larger than it is in CCM. However, the V_{FB} ripple does not affect noise immunity directly.

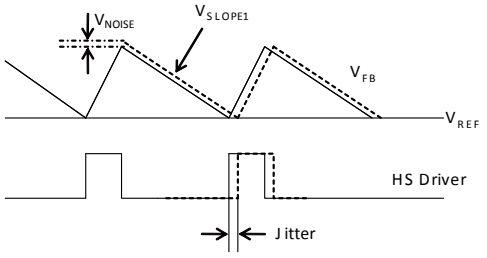


Figure 4: Jitter in PWM Mode

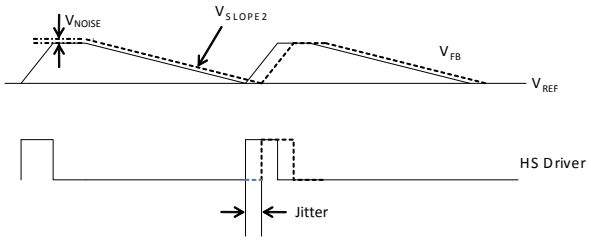


Figure 5: Jitter in Skip Mode

Operating without External Ramp Compensation

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to act as an effective current-sense resistor.

Usually, ceramic capacitors cannot be used directly as output capacitors.

The MP8720 has built-in internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. Use the pure ceramic capacitor solution, which reduces the output ripple, total BOM cost, and board area significantly.

Figure 6 shows a typical output circuit in PWM mode without an external ramp circuit. Refer to the Application Information section on page 17 for design steps without external compensation.

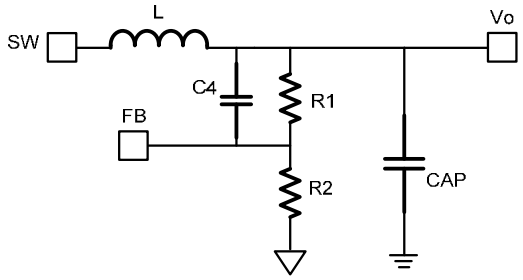


Figure 6: Simplified Output Circuit

When using a large capacitor (e.g.: OSCON) on the output, add a >10μF ceramic capacitor in parallel to minimize the effect of ESL.

Operating with External Ramp Compensation

Usually, the MP8720 is able to support ceramic output capacitors without an external ramp. However in some cases, the internal ramp may not be enough to stabilize the system, or there is too much jitter, which requires external ramp compensation. Refer to the Application Information section on page 17 for design steps with external ramp compensation.

MODE Selection

The MP8720 implements MODE for multiple applications for output and switching mode selection. The output and switch mode can be selected by a different resistor on MODE. There are four modes that can be selected for normal application with external resistors (see Table 2). It is recommended to use a 1% accuracy resistor.

Table 2: MODE Selection

State	V_{OUT}	DCM/CCM	Resistor to GND
M1	Vo < 3V	DCM	0Ω
M2	Vo < 3V	CCM	90kΩ
M3	Vo ≥ 3V	CCM	150kΩ
M4	Vo ≥ 3V	DCM	>230kΩ or float

Power Good (PG)

The MP8720 uses a power good (PG) output to indicate whether the output voltage of the V_{OUT} regulator is ready. PG is the open drain of a MOSFET. It should be connected to V_{CC} or another voltage source through a resistor (e.g.: 100kΩ). After the input voltage is applied, the MOSFET is turned on, so PG is pulled to GND before SS is ready. After V_{FB} reaches 95% of V_{REF}, PG is pulled high (after a delay time within 10μs). When V_{FB} drops to 90% of V_{REF}, PG is pulled low.

Soft Start (SS)

The MP8720 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN becomes high, the internal reference voltage ramps up gradually, and the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the MP8720 enters steady-state operation (see Figure 7).

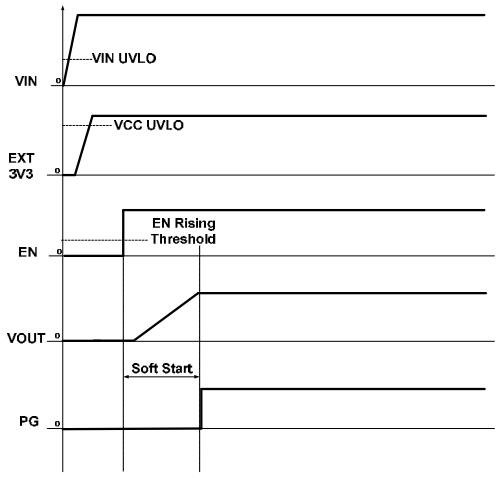


Figure 7: Start-Up Power Sequence

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and the low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Output Discharge

The MP8720 discharges the output through an internal 100Ω resistor when the controller is turned off by a protection function (UVP, OCP, OVP, UVLO, or thermal shutdown).

Over-Current Limit (OCL)

The MP8720 has cycle-by-cycle over-current limiting control. The current-limit circuit employs a valley current-sensing algorithm. The MP8720 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle, even if FB is lower than REF (see Figure 8).

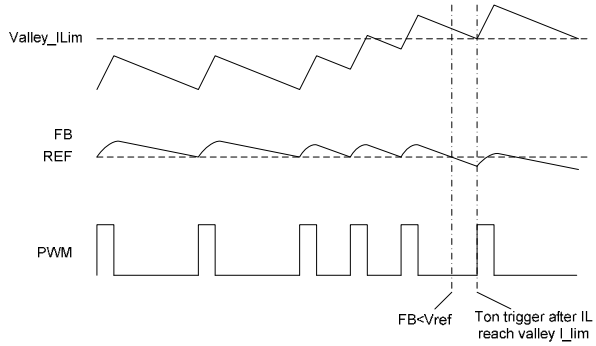


Figure 8: Valley Current-Limit Control

Since the comparison is done during the LS-FET on state, the over-current trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (I_{OC}) can be calculated using Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The over-current limit (OCL) limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, so the output voltage tends to fall off. Eventually, the current ends up crossing the under-voltage protection (UVP) threshold and latches off. Fault latching can be reset by EN going low or cycling the power of VIN.

Current Limit (CLM) Selection

The MP8720 implements an adjustable valley CLM by connecting CLM to GND with different resistor values (see Table 3).

Table 3: CLM Selection

State	CLM	Resistor to GND
M1	8.5A	0Ω
M2	10A	90kΩ
M3	13A	150kΩ
M4	16.5A	>230kΩ or float

Over/Under-Voltage Protection (OVP, UVP)

The MP8720 monitors a resistor divided feedback voltage to detect over- and under-voltage. When the feedback voltage rises higher than 130% of the target voltage, the OVP comparator output goes high, the circuit latches as the HS-FET turns off, and the LS-FET turns on, acting as a -2A current source.

To protect the MP8720 from damage, there is an absolute 3.6V OVP on V_{OUT} when the system is in V_{OUT} < 3V mode. Once V_{OUT} reaches this value, it latches off. The LS-FET behaves the same as it does at 130% OVP.

When the feedback voltage drops below 75% of V_{REF}, but remains higher than 50% of V_{REF}, the UVP-1 comparator output goes high, and the MP8720 latches if V_{FB} remains in this range for about 30μs (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current reaches zero. During this period, the valley current limit helps control the inductor current.

When the feedback voltage drops below 50% of V_{REF}, the UVP-2 comparator output goes high, and the MP8720 latches off directly after the comparator and logic delay (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current reaches zero. Fault latching can be reset by driving EN low or cycling the power of VIN.

Under-Voltage Lockout (UVLO) Protection

The MP8720 has two under-voltage lockout (UVLO) protections: a 3V V_{CC} UVLO and a 4.2V VIN UVLO. The MP8720 starts up only when both V_{CC} and VIN exceed their respective UVLO thresholds. The MP8720 shuts down when either V_{CC} is lower than the UVLO falling threshold voltage (typically 2.8V) or VIN is lower than the 3.8V VIN falling threshold. Both UVLO protections are non-latch off.

If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see Figure 9).

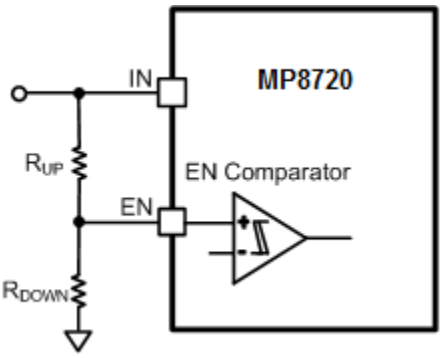


Figure 9: Adjustable UVLO

Thermal Shutdown

Thermal shutdown is employed in the MP8720. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 125°C, a new soft start is initiated.

APPLICATION INFORMATION

Setting the Output Voltage with No External Ramp

The MP8720 does not need ramp compensation for applications where POSCAP or ceramic capacitors are set as output capacitors (when VIN is over 6V), so the external compensation is not needed. The output voltage is then set by feedback resistors R1 and R2 (see Figure 10).

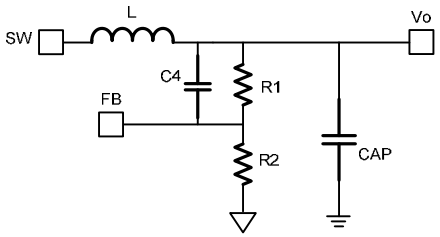


Figure 10: Simplified Circuit without External Ramp

First, choose a value for R2. R2 should be chosen reasonably. A small value for R2 leads to considerable quiescent current loss, but an R2 value that is too large makes FB noise-sensitive. It is recommended to choose a value within 5 - 50kΩ for R2. Use a comparatively larger value for R2 when V_{OUT} is low; use a smaller value for R2 when V_{OUT} is high. Considering the output ripple, R1 is determined with Equation (3):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (3)$$

C4 acts as a feed-forward capacitor to improve the transient and can be set in the range of 0 - 1000pF. A larger value for C4 leads to better transient, but it is more noise sensitive. Reserve room for a noise filter resistor (R9) (see Figure 11).

Setting the Output Voltage with External Compensation

If the system is not stable enough or there is too much jitter when a ceramic capacitor is used on the output (i.e.: with a ceramic C_{OUT} and VIN is 5V or lower), an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Since there is already an internal ramp added in the system, a 1MΩ (R4), 220pF (C4) ramp should suffice.

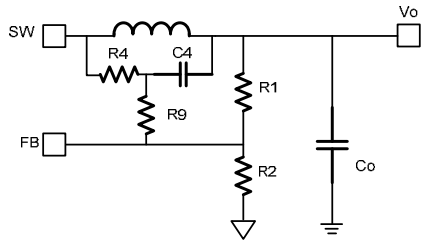


Figure 11: Simplified Circuit with External Ramp

Besides the R1 and R2 divider, the output voltage is influenced by R4 (see Figure 12). R2 should be chosen reasonably. A small value for R2 leads to considerable quiescent current loss, but a value for R2 that is too large makes FB noise sensitive. It is recommended to choose a value within 5 - 50kΩ for R2. Use a comparatively larger value for R2 when V_{OUT} is low; use a smaller value for R2 when V_{OUT} is high. The value of R1 then is determined with Equation (4):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \cdot R_2 \quad (4)$$

To get a pole for better noise immunity, set R9 with Equation (5):

$$R_9 \le \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (5)$$

Set R9 in the range of 100Ω to 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (10)$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, which mainly causes the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The output voltage ripple caused by the ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR dominates the output ripple. The output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

The maximum output capacitor limitation should be considered in the design application. The MP8720 has a soft-start time period around 1.6ms. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (13):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period (which can be equivalent to the current limit), and T_{ss} is the soft-start time.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current, resulting in a lower output ripple voltage, but also has a larger physical footprint, a higher series resistance, and a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 50% of the maximum output current, and the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including a short-current), so I_{SAT} is recommended to be >13A.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation of the IC. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 12 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
   A thick PGND trace under the IC should be top priority.
2. Place the input capacitors as close to VIN and GND as possible on the same layer as the IC.
3. Place the decoupling capacitor as close to VCC and GND as possible.
4. Keep the switching node (SW) short and away from the feedback network.
5. Place the external feedback resistors next to FB.
6. Ensure that there is no via on the FB trace.
7. Keep the BST voltage path (BST, C3, and SW) as short as possible.
8. Keep the VIN and GND pads connected with a large copper plane to achieve better thermal performance.
9. Add several vias with 10mil drill/18mil copper width close to the VIN and GND pads to help thermal dissipation.

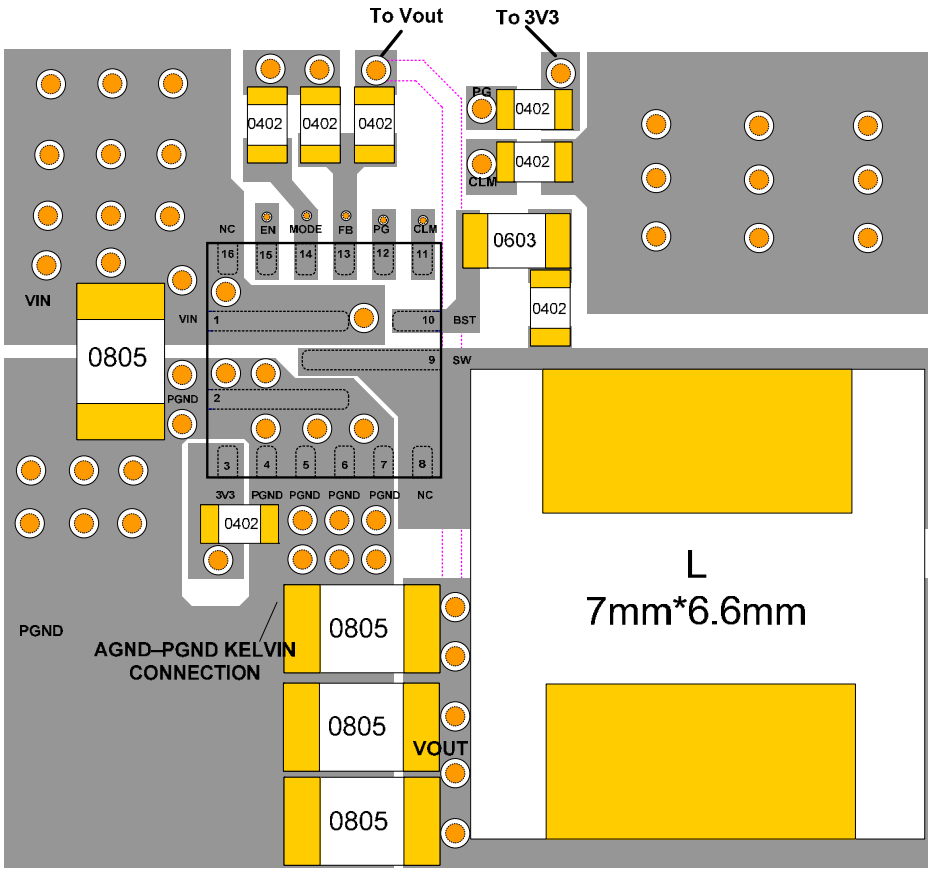


Figure 12: Recommended PCB Layout

Design Example

Table 4 shows the application for different output parameter settings when ceramic capacitors are applied.

There is a resistor from an external 3.3V supply to 3V3 acting as a ripple noise filter of the 3.3V power supply. It is recommended to have a resistor value from 0 - 5.1Ω depending on the noise level. A size 0402 resistor is sufficient if the 3.3V voltage rises up with SS > 100μs. Otherwise, a larger resistor (e.g.: 0603/0805) is needed.

For applications where VIN is 5V or lower, it is recommended to apply the SCH shown in Figure 14 with a proper external ramp.

The MP8720 also supports non-DDR applications with very compact external components (see Figure 15).

Some design examples are provided below when ceramic capacitors are applied:

Table 4: Design Example for 700kHz f_{SW}

V_{OUT} (V)	Cout (F)	L (μH)	R_{Mode} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)
1.0V	22μx3	0.68	0	220	13.3	20	NS
1.2	22μx3	0.68	0	220	20	20	NS
5	220μF poscap	1.5	Float	220	100	13.7	NS
5	22 μx6	1.5	Float	220	100	10	274

TYPICAL APPLICATION CIRCUITS

Application for 5V Output

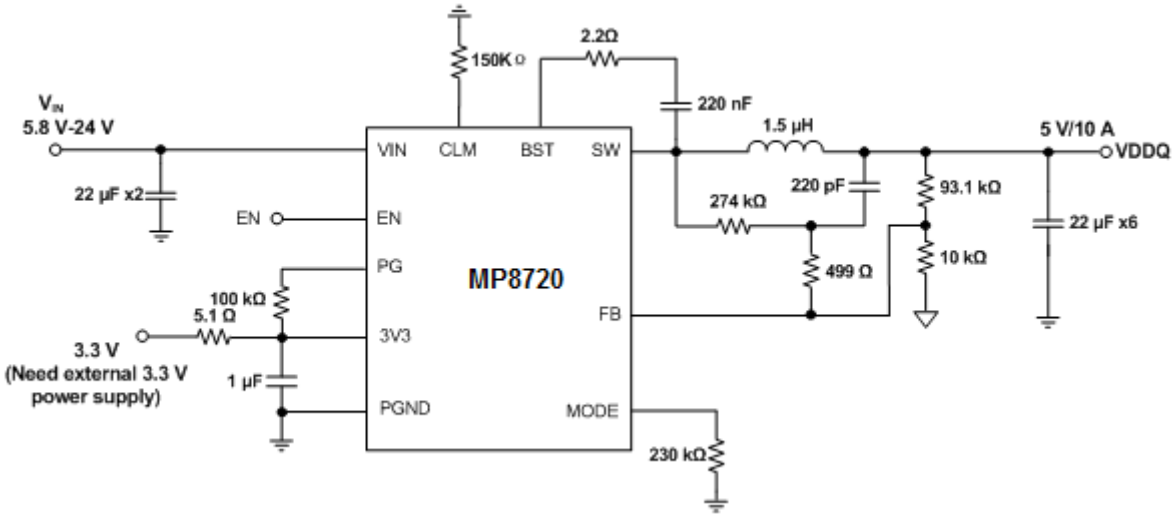


Figure 13: 5V Output Application

1.0V Output Application

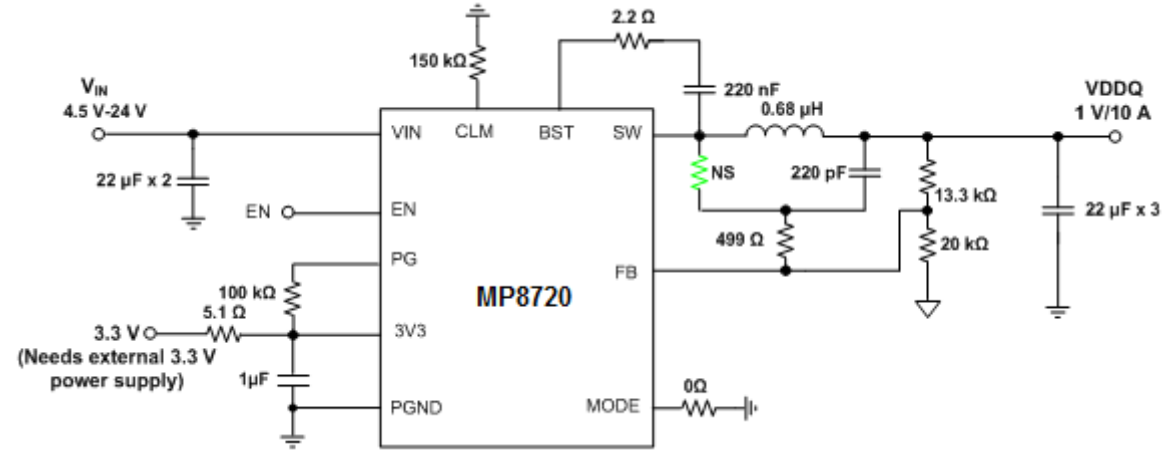


Figure 14: 1.0V Output Application

TYPICAL APPLICATION CIRCUITS *(continued)*

5.0V Output Application with Forced CCM

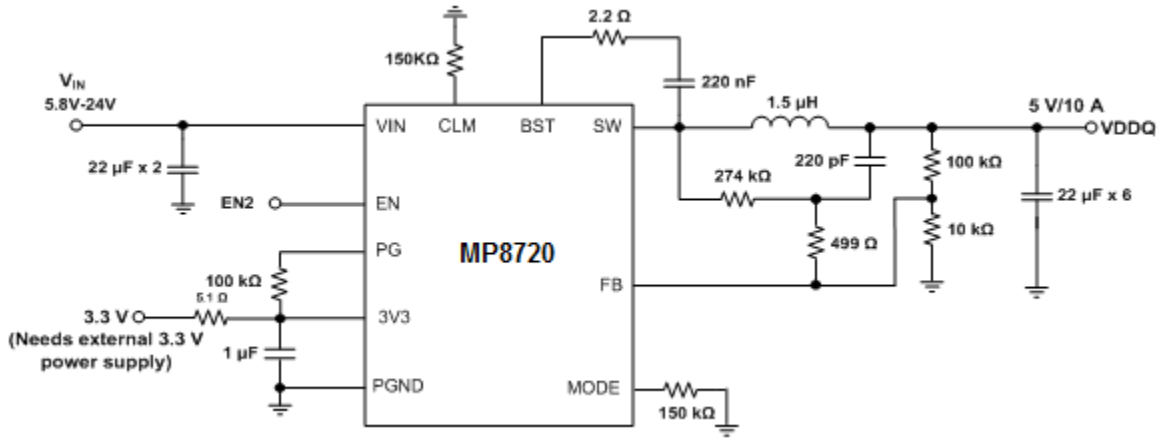
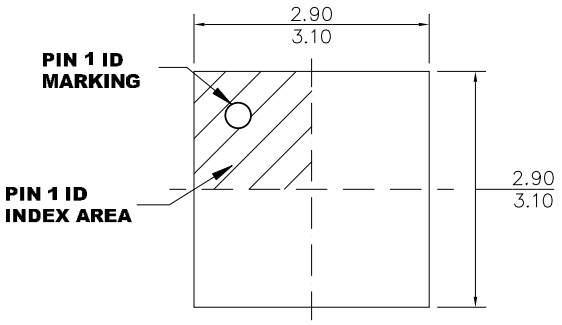


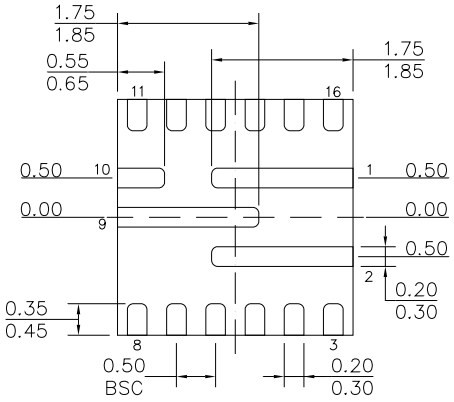
Figure 15: 5V Output Application with Forced CCM

PACKAGE INFORMATION

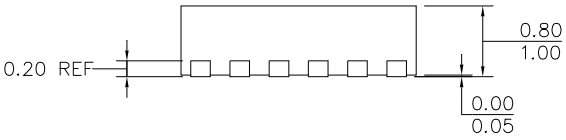
QFN-16 (3mmx3mm)



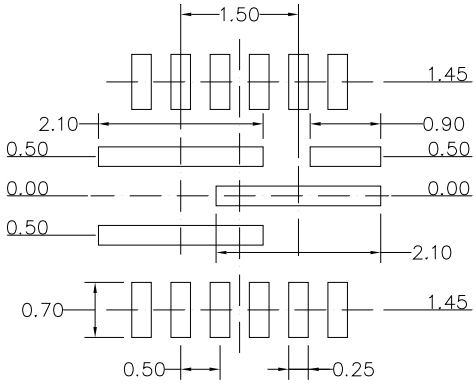
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.