HC5513

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- **DI Monolithic High Voltage Process**
- **Programmable Current Feed (20mA to 60mA)**
- **Programmable Loop Current Detector Threshold and Battery Feed Characteristics**
- **Ground Key and Ring Trip Detection**
- **Compatible with Ericsson's PBL3764**
- **Thermal Shutdown**
- **On-Hook Transmission**
- **Wide Battery Voltage Range (-24V to -58V)**
- **Low Standby Power**
- **Meets TR-NWT-000057 Transmission Requirements**
- **-40°C to 85°C Ambient Temperature Range**

Applications

- **Digital Loop Carrier Systems**
- **Fiber-In-The-Loop ONUs**
- **Wireless Local Loop**
- **Hybrid Fiber Coax**
- **Related Literature**
  - **AN9537, Operation of the HC5513/26 Evaluation Board**
- **Pair Gain**
- **POTS**
- **PABX**

Description

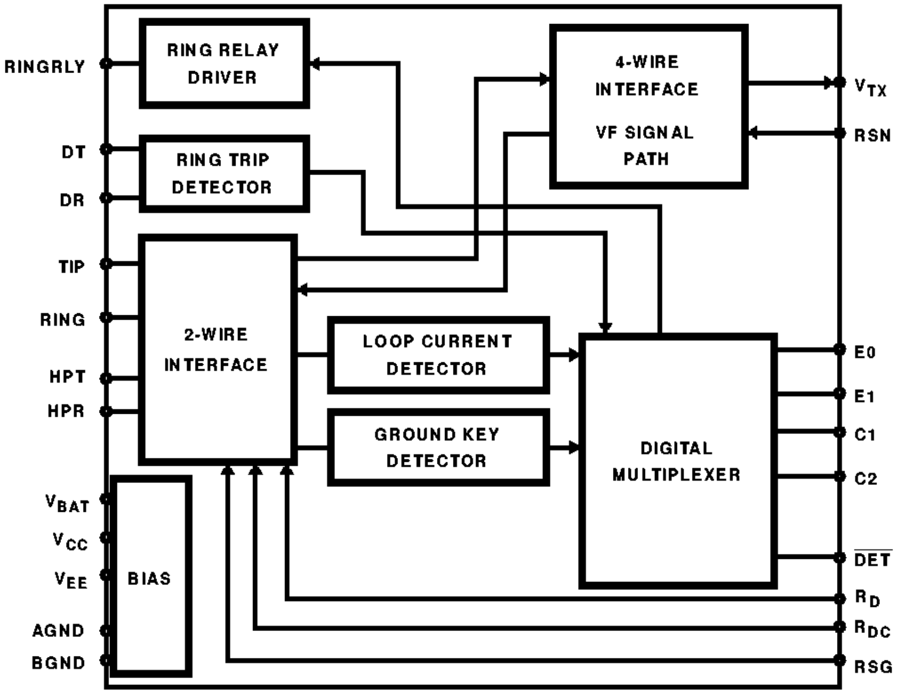
The HC5513 is a subscriber line interface circuit which is interchangeable with Ericsson's PBL3764 for distributed central office applications. Enhancements include immunity to circuit latch-up during hot plug and absence of false signaling in the presence of longitudinal currents.

The HC5513 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with Junction Isolated (JI) ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC5513 ideally suited for use in harsh outdoor environments.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5513BIM	-40 to 85	28 Ld PLCC	N28.45
HC5513BIP	-40 to 85	22 Ld PDIP	E22.4

Block Diagram



Absolute Maximum Ratings

Operating Temperature Range	-40°C to 110°C
Power Supply (-40°C ≤ T_A ≤ 85°C)	
Supply Voltage V_{CC} to GND	0.5V to 7V
Supply Voltage V_{EE} to GND	-7V to 0.5V
Supply Voltage V_{BAT} to GND	-70V to 0.5V
Ground	
Voltage between AGND and BGND	-0.3V to 0.3V
Relay Driver	
Ring Relay Supply Voltage	0V to V_{BAT} 75V
Ring Relay Current	50mA
Ring Trip Comparator	
Input Voltage	V_{BAT} to 0V
Input Current	-5mA to 5mA
Digital Inputs, Outputs (C1, C2, E0, E1, $\overline{DET}$)	
Input Voltage	0V to V_{CC}
Output Voltage ($\overline{DET}$ Not Active)	0V to V_{CC}
Output Current ($\overline{DET}$)	5mA
Tipx and Ringx Terminals (-40°C ≤ T_A ≤ 85°C)	
Tipx or Ringx Voltage, Continuous (Referenced to GND)	V_{BAT} to 2V
Tipx or Ringx, Pulse < 10ms, T_{REP} > 10s	V_{BAT} -20V to 5V
Tipx or Ringx, Pulse < 10µs, T_{REP} > 10s	V_{BAT} -40V to 10V
Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s	V_{BAT} -70V to 15V
Tipx or Ringx Current	70mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}°C/W
22 Lead PDIP Package	53
28 Lead PLCC Package	53
Continuous Dissipation at 70°C	
22 Lead PDIP Package	1.5W
28 Lead PLCC Package	1.5W
Package Power Dissipation at 70°C, t < 100ms, t_{REP} > 1s	
22 Lead PDIP Package	4W
28 Lead PLCC Package	4W
Derate above	70°C
Plastic DIP Package	18.8mW/°C
PLCC Package	18.8mW/°C
Maximum Junction Temperature Range	-40°C to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (PLCC - Lead Tips Only)	300°C

Die Characteristics

Gate Count	543 Transistors, 51 Diodes

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	°C
V_{CC} with Respect to AGND	-40°C to 85°C	4.75	-	5.25	V
V_{EE} with Respect to AGND	-40°C to 85°C	-5.25	-	-4.75	V
V_{BAT} with Respect to BGND	-40°C to 85°C	-58	-	-24	V

Electrical Specifications

T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, $R_{DC1} = R_{DC2}$ = 41.2kΩ, R_D = 39kΩ, $R_{SG} = \infty$, $R_{F1} = R_{F2}$ = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z_L = 600Ω, (Note 2, Figure 1)	3.1	-	-	V_{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 3, Figure 2)	-	20	35	Ω/Wire

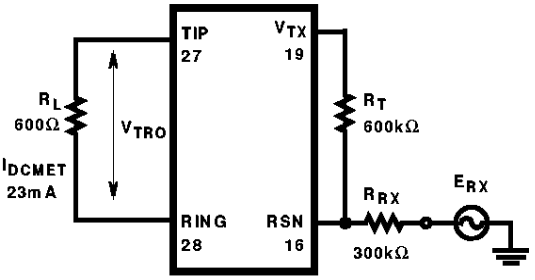


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

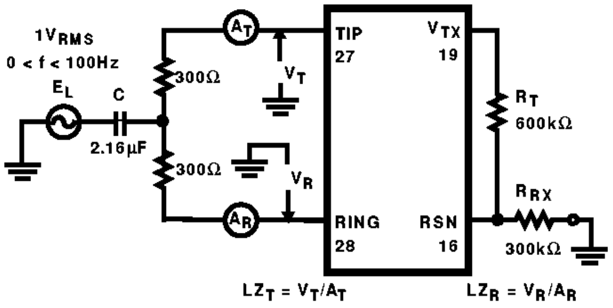


FIGURE 2. LONGITUDINAL IMPEDANCE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LONGITUDINAL CURRENT LIMIT (TIP/RING)					
Off-Hook (Active)	No False Detections, (Loop Current), LB > 45dB (Note 4, Figure 3A)	-	-	20	mA_{PEAK}/Wire
On-Hook (Standby), R_L = ∞	No False Detections (Loop Current) (Note 5, Figure 3B)	-	-	5	mA_{PEAK}/Wire

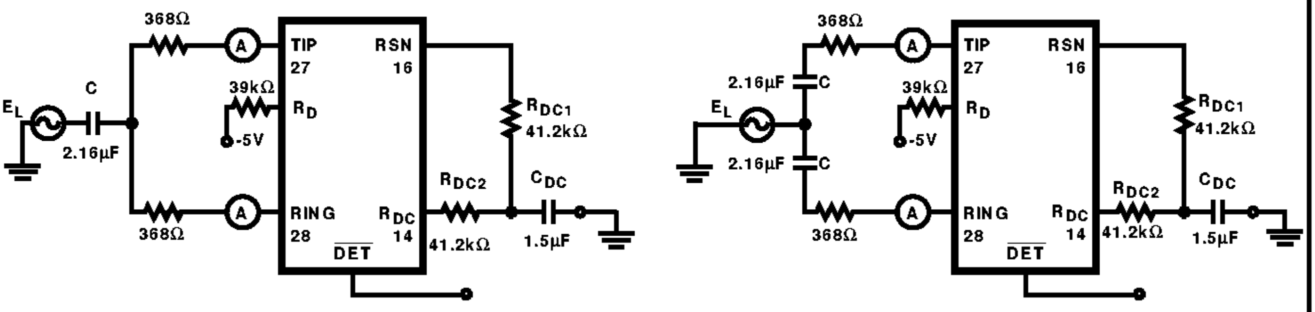


FIGURE 3A. OFF-HOOK

FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, R_{LR}, R_{LT} = 368Ω 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	55	70	-	dB
Longitudinal to Metallic	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	55	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 0.2kHz < f < 1.0kHz	50	55	-	dB
	1.0kHz < f < 4.0kHz (Note 7)	50	55	-	dB
Longitudinal to 4-Wire	0.2kHz < f < 4.0kHz (Note 8, Figure 4)	55	70	-	dB
Metallic to Longitudinal	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 9, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	0.2kHz < f < 4.0kHz (Note 10, Figure 5)	50	55	-	dB

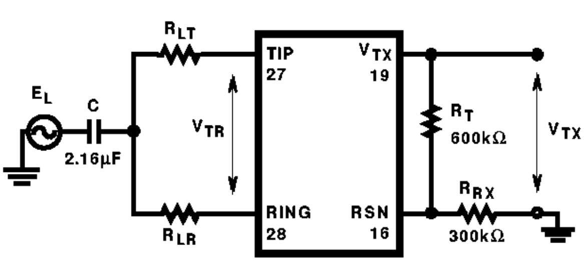


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

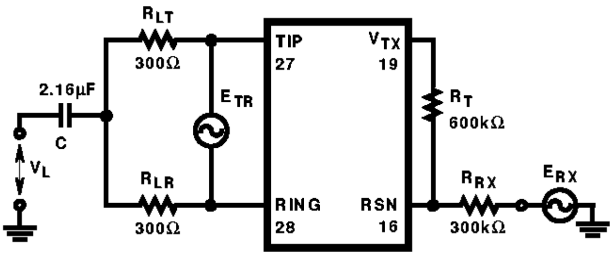


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-Wire Return Loss C_{HP} = 20nF	0.2kHz to 0.5kHz (Note 11, Figure 6)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 11, Figure 6)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 11, Figure 6)	23	-	-	dB

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIP IDLE VOLTAGE					
Active, I_L = 0		-	-4	-	V
Standby, I_L = 0		-	<0	-	V
RING IDLE VOLTAGE					
Active, I_L = 0		-	-24	-	V
Standby, I_L = 0		-	>-28	-	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	(Z_L > 20kΩ, 1% THD) (Note 12, Figure 7)	3.1	-	-	V_{PEAK}
Output Offset Voltage	E_G = 0, Z_L = ∞, (Note 13, Figure 7)	-60	-	60	mV
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz < f < 03.4kHz (Note 14, Figure 7)	0.98	1.0	1.02	V/V

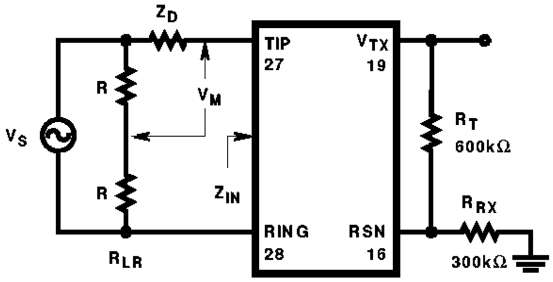


FIGURE 6. TWO-WIRE RETURN LOSS

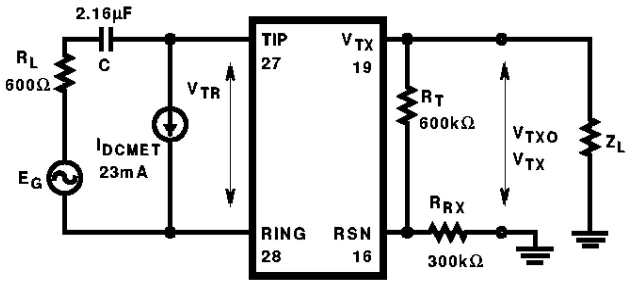


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
4-WIRE RECEIVE PORT (RSN)					
DC Voltage	I_{RSN} = 0mA	-	0	-	V
R_X Sum Node Impedance (Guaranteed by Design)	0.3kHz < f < 3.4kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz < f < 3.4kHz (Note 15, Figure 8)	980	1000	1020	Ratio
FREQUENCY RESPONSE (OFF-HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, E_{RX} = 0V 0.3kHz < f < 3.4kHz (Note 16, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 17, Figure 9)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 18, Figure 9)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 19, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 20, Figure 9)	-0.2	-	0.2	dB
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	-40dBm to +3dBm (Note 21, Figure 9)	-0.1	-	0.1	dB
2-Wire to 4-Wire	-55dBm to -40dBm (Note 21, Figure 9)	-	±0.03	-	dB

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
4-Wire to 2-Wire	-40dBm to +3dBm (Note 22, Figure 9)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 22, Figure 9)	-	±0.03	-	dB

GRX = $((V_{TR1} - V_{TR2})(300k))/(-3)(600)$

Where: V_{TR1} is the Tip to Ring Voltage with V_{RSN} = 0V
and V_{TR2} is the Tip to Ring Voltage with V_{RSN} = -3V

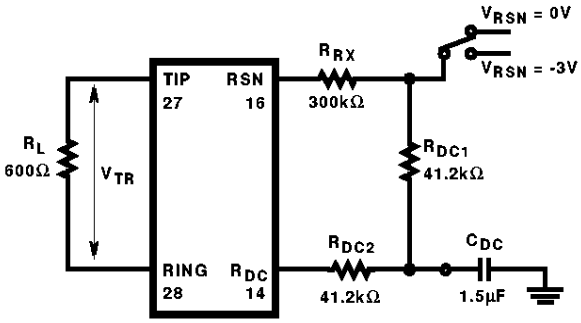


FIGURE 8. CURRENT GAIN-RSN TO METALLIC

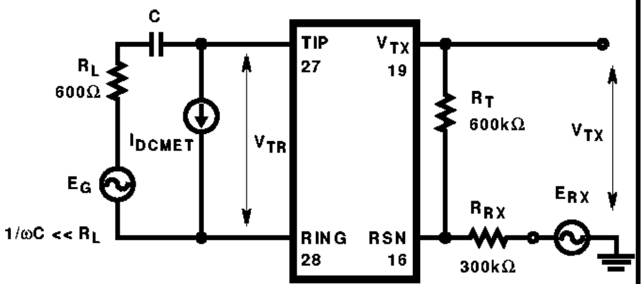


FIGURE 9. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE					
Idle Channel Noise at 2-Wire	C-Message Weighting (Note 23, Figure 10)	-	12	-	dBrnC
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 24, Figure 10)	-	12	-	dBrnC
HARMONIC DISTORTION					
2-Wire to 4-Wire	0dBm, 1kHz (Note 25, Figure 7)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 9)	-	-65	-54	dB
BATTERY FEED CHARACTERISTICS					
Constant Loop Current Tolerance R_{DCX} = 41.2kΩ	$I_L = 2500/(R_{DC1} + R_{DC2})$, -40°C to 85°C (Note 27)	$0.9I_L$	I_L	$1.1I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT}-3)/(R_L + 1800)$, -40°C to 85°C (Note 28)	$0.8I_L$	I_L	$1.2I_L$	mA
Open Circuit Voltage (V_{TIP} - V_{RING})	-40°C to 85°C, (Active)	14	-	20	V
LOOP CURRENT DETECTOR					
On-Hook to Off-Hook	R_D = 39kΩ, -40°C to 85°C	$372/R_D$	$465/R_D$	$558/R_D$	mA
Off-Hook to On-Hook	R_D = 39kΩ, -40°C to 85°C	$325/R_D$	$405/R_D$	$485/R_D$	mA
Loop Current Hysteresis	R_D = 39kΩ, -40°C to 85°C	$25/R_D$	$60/R_D$	$95/R_D$	mA
GROUND KEY DETECTOR					
Tip/Ring Current Difference - Trigger	(Note 29, Figure 11)	8	12	17	mA
Tip/Ring Current Difference - Reset	(Note 29, Figure 11)	3	7	12	mA
Hysteresis	(Note 29, Figure 11)	0	5	9	mA

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

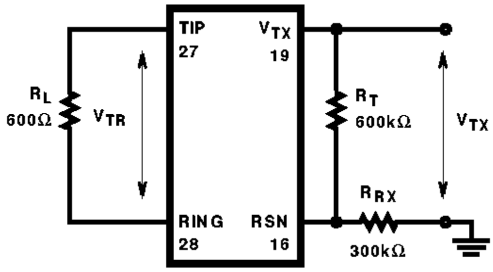


FIGURE 10. IDLE CHANNEL NOISE

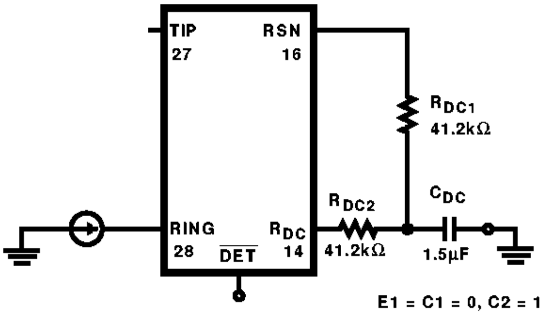


FIGURE 11. GROUND KEY DETECT

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-500	-	500	nA
Input Common-Mode Range	Source Res = 0	V_{BAT} +1	-	0	V
Input Resistance	Source Res = 0, Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	I_{OL} = 25mA	-	1.0	1.5	V
Off-State Leakage Current	V_{OH} = 12V	-	-	10	µA
DIGITAL INPUTS (E0, E1, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL}: C1, C2	V_{IL} = 0.4V	-200	-	-	µA
Input Low Current, I_{IL}: E0, E1	V_{IL} = 0.4V	-100	-	-	µA
Input High Current	V_{IH} = 2.4V	-	-	40	µA
DETECTOR OUTPUT ($\overline{DET}$)					
Output Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.45	V
Output High Voltage, V_{OH}	I_{OH} = 100µA	2.7	-	-	V
Internal Pull-Up Resistor		10	15	20	kΩ
POWER DISSIPATION					
Open Circuit State	C1 = C2 = 0	-	-	23	mW
On-Hook, Standby	C1 = C2 = 1	-	-	30	mW
On-Hook, Active	C1 = 0, C2 = 1, R_L = High Impedance	-	-	150	mW
Off-Hook, Active	R_L = 0Ω	-	-	1.1	W
	R_L = 300Ω	-	-	0.75	W
	R_L = 600Ω	-	-	0.5	W
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	°C

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENTS (V_{BAT} = -28V)					
I_{CC}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	1.5	mA
	Standby State (C1, 2 = 1, 1)	-	-	1.7	mA
	Active State (C1, 2 = 0,1)	-	-	5.5	mA
I_{EE}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.8	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.8	mA
	Active State (C1, 2 = 0, 1)	-	-	2.2	mA
I_{BAT}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.4	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.6	mA
	Active State (C1, 2 = 0, 1)	-	-	3.9	mA
PSRR					
V_{CC} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{EE} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{BAT} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB

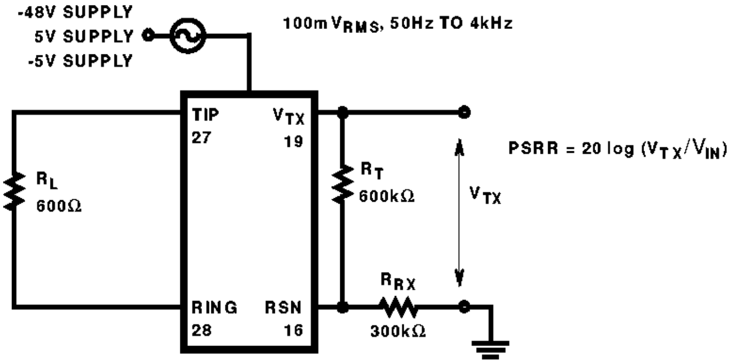


FIGURE 12. POWER SUPPLY REJECTION RATIO

Circuit Operation and Design Information

The HC5513 is a current feed voltage sense **S**ubscriber **L**ine **I**nterface **C**ircuit (SLIC). This means that for short loop applications the SLIC provides a programed constant current to the tip and ring terminals while sensing the tip to ring voltage.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit and design information.

Constant Loop Current (DC) Path

SLIC in the Active Mode

The DC path establishes a constant loop current that flows out of tip and into the ring terminal. The loop current is programmed by resistors R_{DC1}, R_{DC2} and the voltage on the R_{DC} pin (Figure 13). The R_{DC} voltage is determined by the voltage across R_1 in the saturation guard circuit. Under

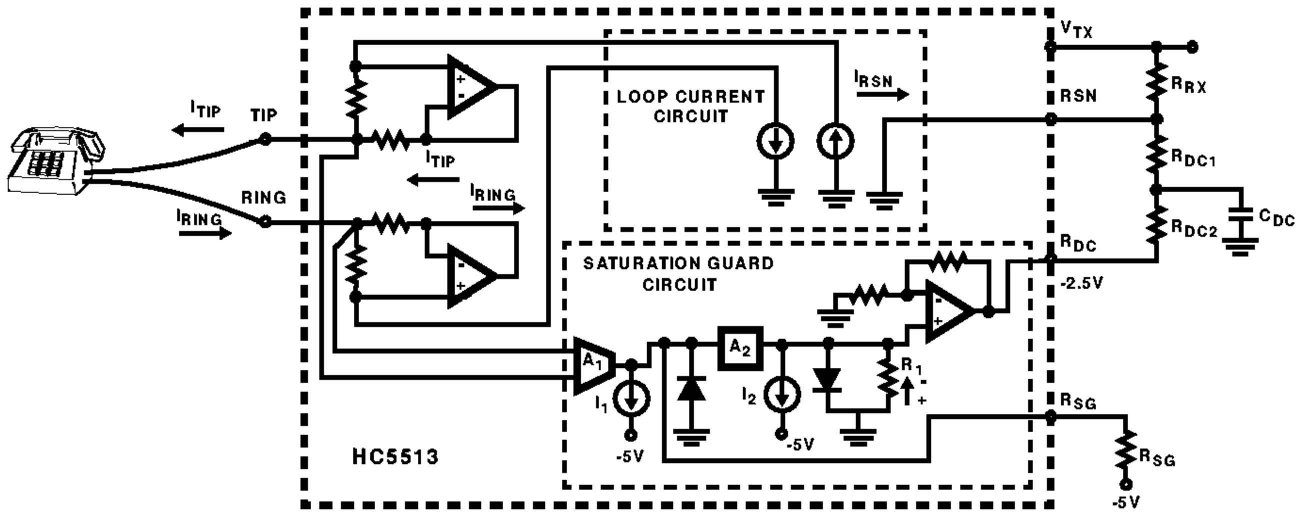


FIGURE 13. DC LOOP CURRENT

constant current feed conditions, the voltage drop across R_1 sets the R_{DC} voltage to -2.5V. This occurs when current flows through R_1 into the current source I_2. The R_{DC} voltage establishes a current (I_{RSN}) that is equal to $V_{RDC}/(R_{DC1}+R_{DC2})$. This current is then multiplied by 1000, in the loop current circuit, to become the tip and ring loop currents.

For the purpose of the following discussion, the saturation guard voltage is defined as the maximum tip to ring voltage at which the SLIC can provide a constant current for a given battery and overhead voltage.

For loop resistances that result in a tip to ring voltage less than the saturation guard voltage the loop current is defined as:

$$I_L = \frac{2.5V}{R_{DC1}+R_{DC2}} \times 1000 \qquad \text{(EQ. 1)}$$

where: I_L = Constant loop current.

R_{DC1} and R_{DC2} = Loop current programming resistors.

Capacitor C_{DC} between R_{DC1} and R_{DC2} removes the VF signals from the battery feed control loop. The value of C_{DC} is determined by Equation 2:

$$C_{DC} = T \times \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right) \qquad \text{(EQ. 2)}$$

where T = 30ms

NOTE: The minimum C_{DC} value is obtained if $R_{DC1} = R_{DC2}$

Figure 14 illustrates the relationship between the tip to ring voltage and the loop resistance. For a 0Ω loop resistance both tip and ring are at $V_{BAT}/2$. As the loop resistance increases, so does the voltage differential between tip and ring. When this differential voltage becomes equal to the saturation guard voltage, the operation of the SLIC's loop feed changes from a constant current feed to a resistive feed. The loop current in the resistive feed region is no longer constant but varies as a function of the loop resistance.

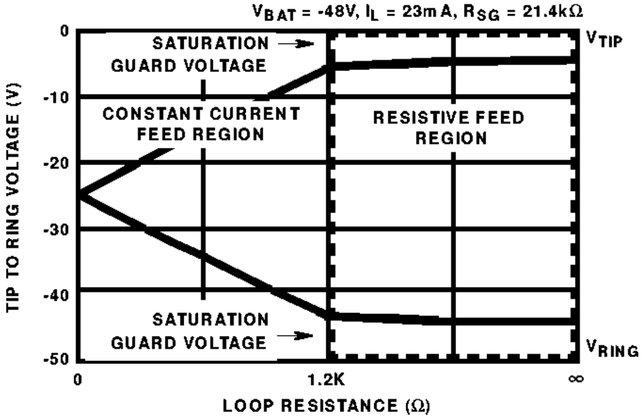
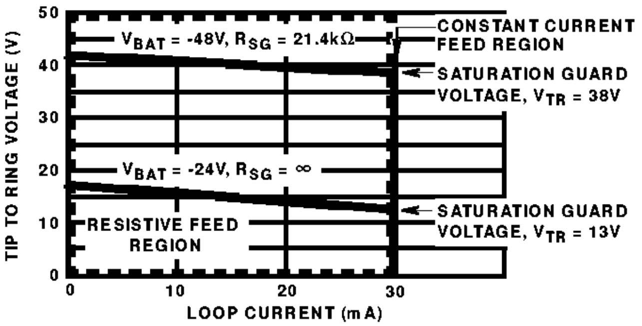


FIGURE 14. V_{TR} vs R_L

Figure 15 shows the relationship between the saturation guard voltage, the loop current and the loop resistance. Notice from Figure 15 that for a loop resistance <1.2kΩ (R_{SG} = 21.4kΩ) the SLIC is operating in the constant current feed region and for resistances >1.2kΩ the SLIC is operating in the resistive feed region. Operation in the resistive feed region allows long loop and off-hook transmission by keeping the tip and ring voltages off the rails. Operation in this region is transparent to the customer.



R_L	100kΩ	4kΩ	2kΩ	<1.2kΩ	R_{RSG} = 21.4kΩ
R_L	100kΩ	1.5kΩ	700Ω	<400Ω	R_{RSG} = ∞Ω

FIGURE 15. V_{TR} vs I_L and R_L

The Saturation Guard circuit (Figure 13) monitors the tip to ring voltage via the transconductance amplifier A_1. A_1 generates a current that is proportional to the tip to ring voltage difference. I_1 is internally set to sink all of A_1's current until the tip to ring voltage exceeds 12.5V. When the tip to ring voltage exceeds 12.5V (with no R_{SG} resistor) A_1 supplies more current than I_1 can sink. When this happens A_2 amplifies its input current by a factor of 12 and the current through R_1 becomes the difference between I_2 and the output current from A_2. As the current from A_2 increases, the voltage across R_1 decreases and the output voltage on R_{DC} decreases. This results in a corresponding decrease in the loop current. The R_{SG} pin provides the ability to increase the saturation guard reference voltage beyond 12.5V. Equation 3 gives the relationship between the R_{SG} resistor value and the programmable saturation guard reference voltage:

$$V_{SGREF} = 12.5 + \frac{5 \bullet 10^5}{R_{SG}} \qquad \text{(EQ. 3)}$$

where:

V_{SGREF} = Saturation Guard reference voltage.

R_{SG} = Saturation Guard programming resistor.

When the Saturation guard reference voltage is exceeded, the tip to ring voltage is calculated using Equation 4:

$$V_{TR} = R_L \times \frac{16.66 + 5 \bullet 10^5 / R_{SG}}{R_L + (R_{DC1} + R_{DC2}) / 600} \qquad \text{(EQ. 4)}$$

where:

V_{TR} = Voltage differential between tip and ring.

R_L = Loop resistance.

For on-hook transmission $R_L = \infty$, Equation 4 reduces to:

$$V_{TR} = 16.66 + \frac{5 \bullet 10^5}{R_{SG}} \qquad \text{(EQ. 5)}$$

The value of R_{SG} should be calculated to allow maximum loop length operation. This requires that the saturation guard reference voltage be set as high as possible without clipping the incoming or outgoing VF signal. A voltage margin of -4V on tip and -4V on ring, for a total of -8V margin, is recommended as a general guideline. The value of R_{SG} is calculated using Equation 6:

$$R_{SG} = \frac{5 \bullet 10^5}{(|V_{BAT}| - V_{MARGIN}) \times \left(1 + \frac{(R_{DC1} + R_{DC2})}{600 R_L}\right) - 16.66V} \qquad \text{(EQ. 6)}$$

where:

V_{BAT} = Battery voltage.

V_{MARGIN} = Recommended value of -8V to allow a maximum overload level of 3.1V peak.

For on-hook transmission $R_L = \infty$, Equation 6 reduces to:

$$R_{SG} = \frac{5 \bullet 10^5}{|V_{BAT}| - V_{MARGIN} - 16.66V} \qquad \text{(EQ. 7)}$$

SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to V_{BAT}. This connection enables a loop current to flow when the phone goes off-hook. The loop current detector then detects this current and the SLIC is configured in the active mode for voice transmission. The loop current in standby state is calculated as follows:

$$I_L \approx \frac{|V_{BAT}| - 3V}{R_L + 1800\Omega} \qquad \text{(EQ. 8)}$$

where:

I_L = Loop current in the standby state.

R_L = Loop resistance.

V_{BAT} = Battery voltage.

(AC) Transmission Path

SLIC in the Active Mode

Figure 16 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_{TR} = V_{TX} + I_M \bullet 2R_F \qquad \text{(EQ. 9)}$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \qquad \text{(EQ. 10)}$$

$$V_{TR} = E_G - I_M \bullet Z_L \qquad \text{(EQ. 11)}$$

where:

V_{TR} = Is the AC metallic voltage between tip and ring, including the voltage drop across the fuse resistors R_F.

V_{TX} = Is the AC metallic voltage. Either at the ground referenced 4-wire side or the SLIC tip and ring terminals.

I_M = Is the AC metallic current.

R_F = Is a fuse resistor.

Z_T = Is used to set the SLIC's 2-wire impedance.

V_{RX} = Is the analog ground referenced receive signal.

Z_{RX} = Is used to set the 4-wire to 2-wire gain.

E_G = Is the AC open circuit voltage.

Z_L = Is the line impedance.

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors, and is calculated as follows:

Let $V_{RX} = 0$. Then from Equation 10

$$V_{TX} = Z_T \bullet \frac{I_M}{1000} \qquad \text{(EQ. 12)}$$

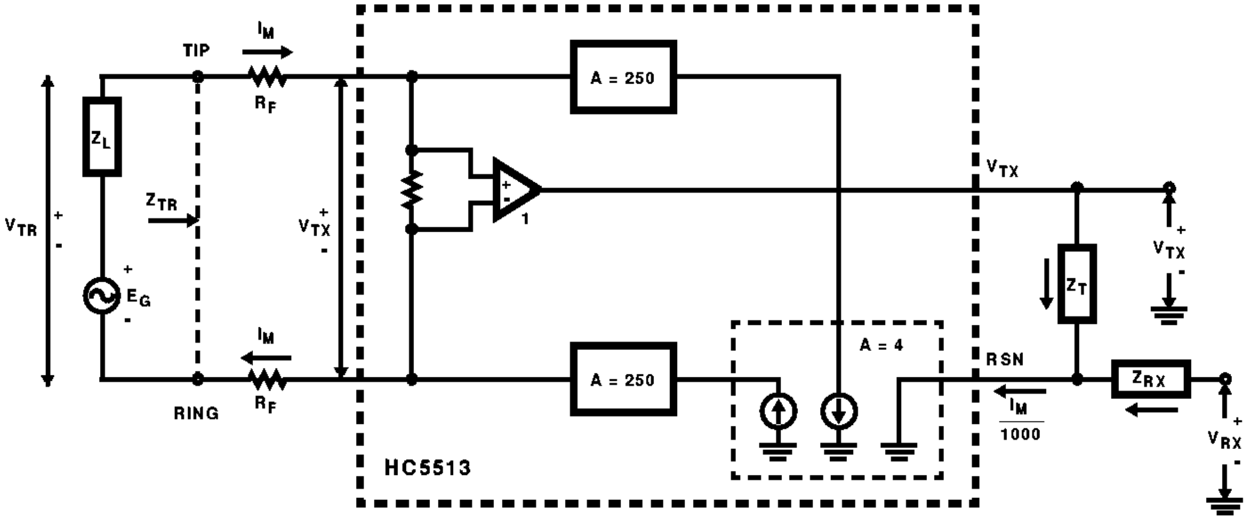


FIGURE 16. SIMPLIFIED AC TRANSMISSION CIRCUIT

Z_{TR} is defined as:

$$Z_{TR} = \frac{V_{TR}}{I_M} \qquad \text{(EQ. 13)}$$

Substituting in Equation 9 for V_{TR}

$$Z_{TR} = \frac{V_{TX}}{I_M} + \frac{2R_F \bullet I_M}{I_M} \qquad \text{(EQ. 14)}$$

Substituting in Equation 12 for V_{TX}

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F \qquad \text{(EQ. 15)}$$

Therefore

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F) \qquad \text{(EQ. 16)}$$

Equation 16 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

EXAMPLE:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_F = 20\Omega$.

$$Z_T = 1000 \bullet \left(600 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 20\right)$$

$Z_T = 560\text{k}\Omega$ in series with 2.16nF

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/V_{TR}

From Equations 9 and 10 with $V_{RX} = 0$

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F} \qquad \text{(EQ. 17)}$$

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{\frac{Z_T}{1000} + 2R_F + Z_L} \qquad \text{(EQ. 18)}$$

For applications where the 2-wire impedance (Z_{TR}, Equation 15) is chosen to equal the line impedance (Z_L), the expression for $A_{4\text{-}2}$ simplifies to:

$$A_{4-2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2} \qquad \text{(EQ. 19)}$$

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{\frac{Z_T}{1000} + 2R_F + Z_L} \qquad \text{(EQ. 20)}$$

Transhybrid Circuit

The purpose of the transhybrid circuit is to remove the receive signal (V_{RX}) from the transmit signal (V_{TX}), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (RSN) to the 4-wire transmit port (V_{TX}). Figure 17 shows the transhybrid circuit. The input signal will be subtracted from the output signal if I_1 equals I_2. Node analysis yields the following equation:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \qquad \text{(EQ. 21)}$$

The value of Z_B is then

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} \qquad \text{(EQ. 22)}$$

Where V_{RX}/V_{TX} equals $1/A_{4\text{-}4}$

Therefore

$$Z_B = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{\frac{Z_T}{1000} + 2R_F + Z_L}{Z_L + 2R_F} \qquad \text{(EQ. 23)}$$

Example:

Given: R_{TX} = 20kΩ, Z_{RX} = 280kΩ, Z_T = 562kΩ (standard value), R_F = 20Ω and Z_L = 600Ω

The value of Z_B = 18.7kΩ

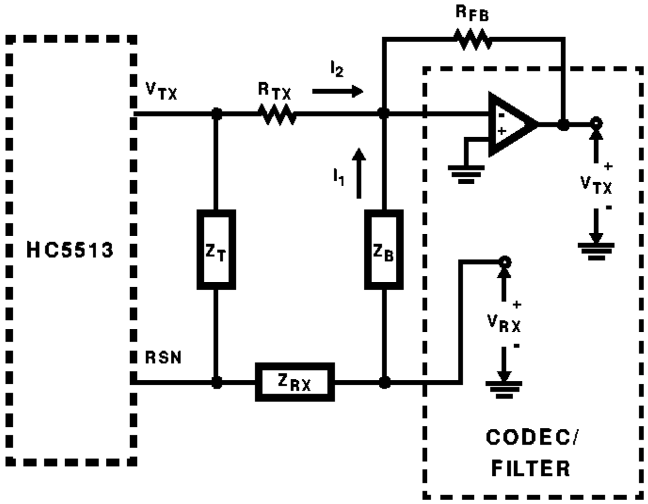


FIGURE 17. TRANSHYBRID CIRCUIT

Supervisory Functions

The loop current, ground key and the ring trip detector outputs are multiplexed to a single logic output pin called $\overline{\text{DET}}$. See Table 1 to determine the active detector for a given logic input. For further discussion of the logic circuitry see section titled “Digital Logic Inputs”.

Before proceeding with an explanation of the loop current detector, ground key detector and later the longitudinal impedance, it is important to understand the difference between a “metallic” and “longitudinal” loop currents. Figure 18 illustrates 3 different types of loop current encountered.

Case 1 illustrates the metallic loop current. The definition of a metallic loop current is when **equal** currents flow out of tip and into ring. Loop current is a metallic current.

Cases 2 and 3 illustrate the longitudinal loop current. The definition of a longitudinal loop current is a common mode current, that flows either out of or into tip and ring simultaneously. Longitudinal currents in the on-hook state result in **equal** currents flowing through the sense resistors R_1 and R_2 (Figure 18). And longitudinal currents in the off-hook state result in **unequal** currents flowing through the sense resistors R_1 and R_2. Notice that for case 2, longitudinal currents flowing away from the SLIC, the current through R_1 is the metallic loop current plus the longitudinal current; whereas the current through R_2 is the metallic loop current minus the longitudinal current. Longitudinal currents are generated when the phone line is influenced by magnetic fields (e.g. power lines).

Loop Current Detector

Figure 18 shows a simplified schematic of the loop current and ground key detectors. The loop current detector works by sensing the metallic current flowing through resistors R_1 and R_2. This results in a current (I_{RD}) out of the transconductance amplifier (gm_1) that is equal to the product of gm_1 and the metallic loop current. I_{RD} then flows out the R_D pin and through resistor R_D to V_{EE}. The value of I_{RD} is equal to:

$$I_{RD} = \frac{|I_{TIP} - I_{RING}|}{600} = \frac{I_L}{300} \qquad \text{(EQ. 24)}$$

The I_{RD} current results in a voltage drop across R_D that is compared to an internal 1.25V reference voltage. When the voltage drop across R_D exceeds 1.25V, and the logic is configured for loop current detection, the $\overline{\text{DET}}$ pin goes low.

The hysteresis resistor R_H adds an additional voltage effectively across R_D, causing the on-hook to off-hook threshold to be slightly higher than the off-hook to on-hook threshold.

Taking into account the hysteresis voltage, the typical value of R_D for the on-hook to off-hook condition is:

$$R_D = \frac{465}{I_{ON-HOOK\ to\ OFF-HOOK}} \qquad \text{(EQ. 25)}$$

Taking into account the hysteresis voltage, the typical value of R_D for the off-hook to on-hook condition is:

$$R_D = \frac{375}{I_{OFF-HOOK\ to\ ON-HOOK}} \qquad \text{(EQ. 26)}$$

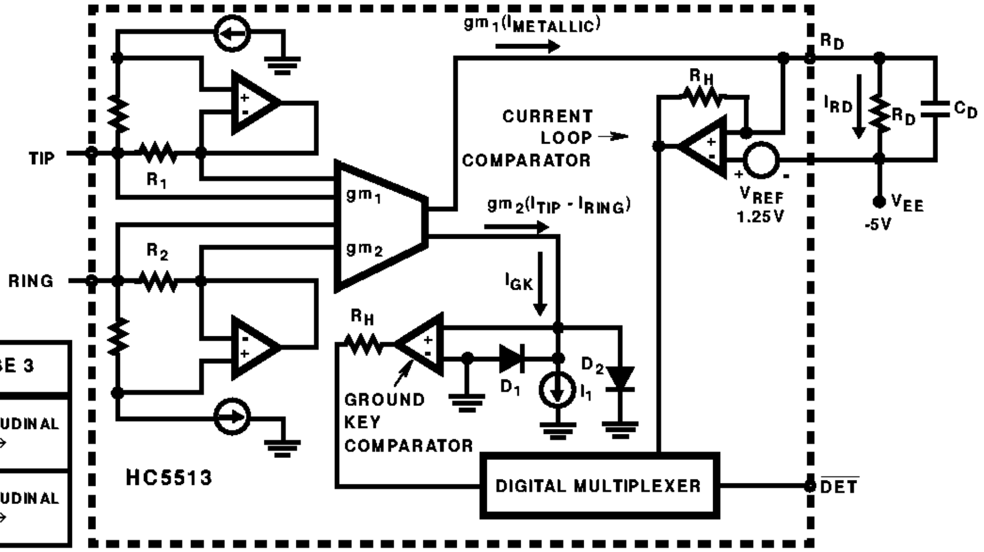
A filter capacitor (C_D) in parallel with R_D will improve the accuracy of the trip point in a noisy environment. The value of this capacitor is calculated using the following Equation:

$$C_D = \frac{T}{R_D} \qquad \text{(EQ. 27)}$$

where: T = 0.5ms

Ground Key Detector

A simplified schematic of the ground key detector is shown in Figure 18. Ground key, is the process in which the ring terminal is shorted to ground for the purpose of signaling an Operator or seizing a phone line (between the Central Office and a Private Branch Exchange). The Ground Key detector is activated when unequal current flow through resistors R_1 and R_2. This results in a current (I_{GK}) out of the transconductance amplifier (gm_2) that is equal to the product of gm_2 and the differential (I_{TIP} -I_{RING}) loop current. If I_{GK} is less than the internal current source (I_1), then diode D_1 is on and the output of the ground key comparator is low. If I_{GK} is greater than the internal current source (I_1), then diode D_2 is on and the output of the ground key comparator is high. With the output of the ground key comparator high, and the logic configured for ground key detect, the $\overline{\text{DET}}$ pin goes low. The ground key detector has a built in hysteresis of typically 5mA between its trigger and reset values.



CASE 1	CASE 2	CASE 3
$I_{METALLIC}$ ←	$I_{LONGITUDINAL}$ ←	$I_{LONGITUDINAL}$ →
$I_{METALLIC}$ →	$I_{LONGITUDINAL}$ ←	$I_{LONGITUDINAL}$ →

FIGURE 18. LOOP CURRENT AND GROUND KEY DETECTORS

Ring Trip Detector

Ring trip detection is accomplished with the internal ring trip comparator and the external circuitry shown in Figure 19. The process of ring trip is initiated when the logic input pins are in the following states: E0 = 0, E1 = 1/0, C1 = 1 and C2 = 0. This logic condition connects the ring trip comparator to the $\overline{DET}$ output, and causes the Ringrly pin to energize the ring relay. The ring relay connects the tip and ring of the phone to the external circuitry in Figure 19. When the phone is on-hook the DT pin is more positive than the DR pin and the $\overline{DET}$ output is high. For off-hook conditions DR is more positive than DT and $\overline{DET}$ goes low. When $\overline{DET}$ goes low, indicating that the phone has gone off-hook, the SLIC is commanded by the logic inputs to go into the active state. In the active state, tip and ring are once again connected to the phone and normal operation ensues.

Figure 19 illustrates battery backed unbalanced ring injected ringing. For tip injected ringing just reverse the leads to the phone. The ringing source could also be balanced.

NOTE: The $\overline{DET}$ output will toggle at 20Hz because the DT input is not completely filtered by C_{RT}. Software can examine the duty cycle and determine if the $\overline{DET}$ pin is low for more that half the time, if so the off-hook condition is indicated.

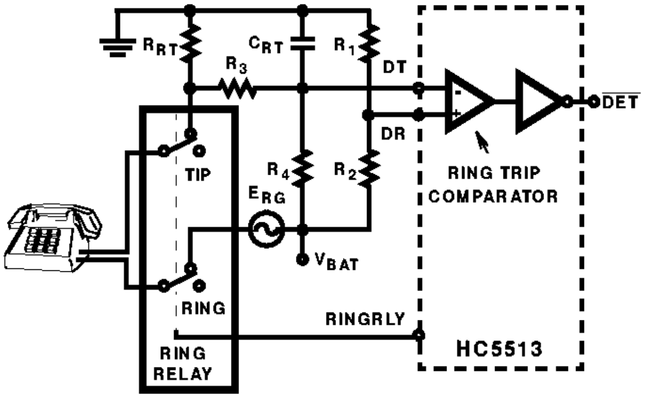


FIGURE 19. RING TRIP CIRCUIT FOR BATTERY BACKED RINGING

Longitudinal Impedance

The feedback loop described in Figure 20(A, B) realizes the desired longitudinal impedances from tip to ground and from ring to ground. Nominal longitudinal impedance is resistive and in the order of 22Ω.

In the presence of longitudinal currents this circuit attenuates the voltages that would otherwise appear at the tip and ring terminals, to levels well within the common mode range of the SLIC. In fact, longitudinal currents may exceed the programmed DC loop current without disturbing the SLIC's VF transmission capabilities.

The function of this circuit is to maintain the tip and ring voltages symmetrically around $V_{BAT}/2$, in the presence of longitudinal currents. The differential transconductance amplifiers G_T and G_R accomplish this by sourcing or sinking the required current to maintain V_C at $V_{BAT}/2$.

When a longitudinal current is injected onto the tip and ring inputs, the voltage at V_C moves from it's equilibrium value $V_{BAT}/2$. When V_C changes by the amount ΔV_C, this change appears between the input terminals of the differential transconductance amplifiers G_T and G_R. The output of G_T and G_R are the differential currents ΔI_1 and ΔI_2, which in turn feed the differential inputs of current sources I_T and I_R respectively. I_T and I_R have current gains of 250 single ended and 500 differentially, thus leading to a change in I_T and I_R that is equal to $500(\Delta_I)$ and $500(\Delta I_2)$.

The circuit shown in Figure 20(B) illustrates the tip side of the longitudinal network. The advantages of a differential input current source are: improved noise since the noise due to current source $2I_O$ is now correlated, power savings due to differential current gain and minimized offset error at the Operational Amplifier inputs via the two 5kΩ resistors.

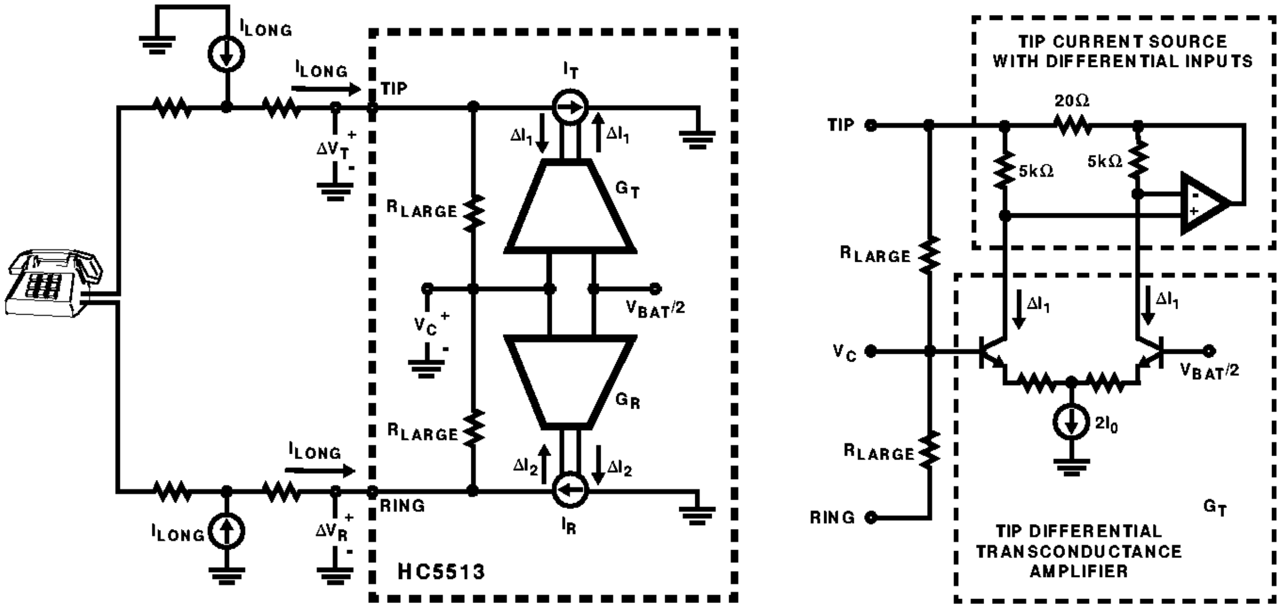


FIGURE 20A. FIGURE 20B.

FIGURE 20. LONGITUDINAL IMPEDANCE NETWORK

Digital Logic Inputs

Table 1 is the logic truth table for the TTL compatible logic input pins. The HC5513 has two enable inputs pins (E0, E1) and two control inputs pins (C1, C2).

The enable pin E0 is used to enable or disable the $\overline{\text{DET}}$ output pin. The $\overline{\text{DET}}$ pin is enabled if E0 is at a logic level 0 and disabled if E0 is at a logic level 1.

The enable pin E1 gates the ground key detector to the $\overline{\text{DET}}$ output with a logic level 0, and gates the loop or ring trip detector to the $\overline{\text{DET}}$ output with a logic level 1.

A combination of the control pins C1 and C2 is used to select 1 of the 4 possible operating states. A description of each operating state and the control logic follow:

Open Circuit State (C1 = 0, C2 = 0)

In this state the SLIC is effectively off. All detectors and both the tip and ring line drive amplifiers are powered down, presenting a high impedance to the line. Power dissipation is at a minimum.

Active State (C1 = 0, C2 = 1)

The tip output is capable of sourcing loop current and for open circuit conditions is about -4V from ground. The ring output is capable of sinking loop current and for open circuit conditions is about V_{BAT} + 4V. VF signal transmission is normal. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{\text{DET}}$ output.

Ringing State (C1 = 1, C2 = 0)

The ring relay driver and the ring trip detector are activated. Both the tip and ring line drive amplifiers are powered down. Both tip and ring are disconnected from the line via the external ring relay.

Standby State (C1 = 1, C2 = 1)

Both the tip and ring line drive amplifiers are powered down. Internal resistors are connected between tip to ground and ring to V_{BAT} to allow loop current detect in an off-hook condition. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{\text{DET}}$ output.

AC Transmission Circuit Stability

To ensure stability of the AC transmission feedback loop two compensation capacitors C_{TC} and C_{RC} are required. Figure 21 (Application Circuit) illustrates their use. Recommended value is 2200pF.

AC-DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between pins HPT and HPR provides the separation between circuits sensing tip to ring DC conditions and circuits processing AC signals. A 10nf C_{HP} will position the low end frequency response 3dB break point at 48Hz. Where:

$$f_{3dB} = \frac{1}{(2 \bullet \pi \bullet R_{HP} \bullet C_{HP})} \qquad \text{(EQ. 28)}$$

where R_{HP} = 330kΩ

SLIC Operating States

TABLE 1. LOGIC TRUTH TABLE

E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	$\overline{\text{DET}}$ OUTPUT
0	0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	0	1	Active	Ground Key Detector	Ground Key Status
0	0	1	0	Ringing	No Active Detector	Logic Level High
0	0	1	1	Standby	Ground Key Detector	Ground Key Status
0	1	0	0	Open Circuit	No Active Detector	Logic Level High
0	1	0	1	Active	Loop Current Detector	Loop Current Status
0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	1	Standby	Loop Current Detector	Loop Current Status
1	0	0	0	Open Circuit	No Active Detector	Logic Level High
1	0	0	1	Active	Ground Key Detector	
1	0	1	0	Ringing	No Active Detector	
1	0	1	1	Standby	Ground Key Detector	
1	1	0	0	Open Circuit	No Active Detector	
1	1	0	1	Active	Loop Current Detector	
1	1	1	0	Ringing	Ring Trip Detector	
1	1	1	1	Standby	Loop Current Detector	

Thermal Shutdown Protection

The HC5513's thermal shutdown protection is invoked if a fault condition on the tip or ring causes the temperature of the die to exceed 160°C. If this happens, the SLIC goes into a high impedance state and will remain there until the temperature of the die cools down by about 20°C. The SLIC will return back to its normal operating mode, providing the fault condition has been removed.

Surge Voltage Protection

The HC5513 must be protected against surge voltages and power crosses. Refer to "Maximum Ratings" TIPX and RINGX terminals for maximum allowable transient tip and ring voltages. The protection circuit shown in Figure 20 utilizes diodes together with a clamping device to protect tip and ring against high voltage transients.

Positive transients on tip or ring are clamped to within a couple of volts above ground via diodes D_1 and D_2. Under normal operating conditions D_1 and D_2 are reverse biased and out of the circuit.

Negative transients on tip and ring are clamped to within a couple of volts below ground via diodes D_3 and D_4 with the help of a Surgector. The Surgector is required to block conduction through diodes D_3 and D_4 under normal operating conditions and allows negative surges to be returned to system ground.

In applications where only low energy transients (<300V) are possible, diodes D_3 and D_4 could be connected to V_{BAT}, eliminating the requirement of the Surgector. Caution should be used with this application. Be aware that: surge protection is for low level transients only and will subject the batteries to negative voltage surges.

The fuse resistors (R_F) serve a dual purpose of being non-destructive power dissipaters during surge and fuses when the line in exposed to a power cross.

Power-Up Sequence

The HC5513 has **no** required power-up sequence. This is a result of the **D**ielectrically **I**solated (DI) process used in the fabrication of the part. By using the DI process, care is no longer required to insure that the substrate be kept at the most negative potential as with junction isolated ICs.

Printed Circuit Board Layout

Care in the printed circuit board layout is essential for proper operation. All connections to the RSN pin should be made as close to the device pin as possible, to limit the interference that might be injected into the RSN terminal. It is good practice to surround the RSN pin with a ground plane.

The analog and digital grounds should be tied together at the device.

NOTES:

2. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). I_{DCMET} = 23mA, increase the amplitude of E_{RX} until 1% THD is measured at V_{TRO}. Reference Figure 1.

3. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.

   (TIP) $L_{ZT} = V_T/A_T$

   (RING) $L_{ZR} = V_R/A_R$

   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)

4. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook (Active, $C_1 = 1$, $C_2 = 0$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3A) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains low (no false detection).

5. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook (Active, $C_1 = 1$, $C_2 = 1$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3B) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).

6. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:

   BLME = 20 • log (E_L/V_{TR}), where: E_L and V_{TR} are defined in Figure 4.

7. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.

8. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:

   BLFE = 20 • log (E_L/V_{TX}),: E_L and V_{TX} are defined in Figure 4.

9. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:

   BMLE = 20 • log (E_{TR}/V_L), $E_{RX} = 0$

   where: E_{TR}, V_L and E_{RX} are defined in Figure 5.

10. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:

    BFLE = 20 • log (E_{RX}/V_L), E_{TR} = source is removed.

    where: E_{RX}, V_L and E_{TR} are defined in Figure 5.

11. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:

    r = -20 • log ($2V_M/V_S$)

    where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).

12. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TXO}) with the signal source (E_G) at the 2-wire port, I_{DCMET} = 23mA, Z_L = 20kΩ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TXO}. Note that the gain from the 2-wire port to the 4-wire port is equal to 1.

13. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: $E_G = 0$, I_{DCMET} = 23mA, $Z_L = \infty$ and is measured at V_{TX}. E_G, I_{DCMET}, V_{TX} and Z_L are defined in Figure 7. Note: I_{DCMET} is established with a series 600Ω resistor between tip and ring.

14. **Two-Wire to Four-Wire (Metallic to V_{TX}) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.

    $G_{2\text{-}4} = (V_{TX}/V_{TR})$, E_G = 0dBm0, V_{TX}, V_{TR}, and E_G are defined in Figure 7.

15. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation:

    $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K, I_M, R_{DC1}, R_{DC2}, V_{RDC} and V_{RSN} are defined in Figure 8.

16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    $F_{2\text{-}4}$ = 20 • log (V_{TX}/V_{TR}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, and E_G are defined in Figure 9.

17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    $F_{4\text{-}2}$ = 20 • log (V_{TR}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR} and E_{RX} are defined in Figure 9.

18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    $F_{4\text{-}4}$ = 20 • log (V_{TX}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX} and E_{RX} are defined in Figure 9.

19. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{2\text{-}4}$ = 20 • log (V_{TX}/V_{TR})

    where: V_{TX}, V_{TR}, and E_G are defined in Figure 9. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for $R_F = 0$).

20. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{4\text{-}2}$ = 20 • log (V_{TR}/E_{RX})

    where: V_{TR} and E_{RX} are defined in Figure 9.

21. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

    $G_{2\text{-}4}$ = 20 • log (V_{TX}/V_{TR}) vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX} and V_{TR} are defined in Figure 9.

22. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $G_{4\text{-}2}$ = 20 • log (V_{TR}/E_{RX}) vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TR} and E_{RX} are defined in Figure 9. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

23. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 10).

24. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port is grounded (Reference Figure 10).

25. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = 0dBm at 1kHz, I_{DCMET} = 23mA. Measurement taken at V_{TX}. (Reference Figure 7).

26. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, I_{DCMET} = 23mA. Measurement taken at V_{TR}. (Reference Figure 9).

27. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 2500 / (R_{DC1} + R_{DC2})$

28. **Standby State Loop Current** - The standby state loop current is calculated using the following equation:

    $I_L = [|V_{BAT}| - 3] / [R_L + 1800]$, $T_A = 25^oC$

29. **Ground Key Detector** - (TRIGGER) Increase the input current to 8mA and verify that $\overline{DET}$ goes low.

    (RESET) Decrease the input current from 17mA to 3mA and verify that $\overline{DET}$ goes high.

    (Hysteresis) Compare difference between trigger and reset.

30. **Power Supply Rejection Ratio** - Inject a 100mV_{RMS} signal (50Hz to 4kHz) on V_{BAT}, V_{CC} and V_{EE} supplies. PSRR is computed using the following equation:

    PSRR = 20 • log (V_{TX}/V_{IN}). V_{TX} and V_{IN} are defined in Figure 12.

Pin Descriptions

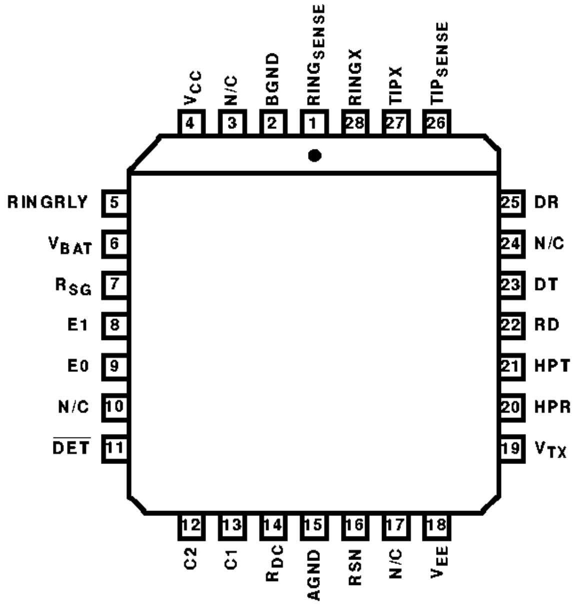
PLCC	PDIP	SYMBOL	DESCRIPTION
1		$RING_{SENSE}$	Internally connected to output of RING power amplifier.
2	7	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
4	8	V_{CC}	5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage, -24V to -56V.
7	11	R_{SG}	Saturation guard programming resistor pin.
8	12	E1	TTL compatible logic input. The logic state of E1 in conjunction with the logic state of C1 determines which detector is gated to the $\overline{DET}$ output.
9	13	E0	TTL compatible logic input. Enables the $\overline{DET}$ output when set to logic level zero and disables $\overline{DET}$ output when set to a logic level one.
11	14	$\overline{DET}$	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see Truth Table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{DET}$ output is an open collector with an internal pull-up of approximately 15kΩ to V_{CC}.
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	R_{DC}	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between tip and ring. The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic voltage. The network for programming the 2-wire input impedance connects between this pin and RSN.

Pin Descriptions (Continued)

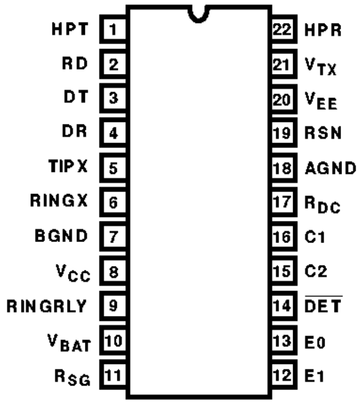
PLCC	PDIP	SYMBOL	DESCRIPTION
20	22	HPR	RING side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the ring AC current from the DC loop current. The other end of C_{HP} is connected to HPT.
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the tip AC current from the DC loop current. The other end of C_{HP} is connected to HPR.
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_D is also connected between this pin and V_{EE}.
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
26		TIP_{SENSE}	Internally connected to output of tip power amplifier.
27	5	TIPX	Output of tip power amplifier.
28	6	RINGX	Output of ring power amplifier.
3, 10 17, 24		N/C	No internal connection.

Pinouts

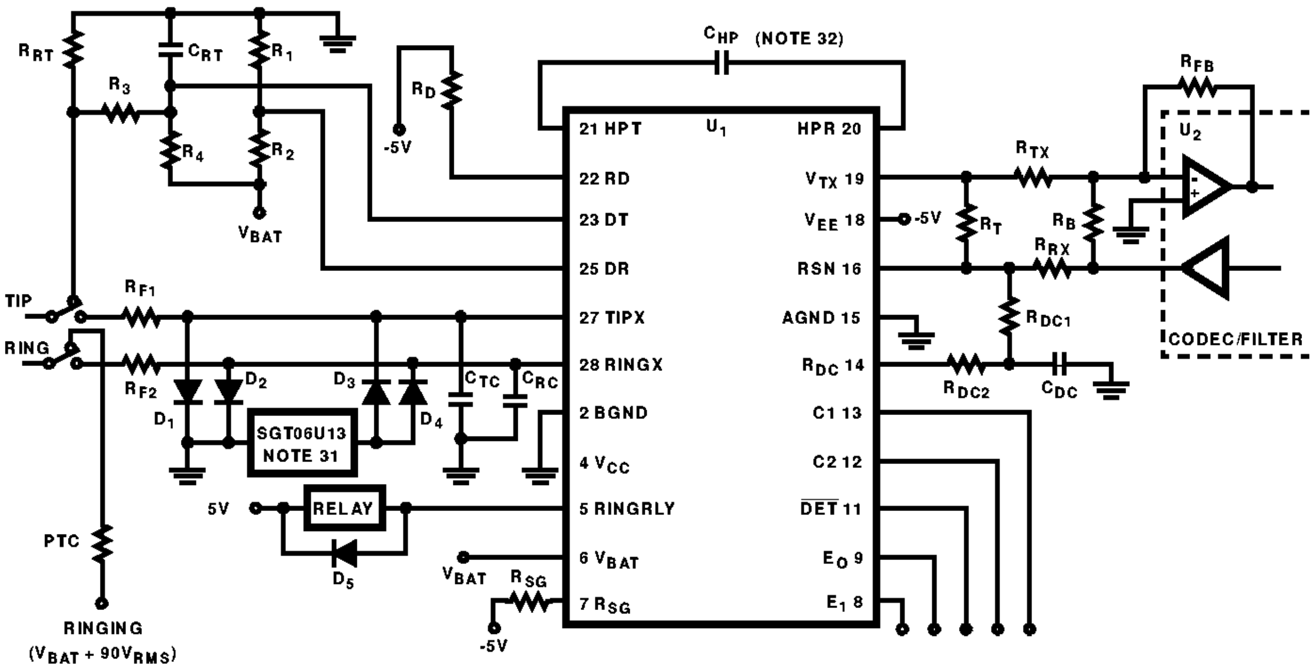
HC5513
(PLCC)
TOP VIEW



HC5513
(PDIP)
TOP VIEW



Application Circuit



U1	SLIC (Subscriber Line Interface Circuit) HC5513
U2	Combination CODEC/Filter e.g. CD22354A or Programmable CODEC/ Filter, e.g. SLAC
C_{DC}	1.5µF, 20%, 10V
C_{HP}	10nF, 20%, 100V (Note 2)
C_{RT}	0.39µF, 20%, 100V
C_{TC}, C_{RC}	2200pF, 20%, 100V
Relay	Relay, 2C Contacts, 5V Coil
D_1 - D_4	Diode, 100V, 3A
Surgector	SGT06U13
D_5	Diode, 1N4454

R_{F1}, R_{F2}	Line Resistor, 20Ω, 1% Match
R_1, R_3	200kΩ, 5%, 1/4W
R_2	910kΩ, 5%, 1/4W
R_4	1.2MΩ, 5%, 1/4W
R_B	18.7kΩ,1%, 1/4W
R_D	39kΩ, 5%, 1/4W
R_{DC1}, R_{DC2}	41.2kΩ, 5%, 1/4W
R_{FB}	20.0kΩ, 1%, 1/4W
R_{RX}	280kΩ, 1%, 1/4W
R_T	562kΩ, 1%, 1/4W
R_{TX}	20kΩ, 1%, 1/4W
R_{RT}	150Ω, 5%, 2W
R_{SG}	V_{BAT} = -28V, $R_{SG} = \infty$ V_{BAT} = -48V, R_{SG} = 21.4kΩ, 1/4W 5%

NOTES:

31. The anodes of D_3 and D_4 may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D_3 and D_4 be shorted to ground through a transzorb or surgector.
32. To meet the specified 25dB 2-wire return loss at 200Hz, C_{HP} needs to be 20nF, 20%, 100V.

FIGURE 21. APPLICATION CIRCUIT