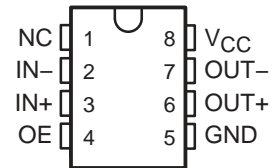


# TL712 DIFFERENTIAL COMPARATOR

SLCS002D – JUNE 1983 – REVISED AUGUST 2003

- Operates From a Single 5-V Supply
- 0-V to 5.5-V Common-Mode Input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- Enable Capability
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

D, P, PS, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

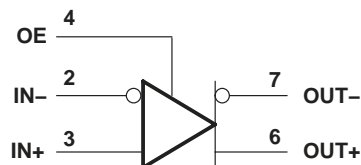
The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable (OE) is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL712CP	TL712CP
	SOIC (D)	Tube of 75	TL712CD	TL712C
		Reel of 2500	TL712CDR	
	SOP (PS)	Reel of 2000	TL712CPSR	T712
	TSSOP (PW)	Tube of 150	TL712CPW	T712
		Reel of 2000	TL712CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## symbol (positive logic)



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 **TEXAS  
INSTRUMENTS**

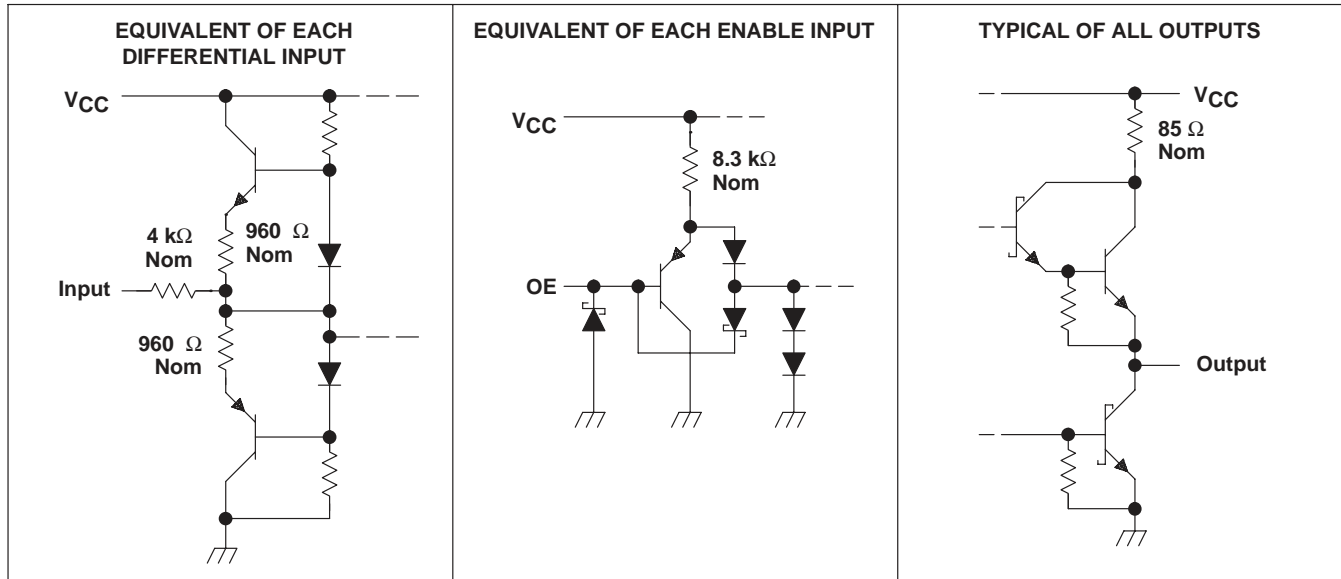
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# TL712 DIFFERENTIAL COMPARATOR

SLCS002D – JUNE 1983 – REVISED AUGUST 2003

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 25$ V
Input voltage, $V_I$ , any differential input	$\pm 25$ V
Output enable voltage	7 V
Low-level output current, $I_{OL}$	50 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4):	
D package	97°C/W
P package	85°C/W
PS package	95°C/W
PW package	149°C/W
Operating virtual junction temperature, $T_J$	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground.
  2. Differential voltage values are at  $IN+$  with respect to  $IN-$ .
  3. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  4. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
V <sub>CC</sub> Supply voltage	4.75	5	5.25	V
V <sub>IC</sub> Common-mode input voltage	0		5.5	V
I <sub>OH</sub> High-level output current			-1	mA
I <sub>OL</sub> Low-level output current			16	mA
T <sub>A</sub> Operating free-air temperature	0		70	°C

**electrical characteristics at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>T</sub> Threshold voltage (V <sub>T+</sub> and V <sub>T-</sub> )	V <sub>ICR</sub> = 0 to 5 V	-100 <sup>†</sup>		100	mV
V <sub>hys</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )			5		mV
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, I <sub>OH</sub> = -1 mA	2.7	3.5		V
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 16 mA		0.4	0.5	V
I <sub>OZ</sub> Off-state output current	V <sub>O</sub> = 2.4 V			-20	μA
I <sub>I</sub> Enable current	V <sub>I</sub> = 5.5 V			100	μA
I <sub>IH</sub> High-level enable current	V <sub>IH</sub> = 2.7 V			20	μA
I <sub>IL</sub> Low-level enable current	V <sub>IL</sub> = 0.4 V			-360	μA
r <sub>i</sub> Differential input resistance		4			kΩ
r <sub>o</sub> Output resistance				100	Ω
I <sub>OS</sub> Short-circuit output current		-15		-85	mA
I <sub>CC</sub> Supply current	V <sub>ID</sub> = 0, No load		17	20	mA

<sup>†</sup> The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

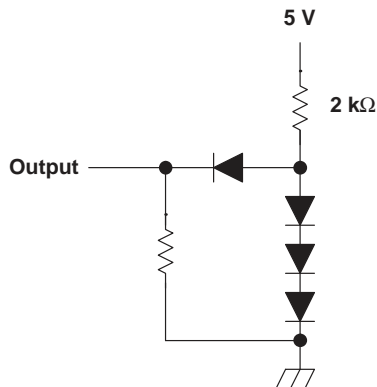
PARAMETER	TEST CONDITIONS	TYP	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	TTL load, See Note 5 and Figure 1	25	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		25	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total) and is the interval between the input step function and the instant when the output crosses 2.5 V.

# TL712 DIFFERENTIAL COMPARATOR

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## PARAMETER MEASUREMENT INFORMATION



NOTE A: All diodes are 1N4148 or equivalent.

Figure 1. TTL Output Load Circuit

## TYPICAL CHARACTERISTICS

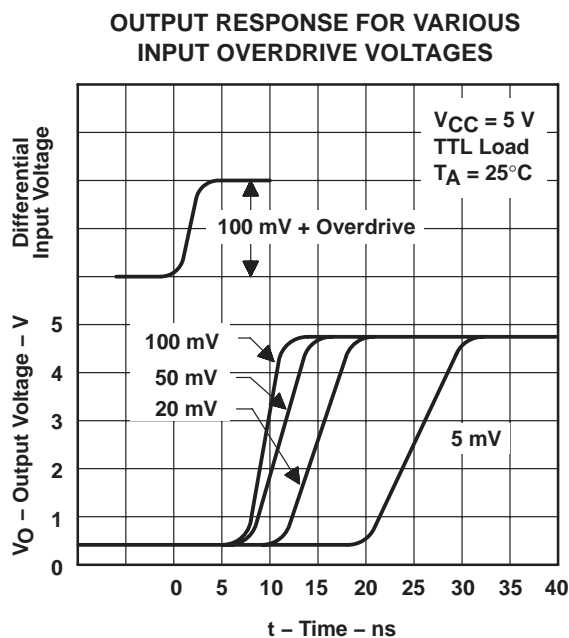


Figure 2

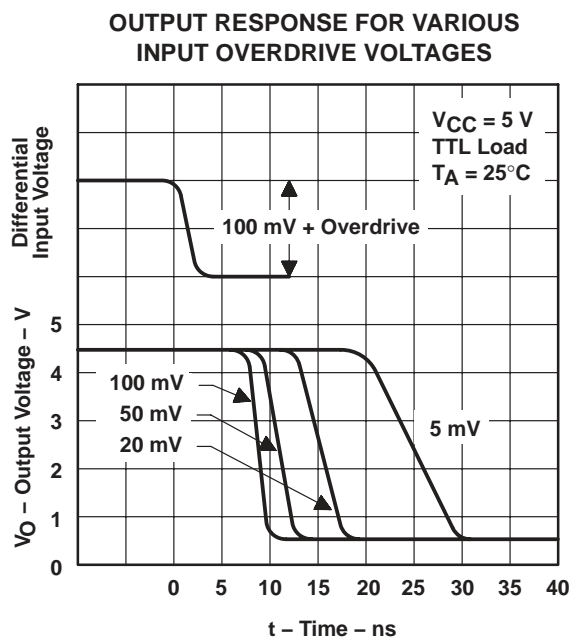


Figure 3

TYPICAL CHARACTERISTICS

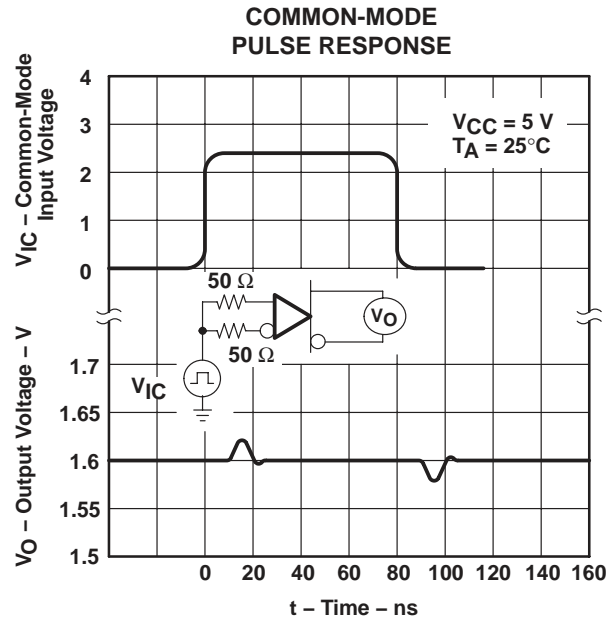
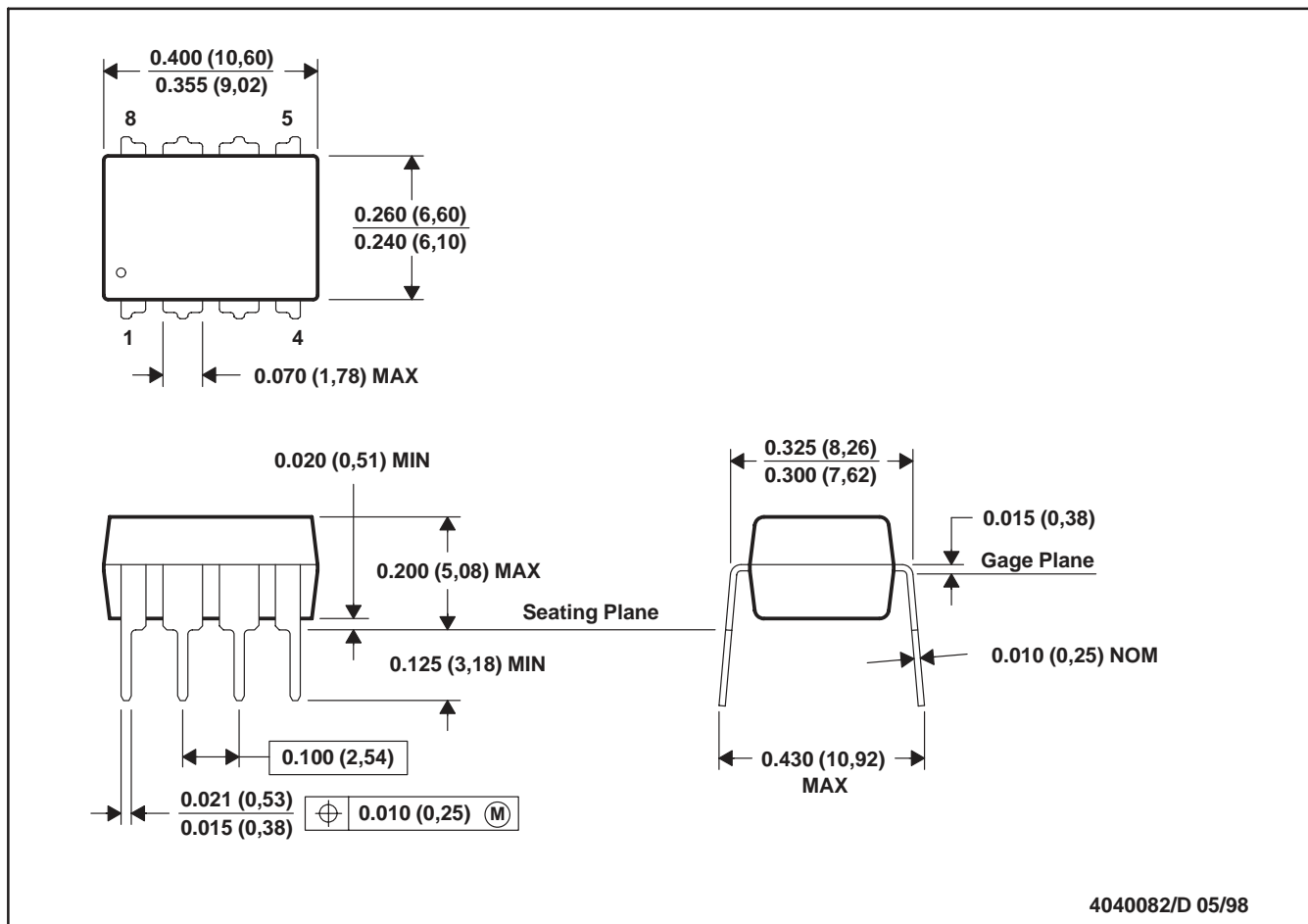


Figure 4

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



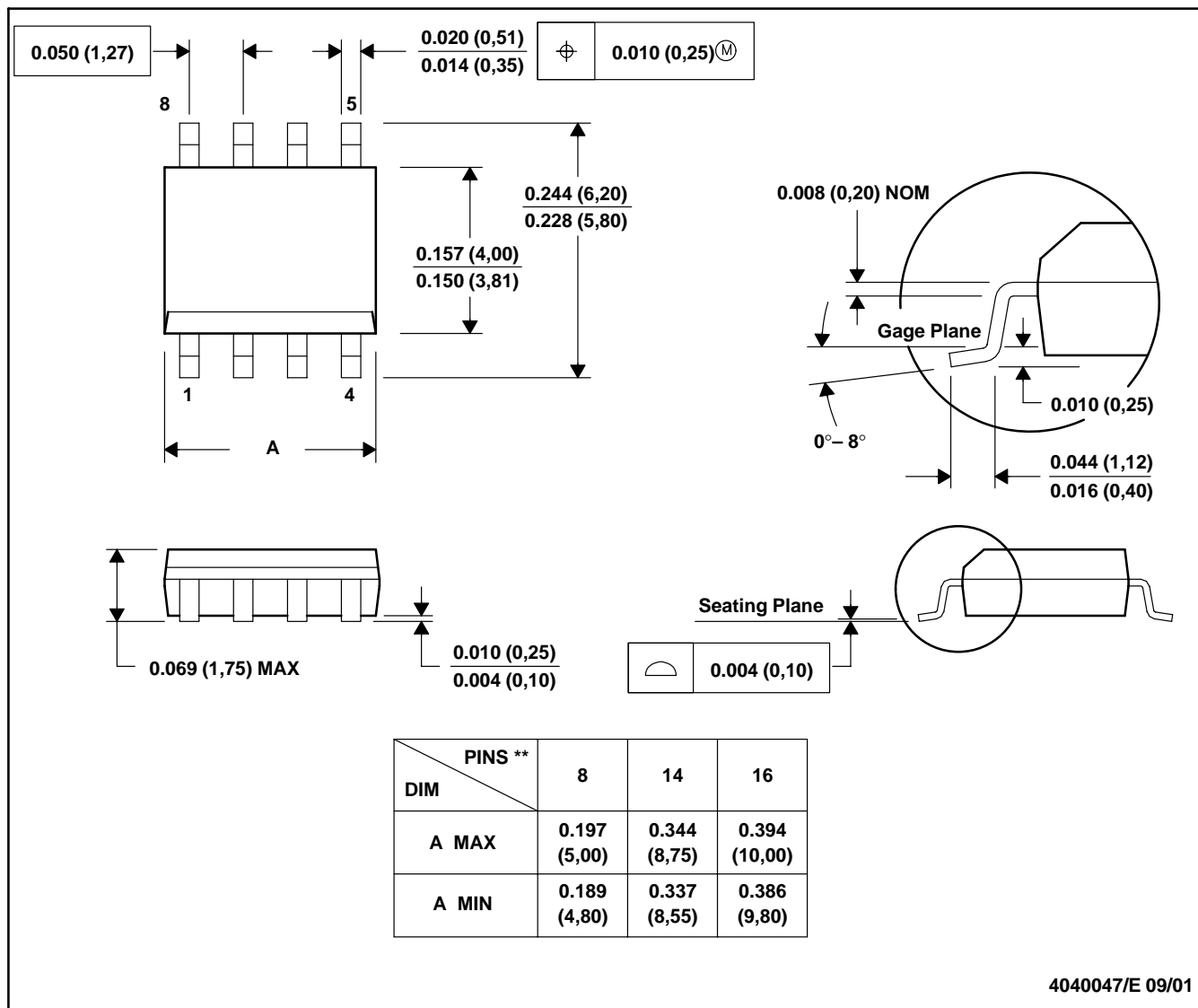
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

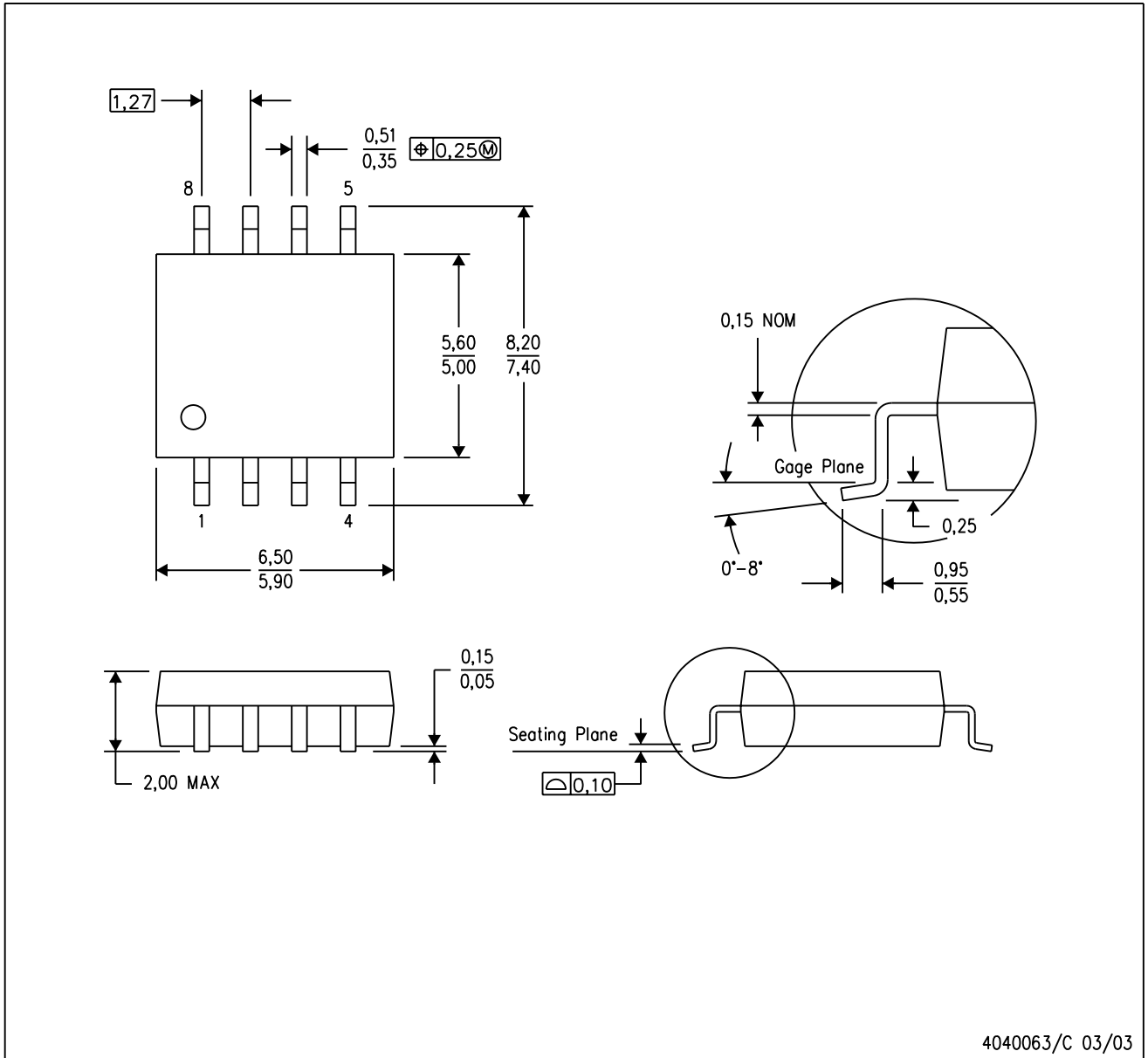


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



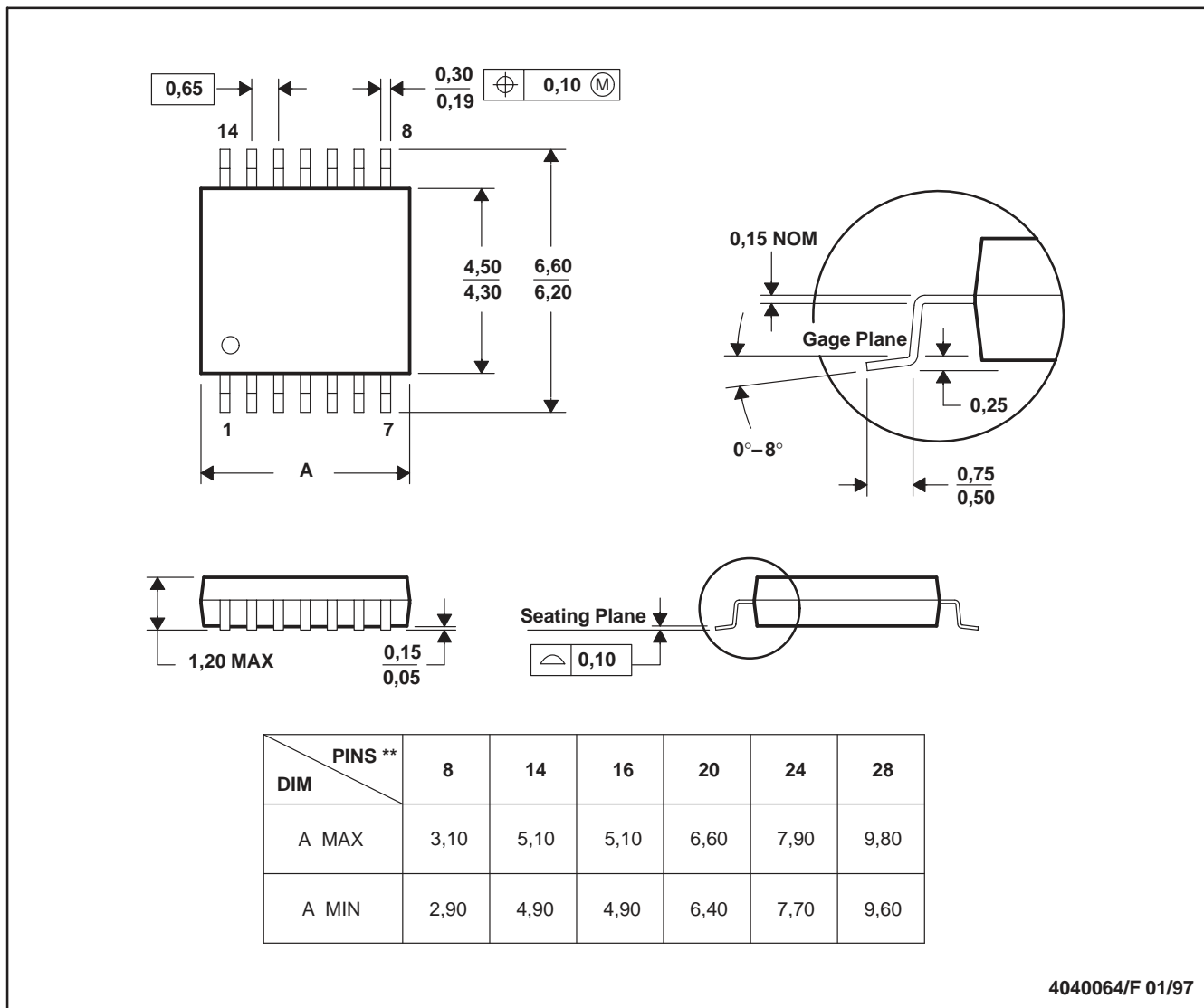
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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