ON Semiconductor

Is Now



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MOSFET - Power, Single N-Channel, μ8FL 100 V, 72 mΩ, 16 A

NTTFS080N10G

Features

- Wide SOA for Linear Mode Operation
- Low R_{DS(on)} to Minimize Conduction Losses
- High Peak UIS Current Capability for Ruggedness
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

• 48 V Hot Swap System, Load Switch, Soft-Start, E-Fuse

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parar	Symbol	Value	Unit		
Drain-to-Source Voltag	V_{DSS}	100	V		
Gate-to-Source Voltage	9		V _{GS}	±20	V
Continuous Drain	Steady	T _C = 25°C	I _D	16	Α
Current R _{θJC} (Note 2)	State	T _C = 100°C		11	
Power Dissipation	Steady	T _C = 25°C	P_{D}	39	W
R _{θJC} (Note 2)	State	T _C = 100°C		19	
Continuous Drain	Steady T _A = 25°C		I _D	4.1	Α
Current R _{θJA} (Notes 1, 2)	State	T _A = 100°C		2.8	
Power Dissipation	Steady T _A = 25°C		P_{D}	2.5	W
R _{θJA} (Notes 1, 2)	State	T _A = 100°C		1.2	
Pulsed Drain Current	$T_A = 25$	°C, t _p = 10 μs	I _{DM}	125	Α
Operating Junction and Range	T _J , T _{stg}	-55 to +175	°C		
Source Current (Body D	IS	32	Α		
Single Pulse Drain-to-S Energy (I _{L(pk)} = 5.2 A, L	E _{AS}	40	mJ		
Lead Temperature Solde dering Purposes (1/8" fr	TL	260	°C		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

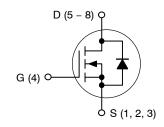


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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX	
100 V	72 mΩ @ 10 V	16 A	

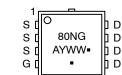
N-Channel





CASE 511AB

MARKING DIAGRAM



80NG = Specific Device Code A = Assembly Location

Y = Year WW = Work Week = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{ heta JC}$	3.8	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{ hetaJA}$	60	

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	oyzer	1001 00110			.,,,,	III UZA	J 0
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D	= 250 µA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	$V_{GS} = 0$ V, $I_D = 250 \mu A$ $I_D = 250 \mu A$, referenced to 25°C			87.6		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25°C			1	μА
			T _J = 150°C			100	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	_S = ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)							Т
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D}$	= 22 μΑ	2.0		4.0	V
Negative Treshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 22 μA, refere	nced to 25°C		-9.37		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 V$	_D = 4 A		60	72	mΩ
Forward Transconductance	9 _{FS}	V _{DS} = 5 V, I _D = 4 A			6		S
Gate-Resistance	R_{G}	T _A = 25°C			0.53		Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V			560.5		pF
Output Capacitance	C _{oss}				64		1
Reverse Transfer Capacitance	C _{rss}	• D2 = 3	,		9		1
Total Gate Charge	Q _{G(TOT)}				8.6		nC
Threshold Gate Charge	Q _{G(TH)}				1.7		7
Gate-to-Source Charge	Q _{GS}	$V_{GS} = 10 \text{ V}, V_{DS} =$	50 V, I _D = 4 A		3.2		1
Gate-to-Drain Charge	Q_{GD}				2		1
Output Charge	Q _{OSS}	V _{GS} = 10 V, V _I	_{OS} = 50 V		6.1		1
SWITCHING CHARACTERISTICS (No	te 4)						
Turn-On Delay Time	t _{d(on)}				8.4		ns
Rise Time	t _r	Voc = 10 V Vo	50 V		3		1
Turn-Off Delay Time	t _{d(off)}	$V_{GS} = 10 \text{ V}, V_{D}$ $I_{D} = 4 \text{ A}, R_{G}$	$= 4.7 \Omega$		11.9		1
Fall Time	t _f				2.8		1
DRAIN-SOURCE DIODE CHARACTER	RISTICS						
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 4 A	T _J = 25°C		0.83	1.2	V
			T _J = 125°C		0.70		1
Reverse Recovery Time	t _{RR}	Voc - 0 V dlc/dt	- 300 A/us		17		ns
Reverse Recovery Charge	Q _{RR}	$V_{GS} = 0 \text{ V, } dl_S/dt = 300 \text{ A/}\mu\text{s,}$ $l_S = 2 \text{ A}$			37		nC
Reverse Recovery Time	t _{RR}	\\ 0\\ d\\ \d\ \d\ 1000\\ -			14		ns
Reverse Recovery Charge	Q _{RR}	$V_{GS} = 0 \text{ V, } dl_S/dt = 1000 \text{ A/}\mu\text{s,}$ $l_S = 2 \text{ A}$			60.5		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

^{4.} Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

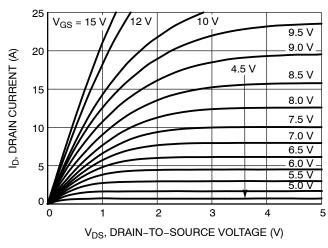


Figure 1. On-Region Characteristics

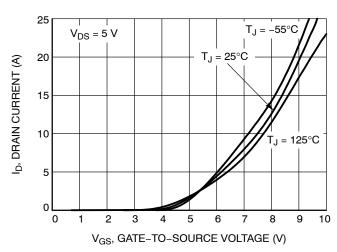


Figure 2. Transfer Characteristics

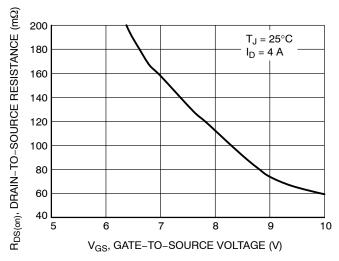


Figure 3. On-Resistance vs. Gate-to-Source Voltage

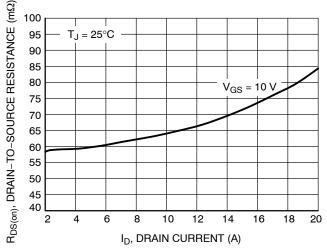


Figure 4. On-Resistance vs. Drain Current

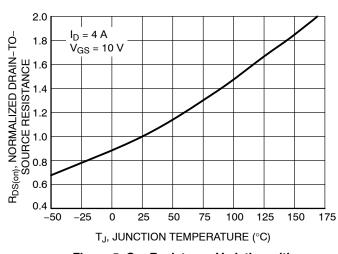


Figure 5. On–Resistance Variation with Temperature

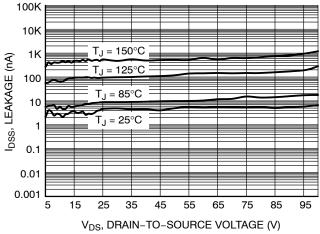


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

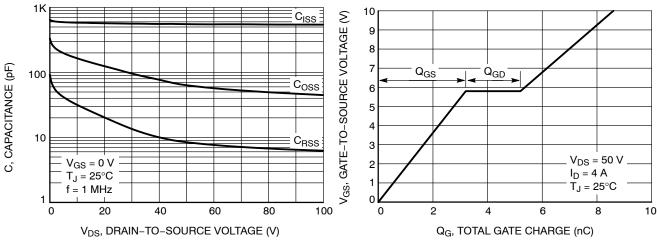


Figure 7. Capacitance Variation

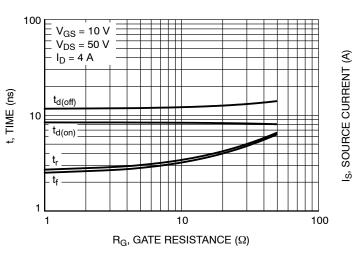


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

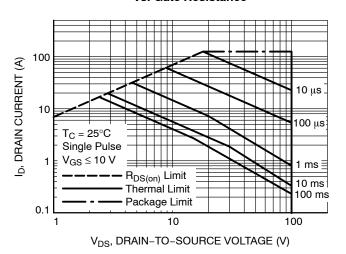


Figure 11. Maximum Rated Forward Biased Safe Operating Area



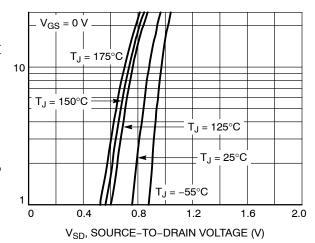


Figure 10. Diode Forward Voltage vs. Current

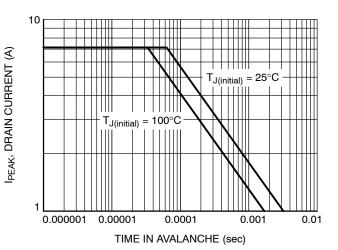


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

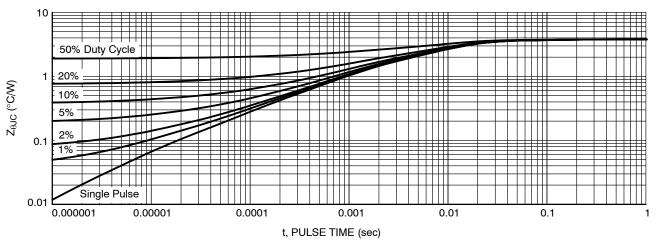


Figure 13. Junction-to-Ambient Transient Thermal Response

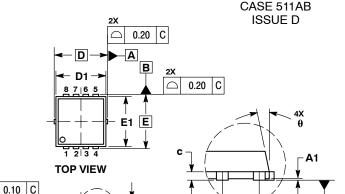
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTTFS080N10G	80NG	μ8FL (Pb–Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P



DETAIL A

6X

е

DETAIL A

NOTES:

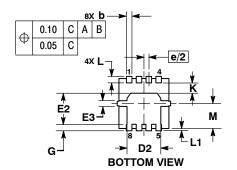
C

SEATING

- NOTES:

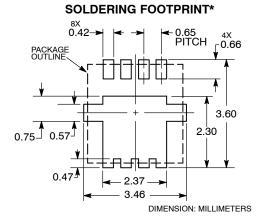
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00		0.05	0.000		0.002	
b	0.23	0.30	0.40	0.009	0.012	0.016	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D		3.30 BSC		0	.130 BSC)	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
E		3.30 BSC		0.130 BSC			
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	0.23	0.30	0.40	0.009	0.012	0.016	
е	0.65 BSC			0.026 BSC			
G	0.30	0.41	0.51	0.012	0.016	0.020	
K	0.65	0.80	0.95	0.026	0.032	0.037	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
M	1.40	1.50	1.60	0.055	0.059	0.063	
θ	0 °		12 °	0 °		12 °	



С 0.10

SIDE VIEW



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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