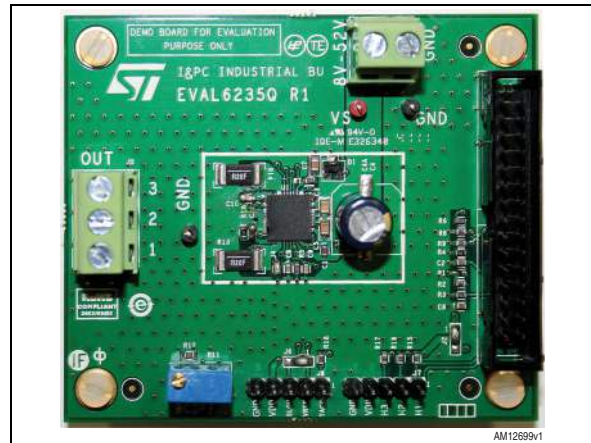


3-phase BLDC motor driver mounting the L6235Q

Data brief

Features

- Voltage range from 8 V to 52 V
- Phase current up to 2.5 A r.m.s.
- Adjustable PWM current control OFF-time
- Logic inputs 5 V / 3.3 V compliant
- Hall sensor inputs
- External speed loop
- Small application footprint with high thermal performance
- Suitable for use in combination with PractiSPIN™ 2 software



Description

The EVAL6235Q is a 3-phase BLDC motor driver board that allows the user to test the L6235Q functions.

The board can be driven using the STEVAL-PCC009V2 communication board and the PractiSPIN 2 evaluation software.

1 Board description

Table 1. EVAL6208Q electrical specifications

| Parameter | Value |
|---|----------------------------|
| Supply voltage (VS) | 8 to 52 V |
| Maximum output current (each phase) | 2.5 Ar.m.s. |
| Low level logic input voltage | 0 V |
| High level logic input voltage | 5 V / 3.3 V ⁽¹⁾ |
| Maximum VREF input voltage (J2 connector) | 3.3 V |
| Switching frequency | Up to 100 kHz |
| Operating temperature | - 25 to +125 °C |
| L6235Q thermal resistance junction-to-ambient | TBD |

1. Logic inputs are 3.3 V and 5 V compliant.

Figure 1. Trimmer, jumper and connector locations

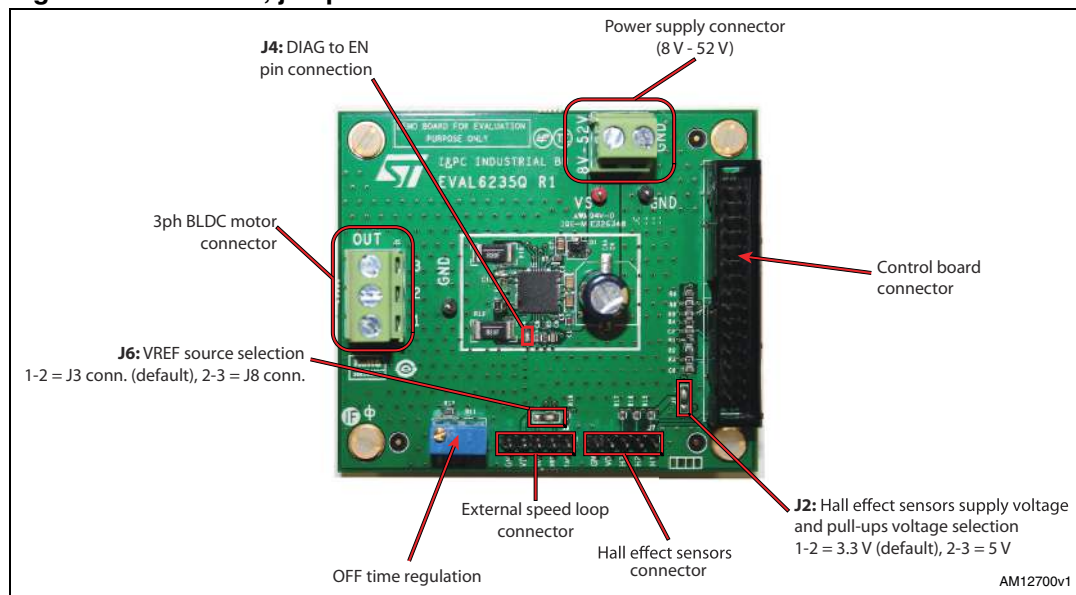


Table 2. Control board connector pinout (J3)

| Pin | Type | Function |
|--------|----------------|--|
| 1 | Power supply | 5 V supply voltage |
| 2 | Ground | Ground |
| 3 | Logic output | Hall effect H1 signal (H1 input of L6235Q) |
| 4 | Logic input | Direction input (FW/REV input of L6235Q) |
| 5 | Logic output | Hall effect H3 signal (H3 input of L6235Q) |
| 6 | Logic input | Motor brake input (BRAKE input of L6235Q) |
| 11 | Analog input | Reference voltage for current control system |
| 13 | Ground | Ground |
| 14 | Supply voltage | 3.3 V supply voltage |
| 15 | Logic output | Hall effect H2 signal (H2 input of L6235Q) |
| 16 | Logic input | Device enable input (EN input of L6235Q) |
| 23 | Ground | Ground |
| 24 | Analog output | Board identification system ID0 |
| 25 | Analog output | Board identification system ID1 |
| 28 | Ground | Ground |
| 29 | Logic output | Fault output (DIAG output of L6235Q) |
| 30 | Logic input | Hall effect H2 signal (H2 input of L6235Q) |
| Others | Unconnected | |

Table 3. Hall effect sensors connector pinout (J7)

| Pin | Type | Function |
|-----|--------------|--|
| 1 | Logic input | Hall effect H1 signal (H1 input of L6235Q) |
| 2 | Logic input | Hall effect H2 signal (H2 input of L6235Q) |
| 3 | Logic input | Hall effect H3 signal (H3 input of L6235Q) |
| 4 | Power supply | Hall effect sensor supply voltage VDD (selected through J2 jumper) |
| 5 | Ground | Ground |

Table 4. External speed loop connector pinout (J8)

| Pin | Type | Function |
|-----|---------------|---|
| 1 | Logic output | TACHO output from L6235Q |
| 2 | Analog output | Speed loop reference voltage from J3 connector |
| 3 | Analog input | Speed loop output to L6235Q VREF pin ⁽¹⁾ |
| 4 | Power supply | Supply voltage VDD (selected through J2 jumper) |
| 5 | Ground | Ground |

1. The J6 jumper must be properly set (closed 2-3).

Figure 2. EVAL6235Q - schematic

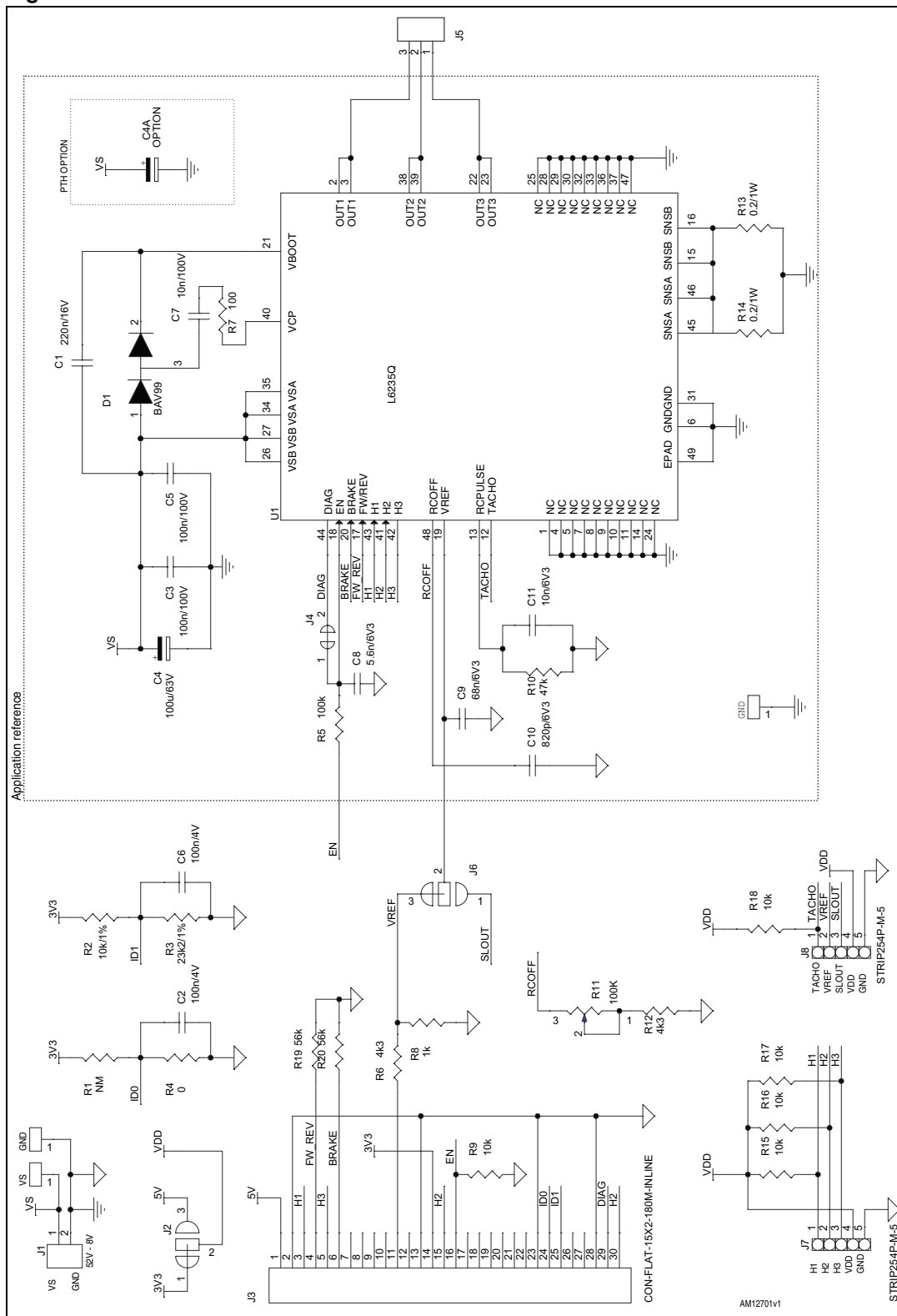


Table 5. EVAL6235Q - bill of material

| Index | Quantity | Reference | Value | Package |
|-------|----------|------------------------|---|----------------------|
| 1 | 1 | C1 | 220 nF / 16 V | CAPC-0603 |
| 2 | 2 | C2, C6 | 100 nF / 4 V | CAPC-0603 |
| 3 | 2 | C3, C5 | 100 nF / 100 V | CAPC-0805 |
| 4 | 1 | C4 | 100 μ F / 63 V | CAPE-R10H10 |
| 5 | 1 | C4A | 100 μ F / 63 V (option) | CAPE-R8H12-P35 |
| 6 | 1 | C7 | 10 nF / 100 V | CAPC-0805 |
| 7 | 1 | C8 | 5.6 nF / 6V3 | CAPC-0603 |
| 8 | 1 | C9 | 68 nF / 6V3 | CAPC-0603 |
| 9 | 1 | C10 | 820 pF / 6V3 | CAPC-0603 |
| 10 | 1 | C11 | 10 nF / 6V3 | CAPC-0603 |
| 11 | 1 | D1 | BAV99 | SOT23 |
| 12 | 1 | J1 | Screw connector 2 poles | MORSV-508-2P |
| 13 | 2 | J2, J6 | Jumper - close 12 | JP3SO |
| 14 | 1 | J3 | Pol. IDC male header vertical 30 poles | CON-FLAT-15X2-180M |
| 15 | 1 | J4 | Jumper - close | JP2SO |
| 16 | 1 | J5 | Screw connector 3 poles | MORSV-508-3P |
| 17 | 2 | J7, J8 | Pin strip header 1x5 poles | STRIP254P-M-5 |
| 18 | 1 | R1 | NM | RESC-0603 |
| 19 | 1 | R2 | 10 k Ω / 1% | RESC-0603 |
| 20 | 1 | R3 | 23.2 k Ω / 1% | RESC-0603 |
| 21 | 1 | R4 | 0 Ω | RESC-0603 |
| 22 | 1 | R5 | 100 k Ω | RESC-0603 |
| 23 | 2 | R6, R12 | 4.3 k Ω | RESC-0603 |
| 24 | 1 | R7 | 100 Ω | RESC-0603 |
| 25 | 1 | R8 | 1 k Ω | RESC-0603 |
| 26 | 5 | R9, R15, R16, R17, R18 | 10 k Ω | RESC-0603 |
| 27 | 1 | R10 | 47 k Ω | RESC-0603 |
| 28 | 1 | R11 | 100 k Ω | TRIMM-100x50x110-64W |
| 29 | 2 | R13, R14 | 0.4 Ω / 1 Ω | RESC-2512 |
| 30 | 2 | R19, R20 | 56 k Ω | RESC-0603 |
| 31 | 1 | TP1 | TPTH-RING-1 mm red | TH |
| 32 | 2 | TP2, TP3 | TPTH-RING-1 mm black | TH |
| 33 | 1 | U1 | L6235Q | QFN7x7_48 |

Figure 3. EVAL6235Q - layout (silk screen)

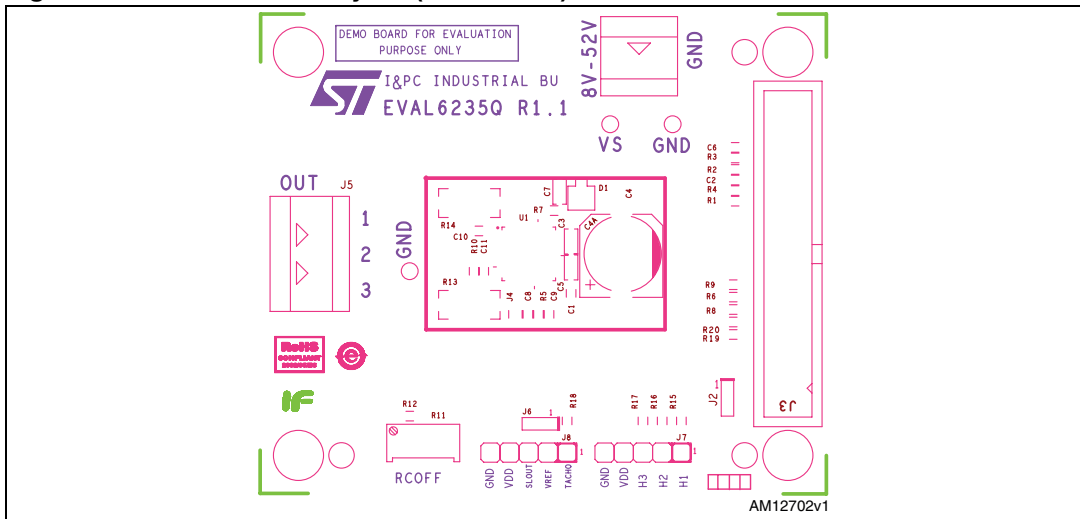


Figure 4. EVAL6235Q - layout (top layer)

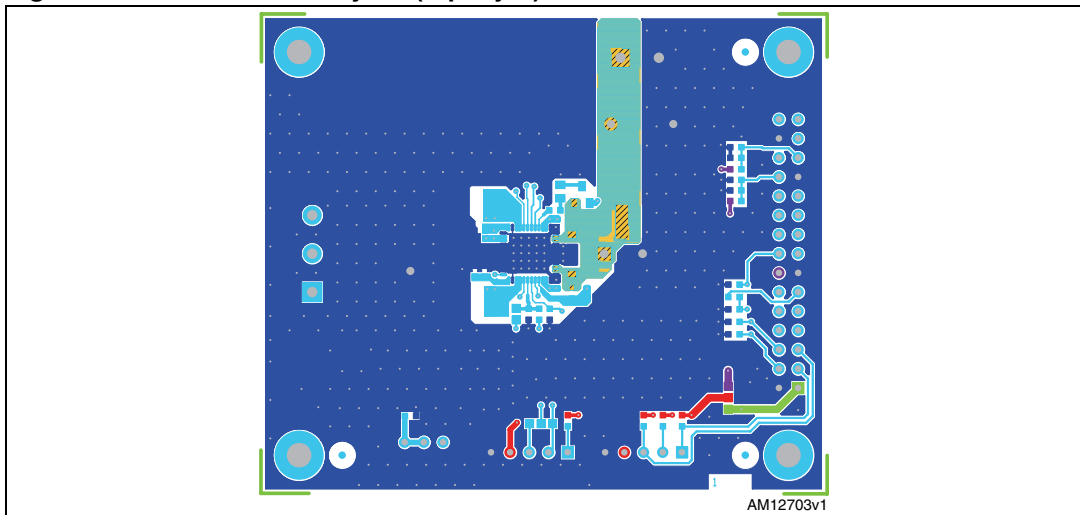


Figure 5. EVAL6235Q - layout (inner layer 2)

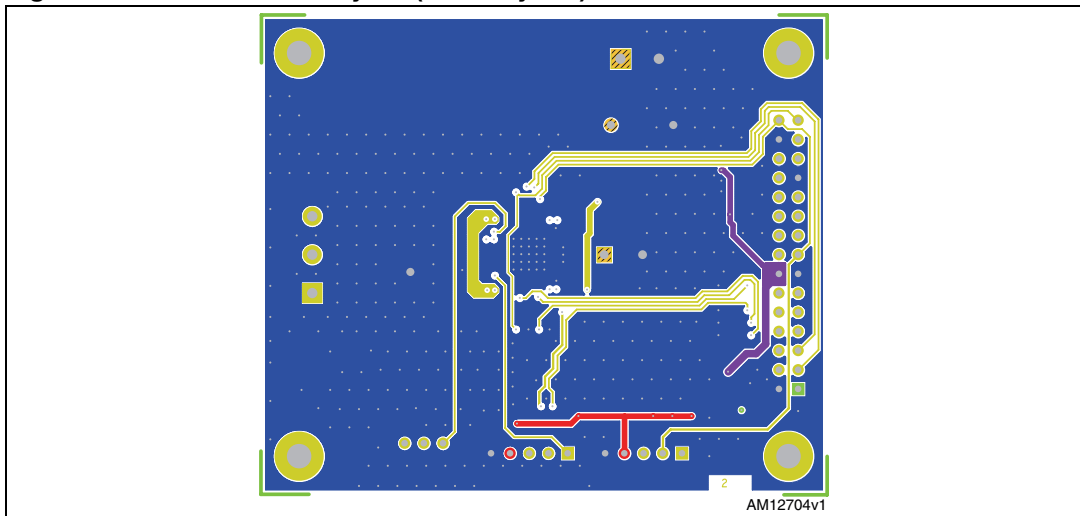


Figure 6. EVAL6235Q - layout (inner layer 3)

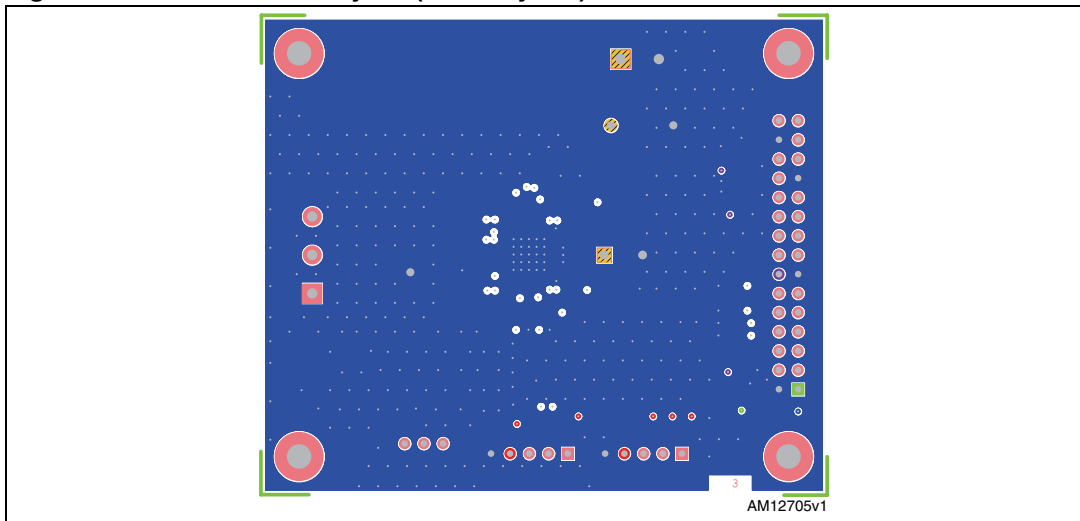
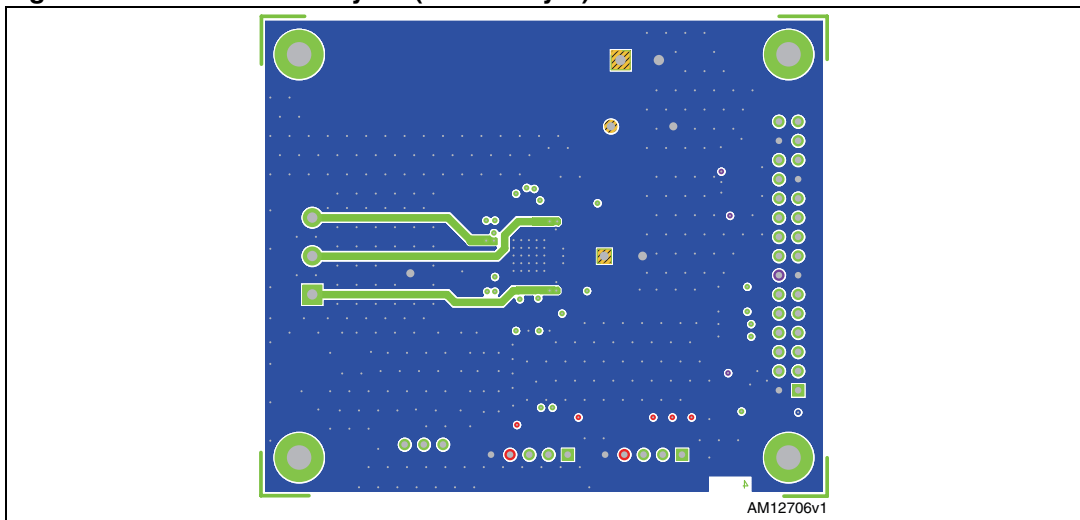


Figure 7. EVAL6235Q - layout (bottom layer)



2 Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 11-Apr-2012 | 1 | Initial release. |

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