Compact, 800 mA, 3 MHz, Simple DVS, Buck Regulator

Data Sheet

ADP2147

FEATURES

Input voltage: 2.3 V to 5.5 V
Peak efficiency: 95%
3 MHz fixed frequency operation
Low quiescent current: 23 µA
Ultralow shutdown current: 0.2 µA (typical)
VSEL pin for simple dynamic voltage scaling (DVS)
100% duty cycle low dropout mode
Internal synchronous rectifier, compensation, and soft start
Current overload and thermal shutdown protection
Small, 6-ball, 1 mm × 1.5 mm WLCSP package

APPLICATIONS

PDAs and palmtop computers
Wireless handsets
Digital audio portable media players
Digital cameras, GPS navigation units
Low power portable medical equipment

GENERAL DESCRIPTION

The ADP2147 is a high efficiency, low quiescent current, step-down (buck) dc-to-dc regulator with an output voltage that can be switched between two different settings under the control of a select pin. The total solution requires only three tiny external components.

The buck regulator automatically switches operating modes, depending on the load current level, to maximize efficiency. At high output loads, the buck regulator operates in PWM mode. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM), improving the light-load efficiency.

The ADP2147 runs on input voltages of 2.3 V to 5.5 V, which allows for single lithium or lithium polymer cells, multiple alkaline or NiMH cells, PCMCIA, USB, and other standard power sources. The maximum load current of 800 mA is achievable across the input voltage range.

The ADP2147 is available with fixed output voltages from 0.8 V to 3.3 V. All versions include an internal power switch and synchronous rectifier for minimal external part count and high efficiency. The ADP2147 has an internal soft start and is internally compensated. During logic controlled shutdown, the input is disconnected from the output, and the ADP2147 draws less than 0.2 µA (typical) from the power source.

Other key features include undervoltage lockout to prevent deep battery discharge and soft start to prevent input current overshoot at startup. The ADP2147 is available in a 6-ball WLCSP.

TYPICAL APPLICATIONS CIRCUIT

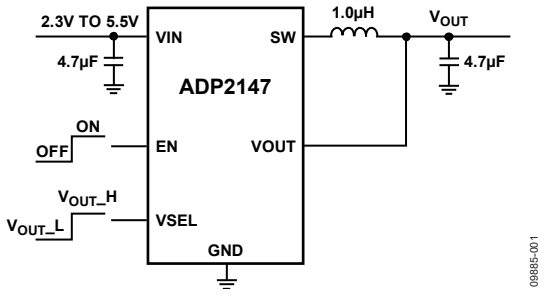

Figure 1.

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REVISION HISTORY

9/2019—Rev. 0 to Rev. A

Changes to Output Capacitor Section ... 14
Changes to Ordering Guide ... 16

5/2011—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, V_{OUT} = 0.8 V to 3.3 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range		2.3		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising			2.3	V
	V_{IN} falling	2.00	2.15	2.25	V
OUTPUT CHARACTERISTICS					
Output Voltage Accuracy	PWM mode, VSEL = Low	−2		+2	%
	PWM mode, VSEL = High	−2.5		+2.5	%
Line Regulation	V_{IN} = 2.3 V to 5.5 V, PWM mode		0.25		%/V
Load Regulation	I_{LOAD} = 0 mA to 800 mA		−0.95		%/A
PWM TO POWER SAVE MODE CURRENT THRESHOLD			100		mA
INPUT CURRENT CHARACTERISTICS					
DC Operating Current	I_{LOAD} = 0 mA, device not switching		23	30	µA
Shutdown Current	EN = 0 V, $T_A = T_J$ = −40°C to +85°C		0.2	1.0	µA
SW CHARACTERISTICS					
SW On Resistance	pFET		155	240	mΩ
	nFET		115	200	mΩ
Current Limit	pFET switch peak current limit	1100	1500	1650	mA
ENABLE/VSEL CHARACTERISTICS					
Input High Threshold		1.2			V
Input Low Threshold				0.4	V
Input Leakage Current	EN = VSEL = 0 V to 3.6 V	−1	0	+1	µA
OSCILLATOR FREQUENCY		2.6	3.0	3.4	MHz
START-UP TIME			250		µs
THERMAL CHARACTERISTICS					
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			20		°C

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

T_A = −40°C to +125°C, unless otherwise specified. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE	C_{MIN}	4.7			µF
CAPACITOR ESR	R_{ESR}	0.001		1	Ω

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN, EN, VSEL	−0.4 V to +6.5 V
VOUT, SW to GND	−1.0 V to (V_{IN} + 0.2 V)
Temperature Range	
Operating Ambient	−40°C to +85°C
Operating Junction	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Model	
Human Body	±1500 V
Charged Device	±500 V
Machine	±100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP2147 can be damaged if the junction temperature limit is exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limit. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit if the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. Refer to JEDEC JESD 51-9 for detailed information pertaining to board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter measured in units of °C/W. The package Ψ_{JB} is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path, which is the procedure for measuring thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications than θ_{JB}. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JEDEC JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
6-Ball WLCSP	170	80	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

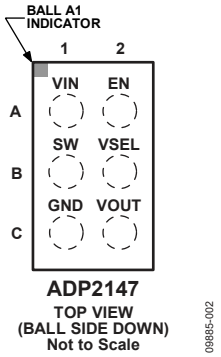

Figure 2. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Power Source Input. VIN is the source of the pFET high-side switch. Bypass VIN to GND with a 4.7 µF or greater capacitor as close to the ADP2147 as possible.
B1	SW	Switch Node Output. SW is the drain of the P-channel MOSFET switch and N-channel synchronous rectifier. Connect the output LC filter between SW and the output voltage.
C1	GND	Ground. Connect the input and output capacitors to GND.
A2	EN	Buck Activation. To turn on the buck, set EN to high. To turn off the buck, set EN to low.
B2	VSEL	Voltage Select Input for Simple Dynamic Voltage Scaling (DVS). Drive VSEL low to switch the VOUT pin to the default voltage setting. Drive VSEL high to switch VOUT to the alternate voltage setting.
C2	VOUT	Output Voltage Sensing Input.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, T_A = 25°C, V_{EN} = V_{IN}, unless otherwise noted.

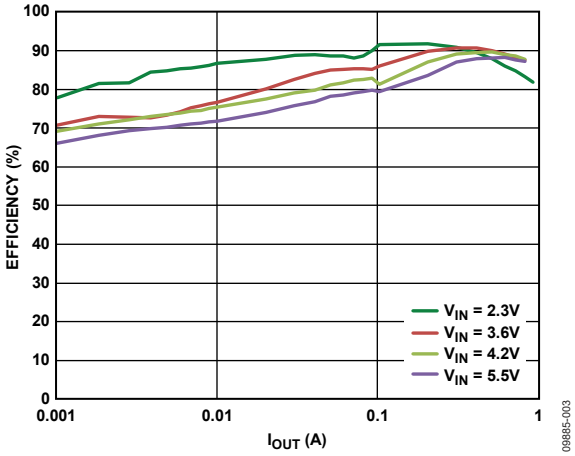

Figure 3. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 1.8 V

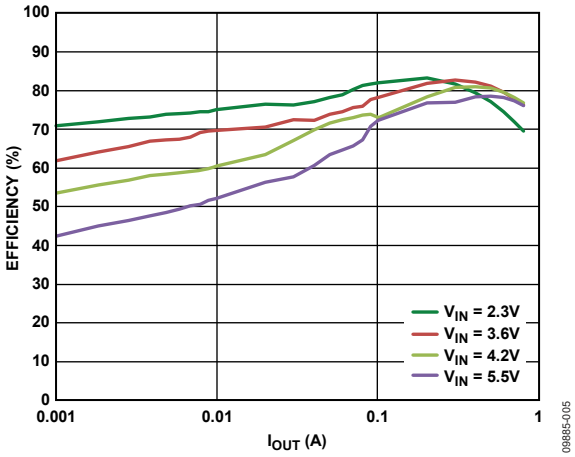

Figure 4. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 0.8 V

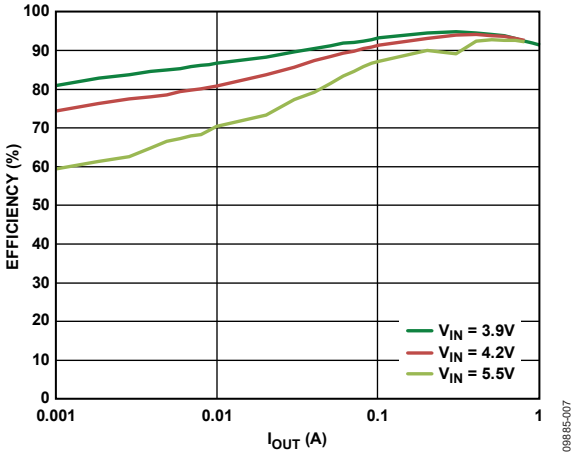

Figure 5. Efficiency vs. Load Current, Across Input Voltage, V_{OUT} = 3.3 V

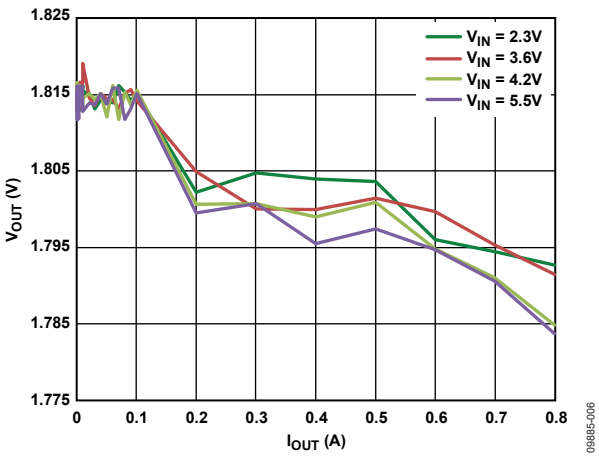

Figure 6. Load Regulation Across Input Voltage, V_{OUT} = 1.8 V

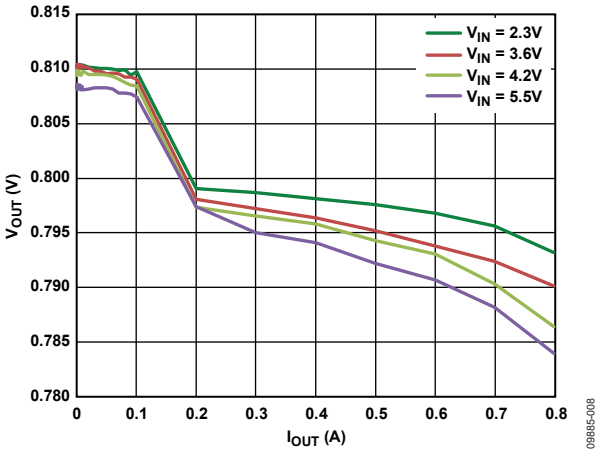

Figure 7. Load Regulation Across Input Voltage, V_{OUT} = 0.8 V

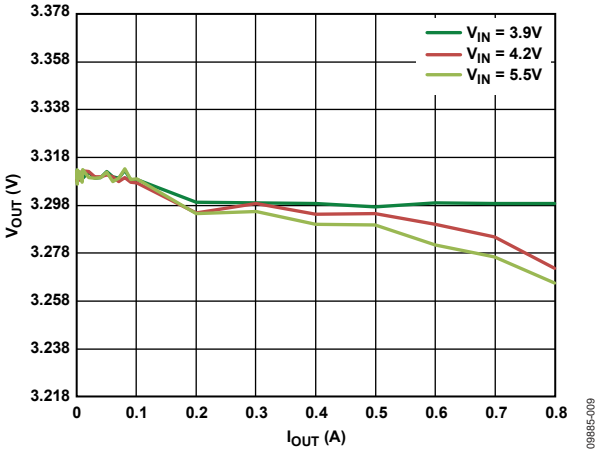

Figure 8. Load Regulation Across Input Voltage, V_{OUT} = 3.3 V

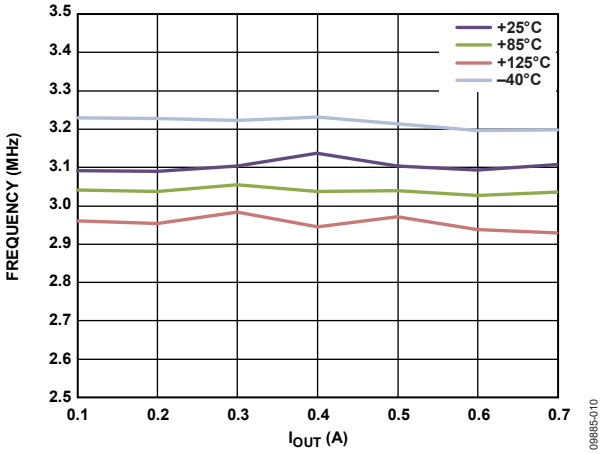

Figure 9. Frequency vs. Output Current, Across Temperature, V_{OUT} = 1.8 V

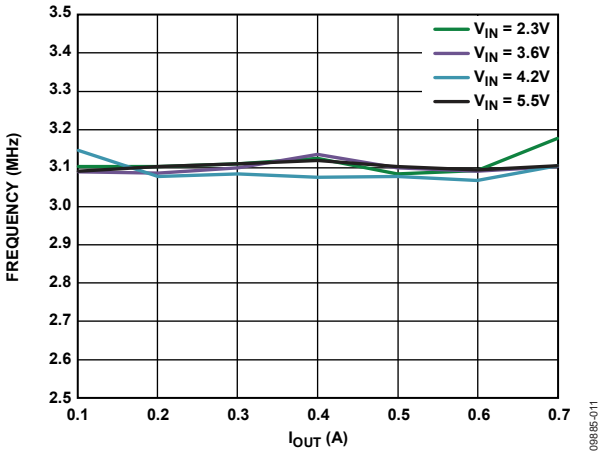

Figure 10. Frequency vs. Output Current, Across Supply Voltage, V_{OUT} = 1.8 V

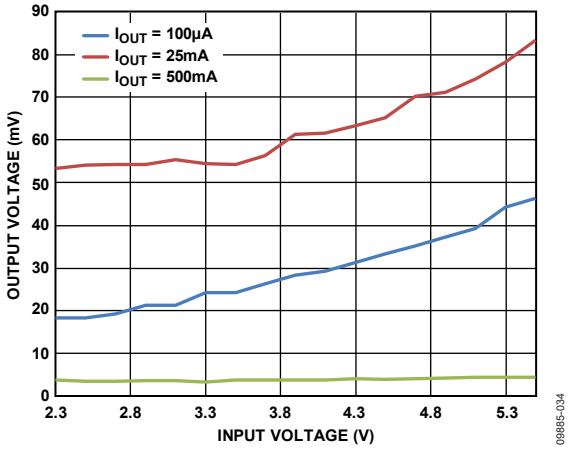

Figure 11. Output Voltage Ripple vs. Input Voltage, Across Output Current, V_{OUT} = 1.8 V

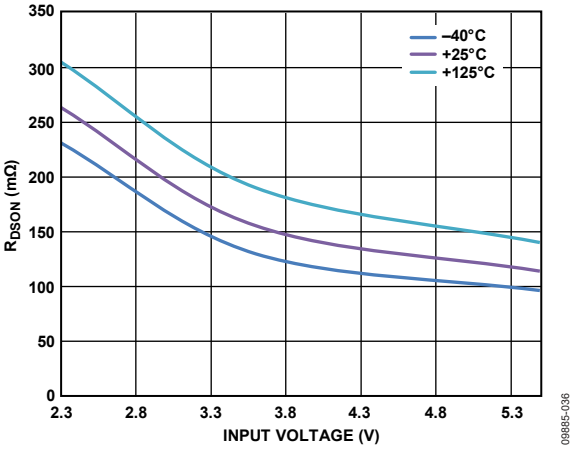

Figure 12. R_{DSON} PFET vs. Input Voltage, Across Temperature

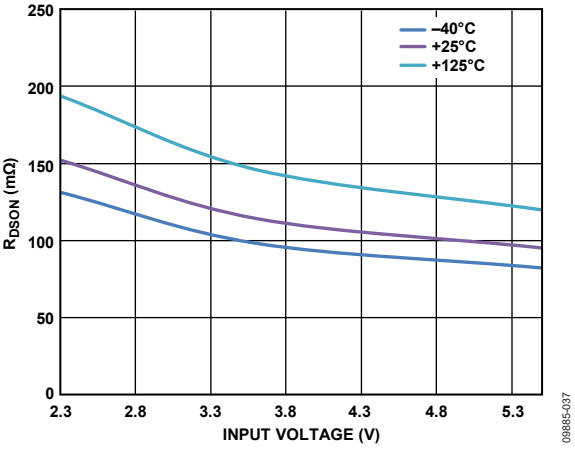

Figure 13. R_{DSON} NFET vs. Input Voltage, Across Temperature

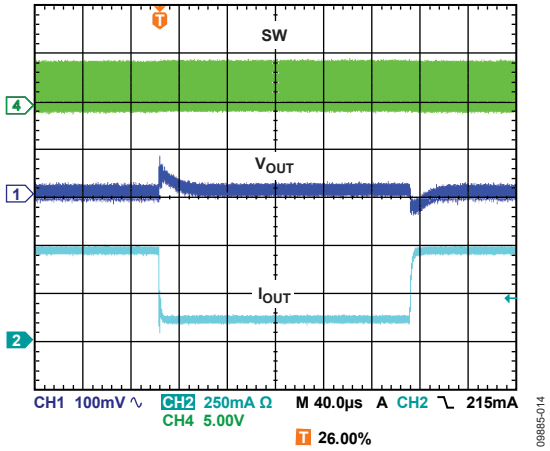

Figure 14. Response to Load Transient, 150 mA to 500 mA, V_{OUT} = 1.8 V

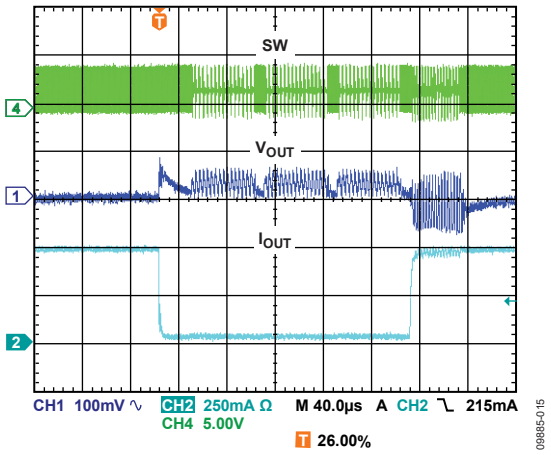

Figure 15. Response to Load Transient, 50 mA to 200 mA, V_{OUT} = 1.8 V

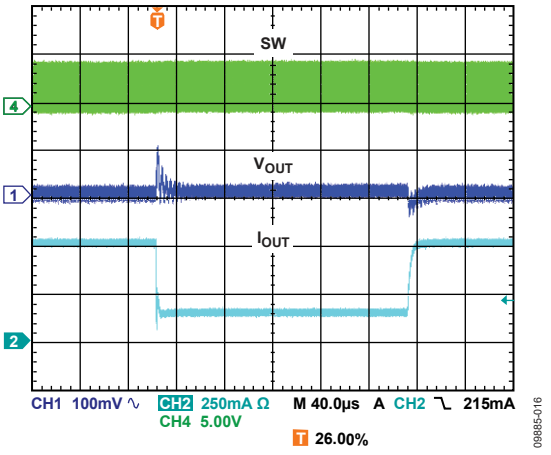

Figure 16. Response to Load Transient, 150 mA to 500 mA, V_{OUT} = 0.8 V

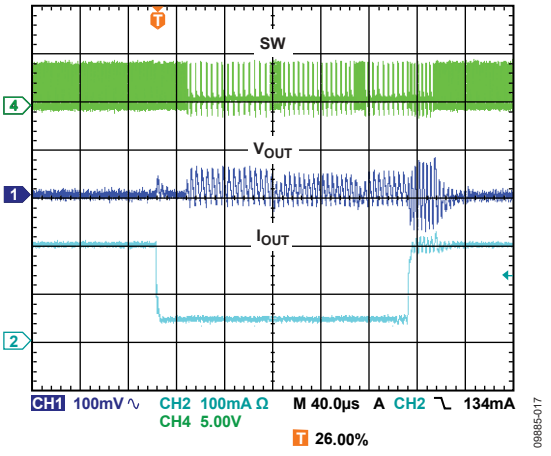

Figure 17. Response to Load Transient, 50 mA to 200 mA, V_{OUT} = 0.8 V

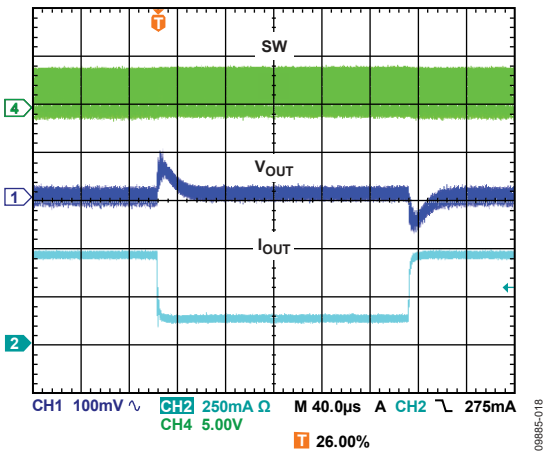

Figure 18. Response to Load Transient, 150 mA to 500 mA, V_{OUT} = 3.3 V

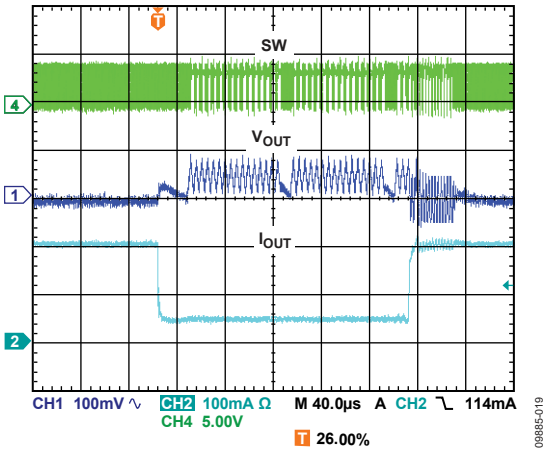

Figure 19. Response to Load Transient, 50 mA to 200 mA, V_{OUT} = 3.3 V

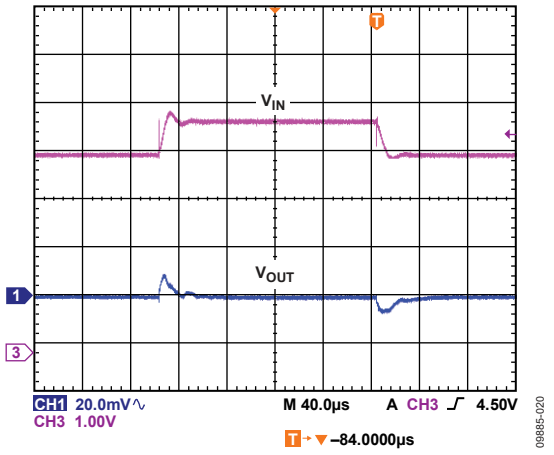

Figure 20. Response to Line Transient, V_{OUT} = 3.3 V, V_{IN} = 4.0 V to 4.8 V

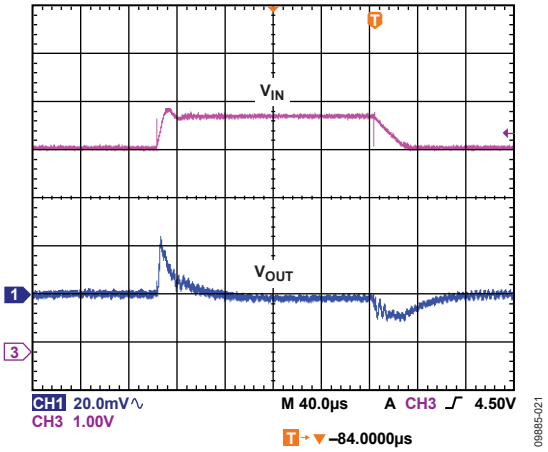

Figure 21. Response to Line Transient, V_{OUT} = 0.8 V, V_{IN} = 4.0 V to 4.8 V

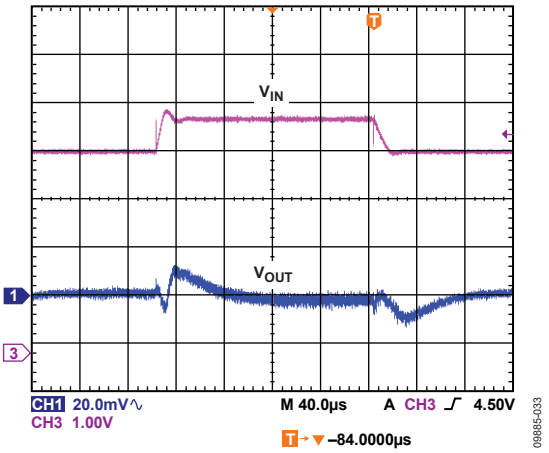

Figure 22. Response to Line Transient, V_{OUT} = 1.8 V, V_{IN} = 4.0 V to 4.8 V

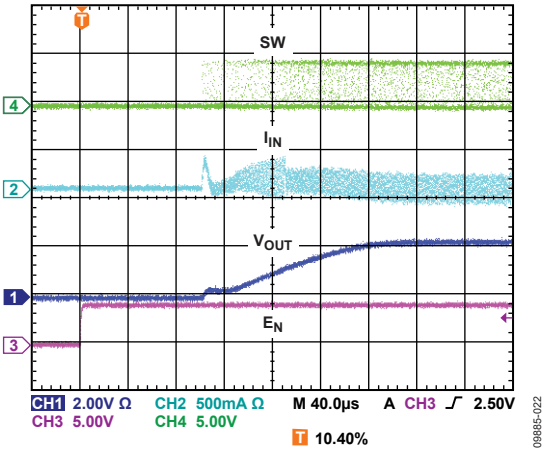

Figure 23. Startup, V_{OUT} = 1.8 V, I_{OUT} = 10 mA

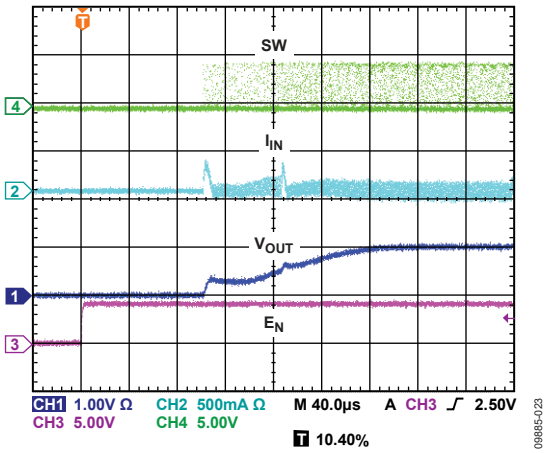

Figure 24. Startup, V_{OUT} = 0.8 V, I_{OUT} = 10 mA

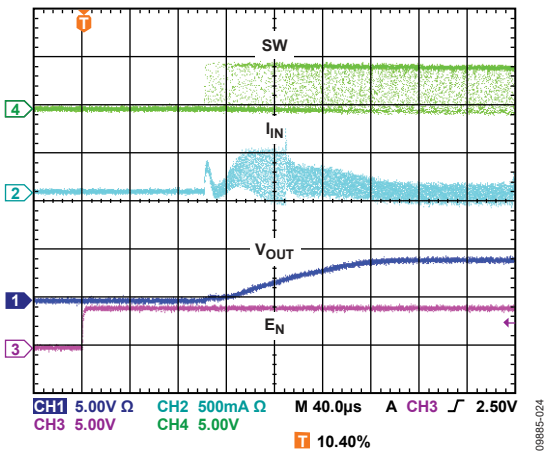

Figure 25. Startup, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

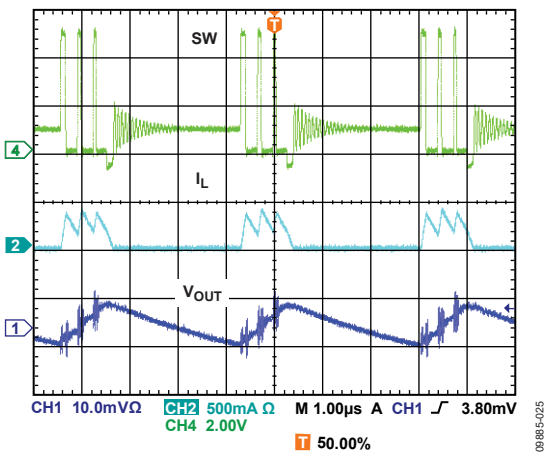

Figure 26. Typical Waveform, V_{OUT} = 1.8 V, PSM Mode, I_{OUT} = 10 mA

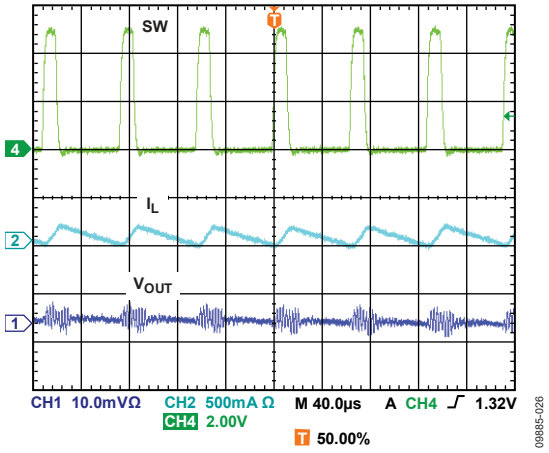

Figure 27. Typical Waveform, V_{OUT} = 1.8 V, PWM Mode, I_{OUT} = 200 mA

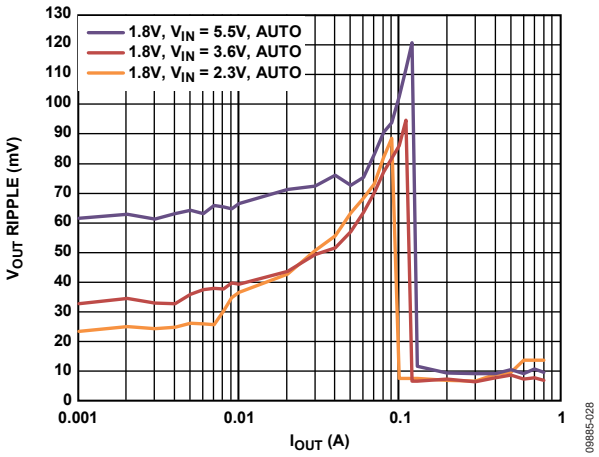

Figure 28. V_{OUT} Peak-to-Peak Ripple vs. Output Current, V_{OUT} = 1.8 V

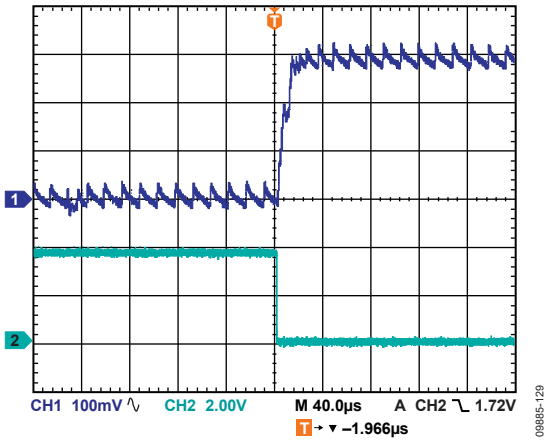

Figure 29. VSEL Change Triggering VOUT Transition from 0.981 V to 1.275 V, I_{LOAD} = 10 mA

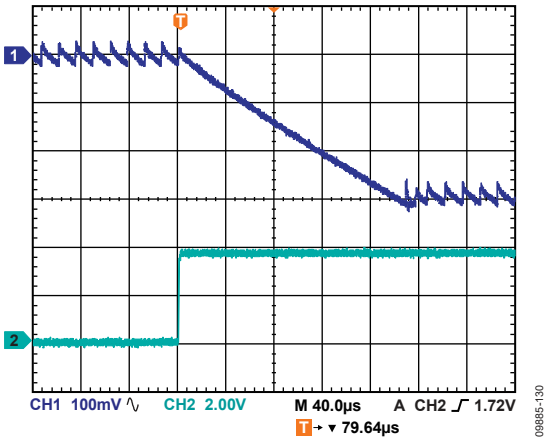

Figure 30. VSEL Change Triggering VOUT Transition from 1.275 V to 0.981 V, I_{LOAD} = 10 mA

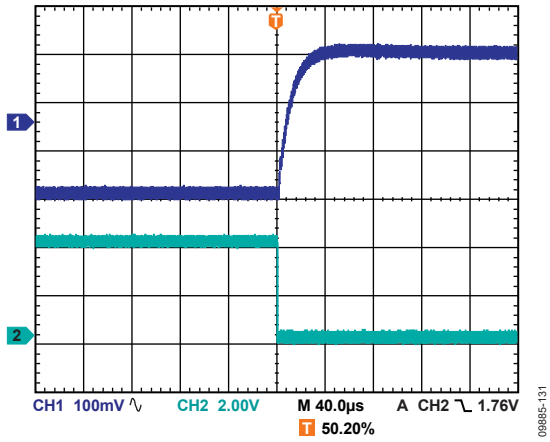

Figure 31. VSEL Change Triggering VOUT Transition from 0.981 V to1.275 V, I_{LOAD} = 200 mA

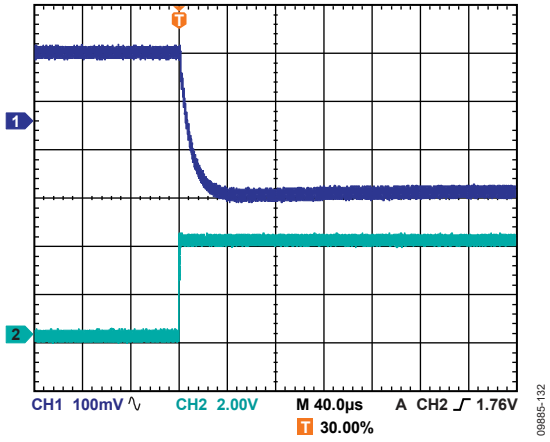

Figure 32. VSEL Change Triggering VOUT Transition from1.275 V to 0.981 V, I_{LOAD} = 200 mA

THEORY OF OPERATION

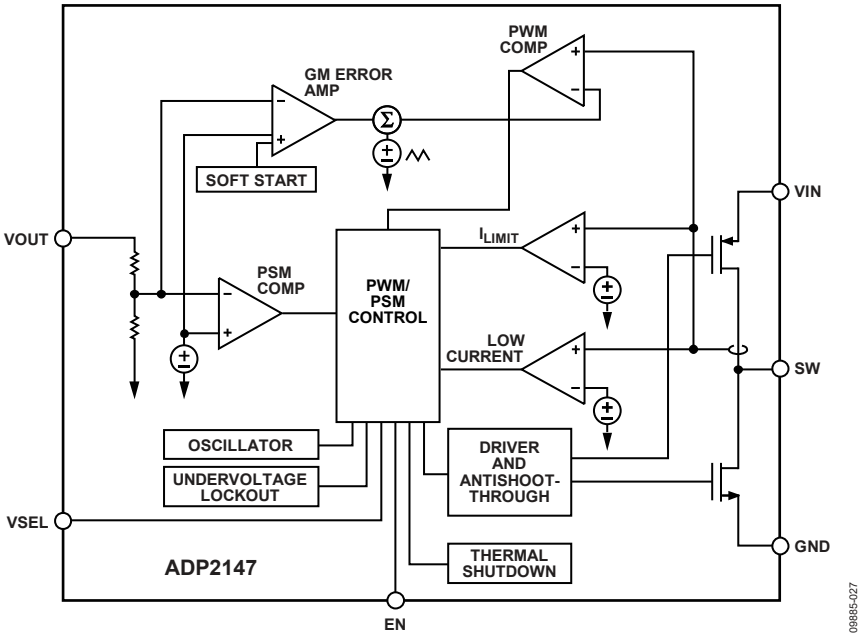

Figure 33. Functional Block Diagram

The ADP2147 is a step-down dc-to-dc regulator that uses a fixed frequency and high speed current-mode architecture. The high switching frequency and tiny 6-ball WLCSP package enable a small step-down dc-to-dc regulator solution.

The ADP2147 operates with an input voltage of 2.3 V to 5.5 V and regulates an output voltage down to 0.8 V.

CONTROL SCHEME

The ADP2147 operates with a fixed frequency, current-mode PWM control architecture at medium to high loads for high efficiency but shifts to a power save mode control scheme at light loads to lower the regulation power losses. When operating in PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in power save mode at light loads, the output voltage is controlled in a hysteretic manner, with higher V_{OUT} ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM MODE

In PWM mode, the ADP2147 operates at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the pFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the magnitude of the current sense signal crosses the peak inductor current threshold. This turns off the pFET switch and turns on the nFET synchronous rectifier, which sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

The ADP2147 regulates the output voltage by adjusting the peak inductor current threshold.

POWER SAVE MODE

The ADP2147 smoothly transitions to the power save mode of operation when the load current decreases below the power save mode current threshold. When the ADP2147 enters power save mode, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation turns off. At this point, both power switches are off, and the ADP2147 enters idle mode. C_{OUT} discharges until V_{OUT} falls to the PWM regulation voltage, at which point the device drives the inductor to cause V_{OUT} to rise again to the upper threshold. This process is repeated for as long as the load current is below the power save mode current threshold.

Power Save Mode Current Threshold

The power save mode current threshold is set to 100 mA. The ADP2147 employs a scheme that ensures that this current is accurately controlled and independent of V_{IN} and V_{OUT} levels. The control scheme also ensures that there is very little hysteresis between the power save mode current threshold and that of the PWM mode. The power save mode current threshold is optimized for excellent efficiency across all load currents.

ENABLE/SHUTDOWN

The ADP2147 starts operating with soft start when the EN pin is toggled from logic low to logic high. Pulling the EN pin low forces the device into shutdown mode, reducing the supply current to 0.2 µA (typical).

SIMPLE DYNAMIC VOLTAGE SCALING (DVS)

The ADP2147 has a VSEL pin that allows the user to force the output voltage to change from one level (the default VOUT setting) when VSEL is low and to another level (the alternate VOUT setting) when VSEL is high. Transition between VOUT levels is achieved within 40 µs when VOUT is commanded to go from a lower voltage to a higher voltage. When VOUT is commanded to go from a higher VOUT voltage to a lower one, the transition time depends on the load current present at that time.

SHORT-CIRCUIT PROTECTION

The ADP2147 includes frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

UNDERVOLTAGE LOCKOUT

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated on the ADP2147. If the input voltage drops below the 2.15 V UVLO threshold, the ADP2147 shuts down, and both the power switch and the synchronous rectifier turn off. When the voltage rises above the UVLO threshold, the soft start period is initiated, and the part is enabled.

THERMAL PROTECTION

In the event that the ADP2147 junction temperature rises above 150°C, the thermal shutdown circuit turns off the regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the ADP2147 does not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, a soft start is initiated.

SOFT START

The ADP2147 has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. The soft start minimizes input voltage drop when a battery or a high impedance power source is connected to the regulator's input.

After the EN pin is driven high, internal circuits begin to power up. Start-up time in the ADP2147 is the measure of when the output is in regulation after the EN pin is driven high. Start-up time consists of the power-up time plus the soft start time.

CURRENT LIMIT

The ADP2147 has protection circuitry to limit the amount of positive current flowing through the PFET switch and the synchronous rectifier. The positive current limit on the power switch controls the amount of current that can flow from the power source to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% DUTY OPERATION

With a drop in V_{IN} or with an increase in I_{LOAD}, the ADP2147 eventually reaches a limit where, even with the pFET switch on 100% of the time, V_{OUT} drops below the desired output voltage. At this limit, the ADP2147 smoothly transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the ADP2147 immediately restarts PWM regulation without allowing overshoot on V_{OUT}.

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Inductor

The high switching frequency of the ADP2147 allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Recommended inductors are shown in Table 6.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal DCR. Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the ADP2147 is a high switching frequency dc-to-dc regulator, shielded ferrite core material is recommended for its low core losses and low electromagnetic interference (EMI). Table 6 shows the suggested inductors that can be used for different output current requirements; several inductors are also listed to minimize PCB space for small current applications.

Table 6. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
	LQM18PN1R0	1.6 × 0.8 × 0.33	700	52
Coilcraft®	EPL2014-102ML	2.0 × 2.0 × 1.4	900	59
	0603LS-102	1.8 × 1.27 × 1.1	400	81
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1800	100
TDK	GLFR1608T1R0M-LR	1.6 × 0.8 × 0.8	360	80
Taiyo Yuden	CBMF1608T1R0M	1.6 × 0.8 × 0.8	290	90

Output Capacitor

Increasing the value of the output capacitor reduces the output voltage ripple and improves load transient response. When choosing the capacitor value, it is also important to account for the loss of capacitance due to dc output voltage bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc regulator because of their poor temperature and dc bias characteristics.

The worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage, is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 4.0466 µF at 1.8 V, as shown in Figure 34.

Substituting these values in the equation yields

$$C_{EFF} = 4.0466\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.0956\ \mu F$$

To guarantee the performance of the ADP2147, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

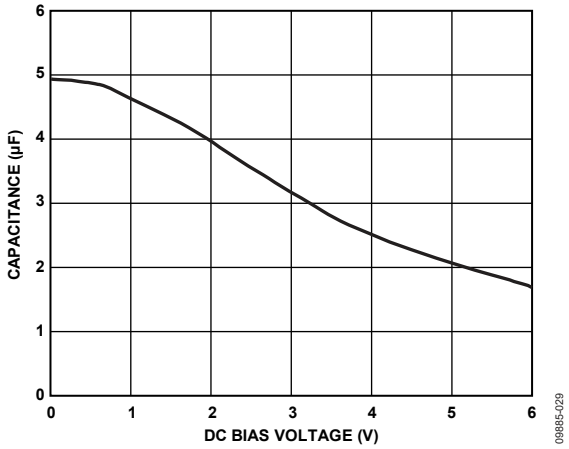

Figure 34. Typical Capacitor Performance

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = I_{RIPPLE} \times (ESR_{COUT} + 1/(8 \times f_{SW} \times C_{OUT}))$$

where:
V_{RIPPLE} is allowable peak-to-peak output voltage ripple in Volts.
I_{RIPPLE} is the inductor ripple current in Amperes.
$ESRC_{OUT}$ is the equivalent series resistance of the output capacitor in Ω.
f_{SW} is the converter switching frequency in Hertz.

Capacitors with low equivalent series resistance (ESR) values are recommended to produce low output ripple. The effective capacitance needed for stability, which includes temperature and dc bias effects, is 3 µF.

Table 7. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
TDK	X5R	C1608X5R0J475	0603	6.3

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the ADP2147 as possible. As with the output capacitor, a low ESR capacitor is recommended. The list of recommended capacitors is shown in Table 8.

Table 8. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
TDK	X5R	C1608X5R0J475	0603	6.3

THERMAL CONSIDERATIONS

Because of the high efficiency of the ADP2147, only a small amount of power is dissipated inside the ADP2147 package, which reduces thermal constraints of the design.

However, in applications with maximum loads at high ambient temperature, low supply voltage, and high duty cycle, the heat dissipated in the package is high enough that it may cause the junction temperature of the die to exceed the 125°C maximum. If the junction temperature exceeds 150°C, the converter enters thermal shutdown. The regulator recovers when the junction temperature falls below 130°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The package's rise in temperature is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.
P_D is the power dissipation in the package.

PCB LAYOUT GUIDELINES

Poor layout can affect the ADP2147 performance, causing EMI and electromagnetic compatibility problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. To implement a good layout, use the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

EVALUATION BOARD

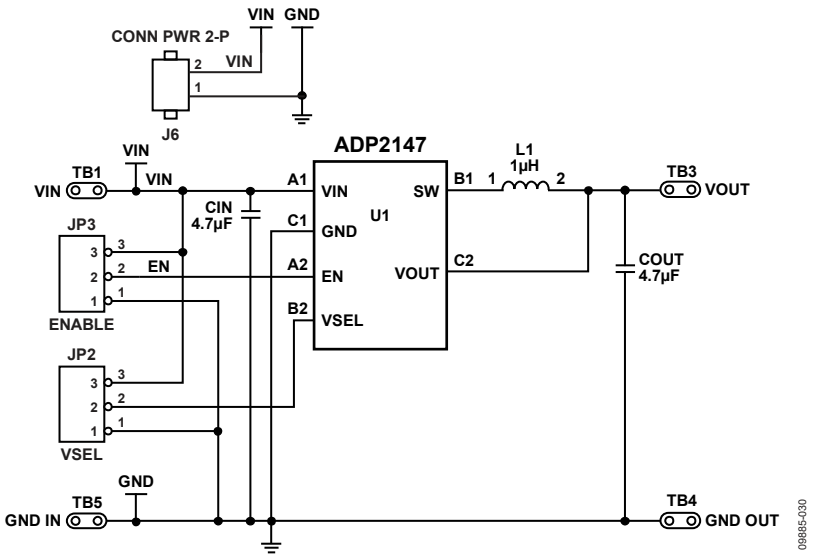

Figure 35. Evaluation Board Schematic

EVALUATION BOARD LAYOUT

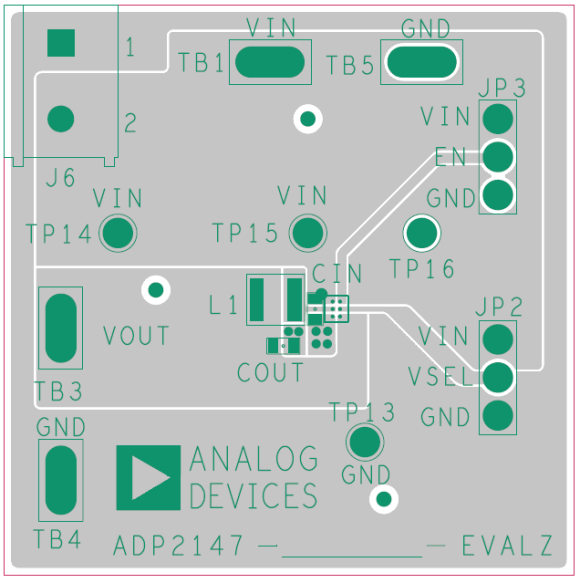

Figure 36. Top Layer

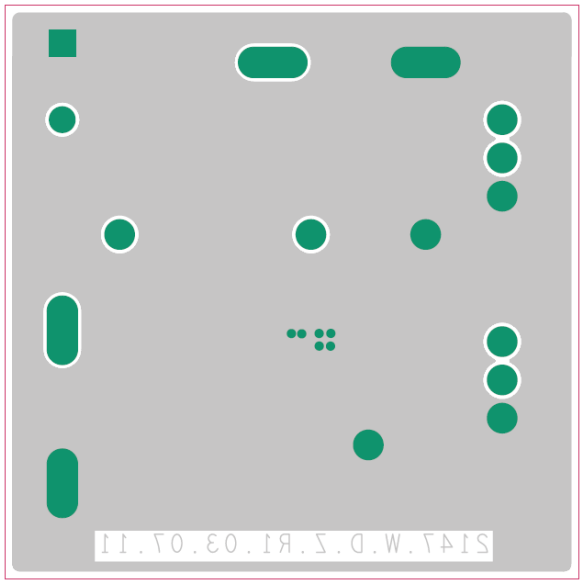

Figure 37. Bottom Layer

OUTLINE DIMENSIONS

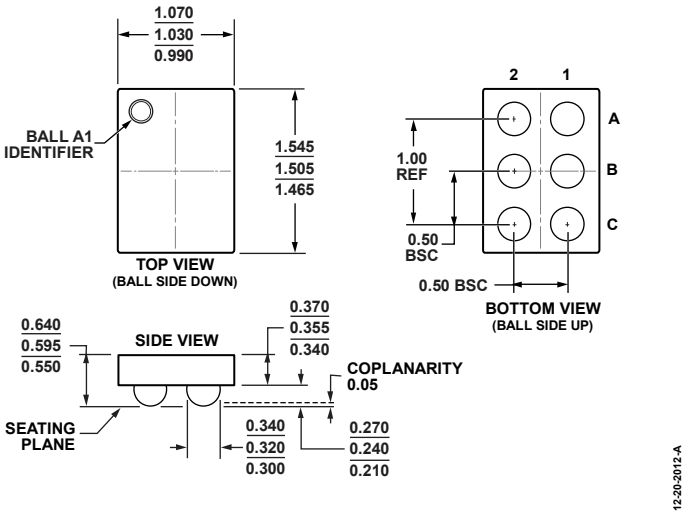

Figure 38. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	V_{OUT} (V) (VSEL = 0)	V_{OUT} (V) (VSEL = 1)	Package Description	Package Option	Marking Code
ADP2147ACBZ-110-R7	−40°C to +125°C	1.275	0.981	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LLE
ADP2147ACBZ-130-R7	−40°C to +125°C	0.9	1.3	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LLF
ADP2147ACBZ-150-R7	−40°C to +125°C	1.2	1.0	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LLG
ADP2147ACBZ-170-R7	−40°C to +125°C	0.9	1.1	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-12	LLH
ADP2147CB-110EVALZ				ADP2147CB-110 Evaluation Board		
ADP2147CB-130EVALZ				ADP2147CB-130 Evaluation Board		

[1] Z = RoHS Compliant Part.

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