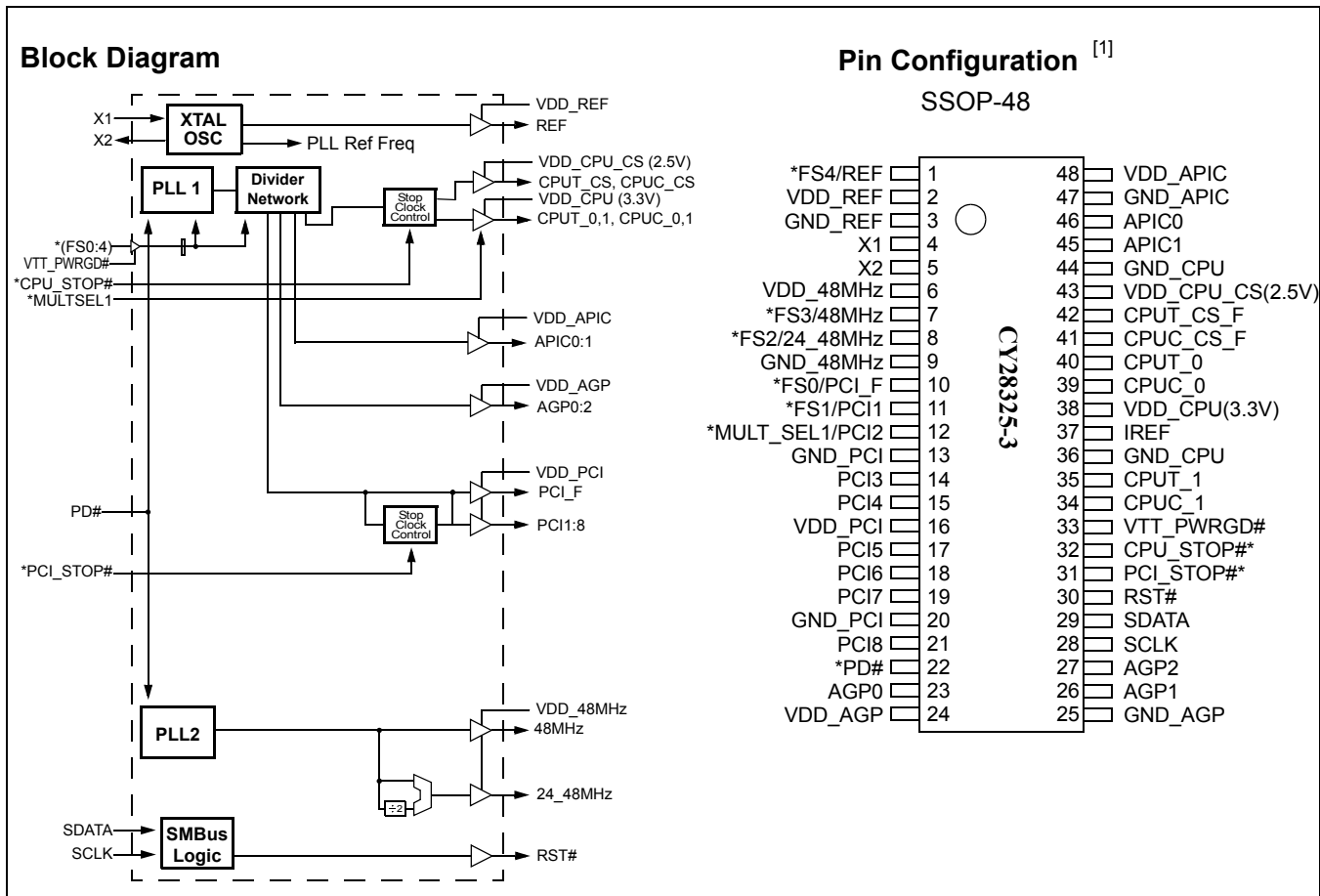# FTG for VIA™ Pentium 4™ Chipsets

## Features

- Spread Spectrum Frequency Timing Generator for VIA PT/M 266-800 Pentium® 4 Chipsets
- Programmable clock output frequency with less than 1 MHz increment
- Integrated fail-safe Watchdog Timer for system recovery
- Selectable hardware or software-programmed clock frequency when Watchdog Timer time-out
- Capable to generate system RESET after a Watchdog Timer time-out occurs or a change in output frequency via SMBus interface
- Support SMBus Byte Read/Write and Block Read/Write operations to simplify system BIOS development

- Vendor ID and Revision ID support
- Programmable-drive strength support
- Programmable-output skew support
- Three copies AGP Clocks
- Power management control inputs
- Available in 48-pin SSOP

| CPU | AGP | PCI | REF | APIC | 48M | 24_48M |
|-----|-----|-----|-----|------|-----|--------|
| x 3 | x 3 | x 9 | x 1 | x 2  | x 1 | x 1    |

## Block Diagram

## Pin Configuration [1]

### SSOP-48



**Note:**
1. Pins marked with [*] have internal pull-up resistors. Pins marked with[^] have internal pull-down resistors.

## Pin Definitions

| Pin Name | No. | Type | Description |
|---|---|---|---|
| X1 | 4 | I | **Crystal Connection or External Reference Frequency Input:** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| X2 | 5 | O | **Crystal Connection:** Connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected. |
| REF/FS4 | 1 | I/O | **Reference Clock Output/Frequency Select 4:** 3.3V 14.318-MHz output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table. |
| CPUT_0:1 CPUC_0:1 | 40, 39, 35, 34 | O | **CPU Clock Outputs:** Frequency is set by the FS0:4 inputs or through serial input interface. |
| CPUT_CS_F CPUC_CS_F | 42, 41 | O | **CPU Clock Outputs for Chipset:** Frequency is set by the FS0:4 inputs or through serial input interface. |
| APIC0:1 | 46, 45 | O | **APIC Clock Output:** APIC clock outputs running at half of PCI output frequency. |
| AGP 0:2 | 23, 26, 27 | O | **AGP Clock Output:** 3.3V AGP clock. |
| PCI_F/FS0 | 10 | I/O | **Free-running PCI Output 1/Frequency Select 1:** 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table. |
| PCI1/FS1 | 11 | I/O | **PCI Output 1 /Frequency Select 1:** 3.3V PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table. |
| PCI2/MULTSEL1 | 12 | I/O | **PCI Output 2/Current Multiplier Selection 1:** 3.3V PCI output. This pin also serves as a power-on strap option to determine the current multiplier for the CPU clock outputs. The MULTSEL definitions are as follows: MULTISEL<br>0 = Ioh is 4 × IREF<br>1 = Ioh is 6 × IREF |
| PCI3:8 | 14, 15, 17, 18, 19, 21 | O | **PCI Clock Output 3 to 8:** 3.3V PCI clock outputs. |
| 48MHz/FS3 | 7 | I/O | **48-MHz Output/Frequency Select 3:** 3.3V fixed 48-MHz, non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table. |
| 24_48MHz/FS2 | 8 | I/O | **24- or 48-MHz Output/Frequency Select 2:** 3.3V fixed 24- or 48-MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table. |
| CPU_STOP# | 32 | I | **CPU Output Control:** 3.3V LVTTL-compatible input that disables CPUT_CS, CPUC_CS, CPUT_0:1 and CPUC_0:1. |
| PCI_ST0P# | 31 | I | **PCI Output Control:** 3.3V LVTTL-compatible input that disables PCI1:8. |
| PD# | 22 | I | **Power-down Control:** 3.3V LVTTL-compatible input that places the device in power down mode when held LOW. |
| SCLK | 28 | I | **SMBus Clock Input:** Clock pin for serial interface. |
| SDATA | 29 | I/O | **SMBus Data Input:** Data pin for serial interface. |
| RST# | 30 | O (open-drain) | **System Reset Output:** Open-drain system reset output. |
| IREF | 37 | I | **Current Reference for CPU output:** A precision resistor is attached to this pin, which is connected to the internal current reference. |

**Pin Definitions** (continued)

| Pin Name | No. | Type | Description |
|---|---|---|---|
| VTT_PWRGD# | 33 | I | ***Power-good from Voltage Regulator Module (VRM):*** 3.3V LVTTL input. VTT_PWRGD# is a level sensitive strobe used to determine when FS0:4 and MULTSEL inputs are valid and OK to be sampled (Active LOW). Once VTT_PWRGD# is sampled LOW, the status of this input will be ignored. |
| VDD_CPU_CS, VDD_APIC | 43, 48 | P | ***2.5V Power Connection:*** Power supply for CPU_CS outputs buffers and APIC output buffers. Connect to 2.5V. |
| VDD_REF, VDD_48MHz, VDD _PCI, VDD_AGP, VDD_CPU | 2, 6, 16, 24, 38 | P | ***3.3V Power Connection:*** Power supply for CPU outputs buffers, 3V66 output buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V. |
| GND_REF GND_48MHz, GND_PCI, GND_AGP, GND_CPU, GND_APIC | 3, 9, 13, 20, 25, 36, 44, 47 | G | ***Ground Connection:*** Connect all ground pins to the common system ground plane. |

**Table 1. Frequency Selection Table**

| Input Conditions | | | | | Output Frequency | | | | PLL Gear Constants (G) |
|---|---|---|---|---|---|---|---|---|---|
| FS4 SEL4 | FS3 SEL3 | FS2 SEL2 | FS1 SEL1 | FS0 SEL0 | CPU | AGP | PCI | APIC | |
| 0 | 0 | 0 | 0 | 0 | 102.0 | 68.0 | 34.0 | 17.0 | 48.00741 |
| 0 | 0 | 0 | 0 | 1 | 105.0 | 70.0 | 35.0 | 17.5 | 48.00741 |
| 0 | 0 | 0 | 1 | 0 | 108.0 | 72.0 | 36.0 | 18.0 | 48.00741 |
| 0 | 0 | 0 | 1 | 1 | 111.0 | 74.0 | 37.0 | 18.5 | 48.00741 |
| 0 | 0 | 1 | 0 | 0 | 114.0 | 76.0 | 38.0 | 19.0 | 48.00741 |
| 0 | 0 | 1 | 0 | 1 | 117.0 | 78.0 | 39.0 | 19.5 | 48.00741 |
| 0 | 0 | 1 | 1 | 0 | 120.0 | 80.0 | 40.0 | 20.0 | 48.00741 |
| 0 | 0 | 1 | 1 | 1 | 123.0 | 82.0 | 41.0 | 20.5 | 48.00741 |
| 0 | 1 | 0 | 0 | 0 | 126.0 | 63.0 | 31.5 | 18.0 | 48.00741 |
| 0 | 1 | 0 | 0 | 1 | 130.0 | 65.0 | 32.5 | 18.5 | 48.00741 |
| 0 | 1 | 0 | 1 | 0 | 136.0 | 68.0 | 34.0 | 17.0 | 48.00741 |
| 0 | 1 | 0 | 1 | 1 | 140.0 | 70.0 | 35.0 | 17.5 | 48.00741 |
| 0 | 1 | 1 | 0 | 0 | 144.0 | 72.0 | 36.0 | 18.0 | 48.00741 |
| 0 | 1 | 1 | 0 | 1 | 148.0 | 74.0 | 37.0 | 18.5 | 48.00741 |
| 0 | 1 | 1 | 1 | 0 | 152.0 | 76.0 | 38.0 | 19.0 | 48.00741 |
| 0 | 1 | 1 | 1 | 1 | 156.0 | 78.0 | 39.0 | 19.5 | 48.00741 |
| 1 | 0 | 0 | 0 | 0 | 160.0 | 80.0 | 40.0 | 20.0 | 48.00741 |
| 1 | 0 | 0 | 0 | 1 | 164.0 | 82.0 | 41.0 | 20.5 | 48.00741 |
| 1 | 0 | 0 | 1 | 0 | 166.6 | 66.6 | 33.3 | 16.7 | 48.00741 |
| 1 | 0 | 0 | 1 | 1 | 170.0 | 68.0 | 34.0 | 17.0 | 48.00741 |
| 1 | 0 | 1 | 0 | 0 | 175.0 | 70.0 | 35.0 | 17.5 | 48.00741 |
| 1 | 0 | 1 | 0 | 1 | 180.0 | 72.0 | 36.0 | 18.0 | 48.00741 |

**Table 1. Frequency Selection Table** (continued)

| Input Conditions | | | | | Output Frequency | | | | PLL Gear Constants (G) |
|---|---|---|---|---|---|---|---|---|---|
| FS4 | FS3 | FS2 | FS1 | FS0 | | | | | |
| SEL4 | SEL3 | SEL2 | SEL1 | SEL0 | CPU | AGP | PCI | APIC | |
| 1 | 0 | 1 | 1 | 0 | 185.0 | 74.0 | 37.0 | 18.5 | 48.00741 |
| 1 | 0 | 1 | 1 | 1 | 190.0 | 76.0 | 38.0 | 19.0 | 48.00741 |
| 1 | 1 | 0 | 0 | 0 | 100.9 | 67.3 | 33.6 | 16.8 | 48.00741 |
| 1 | 1 | 0 | 0 | 1 | 133.9 | 67.0 | 33.5 | 16.7 | 48.00741 |
| 1 | 1 | 0 | 1 | 0 | 200.5 | 66.8 | 33.4 | 16.7 | 48.00741 |
| 1 | 1 | 0 | 1 | 1 | 166.8 | 66.7 | 33.3 | 16.7 | 48.00741 |
| 1 | 1 | 1 | 0 | 0 | 100.0 | 66.6 | 33.3 | 16.7 | 48.00741 |
| 1 | 1 | 1 | 0 | 1 | 133.3 | 66.6 | 33.3 | 16.7 | 48.00741 |
| 1 | 1 | 1 | 1 | 0 | 200.0 | 66.6 | 33.3 | 16.7 | 48.00741 |
| 1 | 1 | 1 | 1 | 1 | 166.7 | 66.7 | 33.3 | 16.7 | 48.00741 |

## Swing Select Functions

| MultSEL1 | MultSEL0 | Board Target Trace/Term Z | Reference R, IREF = $VDD/(3*Rr)$ | Output Current | $V_{OH}$ @ Z |
|---|---|---|---|---|---|
| 0 | 0 | 50Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 4*Iref | 1.0V @ 50 |
| 0 | 0 | 60Ω | Rr = 221 1%, IREF = 5.00 | $I_{OH}$ = 4*Iref | 1.2V @ 60 |
| 0 | 1 | 50Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 5*Iref | 1.25V @ 50 |
| 0 | 1 | 60Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 5*Iref | 1.5V @ 60 |
| 1 | 0 | 50Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 6*Iref | 1.5V @ 50 |
| 1 | 0 | 60Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 6*Iref | 1.8V @ 60 |
| 1 | 1 | 50Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 7*Iref | 1.75V @ 50 |
| 1 | 1 | 60Ω | Rr = 221 1%, IREF = 5.00 mA | $I_{OH}$ = 7*Iref | 2.1V @ 60 |
| 0 | 0 | 50Ω | Rr = 475 1%, IREF = 2.32 mA | $I_{OH}$ = 4*Iref | 0.47V @ 50 |
| 0 | 0 | 60Ω | Rr = 475 1%, IREF = 2.32 mA | $I_{OH}$ = 4*Iref | 0.56V @ 60 |
| 0 | 1 | 50Ω | Rr = 475 1%, IREF = 2.32 mA | $I_{OH}$ = 5*Iref | 0.58V @ 50 |
| 0 | 1 | 60Ω | Rr = 475 1%, IREF = 2.32 mA | $I_{OH}$ = 5*Iref | 0.7V @ 60 |
| 1 | 0 | 50Ω | Rr = 475 1%, IREF = 2.32 mA | $I_{OH}$ = 6*Iref | 0.7V @ 50 |
| 1 | 0 | 60Ω | Rr = 475 1%, IREF = 2.32 mA | $I_{OH}$ = 6*Iref | 0.84V @ 60 |
| 1 | 1 | 50 Ohm | Rr = 475 1%, IREF = 2.32mA | $I_{OH}$ = 7*Iref | 0.81V @ 50 |
| 1 | 1 | 60 Ohm | Rr = 475 1%, IREF = 2.32mA | $I_{OH}$ = 7*Iref | 0.97V @ 60 |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 2. Command Code Definition**

| Bit | Description |
|---|---|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 3.  Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 Bit '00000000' stands for block operation | 11:18 | Command Code – 8 Bit '00000000' stands for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29:36 | Data byte 1 – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 2 – 8 bits | 30:37 | Byte count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge from master |
| .... | ...................... | 39:46 | Data byte from slave – 8 bits |
| .... | Data Byte (N–1) –8 bits | 47 | Acknowledge from master |
| .... | Acknowledge from slave | 48:55 | Data byte from slave – 8 bits |
| .... | Data Byte N –8 bits | 56 | Acknowledge from master |
| .... | Acknowledge from slave | .... | Data byte N from slave – 8 bits |
| .... | Stop | .... | Acknowledge from master |
| | | .... | Stop |

**Table 4. Byte Read and Byte Write Protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[4:0] of the command code represents the offset of the byte to be accessed | 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[4:0] of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte from master – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29 | Stop | 28 | Read = 1 |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave – 8 bits |
| | | 38 | Acknowledge from master |
| | | 39 | Stop |

## Data Byte Configuration Map

**Data Byte 0**

| Bit | Pin# | Name | Description | Power-on Default |
|-----|------|------|-------------|------------------|
| 7 | – | Reserved | Reserved | 0 |
| 6 | – | SEL2 | SW Frequency selection bits. Refer to Frequency Selection Table | 0 |
| 5 | – | SEL1 | SW Frequency selection bits. Refer to Frequency Selection Table | 0 |
| 4 | – | SEL0 | SW Frequency selection bits. Refer to Frequency Selection Table | 0 |
| 3 | – | FS_Override | 0 = Select operating frequency by FS[4:0] input pins<br>1 = Select operating frequency by SEL[4:0] settings | 0 |
| 2 | – | SEL4 | SW Frequency selection bits. Refer to Frequency Selection Table | 0 |
| 1 | – | SEL3 | SW Frequency selection bits. Refer to Frequency Selection Table | 0 |
| 0 | – | Reserved | Reserved | 0 |

**Data Byte 1**

| Bit | Pin# | Name | Description | Power-on Default |
|-----|------|------|-------------|------------------|
| 7 | – | Reserved | Reserved | 0 |
| 6 | – | Spread Select2 | "000" = OFF | 0 |
| 5 | – | Spread Select1 | "001" = Reserved | 0 |
| 4 | – | Spread Select0 | "010" = Reserved<br>'011" = Reserved<br>"100" = ± 0.25%<br>"101" = − 0.5%<br>"110"= ±0.5%<br>"111" = ±0.38% | 0 |
| 3 | 42, 41 | CPUT_CS, CPUC_CS | (Active/Inactive) | 1 |
| 2 | 35, 34 | CPUT_1, CPUC_1 | (Active/Inactive) | 1 |
| 1 | 40, 39 | CPUT_0, CPUC_0 | (Active/Inactive) | 1 |
| 0 | – | CPU_CS_F STOP Control | 1 = CPUT_CS_F and CPUC_CS_F are Free-running outputs<br>0 = CPUT_CS_F and CPUC_CS_F will be disabled when CPU_STOP# is active | 1 |

**Data Byte 2**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | 21 | PCI8 | 1 = Enabled, 0 = Disabled | 1 |
| 6 | 19 | PCI7 | 1 = Enabled, 0 = Disabled | 1 |
| 5 | 18 | PCI6 | 1 = Enabled, 0 = Disabled | 1 |
| 4 | 17 | PCI5 | 1 = Enabled, 0 = Disabled | 1 |
| 3 | 15 | PCI4 | 1 = Enabled, 0 = Disabled | 1 |
| 2 | 14 | PCI3 | 1 = Enabled, 0 = Disabled | 1 |
| 1 | 12 | PCI2 | 1 = Enabled, 0 = Disabled | 1 |
| 0 | 11 | PCI1 | 1 = Enabled, 0 = Disabled | 1 |

**Data Byte 3**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | – | Reserved | Reserved | 0 |

**Data Byte 3**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 6 | 8 | SEL_48MHZ | 0 = 24 MHz<br>1 = 48 MHz | 0 |
| 5 | 7 | 48MHz | 1 = Enabled, 0 = Disabled | 1 |
| 4 | 8 | 24_48MHz | 1 = Enabled, 0 = Disabled | 1 |
| 3 | 10 | PCI_F | 1 = Enabled, 0 = Disabled | 1 |
| 2 | 27 | AGP2 | 1 = Enabled, 0 = Disabled | 1 |
| 1 | 26 | AGP1 | 1 = Enabled, 0 = Disabled | 1 |
| 0 | 23 | AGP0 | 1 = Enabled, 0 = Disabled | 1 |

**Data Byte 4**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | – | PCI_Skew1 | PCI skew control<br>00 = Normal<br>01 = –500 ps<br>10 = Reserved<br>11 = +500 ps | 0 |
| 6 | – | PCI_Skew0 | | 0 |
| 5 | – | WD_TIMER4 | These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled. | 1 |
| 4 | – | WD_TIMER3 | | 1 |
| 3 | – | WD_TIMER2 | | 1 |
| 2 | – | WD_TIMER1 | | 1 |
| 1 | – | WD_TIMER0 | | 1 |
| 0 | – | WD_PRE_SCALER | 0 = 150 ms<br>1 = 2.5 sec | 0 |

**Data Byte 5**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | 7 | 48MHz_DRV | 48-MHz clock output drive strength<br>0 = Normal<br>1 = High Drive | 1 |
| 6 | 8 | 24_48MHz_DRV | 24_48 MHz clock output drive strength<br>0 = Normal<br>1 = High Drive | 1 |
| 5 | 45 | APCI1 | (Active/Inactive) | 1 |
| 4 | 46 | APIC0 | (Active/Inactive) | 1 |
| 3 | – | SW_MULTSEL1 | IREF multiplier<br>00 = Ioh is 4 × IREF<br>01 = Ioh is 5 × IREF<br>10 = Ioh is 6 × IREF<br>11 = Ioh is 7 × IREF | 0 |
| 2 | – | SW_MULTSEL0 | | 0 |
| 1 | 1 | REF | (Active/Inactive) | 1 |
| 0 | – | MULTSEL_Override | This bit control the selection of IREF multipler.<br>0 = HW control; IREF multiplier is determined by MULTSEL1 input pin<br>1 = SW control; IREF multiplier is determined by SW_MULTSEL[0:1] | 0 |

**Data Byte 6**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | – | Reserved | Reserved | 1 |
| 6 | – | Reserved | Reserved | 1 |

**Data Byte 6** (continued)

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 5 | – | Reserved | Reserved | 1 |
| 4 | – | Reserved | Reserved | 1 |
| 3 | – | Reserved | Reserved | 1 |
| 2 | – | Reserved | Reserved | 1 |
| 1 | – | Reserved | Reserved | 1 |
| 0 | – | Reserved | Reserved | 1 |

**Data Byte 7**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 7 | – | Reserved | Reserved | 1 |
| 6 | – | Reserved | Reserved | 1 |
| 5 | – | Reserved | Reserved | 1 |
| 4 | – | Reserved | Reserved | 1 |
| 3 | – | Reserved | Reserved | 1 |
| 2 | – | Reserved | Reserved | 1 |
| 1 | – | Reserved | Reserved | 1 |
| 0 | – | Reserved | Reserved | 1 |

**Data Byte 8**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 7 | – | Revision_ID3 | Revision ID bit[3] | 0 |
| 6 | – | Revision_ID2 | Revision ID bit[2] | 0 |
| 5 | – | Revision_ID1 | Revision ID bit[1] | 0 |
| 4 | – | Revision_ID0 | Revision ID bit[0] | 0 |
| 3 | – | Vendor_ID3 | Bit[3] of Cypress's Vendor ID. This bit is Read-only. | 1 |
| 2 | – | Vendor_ID2 | Bit[2] of Cypress's Vendor ID. This bit is Read-only. | 0 |
| 1 | – | Vendor _ID1 | Bit[1] of Cypress's Vendor ID. This bit is Read-only. | 0 |
| 0 | – | Vendor _ID0 | Bit[0] of Cypress's Vendor ID. This bit is Read-only. | 0 |

**Data Byte 9**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 7 | – | Reserved | Reserved | 0 |
| 6 | – | PCI_DRV | PCI clock output drive strength<br>0 = Low Drive<br>1 = High Drive | 0 |
| 5 | – | AGP_DRV | AGP clock output drive strength<br>0 = Low Drive<br>1 = High Drive | 0 |
| 4 | – | RST_EN_WD | This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs.<br>0 = Disabled<br>1 = Enabled | 0 |
| 3 | – | RST_EN_FC | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled<br>1 = Enabled | 0 |

**Data Byte 9** (continued)

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 2 | – | WD_TO_STATUS | Watchdog Timer Time-out Status Bit<br>0 = No time-out occurs (Read); Ignore (Write)<br>1 = time-out occurred (Read); Clear WD_TO_STATUS (Write) | 0 |
| 1 | – | WD_EN | 0 = Stop and re-load Watchdog timer<br>1 = Enable Watchdog timer. It will start counting down after a frequency change occurs.<br>**Note:**CY28325-3 will generate system reset, re-load a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog timer time-out occurs. Under recovery frequency mode, CY28325-2 will not respond to any attempt to change the output frequency via the SMBus control bytes. System software can unlock the CY28325-3 from its recovery frequency mode by clearing the WD_EN bit. | 0 |
| 0 | – | Reserved | Reserved | 0 |

**Data Byte 10**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | – | CPU_CS_F Skew2 | CPU_CS_F Skew Control | 0 |
| 6 | – | CPU_CS_F Skew1 | 000 = Normal<br>001 = –150 ps | 0 |
| 5 | – | CPU_CS_F Skew0 | 010 = –300 ps<br>011 = –450 ps<br>100 = +150 ps<br>101 = +300 ps<br>110 = +450 ps<br>111 = +600 ps | 0 |
| 4 | – | CPU_Skew2 | CPUT_0:1 and CPUC_0:1 Skew Control | 0 |
| 3 | – | CPU_Skew1 | 000 = Normal<br>001 = –150 ps | 0 |
| 2 | – | CPU_Skew0 | 010 = –300 ps<br>011 = –450 ps<br>100 = +150 ps<br>101 = +300 ps<br>110 = +450 ps<br>111 = +600 ps | 0 |
| 1 | – | AGP_Skew1 | AGP Skew control | 0 |
| 0 | – | AGP_Skew0 | 00 = Normal<br>01 = –150 ps<br>10 = +150 ps<br>11 = +300 ps | 0 |

**Data Byte 11**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|-----------------|------------------|
| 7 | – | ROCV_FREQ_N7 | If ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When FS_Override bit is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0 |
| 6 | – | ROCV_FREQ_N6 | | 0 |
| 5 | – | ROCV_FREQ_N5 | | 0 |
| 4 | – | ROCV_FREQ_N4 | | 0 |
| 3 | – | ROCV_FREQ_N3 | | 0 |
| 2 | – | ROCV_FREQ_N2 | | 0 |
| 1 | – | ROCV_FREQ_N1 | | 0 |
| 0 | – | ROCV_FREQ_N0 | | 0 |

**Data Byte 12**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|----------------|------------------|
| 7 | – | ROCV_FREQ_SEL | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog tImer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0]<br>1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0] | 0 |
| 6 | – | ROCV_FREQ_M6 | If ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be use to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When FS_Override bit is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0 |
| 5 | – | ROCV_FREQ_M5 | | 0 |
| 4 | – | ROCV_FREQ_M4 | | 0 |
| 3 | – | ROCV_FREQ_M3 | | 0 |
| 2 | – | ROCV_FREQ_M2 | | 0 |
| 1 | – | ROCV_FREQ_M1 | | 0 |
| 0 | – | ROCV_FREQ_M0 | | 0 |

**Data Byte 13**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|----------------|------------------|
| 7 | – | CPU_FSEL_N7 | If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0 |
| 6 | – | CPU_FSEL_N6 | | 0 |
| 5 | – | CPU_FSEL_N5 | | 0 |
| 4 | – | CPU_FSEL_N4 | | 0 |
| 3 | – | CPU_FSEL_N3 | | 0 |
| 2 | – | CPU_FSEL_N2 | | 0 |
| 1 | – | CPU_FSEL_N1 | | 0 |
| 0 | – | CPU_FSEL_N0 | | 0 |

**Data Byte 14**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|----------------|------------------|
| 7 | – | Pro_Freq_EN | Programmable output frequencies enabled<br>0 = Disabled<br>1 = Enabled | 0 |
| 6 | – | CPU_FSEL_M6 | If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0 |
| 5 | – | CPU_FSEL_M5 | | 0 |
| 4 | – | CPU_FSEL_M4 | | 0 |
| 3 | – | CPU_FSEL_M3 | | 0 |
| 2 | – | CPU_FSEL_M2 | | 0 |
| 1 | – | CPU_FSEL_M1 | | 0 |
| 0 | – | CPU_FSEL_M0 | | 0 |

**Data Byte 15**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|-----|------|------|----------------|------------------|
| 7 | 1 | Latched FS4 input | Latched FS[4:0] inputs. These bits are Read-only. | X |
| 6 | 7 | Latched FS3 input | | X |
| 5 | 8 | Latched FS2 input | | X |
| 4 | 11 | Latched FS1 input | | X |
| 3 | 10 | Latched FS0 input | | X |

**Data Byte 15**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 2 | – | Reserved | Reserved | 0 |
| 1 | – | Vendor Test Mode | Reserved. Set = 1 | 1 |
| 0 | – | Vendor Test Mode | Reserved. Set = 1 | 1 |

**Data Byte 16**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 7 | – | Reserved | Reserved | 0 |
| 6 | – | Reserved | Reserved | 0 |
| 5 | – | Reserved | Reserved | 0 |
| 4 | – | Reserved | Reserved | 0 |
| 3 | – | Reserved | Reserved | 0 |
| 2 | – | Reserved | Reserved | 0 |
| 1 | – | Reserved | Reserved | 0 |
| 0 | – | Reserved | Reserved | 0 |

**Data Byte 17**

| Bit | Pin# | Name | Pin Description | Power-on Default |
|---|---|---|---|---|
| 7 | – | Reserved | Reserved | 0 |
| 6 | – | Reserved | Reserved | 0 |
| 5 | – | Reserved | Reserved | 0 |
| 4 | – | Reserved | Reserved | 0 |
| 3 | – | Reserved | Reserved | 0 |
| 2 | – | Reserved | Reserved | 0 |
| 1 | – | Reserved | Reserved | 0 |
| 0 | – | Reserved | Reserved | 0 |

**Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency Functional Description**

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or getting unstable. System BIOS or other control software can enable the Watchdog timer before they attempt to make a frequency change. If the system hangs and a Watchdog timer time-out occurs, a system reset will be generated and a recovery frequency will be activated. All the related registers are summarized in the following table.

**Table 5. Register Summary .**

| Name | Description |
|---|---|
| Pro_Freq_EN | Programmable output frequencies enabled<br>0 = Disabled (default).<br>1 = Enabled.<br>When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used. When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs. |

**Table 5.  Register Summary** (continued)**.**

| Name | Description |
|---|---|
| FS_Override | When Pro_Freq_EN is cleared or disabled<br>0 = Select operating frequency by FS input pins (default).<br>1 = Select operating frequency by SEL bits in SMBus control bytes.<br>When Pro_Freq_EN is set or enabled<br>0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default).<br>1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes. |
| CPU_FSEL_N, CPU_FSEL_M | When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block Write to update both registers within the same SMBus bus operation. The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes. |
| ROCV_FREQ_SEL | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0]<br>1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0]. |
| ROCV_FREQ_N[7:0], ROCV_FREQ_M[6:0] | When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block Write to update both registers within the same SMBus bus operation. |
| WD_EN | 0 = Stop and reload Watchdog Timer.<br>1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs. |
| WD_TO_STATUS | Watchdog Timer Time-out Status bit<br>0 = No time-out occurs (Read); Ignore (Write)<br>1 = time-out occurred (Read); Clear WD_TO_STATUS (Write). |
| WD_TIMER[4:0] | These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the pre-scaler is set to 150 ms. If the pre-scaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit. |
| WD_PRE_SCALER | 0 = 150 ms<br>1 = 2.5 sec |
| RST_EN_WD | This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs.<br>0 = Disabled<br>1 = Enabled |
| RST_EN_FC | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled<br>1 = Enabled |

**Program the CPU output frequency**

When the programmable output frequency feature is enabled (Pro_Freq_EN bit is set), the CPU output frequency is determined by the following equation:

$F_{cpu} = G * (N+3)/(M+3)$.

"N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 6*.

The ratio of (N+3) and (M+3) need to be greater than "1" [(N+3)/(M+3) > 1].

The following table lists set of N and M values for different frequency output ranges. This example use a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

**Table 6. Examples of N and M Value for Different CPU Frequency Range**

| Frequency Ranges | Gear Constants | Fixed Value for M-Value Register | Range of N-Value Register for Different CPU Frequency |
|---|---|---|---|
| 50 MHz–129 MHz | 48.00741 | 93 | 97 - 255 |
| 130 MHz–248 MHz | 48.00741 | 45 | 127 - 245 |

## Absolute Maximum Conditions[2]

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $V_{DDC}$, $V_{DDA}$, $V_{DDX}$ | 3.3V Supply Voltage | Maximum functional voltage | −0.5 | 5.5 | V |
| $V_{DDQ}$ | Analog Supply Voltage | Maximum functional voltage | −0.5 | 5.5 | V |
| $V_{IN}$ | Input Voltage | Relative to $V_{SS}$ | −0.5 | $V_{DD}$ + 0.5 | V |
| $T_S$ | Temperature, Storage | Non-functional | −65 | 150 | °C |
| $T_A$ | Temperature, Operating Ambient | Functional | 0 | 70 | °C |
| $T_J$ | Temperature, Junction | Functional | | 150 | °C |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | – | V |
| $\varnothing_{JC}$ | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | 31.03 | | °C/W |
| $\varnothing_{JA}$ | Dissipation, Junction to Ambient | JEDEC (JESD 51) | 77.42 | | °C/W |
| UL–94 | Flammability Rating | At 1/8 in. | V–0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

## Operating Conditions

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD\_REF}$, $V_{DD\_PCI}$, $V_{DD\_AGP}$, $V_{DD\_CPU}$, VDD_48MHz | 3.3V Supply Voltages | 3.135 | 3.465 | V |
| $V_{DD\_CPPU\_CS}$ | CPU_CS Supply Voltage | 2.375 | 2.625 | V |
| $C_{in}$ | Input Pin Capacitance | | 5 | pF |
| $C_{XTAL}$ | XTAL Pin Capacitance | – | 22.5 | pF |
| $C_L$ | Max. Capacitive Load on 24_48MHz, 48 MHz, REF PCI, AGP | – | 20 30 | pF |
| $f_{(REF)}$ | Reference Frequency, Oscillator Nominal Value | 14.318 | 14.318 | MHz |

**Note:**
2. **Multiple Sequence:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## DC Electrical Specifications

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level Input Voltage | Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}$/2 | | 2.4 | – | V |
| $V_{IL}$ | Low-level Input Voltage | Except Crystal Pads | | – | 0.8 | V |
| $V_{OH}$ | High-level Output Voltage | 24_48MHz, 48 MHz, REF, AGP | $I_{OH}$ = –1 mA | 2.4 | – | V |
| | | PCI | $I_{OH}$ = –1 mA | 2.4 | – | V |
| $V_{OL}$ | Low-level Output Voltage | 24_48MHz, 48 MHz, REF, AGP | $I_{OL}$ = 1 mA | – | 0.4 | V |
| | | PCI | $I_{OL}$ = 1 mA | – | 0.55 | V |
| $I_{IH}$ | Input HIGH Current | $0 \leq V_{IN} \leq V_{DD}$ | | –5 | 5 | µA |
| $I_{IL}$ | Input LOW Current | $0 \leq V_{IN} \leq V_{DD}$, except inputs with pull-ups | | –5 | 5 | µA |
| $I_{IPUL}$ | Input LOW Current | $0 \leq V_{IN} \leq V_{DD}$, inputs with pull-ups | | –50 | – | µA |
| $I_{OH}$ | High-level Output Current | CPUT0:1,CPUC0:1 For $I_{OH}$ =6*IRef Configuration | Type X1, $V_{OH}$ = 0.65V | –12.9 | – | mA |
| | | | Type X1, $V_{OH}$ = 0.74V | – | –14.9 | |
| | | REF, 24_48MHz, 48 MHz | Type 3, $V_{OH}$ = 1.00V | –29 | – | |
| | | | Type 3, $V_{OH}$ = 3.135V | – | –23 | |
| | | AGP, PCI | Type 5, $V_{OH}$ = 1.00V | –33 | – | |
| | | | Type 5, $V_{OH}$ = 3.135V | – | –33 | |
| $I_{OL}$ | Low-level Output Current | REF, 24_48MHz, 48 MHz | Type 3, $V_{OL}$ = 1.95V | 29 | – | mA |
| | | | Type 3, $V_{OL}$ = 0.4V | – | 27 | |
| | | AGP, PCI | Type 5, $V_{OL}$ =1.95 V | 30 | – | |
| | | | Type 5, $V_{OL}$ = 0.4V | – | 38 | |
| $I_{DD33}$ | Power Supply Current | 3.3 $V_{DD}$ = 3.465V, | | – | 250 | mA |
| $I_{DD25}$ | Power Supply Current | 2.5 $V_{DD}$ = 2.625V | | – | 75 | mA |
| $I_{DDPD}$ | Shutdown Current | 3.3 $V_{DD}$ = 3.465V | | – | 20 | mA |

## AC Electrical Specifications[3]

| Parameter | Output | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_1$ | 24_48 MHz, 48 MHz, REF, PCI | Output Duty Cycle[4] | Measured at 1.5V | 40 | 60 | % |
| $t_1$ | APIC, AGP | Output Duty Cycle[4] | Measured at 1.5V | 35 | 65 | % |
| $t_1$ | CPUT/C | Output Duty Cycle | Measured at $V_{CROSS}$ | 45 | 55 | % |
| $t_1$ | CPUT/C_CS | Output Duty Cycle | Measured at $V_{CROSS} \leq$ 166MHz | 45 | 55 | % |
| $t_1$ | CPUT/C_CS | Output Duty Cycle | Measured at $V_{CROSS}$ @ 200MHz | 30 | 70 | % |
| $t_2$ | 24_48 MHz, 48 MHz, PCI, PCI_F, REF, AGP | Rising Edge Rate[6] | Between 0.8V and 2.0V | 0.5 | 2.2 | ns |
| $t_2$ | APIC | Rising Edge Rate[6] | Between 0.8V and 2.0V | 0.5 | 2.3 | ns |
| $t_3$ | 24_48 MHz, 48 MHz, PCI, PCI_F, REF, AGP | Falling Edge Rate | Between 2.0V and 0.8V | 0.5 | 2.2 | ns |
| $t_3$ | APIC | Falling Edge Rate[7] | Between 2.0V and 0.8V | 0.5 | 2.3 | ns |
| $t_5$ | AGP[0:2] | AGP-AGP Skew | Measured at 1.5V | – | 300 | ps |
| $t_6$ | PCI | PCI-PCI Skew | Measured at 1.5V | – | 500 | ps |
| $t_9$ | AGP, APIC | Cycle-Cycle Clock Jitter | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$ | – | 500 | ps |
| $t_9$ | 24_48 MHz, 48 MHz | Cycle-Cycle Clock Jitter | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$ | – | 350 | ps |
| $t_9$ | PCI | Cycle-Cycle Clock Jitter | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$ | – | 500 | ps |

## AC Electrical Specifications[3] (continued)

| Parameter | Output | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_9$ | REF | Cycle-Cycle Clock Jitter | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$ | – | 1000 | ps |
| **0.7V CPUT/C, CPU_CS** | | | | | | |
| $t_2$ | CPU | Rise Time | Measured single ended waveform from 0.175V to 0.525V | 0.175 | 1.6 | ns |
| $t_3$ | CPU | Fall Time | Measured single ended waveform from 0.525V to 0.175V | 0.175 | 1.6 | ns |
| $t_4$ | CPU | CPU-CPU Skew | Measured at Crossover | – | 150 | ps |
| $t_8$ | CPU | Cycle-Cycle Clock Jitter | Measured at Crossover $t_8 = t_{8A} - t_{8B}$ With all outputs running | – | 300 | ps |
| | CPU | Rise/Fall Matching | Measured with test loads[5, 6] | – | 20 | % |
| $V_{oh}$ | CPU | High-level Output Voltage including overshoot | Measured with test loads[6] | – | 0.85 | V |
| $V_{ol}$ | CPU | Low-level Output Voltage including undershoot | Measured with test loads[6] | –0.15 | – | V |
| $V_{crossover}$ | CPU | Crossover Voltage | Measured with test loads[6] | 0.28 | 0.43 | V |

## Switching Waveforms

**Duty Cycle Timing**    **(Single-ended Output)**



**Duty Cycle Timing**    **(CPU Differential Output)**
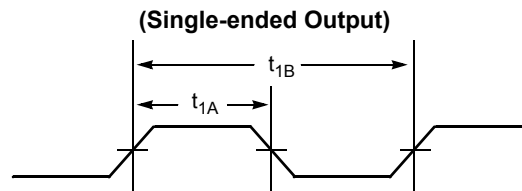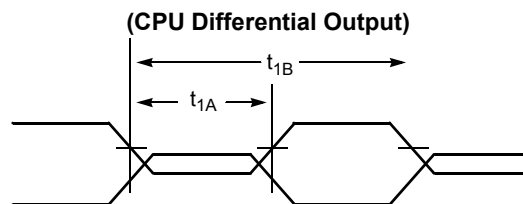


**All Outputs Rise/Fall Time**
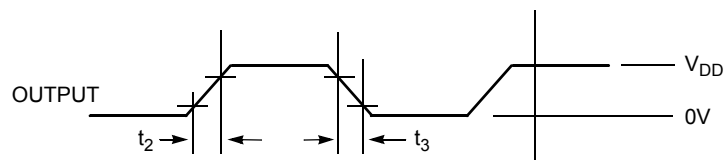


**Notes:**
3. All parameters specified with loaded outputs.
4. Duty cycle is measured at 1.5V when $V_{DD}$ = 3.3V. When $V_{DD}$ = 2.5V, duty cycle is measure at 1.25V.
5. Determined as a fraction of 2*(Trp-Trn)(TRP+Trn) where Trp is a rising edge and Trp is an intersectiong falling edge.
6. The 0.7V test load is $R_S$=33.2ohm, $R_P$ = 49.9ohm in test circuit.
7. Characterize with control register, data byte 9, bits 5 and 6 = 1.

## Switching Waveforms (continued)

**CPU-CPU Clock Skew**
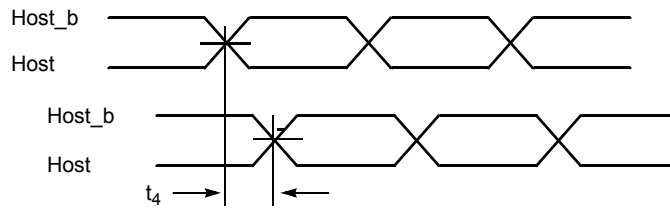
**AGP-AGP Clock Skew**
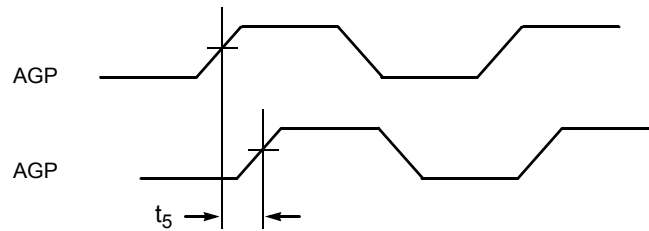
**PCI-PCI Clock Skew**
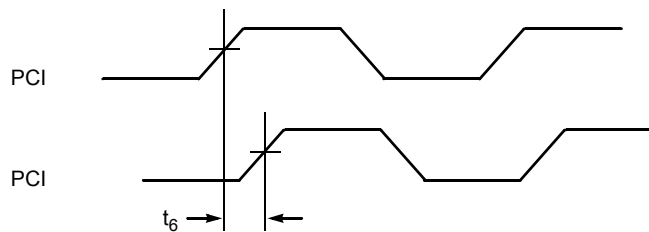
**CPU Clock Cycle-Cycle Jitter**
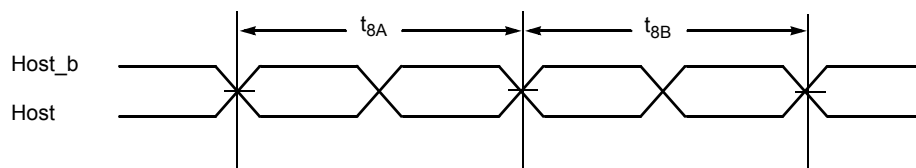
**Cycle-Cycle Clock Jitter**
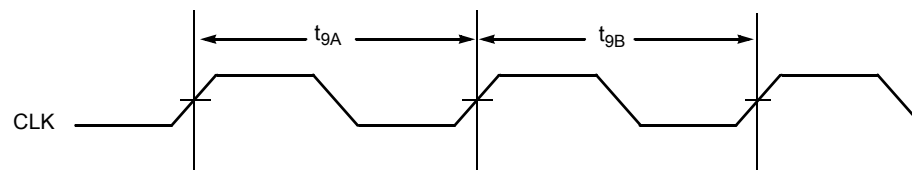
## Ordering Information

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| CY28325OC-3 | 48-pin Shrunk Small Outline Package (SSOP) | Commercial, 0°C to 70°C |
| CY28325OC-3T | 48-pin Shrunk Small Outline Package (SSOP) - Tape and Reel | Commercial, 0°C to 70°C |
| CY28325OXC-3 | 48-pin Shrunk Small Outline Package (SSOP)- Lead Free | Commercial, 0°C to 70°C |
| CY28325OXC-3T | 48-pin Shrunk Small Outline Package (SSOP) - Tape and Reel- Lead Free | Commercial, 0°C to 70°C |

## Package Diagram

**48-lead Shrunk Small Outline Package O48**



DIMENSIONS IN INCHES MIN.
MAX.
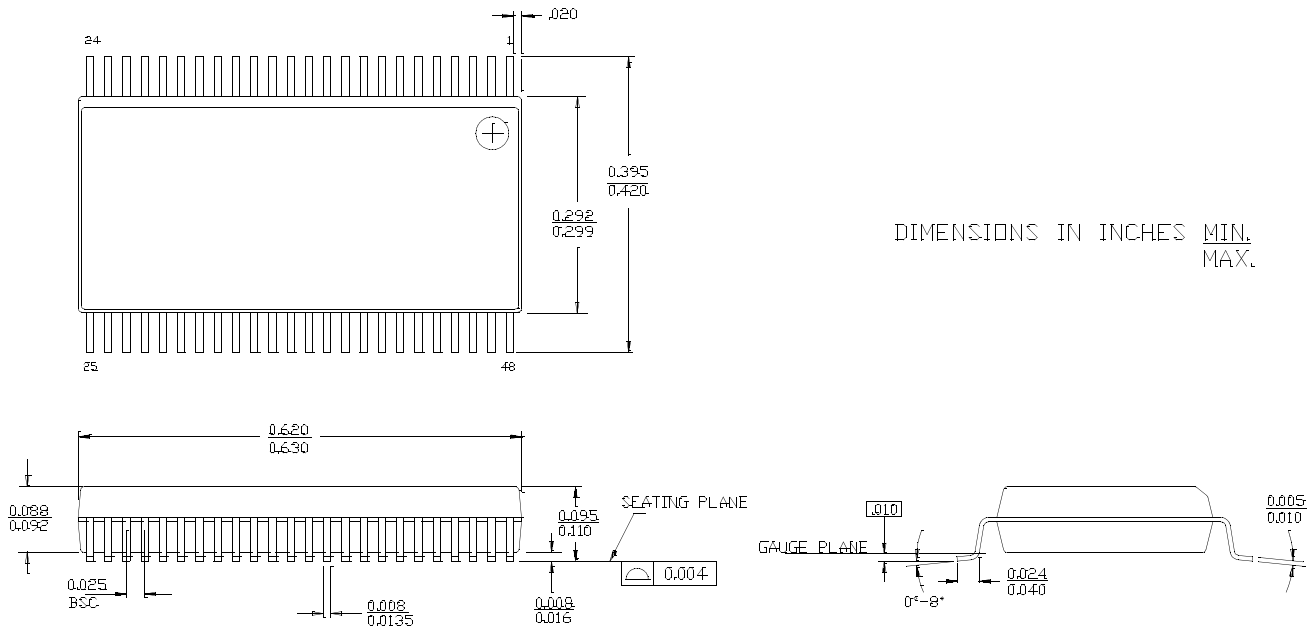
51-85061-*C

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## Document History Page

| Document Title: CY28325-3 FTG for Via Pentium 4® Chipsets<br>Document Number: 38-07590 Rev. *.* | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 224401 | See ECN | RGL | New Datasheet |