Features

- ESD Protect for 8 high-speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±15kV (air), ±12kV (contact)
  IEC 61000-4-5 (Lightning) 5A (8/20μs)
- **For low operating voltage of 3.3V and below**
- **Ultra low capacitance: 0.5pF typical**
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high-speed differential signaling channels
- ***Green Part***

Applications

- **High Definition Multi-Media Interface (HDMI) 1.3, 1.4 and 2.0 version**
- **DisplayPort interface**
- **SATA and eSATA interface**
- **V-By-One**
- **LVDS interfaces**
- **Ethernet port: 10/100/1000 Mb/s**

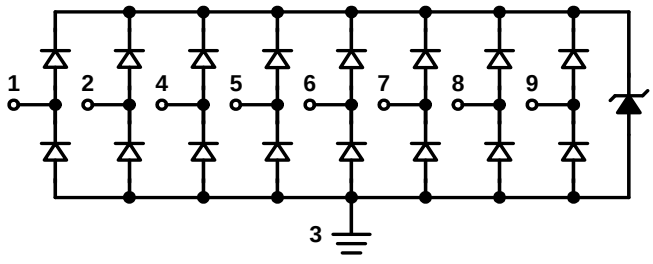
Description

AZ1043-08F is a design which includes ESD rated clamping cell arrays to protect high speed data interfaces. The AZ1043-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

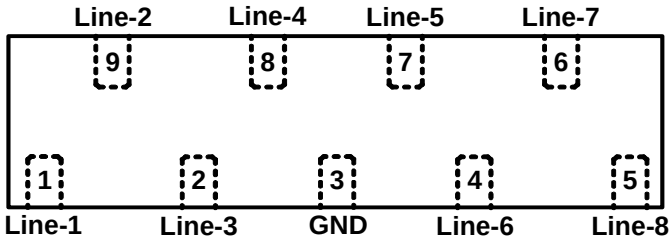
AZ1043-08F is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1043-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN3810P9E
(Top View)

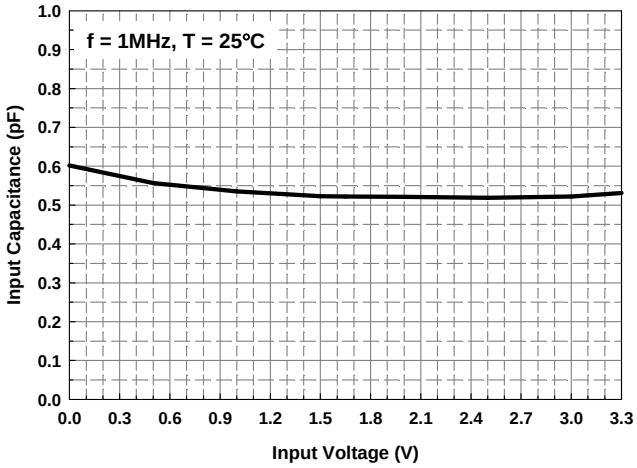
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
Operating Supply Voltage (I/O pin – GND)	V_{DC}	(GND-0.5) to 3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ±12	kV kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

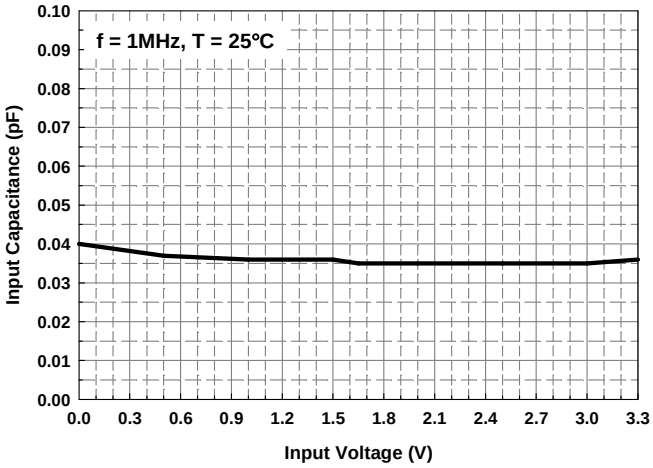
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1, -2, -4, -5, -6, -7, -8, -9 to pin-3, T=25 °C.			3.3	V
Reverse Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5,-6,-7,-8,-9}$ = 3.3V, V_{Pin-3} = 0V, T=25 °C.			1	μA
Reverse DC Breakdown Voltage	V_{BV}	I_{BV} = 1mA, pin-1, -2, -4, -5, -6, -7, -8, -9 to pin-3, T=25 °C.	4.5		7	V
Forward Voltage	V_F	I_F = 15mA, pin-3 to pin-1, -2, -4, -5, -6, -7, -8, -9, T=25 °C.		0.9	1.1	V
ESD Clamping Voltage	V_{ESD_CL}	IEC 61000-4-2 +6kV, Contact mode, any I/O pin to Ground, T=25 °C.		9		V
Channel Input Capacitance	C_{IN}	V_{pin-3} = 0V, V_{IN} = 1.65V, f =1MHz, T=25 °C, any I/O pin to Ground.		0.5	0.65	pF
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin-3} = 0V, V_{IN} = 1.65V, f = 1MHz, T=25 °C, between I/O pins.		0.04	0.08	pF

Typical Characteristics

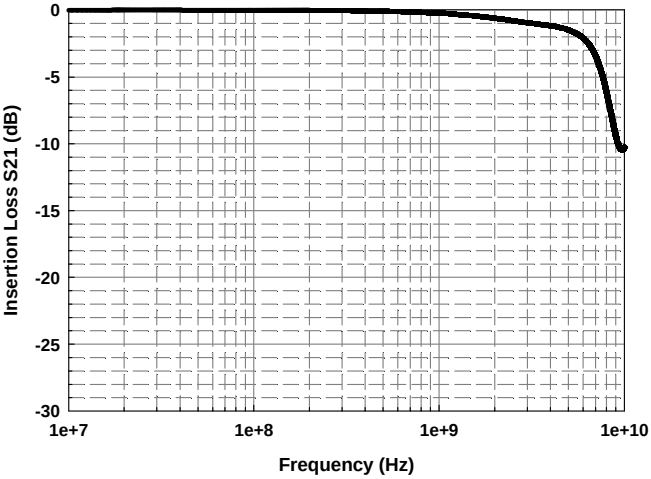
Typical Variation of C_{IN} vs. V_{IN}



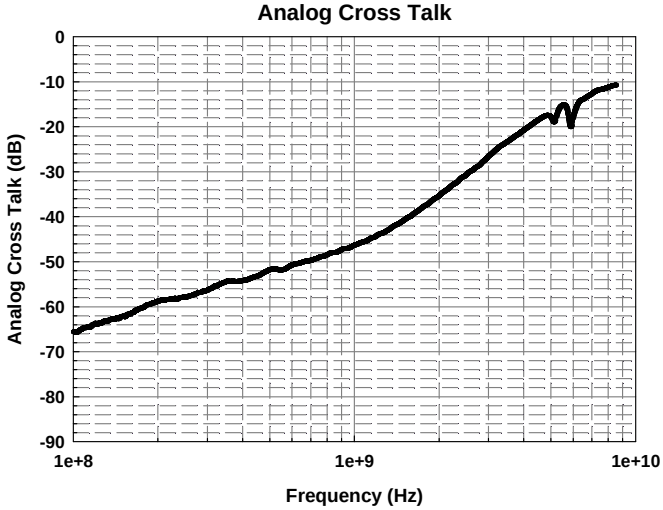
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



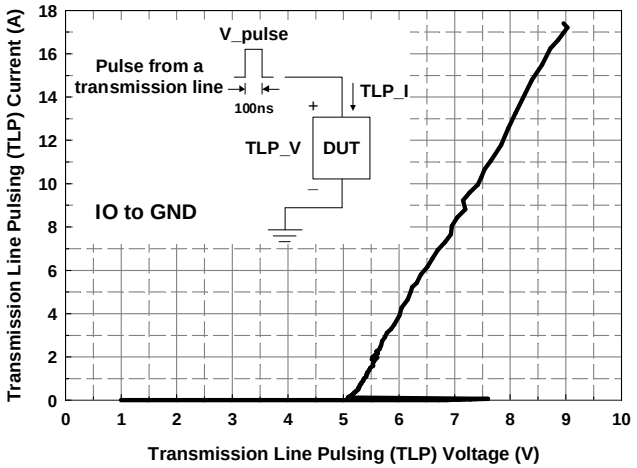
Insertion Loss S21 (I/O-to-GND)



Analog Cross Talk



Transmission Line Pulsing (TLP) Measurement



Applications Information

A. Device Connection

The AZ1043-08F is designed to protect 8 high-speed data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1043-08F is shown in the Fig. 1. In Fig. 1, the 8 protected high-speed data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin6, pin7, pin8, and pin9) of AZ1043-08F. The AZ1043-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. The ground pin (pin3) of AZ1043-08F is a negative reference pin. This pin should be directly connected to the GND rail of PCB. To get minimum parasitic inductance, the path length should keep as short as possible.

AZ1043-08F can provide ESD protection for 8 I/O signal lines simultaneously. If the number of I/O signal lines is less than 8, the unused I/O pins can be simply left as NC pins.

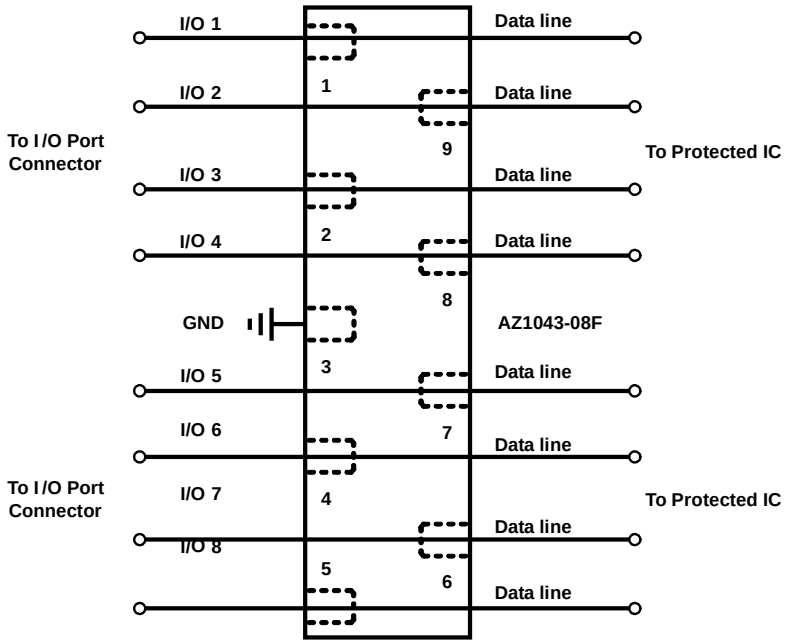


Fig. 1 Data lines connection of AZ1043-08F.

B. Application

AZ1043-08F is designed for protecting high speed I/O ports from over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ1043-08F, especially, the HDMI port.

HDMI Protection for High and Low speed signals

The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%. ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on a HDMI port will cause the impedance of the differential pair to drop. Thus, some form of compensation to the layout will be required to bring the differential pairs back within

the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The AZ1043-08F presents **0.5pF** capacitance to each differential signal while being rated to handle >8kV ESD contact discharges (>15kV air discharge) as outlined in IEC 61000-4-2. Therefore, it is possible to **make none** adjustment to the board layout parameters to compensate for the added capacitance of the AZ1043-08F. Figure 2 shows how to implement the AZ1043-08F in a HDMI application. The AZ1043-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. As shown in Figure 2, the best way to design the PCB trace is using the flow through layout. The solid line represents the PCB trace. The ground pin (pin3) of AZ1043-08F is the negative reference pins. This pin should be directly connected to the GND plane of PCB. To get minimum parasitic inductance, the path length should keep as short as possible. **In Figure 2, the none-TMDS signals, DDC_CLK, DDC_DAT, CE_REMOTE, and HOTPLUG_DET, can be protected with another low cost part, e.g., AZC199-04S.**

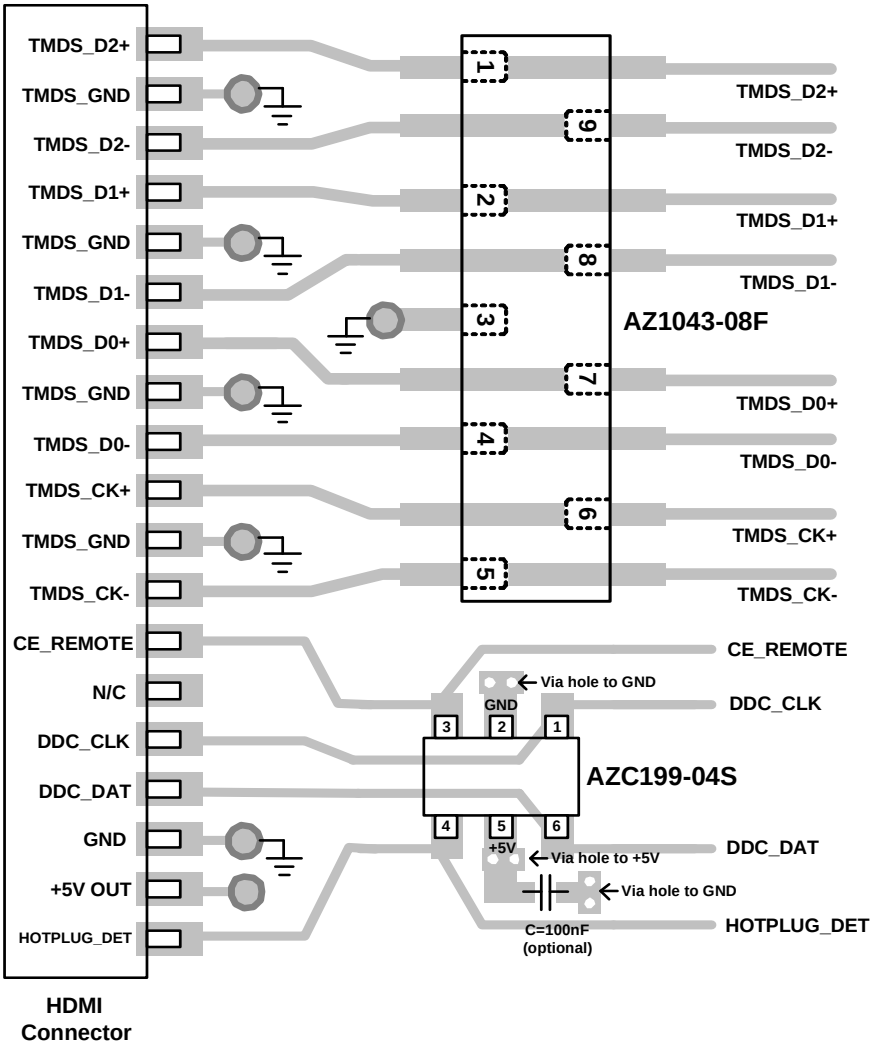
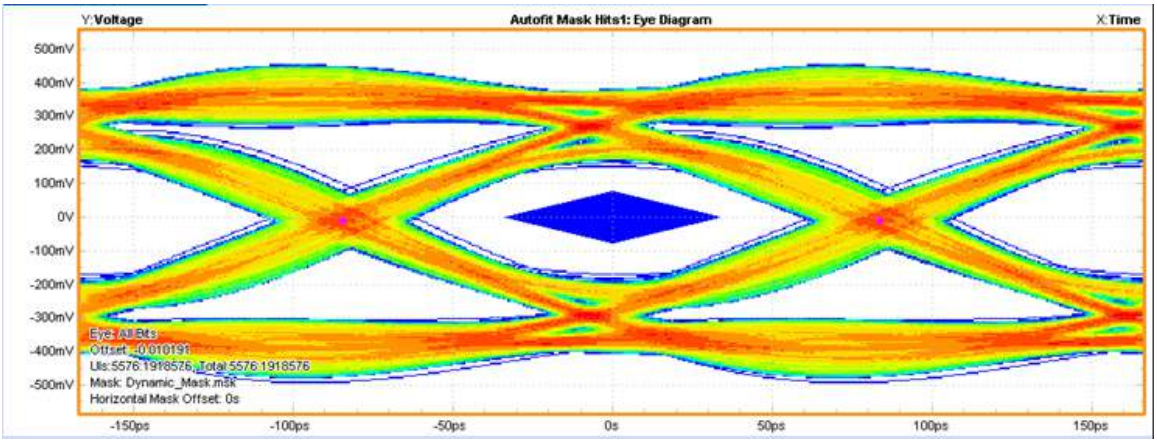
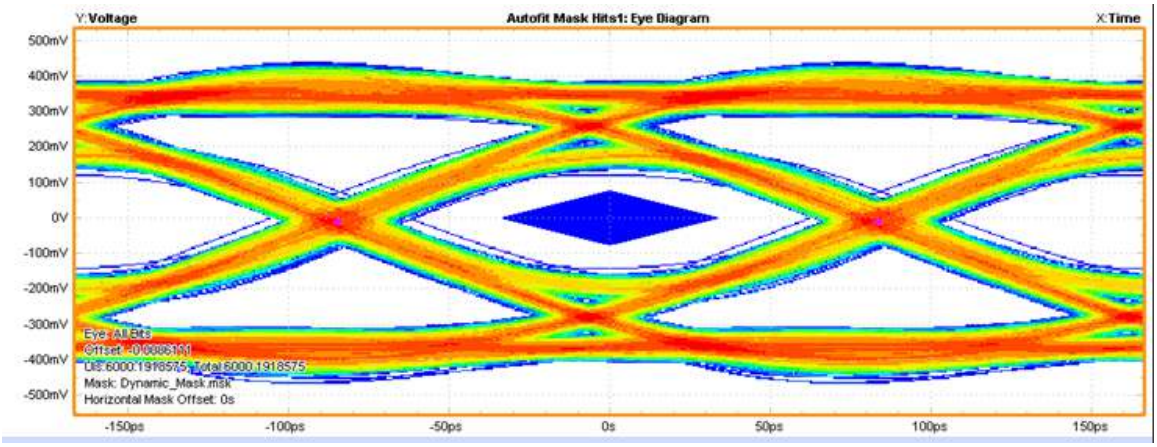


Fig. 2 HDMI Protection for High and Low speed signals.

Fig. 3 shows the HDMI 2.0 (6 Gb/s) eye diagrams with and without AZ1043-08F. Due to ultra low capacitance of AZ1043-08F, no degradation is observed.



Without AZ1043-08F



With AZ1043-08F

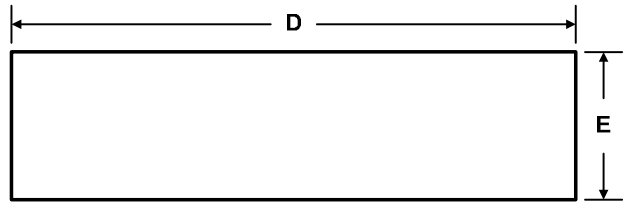
Fig. 3 HDMI 2.0 (6 Gb/s) Eye Diagrams with and without AZ1043-08F.

Mechanical Details

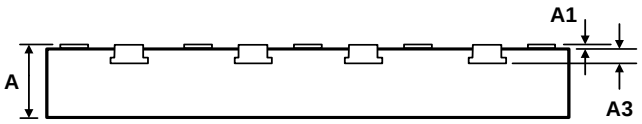
DFN3810P9E

PACKAGE DIAGRAMS

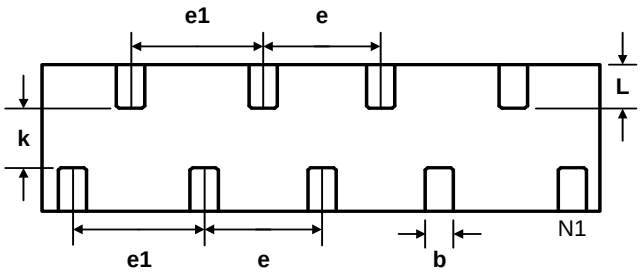
TOP VIEW



SIDE VIEW



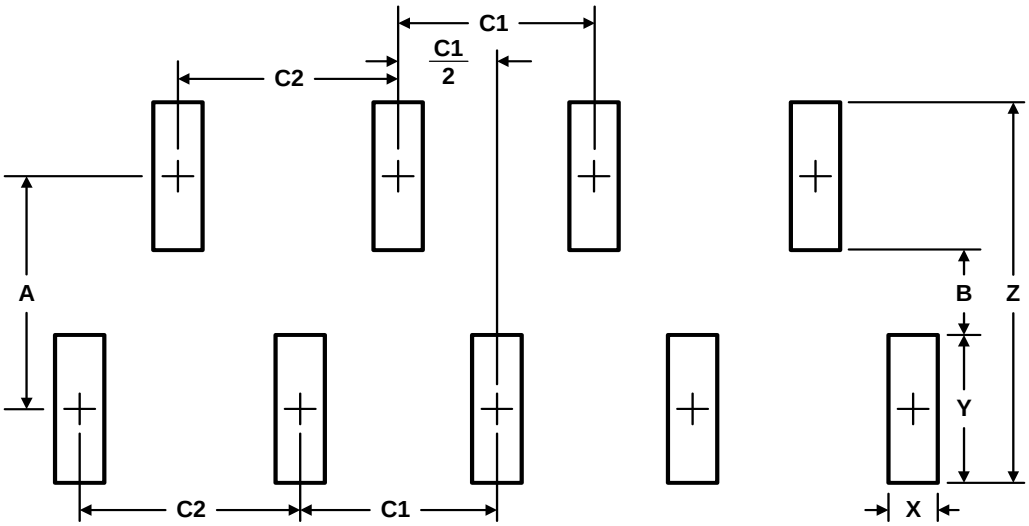
BOTTOM VIEW



PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.110REF.		0.004REF.	
D	3.700	3.900	0.146	0.154
E	0.900	1.100	0.035	0.043
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.800TYP.		0.031TYP.	
e1	0.900TYP.		0.035TYP.	
L	0.250	0.350	0.010	0.014

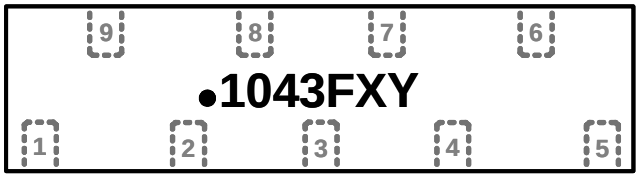
LAND LAYOUT



Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Dimensions	
Index	**Millimeters**
A	0.95
B	0.35
C1	0.80
C2	0.90
X	0.20
Y	0.60
Z	1.55

MARKING CODE



1043F=Device Code
X=Date Code
Y=Control Code

Part Number	Marking Code
AZ1043-08F (Green Part)	**1043F**

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Real Size	MOQ	MOQ / internal box	MOQ / carton
AZ1043-08F.R7G	Green	T/R	7 inch	3,000/reel	3 reel = 9,000/box	6 box = 54,000/carton

Revision History

Revision	Modification Description
Revision 2013/07/30	Preliminary release.
Revision 2014/03/06	Formal release.
Revision 2014/08/07	1. Update the characteristics of Insertion Loss S21 and Analog Cross Talk. 2. Add HDMI 2.0 Eye Diagram.