

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.



ON Semiconductor®

FDD14AN06LA0-F085

N-Channel PowerTrench® MOSFET 60V, 50A, 14.6mΩ

Features

- $r_{DS(ON)} = 12.8m\Omega$ (Typ.), $V_{GS} = 5V$, $I_D = 50A$
- $Q_g(tot) = 25nC$ (Typ.), $V_{GS} = 5V$
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant



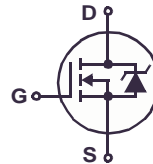
Applications

- Motor / Body Load Control
- ABS Systems
- Powertrain Management
- Injection Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 12V and 24V systems

Formerly developmental type 83557



TO-252AA
FDD SERIES



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C < 100^\circ C$, $V_{GS} = 10V$)	50	A
	Continuous ($T_C < 80^\circ C$, $V_{GS} = 5V$)	50	A
	Continuous ($T_{amb} = 25^\circ C$, $V_{GS} = 5V$, with $R_{\theta JA} = 52^\circ C/W$)	9.5	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	55	mJ
P_D	Power dissipation	125	W
	Derate above $25^\circ C$	0.83	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case TO-252	1.2	$^\circ C/W$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ C/W$

FDD14AN06LA0-F085 N-Channel PowerTrench® MOSFET

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD14AN06LA0	FDD14AN06LA0-F085	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{V}$	-	-	1	μA
		$V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 50\text{A}$, $V_{GS} = 10\text{V}$	-	0.0102	0.0116	Ω
		$I_D = 50\text{A}$, $V_{GS} = 5\text{V}$	-	0.0128	0.0146	
		$I_D = 50\text{A}$, $V_{GS} = 5\text{V}$, $T_J = 175^\circ\text{C}$	-	0.028	0.033	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	2810	-	pF
C_{OSS}	Output Capacitance		-	270	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	115	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V	-	25	32	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V	-	2.7	3.5	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 30\text{V}$ $I_D = 50\text{A}$ $I_g = 1.0\text{mA}$	-	9.7	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	7.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	8.7	-	nC

Switching Characteristics ($V_{GS} = 5\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 30\text{V}$, $I_D = 50\text{A}$ $V_{GS} = 5\text{V}$, $R_{GS} = 5.1\Omega$	-	-	218	ns
$t_{d(ON)}$	Turn-On Delay Time		-	14	-	ns
t_r	Rise Time		-	132	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	27	-	ns
t_f	Fall Time		-	47	-	ns
t_{OFF}	Turn-Off Time		-	-	111	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 50\text{A}$	-	-	1.25	V
		$I_{SD} = 25\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	30	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 50\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	24	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 70\mu\text{H}$, $I_{AS} = 40\text{A}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

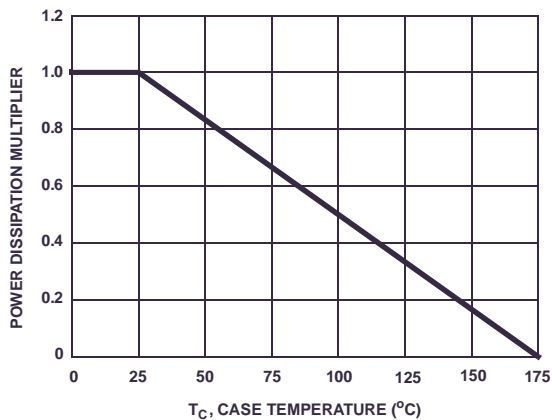


Figure 1. Normalized Power Dissipation vs Ambient Temperature

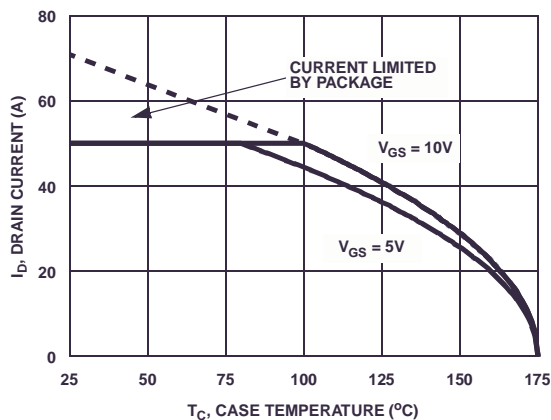


Figure 2. Maximum Continuous Drain Current vs Case Temperature

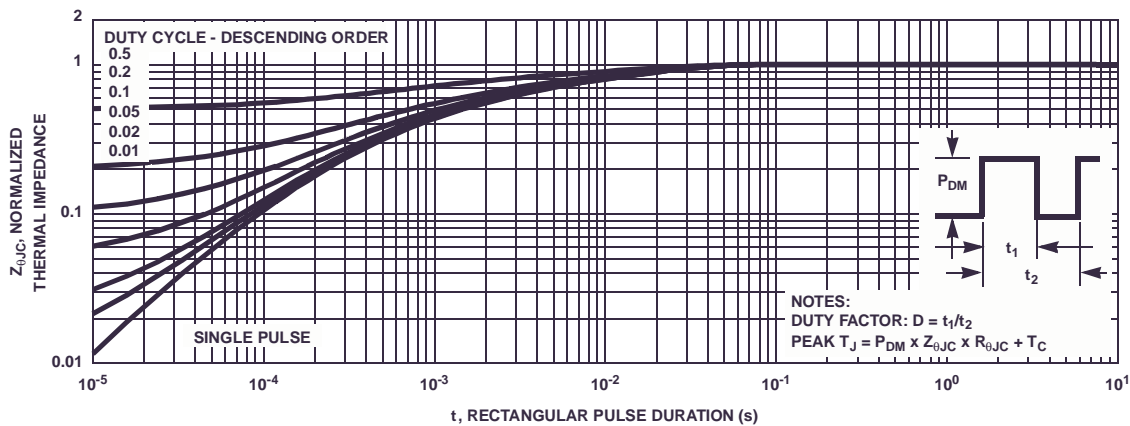


Figure 3. Normalized Maximum Transient Thermal Impedance

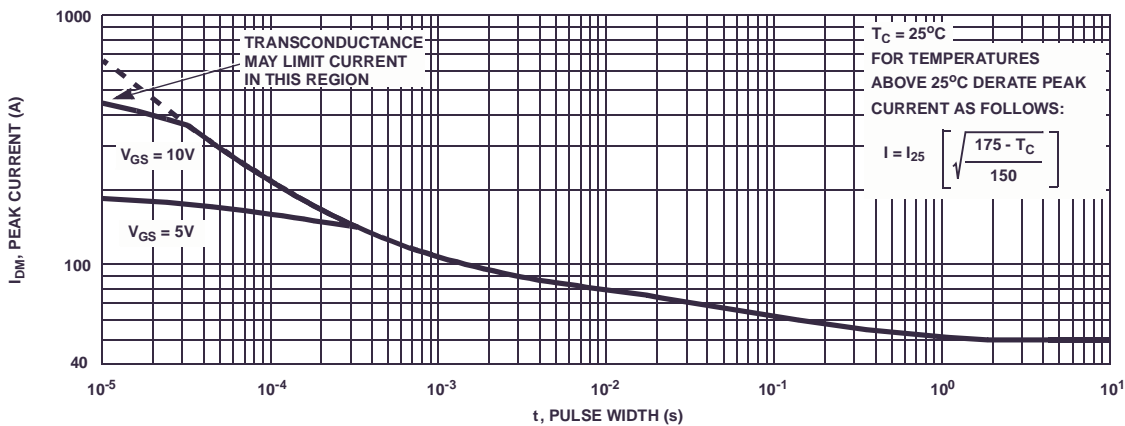


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

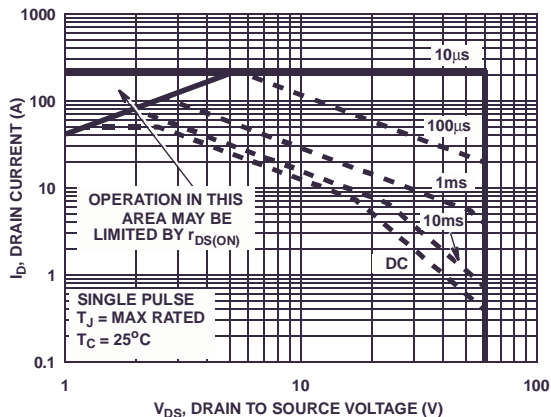
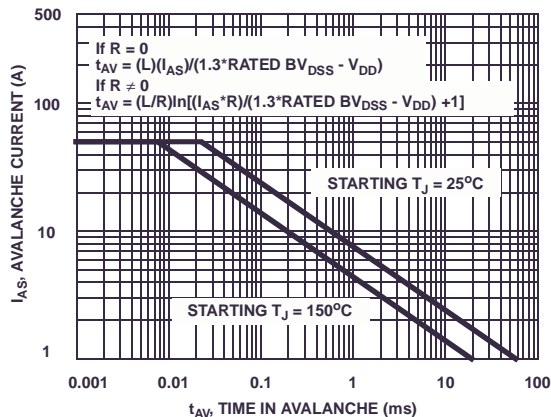


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

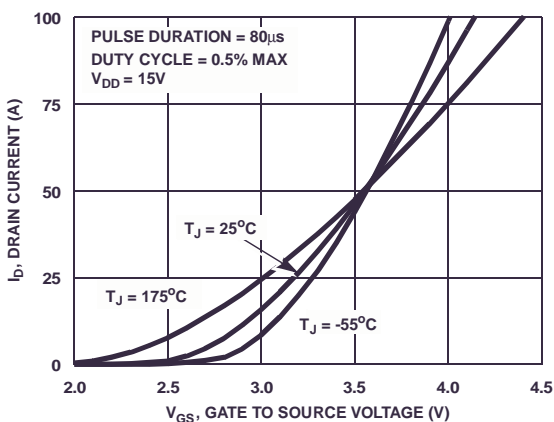


Figure 7. Transfer Characteristics

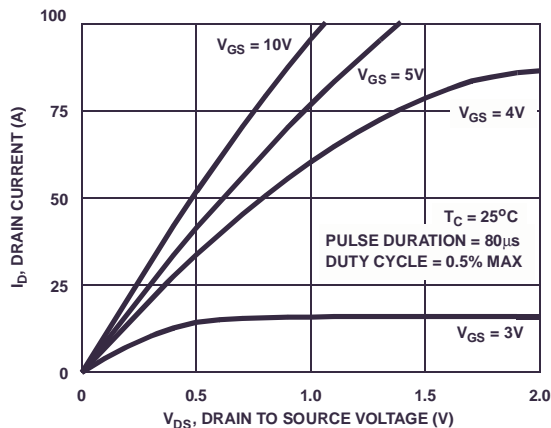


Figure 8. Saturation Characteristics

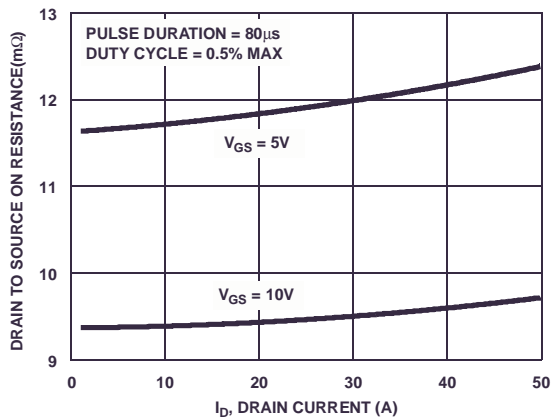


Figure 9. Drain to Source On Resistance vs Drain Current

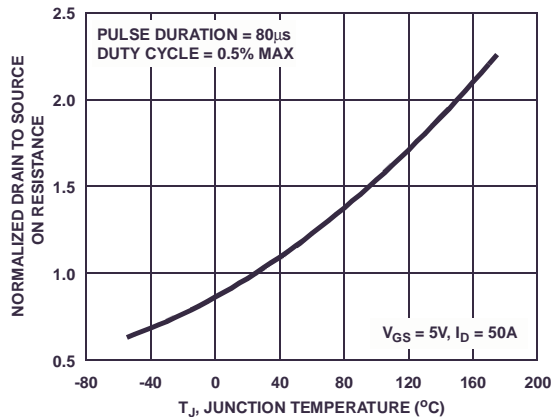


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

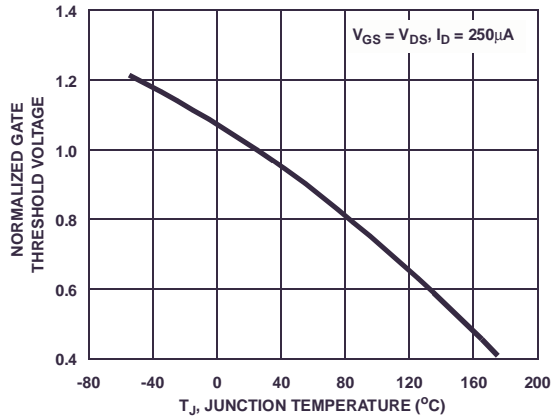


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

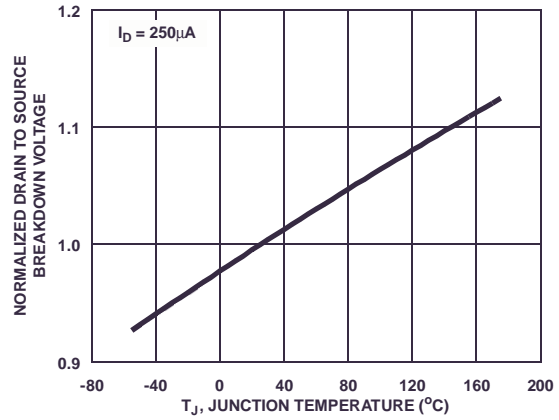


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

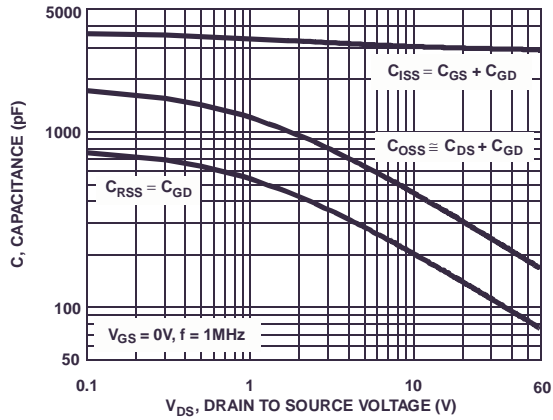


Figure 13. Capacitance vs Drain to Source Voltage

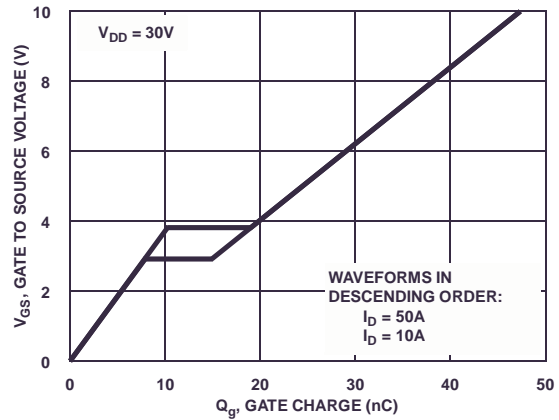


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

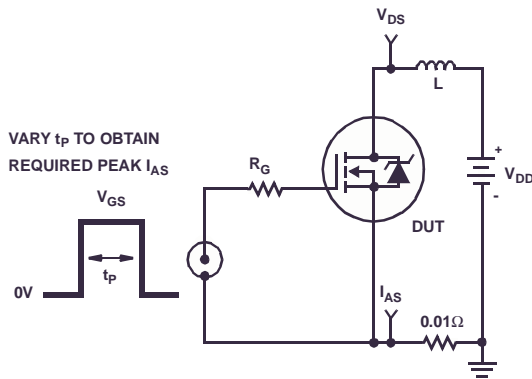


Figure 15. Unclamped Energy Test Circuit

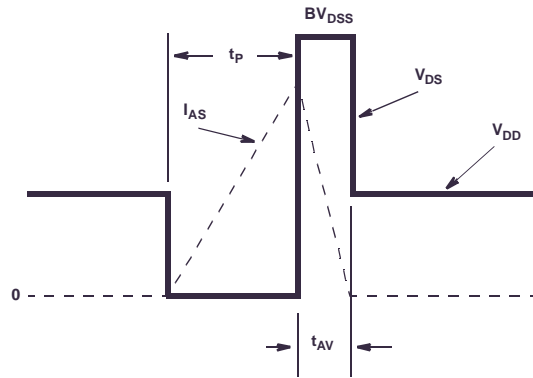


Figure 16. Unclamped Energy Waveforms

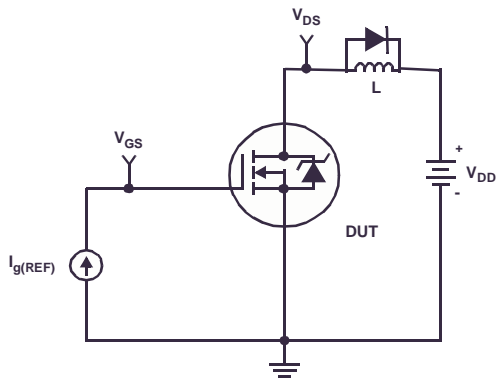


Figure 17. Gate Charge Test Circuit

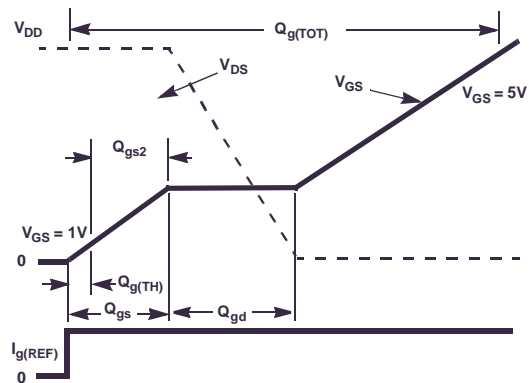


Figure 18. Gate Charge Waveforms

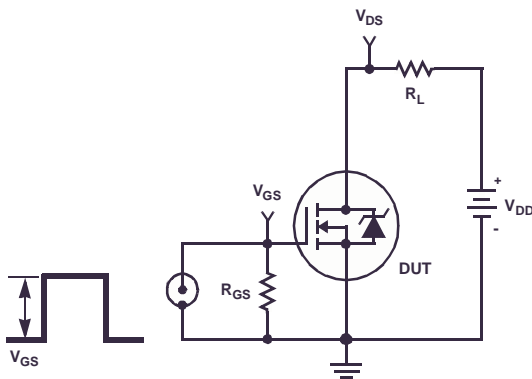


Figure 19. Switching Time Test Circuit

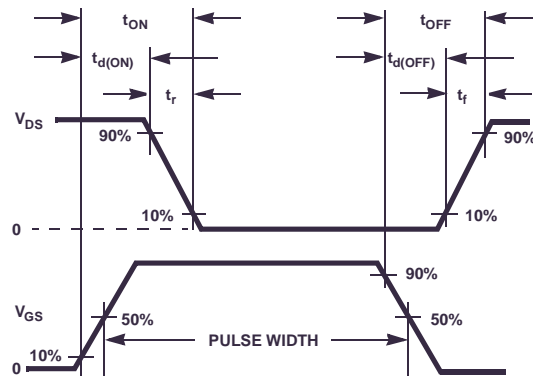


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}C$), and thermal resistance $R_{\theta JA}$ ($^{\circ}C/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the designer's preliminary application evaluation. Figure 21

defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

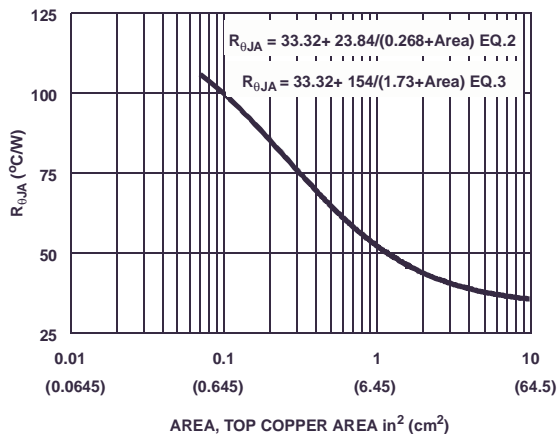


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDD14AN06LA0 2 1 3 ; rev January 2004

Ca 12 8 1.5e-9
Cb 15 14 1.5e-9
Cin 6 8 28.5e-10

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 64.8
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Etemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5e-9
Ldrain 2 5 1.00e-9
Lsource 3 7 2e-9

RLgate 1 9 50
RLdrain 2 5 10
RLsource 3 7 20

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 4.2e-3
Rgate 9 20 2.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 4e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1
ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))/(1e-6*200),3))}}

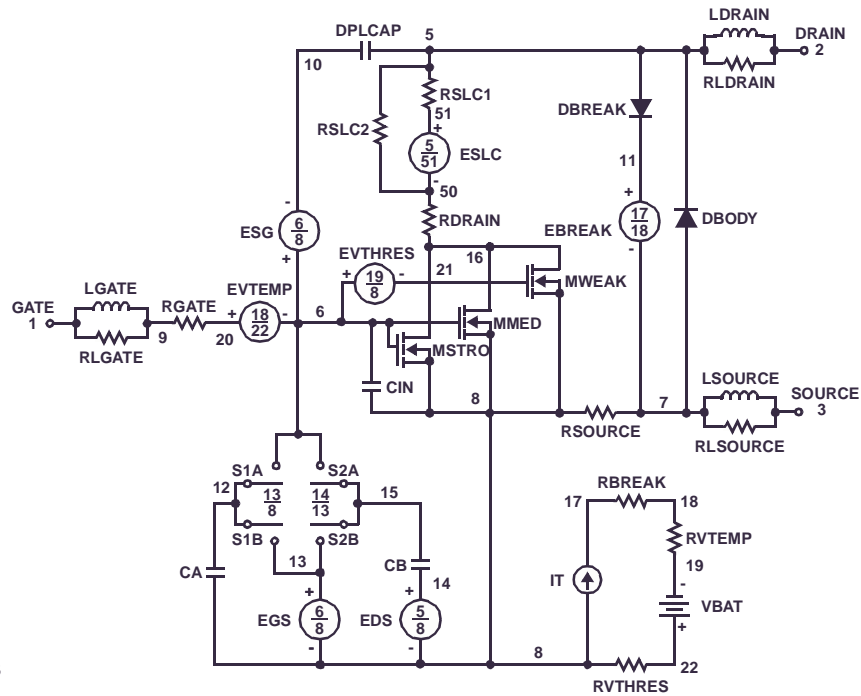
.MODEL DbodyMOD D (IS=15e-12 RS=3.2e-3 N=1.05 TRS1=1.5e-3 TRS2=1e-6
+ CJO=10e-10 TT=1.5e-8 M=0.58 IKF=15.00 XTI=3)
.model dbreakmod d (RS=1e-1 TRS1=1.12e-3 TRS2=1.25e-6)
.MODEL DplcapMOD D (CJO=80e-11 IS=1e-30 N=10 M=0.57)

.MODEL MmedMOD NMOS (VTO=2 KP=8 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.7)
.MODEL MstroMOD NMOS (VTO=2.45 KP=105 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=1.61 KP=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=27 RS=0.1)

.MODEL RbreakMOD RES (TC1=0.92e-3 TC2=-0.35e-6)
.MODEL RdrainMOD RES (TC1=7.92e-3 TC2=3.4e-5)
.MODEL RSLCMOD RES (TC1=2.8E-3 TC2=1E-7)
.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-2.5e-3 TC2=-1e-5)
.MODEL RvtempMOD RES (TC1=-2.3e-3 TC2=1.5e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.5 VOFF=-0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2.5)
.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

REV January 2004

template FDD14AN06LA0 n2,n1,n3

electrical n2,n1,n3

{

var i iscl

dp..model dbodymod = (isl=15e-12,rs=3.2e-3,nl=1.05,trs1=1.5e-3,trs2=1e-6,cjo=10e-10,tt=1.5e-8,m=0.58,ikf=15.00,xti=3)

dp..model dbreakmod = (rs=1e-1,trs1=1.12e-3,trs2=1.25e-6)

dp..model dplcapmod = (cjo=80e-11,isl=10e-30,nl=10,m=0.57)

m..model mmedmod = (type=_n,vto=2,kp=8,is=1e-30,tox=1)

m..model mstrongmod = (type=_n,vto=2.45,kp=105,is=1e-30,tox=1)

m..model mweakmod = (type=_n,vto=1.61,kp=0.04,is=1e-30,tox=1,rs=0.1)

sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3)

sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)

sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2.5,voff=-0.5)

sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2.5)

c.ca n12 n8 = 1.5e-9

c.cb n15 n14 = 1.5e-9

c.cin n6 n8 = 28.5e-10

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 64.8

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5e-9

l.ldrain n2 n5 = 1.00e-9

l.lsource n3 n7 = 2e-9

res.rlgate n1 n9 = 50

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 20

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=0.92e-3,tc2=-0.35e-6

res.rdrain n50 n16 = 4.2e-3, tc1=7.92e-3,tc2=3.4e-5

res.rgate n9 n20 = 2.7

res.rslc1 n5 n51 = 1e-6, tc1=2.8e-3,tc2=1e-7

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 4e-3, tc1=4.0e-3,tc2=1e-6

res.rvthres n22 n8 = 1, tc1=-2.5e-3,tc2=-1e-5

res.rvtemp n18 n19 = 1, tc1=-2.3e-3,tc2=1.5e-6

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

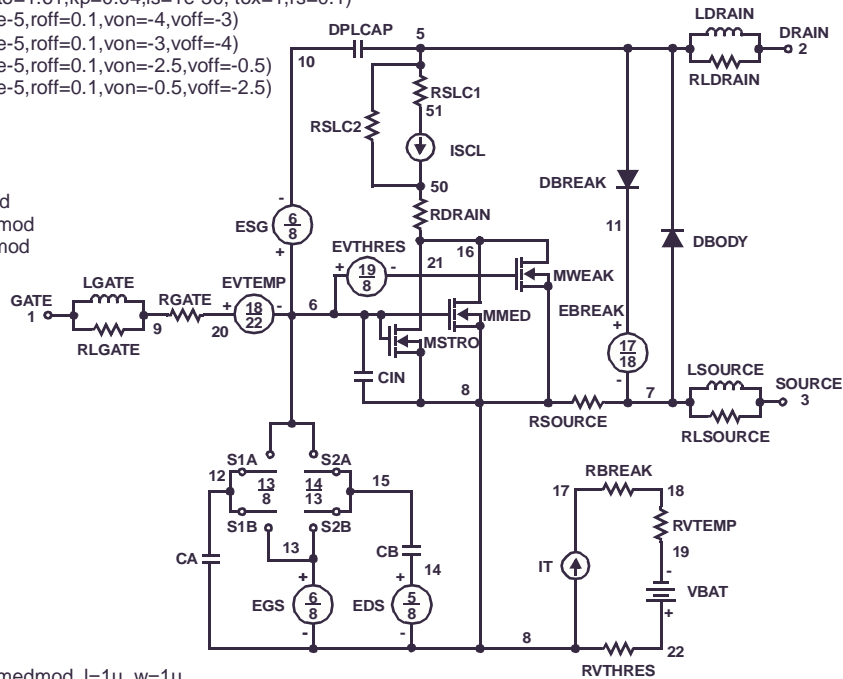
v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = (((n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/200)** 3))

}



SPICE Thermal Model

REV January 2004
FDD14AN06LA0T

CTHERM1 TH 6 2.5e-3
CTHERM2 6 5 3e-3
CTHERM3 5 4 4e-3
CTHERM4 4 3 7e-3
CTHERM5 3 2 8.2e-3
CTHERM6 2 TL 5e-2

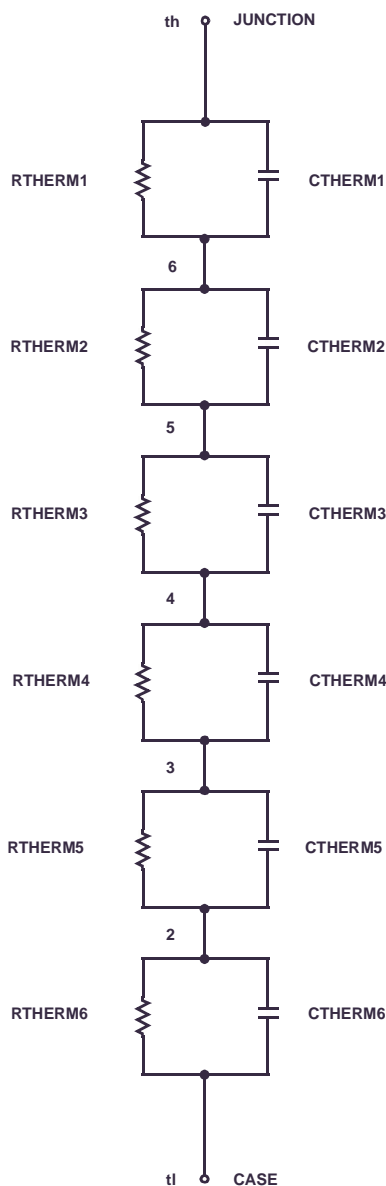
RTHERM1 TH 6 4.2e-2
RTHERM2 6 5 8.4e-2
RTHERM3 5 4 1.04e-1
RTHERM4 4 3 1.14e-1
RTHERM5 3 2 2.74e-1
RTHERM6 2 TL 3.44e-1


SABER Thermal Model

SABER thermal model FDD14AN06LA0T
template thermal_model th tl
thermal_c th, tl

```
{
  ctherm.ctherm1 th 6 =2.5e-3
  ctherm.ctherm2 6 5 =3e-3
  ctherm.ctherm3 5 4 =4e-3
  ctherm.ctherm4 4 3 =7e-3
  ctherm.ctherm5 3 2 =8.2e-3
  ctherm.ctherm6 2 tl =5e-2
```

```
rtherm.rtherm1 th 6 =4.2e-2
rtherm.rtherm2 6 5 =8.4e-2
rtherm.rtherm3 5 4 =1.04e-1
rtherm.rtherm4 4 3 =1.14e-1
rtherm.rtherm5 3 2 =2.74e-1
rtherm.rtherm6 2 tl =3.44e-1
}
```



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative