TigerSHARC Embedded Processor

ADSP-TS203S

KEY FEATURES

- 500 MHz, 2.0 ns instruction cycle rate
- 4M bits of internal—on-chip—DRAM memory
- 25 mm × 25 mm (576-ball) thermally enhanced ball grid array package
- Dual-computation blocks—each containing an ALU, a multiplier, a shifter, and a register file
- Dual-integer ALUs, providing data addressing and pointer manipulation
- Single-precision IEEE 32-bit and extended-precision 40-bit floating-point data formats and 8-, 16-, 32-, and 64-bit fixed-point data formats
- Integrated I/O includes 10-channel DMA controller, external port, two link ports, SDRAM controller, programmable flag pins, two timers, and timer expired pin for system integration
- 1149.1 IEEE-compliant JTAG test access port for on-chip emulation
- On-chip arbitration for glueless multiprocessing

KEY BENEFITS

- Provides high performance static superscalar DSP operations, optimized for large, demanding multiprocessor DSP applications
- Performs exceptionally well on DSP algorithm and I/O benchmarks (see benchmarks in Table 1)
- Supports low overhead DMA transfers between internal memory, external memory, memory-mapped peripherals, link ports, host processors, and other (multiprocessor) DSPs
- Eases programming through extremely flexible instruction set and high-level-language-friendly architecture
- Enables scalable multiprocessing systems with low communications overhead

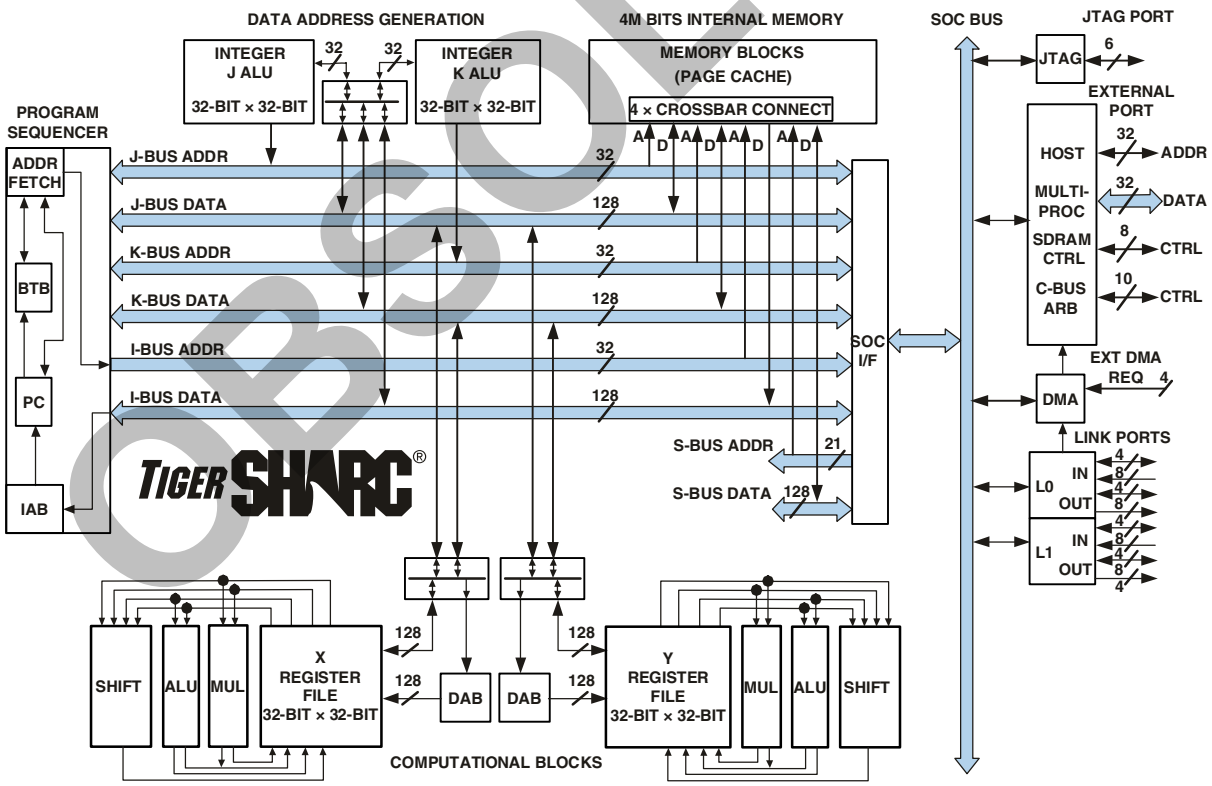

Figure 1. Functional Block Diagram

Rev. D

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REVISION HISTORY

5/12—Rev. C to Rev. D

Added model to Ordering Guide 47

GENERAL DESCRIPTION

The ADSP-TS203S TigerSHARC processor is an ultrahigh performance, static superscalar processor optimized for large signal processing tasks and communications infrastructure. The processor combines very wide memory widths with dual computation blocks—supporting floating-point (IEEE 32-bit and extended precision 40-bit) and fixed-point (8-, 16-, 32-, and 64-bit) processing—to set a new standard of performance for digital signal processors. The TigerSHARC static superscalar architecture lets the processor execute up to four instructions each cycle, performing 24 fixed-point (16-bit) operations or six floating-point operations.

Four independent 128-bit wide internal data buses, each connecting to the four 1M bit memory banks, enable quad-word data, instruction, and I/O access and provide 28G bytes per second of internal memory bandwidth. Operating at 500 MHz, the ADSP-TS203S processor's core has a 2.0 ns instruction cycle time. Using its single-instruction, multiple-data (SIMD) features, the processor can perform four billion 40-bit MACS or one billion 80-bit MACS per second. Table 1 shows the processor's performance benchmarks.

Table 1. General-Purpose Algorithm Benchmarks at 500 MHz

Benchmark	Speed	Clock Cycles
32-bit algorithm, 1 billion MACS/s peak performance		
1K point complex FFT[1] (Radix 2)	18.8 µs	9419 13975
64K point complex FFT[1] (Radix 2)	2.8 ms	44
FIR filter (per real tap)	1 ns	0.5
[8 8][8 8] matrix multiply (complex, floating-point)	2.8 µs	1399
16-bit algorithm, 4 billion MACS/s peak performance		
256 point complex FFT[1] (Radix 2)	1.9 µs	928
I/O DMA transfer rate		
External port	500M bytes/s	n/a
Link ports (each)	500M bytes/s	n/a

[1] Cache preloaded.

The ADSP-TS203S processor is code compatible with the other TigerSHARC processors.

The Functional Block Diagram on Page 1 shows the processor's architectural blocks. These blocks include

- Dual compute blocks, each consisting of an ALU, multiplier, 64-bit shifter, and 32-word register file and associated data alignment buffers (DABs)
- Dual integer ALUs (IALUs), each with its own 31-word register file for data addressing and a status register
- A program sequencer with instruction alignment buffer (IAB) and branch target buffer (BTB)
- An interrupt controller that supports hardware and software interrupts, supports level- or edge-triggers, and supports prioritized, nested interrupts
- Four 128-bit internal data buses, each connecting to the four 1M-bit memory banks
- On-chip DRAM (4M-bit)
- An external port that provides the interface to host processors, multiprocessing space (DSPs), off-chip memory-mapped peripherals, and external SRAM and SDRAM
- A 10-channel DMA controller
- Two full-duplex LVDS link ports
- Two 64-bit interval timers and timer expired pin
- An 1149.1 IEEE-compliant JTAG test access port for on-chip emulation

The TigerSHARC uses a Static Superscalar™* architecture. This architecture is superscalar in that the ADSP-TS203S processor's core can execute simultaneously from one to four 32-bit instructions encoded in a very large instruction word (VLIW) instruction line using the processor's dual compute blocks. Because the processor does not perform instruction reordering at runtime—the programmer selects which operations will execute in parallel prior to runtime—the order of instructions is static.

With few exceptions, an instruction line, whether it contains one, two, three, or four 32-bit instructions, executes with a throughput of one cycle in a 10-deep processor pipeline.

For optimal processor program execution, programmers must follow the processor's set of instruction parallelism rules when encoding an instruction line. In general, the selection of instructions that the processor can execute in parallel each cycle depends both on the instruction line resources each instruction requires and on the source and destination registers used in the instructions. The programmer has direct control of three core components—the IALUs, the compute blocks, and the program sequencer.

The ADSP-TS203S processor, in most cases, has a two-cycle execution pipeline that is fully interlocked, so—whenever a computation result is unavailable for another operation dependent on it—the processor automatically inserts one or more stall cycles as needed. Efficient programming with dependency-free instructions can eliminate most computational and memory transfer data dependencies.

In addition, the processor supports SIMD operations two ways—SIMD compute blocks and SIMD computations. The programmer can load both compute blocks with the same data (broadcast distribution) or different data (merged distribution).

* Static Superscalar is a trademark of Analog Devices, Inc.

DUAL COMPUTE BLOCKS

The ADSP-TS203S processor has compute blocks that can execute computations either independently or together as a single-instruction, multiple-data (SIMD) engine. The processor can issue up to two compute instructions per compute block each cycle, instructing the ALU, multiplier, or shifter to perform independent, simultaneous operations. Each compute block can execute eight 8-bit, four 16-bit, two 32-bit, or one 64-bit SIMD computations in parallel with the operation in the other block. These computation units support IEEE 32-bit single-precision floating-point, extended-precision 40-bit floating point, and 8-, 16-, 32-, and 64-bit fixed-point processing.

The compute blocks are referred to as X and Y in assembly syntax, and each block contains three computational units—an ALU, a multiplier, a 64-bit shifter—and a 32-word register file.

- Register File—each compute block has a multiported 32-word, fully orthogonal register file used for transferring data between the computation units and data buses and for storing intermediate results. Instructions can access the registers in the register file individually (word-aligned), in sets of two (dual-aligned), or in sets of four (quad-aligned).
- ALU—the ALU performs a standard set of arithmetic operations in both fixed- and floating-point formats. It also performs logic and permute operations.
- Multiplier—the multiplier performs both fixed- and floating-point multiplication and fixed-point multiply and accumulate.
- Shifter—the 64-bit shifter performs logical and arithmetic shifts, bit and bit stream manipulation, and field deposit and extraction operations.

Using these features, the compute blocks can

- Provide 8 MACS per cycle peak and 7.1 MACS per cycle sustained 16-bit performance and provide 2 MACS per cycle peak and 1.8 MACS per cycle sustained 32-bit performance (based on FIR)
- Execute six single-precision floating-point or execute 24 fixed-point (16-bit) operations per cycle, providing 3G FLOPS or 12.0G/s regular operations performance at 500 MHz
- Perform two complex 16-bit MACS per cycle

DATA ALIGNMENT BUFFER (DAB)

The DAB is a quad-word FIFO that enables loading of quad-word data from nonaligned addresses. Normally, load instructions must be aligned to their data size so that quad words are loaded from a quad-aligned address. Using the DAB significantly improves the efficiency of some applications, such as FIR filters.

DUAL INTEGER ALU (IALU)

The processor has two IALUs that provide powerful address generation capabilities and perform many general-purpose integer operations. The IALUs are referred to as J and K in assembly syntax and have the following features:

- Provide memory addresses for data and update pointers
- Support circular buffering and bit-reverse addressing
- Perform general-purpose integer operations, increasing programming flexibility
- Include a 31-word register file for each IALU

As address generators, the IALUs perform immediate or indirect (pre- and post-modify) addressing. They perform modulus and bit-reverse operations with no constraints placed on memory addresses for the modulus data buffer placement. Each IALU can specify either a single-, dual-, or quad-word access from memory.

The IALUs have hardware support for circular buffers, bit reverse, and zero-overhead looping. Circular buffers facilitate efficient programming of delay lines and other data structures required in digital signal processing, and they are commonly used in digital filters and Fourier transforms. Each IALU provides registers for four circular buffers, so applications can set up a total of eight circular buffers. The IALUs handle address pointer wraparound automatically, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Because the IALU's computational pipeline is one cycle deep, in most cases integer results are available in the next cycle. Hardware (register dependency check) causes a stall if a result is unavailable in a given cycle.

PROGRAM SEQUENCER

The ADSP-TS203S processor's program sequencer supports:

- A fully interruptible programming model with flexible programming in assembly and C/C++ languages; handles hardware interrupts with high throughput and no aborted instruction cycles
- A 10-cycle instruction pipeline—four-cycle fetch pipe and six-cycle execution pipe—computation results available two cycles after operands are available
- Supply of instruction fetch memory addresses; the sequencer's instruction alignment buffer (IAB) caches up to five fetched instruction lines waiting to execute; the program sequencer extracts an instruction line from the IAB and distributes it to the appropriate core component for execution
- Management of program structures and program flow determined according to JUMP, CALL, RTI, RTS instructions, loop structures, conditions, interrupts, and software exceptions
- Branch prediction and a 128-entry branch target buffer (BTB) to reduce branch delays for efficient execution of conditional and unconditional branch instructions and zero-overhead looping; correctly predicted branches occur with zero overhead cycles, overcoming the five-to-nine stage branch penalty
- Compact code without the requirement to align code in memory; the IAB handles alignment

Interrupt Controller

The processor supports nested and nonnested interrupts. Each interrupt type has a register in the interrupt vector table. Also, each has a bit in both the interrupt latch register and the interrupt mask register. All interrupts are fixed as either level-sensitive or edge-sensitive, except the $\overline{\text{IRQ3–0}}$ hardware interrupts, which are programmable.

The processor distinguishes between hardware interrupts and software exceptions, handling them differently. When a software exception occurs, the processor aborts all other instructions in the instruction pipe. When a hardware interrupt occurs, the processor continues to execute instructions already in the instruction pipe.

Flexible Instruction Set

The 128-bit instruction line, which can contain up to four 32-bit instructions, accommodates a variety of parallel operations for concise programming. For example, one instruction line can direct the processor to conditionally execute a multiply, an add, and a subtract in both computation blocks while it also branches to another location in the program. Some key features of the instruction set include:

- Algebraic assembly language syntax
- Direct support for all DSP, imaging, and video arithmetic types
- Eliminates toggling hardware modes because modes are supported as options (for example, rounding, saturation, and others) within instructions
- Branch prediction encoded in instruction; enables zero-overhead loops
- Parallelism encoded in instruction line
- Conditional execution optional for all instructions
- User-defined partitioning between program and data memory

MEMORY

The processor's internal and external memory is organized into a unified memory map, which defines the location (address) of all elements in the system, as shown in Figure 2.

The memory map is divided into four memory areas—host space, external memory, multiprocessor space, and internal memory—and each memory space, except host memory, is subdivided into smaller memory spaces.

The ADSP-TS203S processor internal memory has 4M bits of on-chip DRAM memory, divided into four blocks of 1M bits (32K words 32 bits). Each block—M0, M2, M4, and M6—can store program instructions, data, or both, so applications can configure memory to suit specific needs. Placing program instructions and data in different memory blocks, however, enables the processor to access data while performing an instruction fetch. Each memory segment contains a 128K bit cache to enable single-cycle accesses to internal DRAM.

The four internal memory blocks connect to the four 128-bit wide internal buses through a crossbar connection, enabling the processor to perform four memory transfers in the same cycle. The processor's internal bus architecture provides a total memory bandwidth of 28G bytes per second, allowing the core and I/O to access eight 32-bit data-words and four 32-bit instructions each cycle. Additional features are:

- Processor core and I/O access to different memory blocks in the same cycle
- Processor core access to three memory blocks in parallel—one instruction and two data accesses
- Programmable partitioning of program and data memory
- Program access of all memory as 32-, 64-, or 128-bit words—16-bit words with the DAB

EXTERNAL PORT (OFF-CHIP MEMORY/PERIPHERALS INTERFACE)

The ADSP-TS203S processor's external port provides the processor's interface to off-chip memory and peripherals. The 4G word address space is included in the processor's unified address space. The separate on-chip buses—four 128-bit data buses and four 32-bit address buses—are multiplexed at the SOC interface and transferred to the external port over the SOC bus to create an external system bus transaction. The external system bus provides a single 32-bit data bus and a single 32-bit address bus. The external port supports data transfer rates of 500M bytes per second over the external bus.

The external bus is configured for 32-bit, little-endian operations. Unlike the ADSP-TS201, the ADSP-TS203S processor's external port cannot support 64-bit operations; the external bus width control bits (Bits 21-19) must = 0 in the SYSCON register—all other values are illegal for the ADSP-TS203S. Because the external port is restricted to 32 bits on the ADSP-TS203S processor, there are a number of pinout differences between the ADSP-TS203S and the ADSP-TS201 processors.

The external port supports pipelined, slow, and SDRAM protocols. Addressing of external memory devices and memory-mapped peripherals is facilitated by on-chip decoding of high order address lines to generate memory bank select signals.

The ADSP-TS203S processor provides programmable memory, pipeline depth, and idle cycle for synchronous accesses, and external acknowledge controls to interface to pipelined or slow devices, host processors, and other memory-mapped peripherals with variable access, hold, and disable time requirements.

Host Interface

The ADSP-TS203S processor provides an easy and configurable interface between its external bus and host processors through the external port. To accommodate a variety of host processors, the host interface supports pipelined or slow protocols for processor access of the host as slave or pipelined for host access of the ADSP-TS203S processor as slave. Each protocol has programmable transmission parameters, such as idle cycles, pipe depth, and internal wait cycles.

The host interface supports burst transactions initiated by a host processor. After the host issues the starting address of the burst and asserts the $\overline{\text{BRST}}$ signal, the processor increments the address internally while the host continues to assert $\overline{\text{BRST}}$.

The host interface provides a deadlock recovery mechanism that enables a host to recover from deadlock situations involving the processor. The $\overline{\text{BOFF}}$ signal provides the deadlock recovery mechanism. When the host asserts $\overline{\text{BOFF}}$, the processor backs off the current transaction and asserts $\overline{\text{HBG}}$ and relinquishes the external bus.

The host can directly read or write the internal memory of the ADSP-TS203S processor, and it can access most of the processor registers, including DMA control (TCB) registers. Vector interrupts support efficient execution of host commands.

Multiprocessor Interface

The processor offers powerful features tailored to multiprocessing processor systems through the external port and link ports. This multiprocessing capability provides the highest bandwidth for interprocessor communication, including

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point-to-point communication

The external port and link ports provide integrated, glueless multiprocessing support.

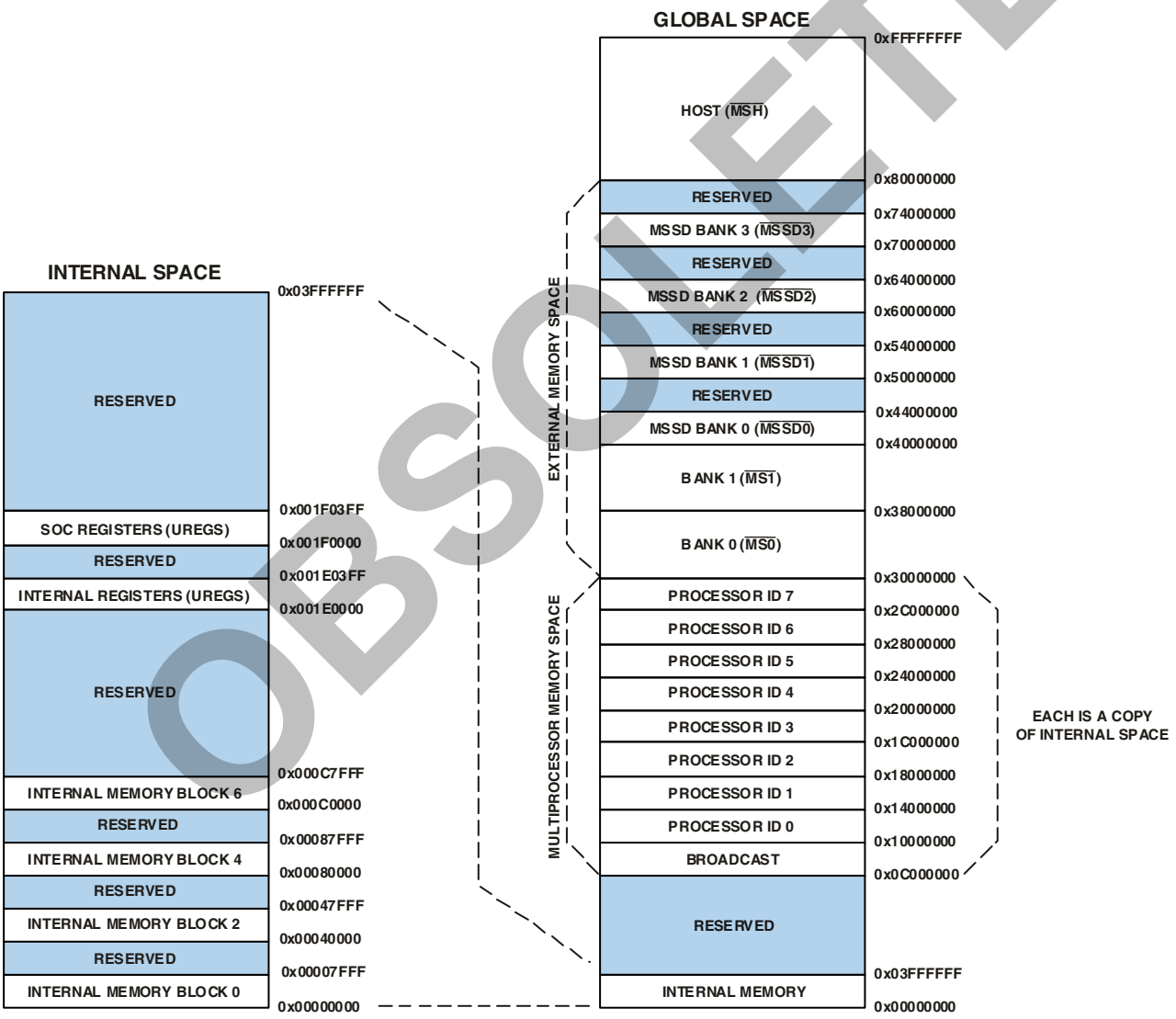


Figure 2. ADSP-TS203S Memory Map

The external port supports a unified address space (see Figure 2) that enables direct interprocessor accesses of each ADSP-TS203S processor's internal memory and registers. The processor's on-chip distributed bus arbitration logic provides simple, glueless connection for systems containing up to eight ADSP-TS203S processors and a host processor. Bus arbitration has a rotating priority. Bus lock supports indivisible read-modify-write sequences for semaphores. A bus fairness feature prevents one processor from holding the external bus too long.

The processor's two link ports provide a second path for interprocessor communications with throughput of 1G byte per second. The cluster bus provides 500M bytes per second throughput—with a total of 1.5G bytes per second interprocessor bandwidth.

SDRAM Controller

The SDRAM controller controls the processor's transfers of data to and from external synchronous DRAM (SDRAM) at a throughput of 32 bits per SCLK cycle using the external port and SDRAM control pins.

The SDRAM interface provides a glueless interface with standard SDRAMs—16M bits, 64M bits, 128M bits, 256M bits and 512M bits. The processor supports directly a maximum of four banks of 64M words 32 bits of SDRAM. The SDRAM interface is mapped in external memory in each processor's unified memory map.

EPROM Interface

The processor can be configured to boot from an external 8-bit EPROM at reset through the external port. An automatic process (which follows reset) loads a program from the EPROM into internal memory. This process uses 16 wait cycles for each read access. During booting, the $\overline{\text{BMS}}$ pin functions as the EPROM chip select signal. The EPROM boot procedure uses DMA Channel 0, which packs the bytes into 32-bit instructions. Applications can also access the EPROM (write flash memories) during normal operation through DMA.

The EPROM or flash memory interface is not mapped in the processor's unified memory map. It is a byte address space limited to a maximum of 16M bytes (24 address bits). The EPROM or flash memory interface can be used after boot via a DMA.

DMA CONTROLLER

The ADSP-TS203S processor's on-chip DMA controller, with 10 DMA channels, provides zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor's core, enabling DMA operations to occur while the processor's core continues to execute program instructions.

The DMA controller performs DMA transfers between internal memory, external memory, and memory-mapped peripherals; the internal memory of other DSPs on a common bus, a host processor, or link port I/O; between external memory and external peripherals or link port I/O; and between an external bus master and internal memory or link port I/O. The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the processor's internal memory and any external memory or memory-mapped peripheral on the external bus. Master mode and handshake mode protocols are supported.
- Link port transfers. Four dedicated DMA channels (two transmit and two receive) transfer quad-word data only between link ports and between a link port and internal or external memory. These transfers only use handshake mode protocol. DMA priority rotates between the two receive channels.
- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or to link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

The DMA controller provides these additional features:

- Flyby transfers. Flyby operations only occur through the external port (DMA channel 0) and do not involve the processor's core. The DMA controller acts as a conduit to transfer data from an external I/O device to external SDRAM memory. During a transaction, the processor relinquishes the external data bus; outputs addresses and memory selects ($\overline{\text{MSSD3–0}}$); outputs the $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{IOEN}}$, and $\overline{\text{RD}}$/$\overline{\text{WR}}$ strobes; and responds to ACK.
- DMA chaining. DMA chaining operations enable applications to automatically link one DMA transfer sequence to another for continuous transmission. The sequences can occur over different DMA channels and have different transmission attributes.
- Two-dimensional transfers. The DMA controller can access and transfer two-dimensional memory arrays on any DMA transmit or receive channel. These transfers are implemented with index, count, and modify registers for both the X and Y dimensions.

LINK PORTS (LVDS)

The processor's two full-duplex link ports each provide additional four-bit receive and four-bit transmit I/O capability, using low-voltage, differential-signal (LVDS) technology. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at 250 MHz, each link port can support up to 250M bytes per second per direction, for a combined maximum throughput of 1G byte per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own triple-buffered quad-word input and double-buffered quad-word output registers. The processor's core can write directly to a link port's transmit register and read

from a receive register, or the DMA controller can perform DMA transfers through four (two transmit and two receive) dedicated link port DMA channels.

Each link port direction has three signals that control its operation. For the transmitter, LxCLKOUT is the output transmit clock, LxACKI is the handshake input to control the data flow, and the $\overline{\text{LxBCMPO}}$ output indicates that the block transfer is complete. For the receiver, LxCLKIN is the input receive clock, LxACKO is the handshake output to control the data flow, and the $\overline{\text{LxBCMPI}}$ input indicates that the block transfer is complete. The LxDATO3–0 pins are the data output bus for the transmitter, and the LxDATI3–0 pins are the input data bus for the receiver.

Applications can program separate error detection mechanisms for transmit and receive operations (applications can use the checksum mechanism to implement consecutive link port transfers), the size of data packets, and the speed at which bytes are transmitted.

TIMER AND GENERAL-PURPOSE I/O

The ADSP-TS203S processor has a timer pin (TMR0E) that generates output when a programmed timer counter has expired, and four programmable general-purpose I/O pins (FLAG3–0) that can function as either single-bit input or output. As outputs, these pins can signal peripheral devices; as inputs, they can provide the test for conditional branching.

RESET AND BOOTING

The processor has three levels of reset:

- Power-up reset – after power-up of the system (SCLK, all static inputs, and strap pins are stable), the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- Normal reset – for any chip reset following the power-up reset, the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- Processor-core reset – when setting the SWRST bit in EMUCTL, the processor core is reset, but not the external port or I/O.

For normal operations, tie the $\overline{\text{RST\_OUT}}$ pin to the $\overline{\text{POR\_IN}}$ pin.

After reset, the processor has four boot options for beginning operation:

- Boot from EPROM.
- Boot by an external master (host or another ADSP-TS203S processor).
- Boot by link port.
- No boot—start running from memory address selected with one of the $\overline{\text{IRQ3–0}}$ interrupt signals. See Table 2. Using the this option, the processor must start running from memory when one of the interrupts is asserted.

The processor core always exits from reset in the idle state and waits for an interrupt. Some of the interrupts in the interrupt vector table are initialized and enabled after reset.

Table 2. No Boot, Run from Memory Addresses

Interrupt	Address
$\overline{\text{IRQ0}}$	0x3000 0000 (External Memory)
$\overline{\text{IRQ1}}$	0x3800 0000 (External Memory)
$\overline{\text{IRQ2}}$	0x8000 0000 (External Memory)
$\overline{\text{IRQ3}}$	0x0000 0000 (Internal Memory)

For more information on boot options, see the *EE-200: ADSP-TS20x TigerSHARC Processor Boot Loader Kernels Operation* on the Analog Devices website (www.analog.com)

CLOCK DOMAINS

The processor uses calculated ratios of the SCLK clock to operate, as shown in Figure 3. The instruction execution rate is equal to CCLK. A PLL from SCLK generates CCLK which is phase-locked. The SCLKRATx pins define the clock multiplication of SCLK to CCLK (see Table 4 on Page 11). The link port clock is generated from CCLK via a software programmable divisor, and the SOC bus operates at 1/2 CCLK. Memory transfers to external and link port buffers operate at the SOCCLK rate. SCLK also provides clock input for the external bus interface and defines the ac specification reference for the external bus signals. The external bus interface runs at the SCLK frequency. The maximum SCLK frequency is one quarter the internal processor clock (CCLK) frequency.

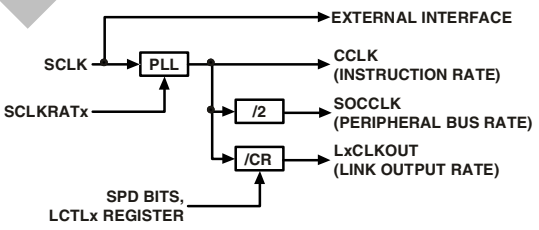
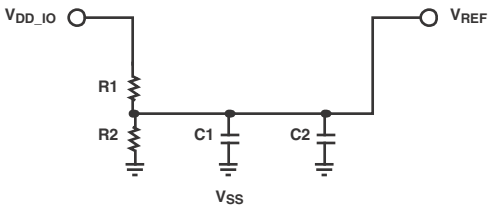


Figure 3. Clock Domains

FILTERING REFERENCE VOLTAGE AND CLOCKS

Figure 4 and Figure 5 show possible circuits for filtering V_{REF}, and SCLK_V_{REF}. These circuits provide the reference voltages for the switching voltage reference and system clock reference.



R1: 2 kΩ SERIES RESISTOR (±1%)
R2: 2.55 kΩ SERIES RESISTOR (±1%)
C1: 1µF CAPACITOR (SMD)
C2: 1nF CAPACITOR (HF SMD) PLACED CLOSE TO PROCESSOR'S PINS

Figure 4. V_{REF} Filtering Scheme

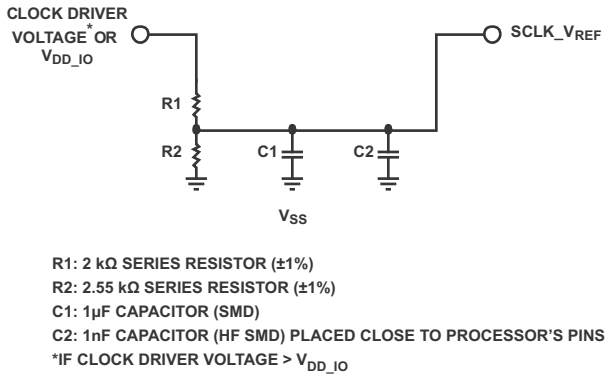


Figure 5. SCLK_V_{REF} Filtering Scheme

POWER DOMAINS

The ADSP-TS203S processor has separate power supply connections for internal logic (V_{DD}), analog circuits (V_{DD_A}), I/O buffer (V_{DD_IO}), and internal DRAM (V_{DD_DRAM}) power supply.

Note that the analog (V_{DD_A}) supply powers the clock generator PLLs. To produce a stable clock, systems must provide a clean power supply to power input V_{DD_A}. Designs must pay critical attention to bypassing the V_{DD_A} supply.

DEVELOPMENT TOOLS

The ADSP-TS203S processor is supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other TigerSHARC processors also fully emulates the ADSP-TS203S processor.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ run-time library that includes DSP and mathematical functions. A key point for theses tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the TigerSHARC processor development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

VCSE is Analog Devices' technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. It is also used for downloading components from the Web, dropping them into the application, and publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the expert linker to visually manipulate the placement of code and data on the embedded system, view memory use in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with a drag of the mouse, and examine runtime stack and heap usage. The expert linker is fully compatible with existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices emulators use the IEEE 1149.1 JTAG test access port of the ADSP-TS203S processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the TigerSHARC processor family. Hardware tools include TigerSHARC processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite® evaluation platforms to use as a cost-effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board flash device to store user-specific boot code, enabling the board to run as a standalone unit, without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom-defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every developer needs to in order test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use the string "EE-68" in site search. This document is updated regularly to keep pace with improvements to emulator support.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-TS203S processor's architecture and functionality. For detailed information on the ADSP-TS203S processor's core architecture and instruction set, see the *ADSP-TS201 TigerSHARC Processor Hardware Reference* and the *ADSP-TS201 TigerSHARC Processor Programming Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide for TigerSHARC Processors*.

PIN FUNCTION DESCRIPTIONS

While most of the ADSP-TS203S processor's input pins are normally synchronous—tied to a specific clock—a few are asynchronous. For these asynchronous signals, an on-chip synchronization circuit prevents metastability problems. Use the ac specification for asynchronous signals when the system design requires predictable, cycle-by-cycle behavior for these signals.

The output pins can be three-stated during normal operation. The processor three-states all output during reset, allowing these pins to get to their internal pull-up or pull-down state. Some pins have an internal pull-up or pull-down resistor (±30% tolerance) that maintains a known value during transitions between different drivers.

Table 3. Pin Definitions—Clocks and Reset

Signal	Type	Term	Description
SCLKRAT2–0	I (pd)	na	Core Clock Ratio. The processor's core clock (CCLK) rate = n SCLK, where n is user-programmable using the SCLKRATx pins to the values shown in Table 4. These pins may change only during reset; connect these pins to V_{DD_IO} or V_{SS}. All reset specifications in Table 25, Table 26, and Table 27 must be satisfied. The core clock rate (CCLK) is the instruction cycle rate.
SCLK	I	na	System Clock Input. The processor's system input clock for cluster bus. The core clock rate is user-programmable using the SCLKRATx pins. For more information, see Clock Domains on Page 8.
$\overline{\text{RST\_IN}}$	I/A	na	Reset. Sets the processor to a known state and causes program to be in idle state. $\overline{\text{RST\_IN}}$ must be asserted a specified time according to the type of reset operation. For details, see Reset and Booting on Page 8, Table 27 on Page 26, and Figure 12 on Page 26.
$\overline{\text{RST\_OUT}}$	O	na	Reset Output. Indicates that the processor reset is complete. Connect to $\overline{\text{POR\_IN}}$.
$\overline{\text{POR\_IN}}$	I/A	na	Power-On Reset for internal DRAM. Connect to $\overline{\text{RST\_OUT}}$.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 4. SCLK Ratio

SCLKRAT2–0	Ratio
000 (default)	4
001	5
010	6
011	7
100	8
101	10
110	12
111	Reserved

Table 5. Pin Definitions—External Port Bus Controls

Signal	Type	Term	Description
ADDR31–0	I/O/T (pu_ad)	nc	Address Bus. The processor issues addresses for accessing memory and peripherals on these pins. In a multiprocessor system, the bus master drives addresses for accessing internal memory or I/O processor registers of other ADSP-TS203S processors. The processor inputs addresses when a host or another processor accesses its internal memory or I/O processor registers.
DATA31–0	I/O/T (pu_ad)	nc	External Data Bus. The processor drives and receives data and instructions on these pins. Pull-up or pull-down resistors on unused DATA pins are unnecessary.
$\overline{RD}$	I/O/T (pu_0)	epu[1]	Memory Read. $\overline{RD}$ is asserted whenever the processor reads from any slave in the system, excluding SDRAM. When the processor is a slave, $\overline{RD}$ is an input and indicates read transactions that access its internal memory or universal registers. In a multiprocessor system, the bus master drives $\overline{RD}$. $\overline{RD}$ changes concurrently with ADDR pins.
$\overline{WRL}$	I/O/T (pu_0)	epu[1]	Write Low. $\overline{WRL}$ is asserted when the ADSP-TS203S processor writes to the external bus (host, memory, or processor). An external master (host or processor) asserts $\overline{WRL}$ for writing to a processor's internal memory. In a multiprocessor system, the bus master drives $\overline{WRL}$. $\overline{WRL}$ changes concurrently with ADDR pins. When the processor is a slave, $\overline{WRL}$ is an input and indicates write transactions that access its internal memory or universal registers.
ACK	I/O/T/OD (pu_od_0)	epu[1]	Acknowledge. External slave devices can deassert ACK to add wait states to external memory accesses. ACK is used by I/O devices, memory controllers, and other peripherals on the data phase. The processor can deassert ACK to add wait states to read and write accesses of its internal memory. The pull-up is 50 Ω on low-to-high transactions and is 500 Ω on all other transactions.
$\overline{BMS}$	O/T (pu_0)	na	Boot Memory Select. $\overline{BMS}$ is the chip select for boot EPROM or flash memory. During reset, the processor uses $\overline{BMS}$ as a strap pin (EBOOT) for EPROM boot mode. In a multiprocessor system, the processor bus master drives $\overline{BMS}$. For details, see Reset and Booting on Page 8 and the EBOOT signal description in Table 16 on Page 18.
$\overline{MS1–0}$	O/T (pu_0)	nc	Memory Select. $\overline{MS0}$ or $\overline{MS1}$ is asserted whenever the processor accesses memory banks 0 or 1, respectively. $\overline{MS1–0}$ are decoded memory address pins that change concurrently with ADDR pins. When ADDR31:27 = 0b00110, $\overline{MS0}$ is asserted. When ADDR31:27 = 0b00111, $\overline{MS1}$ is asserted. In multiprocessor systems, the master processor drives $\overline{MS1–0}$.
$\overline{MSH}$	O/T (pu_0)	nc	Memory Select Host. $\overline{MSH}$ is asserted whenever the processor accesses the host address space (ADDR31 = 0b1). $\overline{MSH}$ is a decoded memory address pin that changes concurrently with ADDR pins. In a multiprocessor system, the bus master processor drives $\overline{MSH}$.
$\overline{BRST}$	I/O/T (pu_0)	epu[1]	Burst. The current bus master (processor or host) asserts this pin to indicate that it is reading or writing data associated with consecutive addresses. A slave device can ignore addresses after the first one and increment an internal address counter after each transfer. For host-to-processor burst accesses, the processor increments the address automatically while $\overline{BRST}$ is asserted.
TM4	I/O/T	epu	Test Mode 4. Must be pulled up to V_{DD_IO} with a 5 kΩ resistor.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

[1] This external pull-up may be omitted for the ID = 000 TigerSHARC processor.

Table 6. Pin Definitions—External Port Arbitration

Signal	Type	Term	Description
$\overline{BR7–0}$	I/O	V_{DD_IO}[1]	Multiprocessing Bus Request Pins. Used by the processors in a multiprocessor system to arbitrate for bus mastership. Each processor drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In systems with fewer than eight processors, set the unused $\overline{BRx}$ pins high (V_{DD_IO}).
ID2–0	I (pd)	na	Multiprocessor ID. Indicates the processor's ID, from which the processor determines its order in a multiprocessor system. These pins also indicate to the processor which bus request ($\overline{BR0}$–$\overline{BR7}$) to assert when requesting the bus: 000 = $\overline{BR0}$, 001 = $\overline{BR1}$, 010 = $\overline{BR2}$, 011 = $\overline{BR3}$, 100 = $\overline{BR4}$, 101 = $\overline{BR5}$, 110 = $\overline{BR6}$, or 111 = $\overline{BR7}$. ID2–0 must have a constant value during system operation and can change during reset only.
$\overline{BM}$	O	na	Bus Master. The current bus master processor asserts $\overline{BM}$. For debugging only. At reset this is a strap pin. For more information, see Table 16 on Page 18.
$\overline{BOFF}$	I	epu	Back Off. A deadlock situation can occur when the host and a processor try to read from each other's bus at the same time. When deadlock occurs, the host can assert $\overline{BOFF}$ to force the processor to relinquish the bus before completing its outstanding transaction.
$\overline{BUSLOCK}$	O/T (pu_0)	na	Bus Lock Indication. Provides an indication that the current bus master has locked the bus. At reset, this is a strap pin. For more information, see Table 16 on Page 18.
$\overline{HBR}$	I	epu	Host Bus Request. A host must assert $\overline{HBR}$ to request control of the processor's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the bus master relinquishes the bus and asserts $\overline{HBG}$ once the outstanding transaction is finished.
$\overline{HBG}$	I/O/T (pu_0)	epu[2]	Host Bus Grant. Acknowledges $\overline{HBR}$ and indicates that the host can take control of the external bus. When relinquishing the bus, the master processor three-states the ADDR31–0, DATA31–0, $\overline{MSH}$, $\overline{MSSD3–0}$, $\overline{MS1–0}$, $\overline{RD}$, $\overline{WRL}$, $\overline{BMS}$, $\overline{BRST}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{IOEN}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, SDCKE, LDQM, and TM4 pins, and the processor puts the SDRAM in self-refresh mode. The processor asserts $\overline{HBG}$ until the host deasserts $\overline{HBR}$. In multiprocessor systems, the current bus master processor drives $\overline{HBG}$, and all slave processors monitor it.
$\overline{CPA}$	I/O/OD (pu_od_0)	epu[2]	Core Priority Access. Asserted while the processor's core accesses external memory. This pin enables a slave processor to interrupt a master processor's background DMA transfers and gain control of the external bus for core-initiated transactions. $\overline{CPA}$ is an open-drain output, connected to all DSPs in the system. If not required in the system, leave $\overline{CPA}$ unconnected (external pull-ups will be required for processor ID = 1 through ID = 7).
$\overline{DPA}$	I/O/OD (pu_od_0)	epu[2]	DMA Priority Access. Asserted while a high priority processor DMA channel accesses external memory. This pin enables a high priority DMA channel on a slave processor to interrupt transfers of a normal priority DMA channel on a master processor and gain control of the external bus for DMA-initiated transactions. $\overline{DPA}$ is an open-drain output, connected to all DSPs in the system. If not required in the system, leave $\overline{DPA}$ unconnected (external pull-ups will be required for processor ID = 1 through ID = 7).

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

[1] The $\overline{BRx}$ pin matching the ID2–0 input selection for the processor should be left nc if unused. For example, the processor with ID = 000 has $\overline{BR0}$ = nc and $\overline{BR7–1}$ = V_{DD_IO}.
[2] This external pull-up resistor may be omitted for the ID = 000 TigerSHARC processor.

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Term	Description
$\overline{\text{DMAR3–0}}$	I/A	epu	DMA Request Pins. Enable external I/O devices to request DMA services from the processor. In response to $\overline{\text{DMARx}}$, the processor performs DMA transfers according to the DMA channel's initialization. The processor ignores DMA requests from uninitialized channels.
$\overline{\text{IOWR}}$	O/T (pu_0)	nc	I/O Write. When a processor DMA channel initiates a flyby mode read transaction, the processor asserts the $\overline{\text{IOWR}}$ signal during the data cycles. This assertion makes the I/O device sample the data instead of the TigerSHARC.
$\overline{\text{IORD}}$	O/T (pu_0)	nc	I/O Read. When a processor DMA channel initiates a flyby mode write transaction, the processor asserts the $\overline{\text{IORD}}$ signal during the data cycle. This assertion with the $\overline{\text{IOEN}}$ makes the I/O device drive the data instead of the TigerSHARC.
$\overline{\text{IOEN}}$	O/T (pu_0)	nc	I/O Device Output Enable. Enables the output buffers of an external I/O device for fly-by transactions between the device and external memory. Active on flyby transactions.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Term	Description
$\overline{\text{MSSD3–0}}$	I/O/T (pu_0)	nc	Memory Select SDRAM. $\overline{\text{MSSD0}}$, $\overline{\text{MSSD1}}$, $\overline{\text{MSSD2}}$, or $\overline{\text{MSSD3}}$ is asserted whenever the processor accesses SDRAM memory space. $\overline{\text{MSSD3–0}}$ are decoded memory address pins that are asserted whenever the processor issues an SDRAM command cycle (access to ADDR31:30 = 0b01—except reserved spaces shown in Figure 2 on Page 6). In a multiprocessor system, the master processor drives $\overline{\text{MSSD3–0}}$.
$\overline{\text{RAS}}$	I/O/T (pu_0)	nc	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$	I/O/T (pu_0)	nc	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to the SDRAM specification.
LDQM	O/T (pu_0)	nc	Low Word SDRAM Data Mask. When sampled high, three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted, and inactive on read transactions.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 8. Pin Definitions—External Port SDRAM Controller (Continued)

Signal	Type	Term	Description
SDA10	O/T (pu_0)	nc	SDRAM Address Bit 10. Separate A10 signals enable SDRAM refresh operation while the processor executes non-SDRAM transactions.
SDCKE	I/O/T (pu_m/ pd_m)	nc	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave processor in a multiprocessor system does not have the pull-up or pull-down. A master processor (or ID = 0 in a single processor system) has a pull-up before granting the bus to the host, except when the SDRAM is put in self refresh mode. In self refresh mode, the master has a pull-down before granting the bus to the host.
$\overline{\text{SDWE}}$	I/O/T (pu_0)	nc	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 9. Pin Definitions—JTAG Port

Signal	Type	Term	Description
$\overline{\text{EMU}}$	O/OD	nc[1]	Emulation. Connected to the processor's JTAG emulator target board connector only.
TCK	I	epd or epu[1]	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI	I (pu_ad)	nc[1]	Test Data Input (JTAG). A serial data input of the scan path.
TDO	O/T	nc[1]	Test Data Output (JTAG). A serial data output of the scan path.
TMS	I (pu_ad)	nc[1]	Test Mode Select (JTAG). Used to control the test state machine.
$\overline{\text{TRST}}$	I/A (pu_ad)	na	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted or pulsed low after power-up for proper device operation. For more information, see Reset and Booting on Page 8.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

[1] See the reference on Page 10 to the JTAG emulation technical reference EE-68.

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Term	Description
FLAG3–0	I/O/A (pu)	nc	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$	I/A (pu)	nc	Interrupt Request. When asserted, the processor generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge-triggered or level-sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option and interrupt vectors are initialized for booting.
TMR0E	O	na	Timer 0 expires. This output pulses whenever timer 0 expires. At reset, this is a strap pin. For more information, see Table 16 on Page 18.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 11. Pin Definitions—Link Ports

Signal	Type	Term	Description
LxDATO3–0P	O	nc	Link Ports 1–0 Data 1–0 Transmit LVDS P
LxDATO3–0N	O	nc	Link Ports 1–0 Data 1–0 Transmit LVDS N
LxCLKOUTP	O	nc	Link Ports 1–0 Transmit Clock LVDS P
LxCLKOUTN	O	nc	Link Ports 1–0 Transmit Clock LVDS N
LxACKI	I (pd)	nc	Link Ports 1–0 Receive Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPO}}$	O (pu)	nc	Link Ports 1–0 Block Completion. When the transmission is executed using DMA, this signal indicates to the receiver that the transmitted block is completed. The pull-up resistor is present on $\overline{\text{L0BCMPO}}$ only. At reset, the $\overline{\text{L1BCMPO}}$ pin is a strap pin. For more information, see Table 16 on Page 18.
LxDATI3–0P	I	V_{DD_IO}	Link Ports 1–0 Data 3–0 Receive LVDS P
LxDATI3–0N	I	V_{DD_IO}	Link Ports 1–0 Data 3–0 Receive LVDS N
LxCLKINP	I/A	V_{DD_IO}	Link Ports 1–0 Receive Clock LVDS P
LxCLKINN	I/A	V_{DD_IO}	Link Ports 1–0 Receive Clock LVDS N
LxACKO	O	nc	Link Ports 1–0 Transmit Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPI}}$	I (pd_l)	V_{SS}	Link Ports 1–0 Block Completion. When the reception is executed using DMA, this signal indicates to the receiver that the transmitted block is completed.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 12. Pin Definitions—Impedance Control, Drive Strength Control, and Regulator Enable

Signal	Type	Term	Description
CONTROLIMP0 CONTROLIMP1	I (pd) I (pu)	na na	Impedance Control. As shown in Table 13, the CONTROLIMP1–0 pins select between normal driver mode and A/D driver mode. When using normal mode (recommended), the output drive strength is set relative to maximum drive strength according to Table 14. When using A/D mode, the resistance control operates in the analog mode, where drive strength is continuously controlled to match a specific line impedance as shown in Table 14.
DS2, 0 DS1	I (pu) I (pd)	na	Digital Drive Strength Selection. Selected as shown in Table 14. For drive strength calculation, see Output Drive Currents on Page 34. The drive strength for some pins is preset, not controlled by the DS2–0 pins. The pins that are always at drive strength 7 (100%) include: $\overline{CPA}$, $\overline{DPA}$, TDO, $\overline{EMU}$, and $\overline{RST\_OUT}$. The drive strength for the ACK pin is always ×2 drive strength 7 (100%).
ENEDREG	I (pu)	V_{SS}	Connect the ENEDREG pin to V_{SS}. Connect the V_{DD_DRAM} pins to a properly decoupled DRAM power supply.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 13. Impedance Control Selection

CONTROLIMP1-0	Driver Mode
00 (recommended)	Normal
01	Reserved
10 (default)	A/D Mode
11	Reserved

Table 14. Drive Strength/Output Impedance Selection

DS2–0 Pins	Drive Strength[1]	Output Impedance[2]
000	Strength 0 (11.1%)	26 Ω
001	Strength 1 (23.8%)	32 Ω
010	Strength 2 (36.5%)	40 Ω
011	Strength 3 (49.2%)	50 Ω
100	Strength 4 (61.9%)	62 Ω
101 (default)	Strength 5 (74.6%)	70 Ω
110	Strength 6 (87.3%)	96 Ω
111	Strength 7 (100%)	120 Ω

[1] CONTROLIMP1 = 0, A/D mode disabled.
[2] CONTROLIMP1 = 1, A/D mode enabled.

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	na	V_{DD} pins for internal logic.
V_{DD_A}	P	na	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	na	V_{DD} pins for I/O buffers.
V_{DD_DRAM}	P	na	V_{DD} pins for internal DRAM.
V_{REF}	I	na	Reference voltage defines the trip point for all input buffers, except SCLK, $\overline{RST\_IN}$, $\overline{POR\_IN}$, $\overline{IRQ3–0}$, FLAG3–0, $\overline{DMAR3–0}$, ID2–0, CONTROLIMP1–0, LxDATO3–0P/N, LxCLKOUTP/N, LxDATI3–0P/N, LxCLKINP/N, TCK, TDI, TMS, and $\overline{TRST}$. V_{REF} can be connected to a power supply or set by a voltage divider circuit as shown in Figure 4. For more information, see Filtering Reference Voltage and Clocks on Page 8.
$SCLK\_V_{REF}$	I	na	System Clock Reference. Connect this pin to a reference voltage as shown in Figure 5. For more information, see Filtering Reference Voltage and Clocks on Page 8.
V_{SS}	G	na	Ground pins.
NC	—	nc	No Connect. Do not connect these pins to anything (not to any supply, signal, or each other). These pins are reserved and must be left unconnected.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set processor operating modes. During reset, the processor samples the strap option pins. Strap pins have an internal pull-up or pull-down for the default value. If a strap pin is not connected to an overdriving external pull-up, pull-down, or logic load, the processor samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-up or pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up or pull-down. Table 16 lists and describes each of the processor's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	Type (at Reset)	On Pin …	Description
EBOOT	I (pd_0)	$\overline{BMS}$	EPROM Boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot processor through the external port or a link port
IRQEN	I (pd)	$\overline{BM}$	Interrupt Enable. 0 = disable and set $\overline{IRQ3–0}$ interrupts to edge-sensitive after reset (default) 1 = enable and set $\overline{IRQ3–0}$ interrupts to level-sensitive immediately after reset
LINK_DWIDTH	I (pd)	TMR0E	Link Port Input Default Data Width. 0 = 1-bit (default) 1 = 4-bit

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Table 16. Pin Definitions—I/O Strap Pins (Continued)

Signal	Type (at Reset)	On Pin …	Description
SYS_REG_WE	I (pd_0)	$\overline{\text{BUSLOCK}}$	SYSCON and SDRCON Write Enable. 0 = one-time writable after reset (default) 1 = always writable
TM1	I (pu)	$\overline{\text{L1BCMPO}}$	Test Mode 1. Do not overdrive default value during reset.
TM2	I (pu)	TM2	Test Mode 2. Do not overdrive default value during reset.
TM3	I (pu)	TM3	Test Mode 3. Do not overdrive default value during reset.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

When default configuration is used, no external resistor is needed on the strap pins. To apply other configurations, a 500 Ω resistor connected to V_{DD_IO} is required. If providing external pull-downs, do not strap these pins directly to V_{SS}; the strap pins require 500 Ω resistor straps.

All strap pins are sampled on the rising edge of $\overline{\text{RST\_IN}}$ (deassertion edge). Each pin latches the strapped pin state (state of the strap pin at the rising edge of $\overline{\text{RST\_IN}}$). Shortly after deassertion of $\overline{\text{RST\_IN}}$, these pins are reconfigured to their normal functionality.

These strap pins have an internal pull-down resistor, pull-up resistor, or no-resistor (three-state) on each pin. The resistor type, which is connected to the I/O pad, depends on whether $\overline{\text{RST\_IN}}$ is active (low) or if $\overline{\text{RST\_IN}}$ is deasserted (high). Table 17 shows the resistors that are enabled during active reset and during normal operation.

Table 17. Strap Pin Internal Resistors—Active Reset ($\overline{\text{RST\_IN}}$ = 0) vs. Normal Operation ($\overline{\text{RST\_IN}}$ = 1)

Pin	$\overline{\text{RST\_IN}}$ = 0	$\overline{\text{RST\_IN}}$ = 1
$\overline{\text{BMS}}$	(pd_0)	(pu_0)
$\overline{\text{BM}}$	(pd)	Driven
TMR0E	(pd)	Driven
$\overline{\text{BUSLOCK}}$	(pd_0)	(pu_0)
$\overline{\text{L1BCMPO}}$	(pu)	Driven
TM2	(pu)	Driven
TM3	(pu)	Driven

pd = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ;
pd_0 = internal pull-down 5 kΩ on processor ID = 0;
pu_0 = internal pull-up 5 kΩ on processor ID = 0

SPECIFICATIONS

Note that component specifications are subject to change with out notice. For information on link port electrical characteristics, see Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing on Page 29.

OPERATING CONDITIONS

Parameter	Description	Test Conditions	Grade[1]	Min	Typ	Max	Unit
V_{DD}	Internal Supply Voltage	@ CCLK = 500 MHz	050	1.00	1.05	1.10	V
V_{DD_A}	Analog Supply Voltage	@ CCLK = 500 MHz	050	1.00	1.05	1.10	V
V_{DD_IO}	I/O Supply Voltage		(all)	2.38	2.50	2.63	V
V_{DD_DRAM}	Internal DRAM Supply Voltage	@ CCLK = 500 MHz	050	1.425	1.500	1.575	V
T_{CASE}	Case Operating Temperature		A	–40		+85	°C
T_{CASE}	Case Operating Temperature		B	0		+85	°C
V_{IH1}	High Level Input Voltage[2, 3]	@ V_{DD}, V_{DD_IO} = Max	(all)	1.7		3.63	V
V_{IH2}	High Level Input Voltage[3, 4]	@ V_{DD}, V_{DD_IO} = Max	(all)	1.9		3.63	V
V_{IL}	Low Level Input Voltage[3, 5]	@ V_{DD}, V_{DD_IO} = Min	(all)	–0.33		+0.8	V
I_{DD}	V_{DD} Supply Current, Typical Activity[6]	@ CCLK = 500 MHz, V_{DD} = 1.05 V, T_{CASE} = 25°C	050		2.06		A
I_{DD_A}	V_{DD_A} Supply Current, Typical Activity	@ CCLK = 500 MHz, V_{DD} = 1.05 V, T_{CASE} = 25°C	050		20	50	mA
I_{DD_IO}	V_{DD_IO} Supply Current, Typical Activity[6]	@ SCLK = 62.5 MHz, V_{DD_IO} = 2.5 V, T_{CASE} = 25°C	(all)		0.15		A
I_{DD_DRAM}	V_{DD_DRAM} Supply Current, Typical Activity[6]	@ CCLK = 500 MHz, V_{DD_DRAM} = 1.5 V, T_{CASE} = 25°C	050		0.25	0.40	A
V_{REF}	Voltage Reference		(all)	(V_{DD_IO} × 0.56) ±5%			V
SCLK_V_{REF}	Voltage Reference		(all)	(V_{CLOCK_DRIVE} × 0.56) ±5%			V

[1] Specifications vary for different grades (for example, SABP–060, SABP–050, SWBP–050). For more information on part grades, see Ordering Guide on Page 47.

[2] V_{IH1} specification applies to input and bidirectional pins: SCLKRAT2–0, SCLK, ADDR31–0, DATA63–0, $\overline{RD}$, $\overline{WRL}$, ACK, $\overline{BRST}$, $\overline{BR7–0}$, $\overline{BOFF}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{MSSD3–0}$, $\overline{RAS}$, $\overline{CAS}$, SDCKE, $\overline{SDWE}$, TCK, FLAG3–0, DS2–0, ENEDREG.

[3] Values represent dc case. During transitions, the inputs may overshoot or undershoot to the voltage shown in Table 18, based on the transient duty cycle. The dc case is equivalent to 100% duty cycle.

[4] V_{IH2} specification applies to input and bidirectional pins: TDI, TMS, $\overline{TRST}$, CIMP1–0, ID2–0, $\overline{LxBCMPI}$, LxACKI, $\overline{POR\_IN}$, $\overline{RST\_IN}$, $\overline{IRQ3–0}$, $\overline{CPA}$, $\overline{DPA}$, $\overline{DMAR3–0}$.

[5] Applies to input and bidirectional pins.

[6] For details on internal and external power calculation issues, including other operating conditions, see *EE-170, Estimating Power for the ADSP-TS203S*.

Table 18. Maximum Duty Cycle for Input Transient Voltage

V_{IN} Max (V)[1]	V_{IN} Min (V)[1]	Maximum Duty Cycle[2]
+3.63	–0.33	100%
+3.64	–0.34	90%
+3.70	–0.40	50%
+3.78	–0.48	30%
+3.86	–0.56	17%
+3.93	–0.63	10%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence. The practical worst case for period of occurrence for either overshoot or undershoot is 2 × t_{SCLK}.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DD_IO} = Min, I_{OH} = –2 mA	2.18		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DD_IO} = Min, I_{OL} = 4 mA		0.4	V
I_{IH}	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max		20	µA
I_{IH_PU}	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max		20	µA
I_{IH_PD}	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{DD_IO} Max	0.3	0.76	mA
$I_{IH\_PD\_L}$	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max	30	76	µA
I_{IL}	Low Level Input Current	@ V_{DD_IO} = Max, V_{IN} = 0 V		20	µA
I_{IL_PU}	Low Level Input Current	@ V_{DD_IO} = Max, V_{IN} = 0 V	0.3	0.76	mA
$I_{IL\_PU\_AD}$	Low Level Input Current	@ V_{DD_IO} = Max, V_{IN} = 0 V	30	100	µA
I_{OZH}	Three-State Leakage Current High	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max		50	µA
I_{OZH_PD}	Three-State Leakage Current High	@ V_{DD_IO} = Max, V_{IN} = V_{DD_IO} Max	0.3	0.76	mA
I_{OZL}	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V		20	µA
I_{OZL_PU}	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V	0.3	0.76	mA
$I_{OZL\_PU\_AD}$	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V	30	100	µA
I_{OZL_OD}	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V	4	7.6	mA
C_{IN}	Input Capacitance[2, 3]	@ f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		3	pF

Parameter name suffix conventions: no suffix = applies to pins without pull-up or pull-down resistors, **_PD** = applies to pin types (pd) or (pd_0), **_PU** = applies to pin types (pu) or (pu_0), **_PU_AD** = applies to pin types (pu_ad), **_OD** = applies to pin types OD, **_PD_L** = applies to pin types (pd_l)

[1] Applies to output and bidirectional pins.
[2] Applies to all signals.
[3] Guaranteed but not tested.

PACKAGE INFORMATION

The information presented in Figure 6 provide details about the package branding for the ADSP-TS203S processors. For a complete listing of product availability, see Ordering Guide on Page 47.

Figure 6. Typical Package Brand

Table 19. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option (optional)
ccc	See Ordering Guide
tppzccc	Silicon Lot Number
2.0	Silicon Revision
yyww	Date Code
vvvvvv	Assembly Lot Code

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 20. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD})	–0.3 V to +1.4 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.4 V
External (I/O) Supply Voltage (V_{DD_IO})	–0.3 V to +3.5 V
External (DRAM) Supply Voltage (V_{DD_DRAM})	–0.3 V to +2.1 V
Input Voltage[1]	–0.63 V to +3.93 V
Output Voltage Swing	–0.5 V to V_{DD_IO} + 0.5 V
Storage Temperature Range	–65°C to +150°C

[1] Applies to 10% transient duty cycle. For other duty cycles see Table 18.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

With the exception of $\overline{\text{DMAR3–0}}$, $\overline{\text{IRQ3–0}}$, TMR0E, and FLAG3–0 (input only) pins, all ac timing for the ADSP-TS203S processor is relative to a reference clock edge. Because input setup/hold, output valid/hold, and output enable/disable times are relative to a clock edge, the timing data for the ADSP-TS203S processor has few calculated (formula-based) values. For information on ac timing, see General AC Timing. For information on link port transfer timing, see Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing on Page 29.

General AC Timing

Timing is measured on signals when they cross the 1.25 V level as described in Figure 13 on Page 28. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.25 V and the point that the second signal reaches 1.25 V.

The general ac timing data appears in Table 22 and Table 29. All ac specifications are measured with the load specified in Figure 34 on Page 36, and with the output drive strength set to strength 4. In order to calculate the output valid and hold times for different load conditions and/or output drive strengths, refer to Figure 35 on Page 36 through Figure 42 on Page 38 (Rise and Fall Time vs. Load Capacitance) and Figure 43 on Page 38 (Output Valid vs. Load Capacitance and Drive Strength).

The ac asynchronous timing data for the $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, FLAG3–0, and TMR0E pins appears in Table 21.

Table 21. AC Asynchronous Signal Specifications

Name	Description	Pulse Width Low (Min)	Pulse Width High (Min)
$\overline{\text{IRQ3–0}}$[1]	Interrupt Request	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
$\overline{\text{DMAR3–0}}$[1]	DMA Request	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
FLAG3–0[2]	FLAG3–0 Input	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
TMR0E[3]	Timer 0 Expired	$4 \times t_{SCLK}$ ns	

[1] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference.
[2] For output specifications on FLAG3–0 pins, see Table 29.
[3] This pin is a strap option. During reset, an internal resistor pulls the pin low.

Table 22. Reference Clocks—Core Clock (CCLK) Cycle Time

Parameter	Description	Grade = 050 (500 MHz) Min	Max	Unit
t_{CCLK}[1]	Core Clock Cycle Time	2.0	12.5	ns

[1] CCLK is the internal processor clock or instruction cycle time. The period of this clock is equal to the system clock period (t_{SCLK}) divided by the system clock ratio (SCLKRAT2–0). For information on available part numbers for different internal processor clock rates, see the Ordering Guide on Page 47.

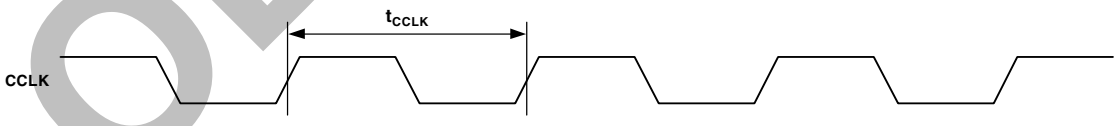


Figure 7. Reference Clocks—Core Clock (CCLK) Cycle Time

Table 23. Reference Clocks—System Clock (SCLK) Cycle Time

Parameter	Description	SCLKRAT = 4×, 6×, 8×, 10×, 12×		SCLKRAT = 5×, 7×		Unit
		Min	Max	Min	Max	
t_{SCLK}[1, 2, 3]	System Clock Cycle Time	8	50	8	50	ns
t_{SCLKH}	System Clock Cycle High Time	0.40 × t_{SCLK}	0.60 × t_{SCLK}	0.45 × t_{SCLK}	0.55 × t_{SCLK}	ns
t_{SCLKL}	System Clock Cycle Low Time	0.40 × t_{SCLK}	0.60 × t_{SCLK}	0.45 × t_{SCLK}	0.55 × t_{SCLK}	ns
t_{SCLKF}	System Clock Transition Time—Falling Edge[4]		1.5		1.5	ns
t_{SCLKR}	System Clock Transition Time—Rising Edge		1.5		1.5	ns
t_{SCLKJ}[5, 6]	System Clock Jitter Tolerance		500		500	ps

[1] For more information, see Table 3 on Page 11.
[2] For more information, see Clock Domains on Page 8.
[3] The value of (t_{SCLK} / SCLKRAT2-0) must not violate the specification for t_{CCLK}.
[4] System clock transition times apply to minimum SCLK cycle time (t_{SCLK}) only.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

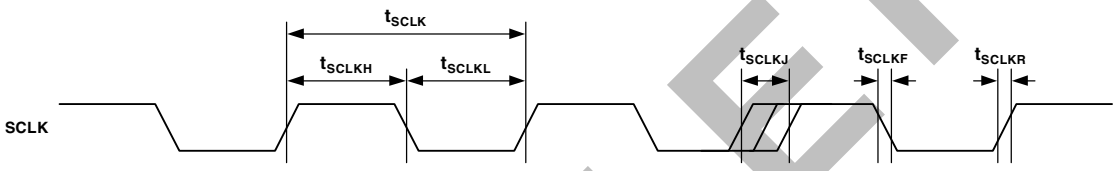


Figure 8. Reference Clocks—System Clock (SCLK) Cycle Time

Table 24. Reference Clocks—JTAG Test Clock (TCK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{TCK}	Test Clock (JTAG) Cycle Time	Greater of 30 or t_{CCLK} × 4		ns
t_{TCKH}	Test Clock (JTAG) Cycle High Time	12		ns
t_{TCKL}	Test Clock (JTAG) Cycle Low Time	12		ns

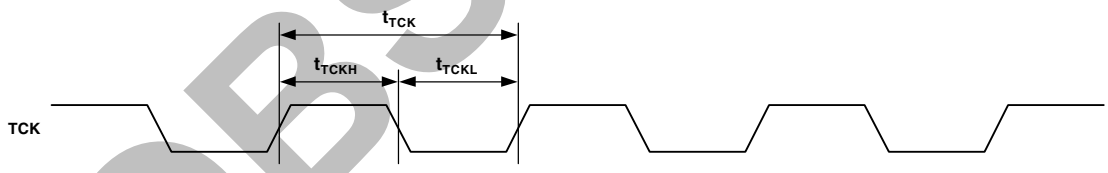


Figure 9. Reference Clocks—JTAG Test Clock (TCK) Cycle Time

Table 25. Power-Up Timing[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{VDD_DRAM}	V_{DD_DRAM} Stable After V_{DD}, V_{DD_A}, V_{DD_IO} Stable	>0		ms

[1] For information about power supply sequencing and monitoring solutions, please visit www.analog.com/sequencing.

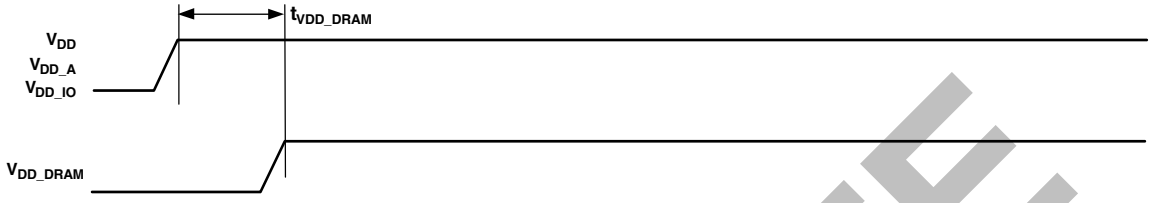


Figure 10. Power-Up Timing

Table 26. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{RST\_IN}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM}, SCLK, and Static/Strap Pins Stable	2		ms
$t_{TRST\_IN\_PWR}$[1]	$\overline{TRST}$ Asserted During Power-Up Reset	100 × t_{SCLK}		ns
Switching Characteristic				
$t_{RST\_OUT\_PWR}$	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM}, and SCLK are stable and before $\overline{RST\_IN}$ deasserted.

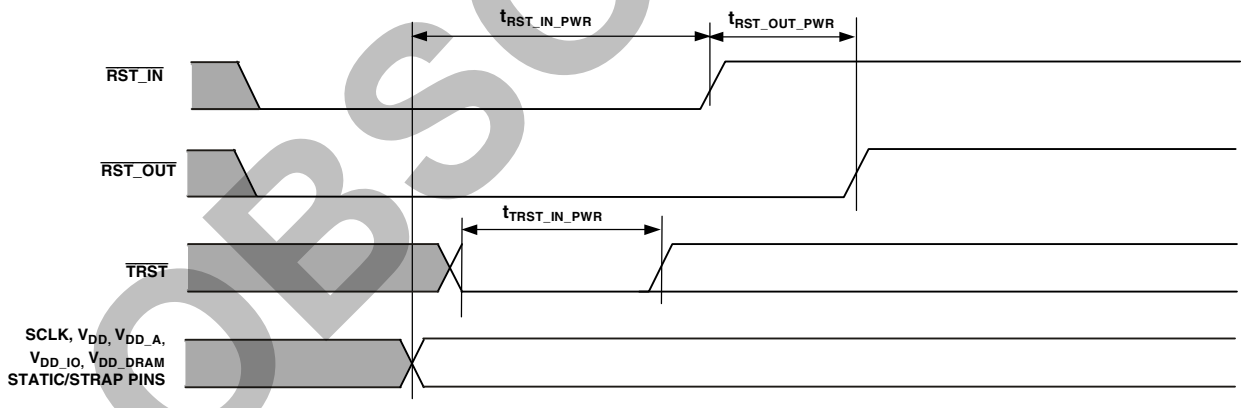


Figure 11. Power-Up Reset Timing

Table 27. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RST\_IN}$ Asserted	2		ms
t_{STRAP}	$\overline{RST\_IN}$ Deasserted After Strap Pins Stable	1.5		ms
Switching Characteristic				
t_{RST_OUT}	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

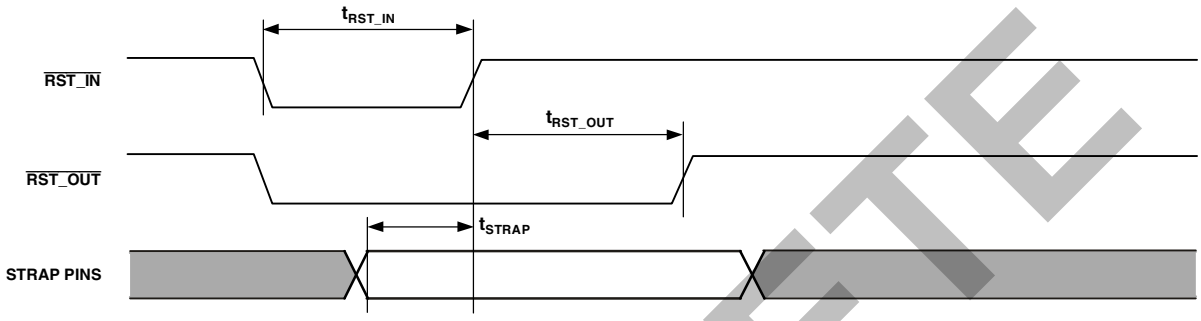


Figure 12. Normal Reset Timing

Table 28. On-Chip DRAM Refresh[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{REF}	On-chip DRAM Refresh Period		1.56	µs

[1] For more information on setting the refresh rate for the on-chip DRAM, refer to the *ADSP-TS201 TigerSHARC Processor Programming Reference*.

Table 29. AC Signal Specifications

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
ADDR31–0	External Address Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
DATA31–0	External Data Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSH}}$	Memory Select HOST Line	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSSD3–0}}$	Memory Select SDRAM Lines	1.5	0.5	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RD}}$	Memory Read	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRL}}$	Write Low Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
ACK	Acknowledge for Data High to Low	1.5	0.5	3.6	1.0	1.15	2.0	SCLK
	Acknowledge for Data Low to High	1.5	0.5	4.2	0.9	1.15	2.0	SCLK
SDCKE	SDRAM Clock Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RAS}}$	Row Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CAS}}$	Column Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
LDQM	Low Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
SDA10	SDRAM ADDR10	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{HBR}}$	Host Bus Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{HBG}}$	Host Bus Grant	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BOFF}}$	Back Off Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BRST}}$	Burst Pin	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request Pins	1.5	0.5	4.0	1.0	—	—	SCLK
$\overline{\text{BM}}$	Bus Master Debug Aid Only	—	—	4.0	1.0	—	—	SCLK
$\overline{\text{IORD}}$	I/O Read Pin	—	—	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{IOWR}}$	I/O Write Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{IOEN}}$	I/O Enable Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CPA}}$	Core Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	Core Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{DPA}}$	DMA Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	DMA Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{BMS}}$	Boot Memory Select	—	—	4.0	1.0	1.15	2.0	SCLK
FLAG3–0[2]	FLAG Pins	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RST\_IN}}$[3, 4]	Global Reset Pin	1.5	2.5	—	—	—	—	SCLK[5]
TMS	Test Mode Select (JTAG)	1.5	0.5	—	—	—	—	TCK
TDI	Test Data Input (JTAG)	1.5	0.5	—	—	—	—	TCK
TDO	Test Data Output (JTAG)	—	—	4.0	1.0	0.75	2.0	TCK[6]
$\overline{\text{TRST}}$[3, 4]	Test Reset (JTAG)	1.5	0.5	—	—	—	—	TCK
$\overline{\text{EMU}}$[7]	Emulation High to Low	—	—	5.5	2.0	1.15	4.0	TCK or SCLK
ID2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
CONTROLIMP1–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
DS2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
SCLKRAT2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—

Table 29. AC Signal Specifications (Continued)

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
ENEDREG	Static Pins—Must Be Connected to V_{SS}	—	—	—	—	—	—	—
STRAP SYS[9, 10]	Strap Pins	1.5	0.5	—	—	—	—	SCLK
JTAG SYS[11, 12]	JTAG System Pins	+2.5	+10.0	+12.0	–1.0	—	—	TCK

[1] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.
[2] For input specifications on FLAG3–0 pins, see Table 21.
[3] These input pins are asynchronous and therefore do not need to be synchronized to a clock reference.
[4] For additional requirement details, see Reset and Booting on Page 8.
[5] $\overline{\text{RST\_IN}}$ clock reference is the falling edge of SCLK.
[6] TDO output clock reference is the falling edge of TCK.
[7] Reference clock depends on function.
[8] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.
[9] STRAP pins include: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, $\overline{\text{L1BCMPO}}$, TM2, and TM3.
[10] Specifications applicable during reset only.
[11] JTAG system pins include: $\overline{\text{RST\_IN}}$, $\overline{\text{RST\_OUT}}$, $\overline{\text{POR\_IN}}$, $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, $\overline{\text{HBR}}$, $\overline{\text{BOFF}}$, $\overline{\text{MS1–0}}$, $\overline{\text{MSH}}$, SDCKE, LDQM, $\overline{\text{BMS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD}}$, $\overline{\text{BM}}$, $\overline{\text{EMU}}$, SDA10, $\overline{\text{IOEN}}$, $\overline{\text{BUSLOCK}}$, TMR0E, DATA31–0, ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WRL}}$, $\overline{\text{BRST}}$, $\overline{\text{MSSD3–0}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{HBG}}$, $\overline{\text{BR7–0}}$, FLAG3–0, L0DATOP3–0, L0DATON3–0, L1DATOP3–0, L1DATON3–0, L0CLKOUTP, L0CLKOUTN, L1CLKOUTP, L1CLKOUTN, L0ACKI, $\overline{\text{L1ACKI}}$, L0DATIP3–0, $\overline{\text{L0DATIN}}$3–0, L1DATIP3–0, L1DATIN3–0, L0CLKINP, L0CLKINN, L1CLKINP, L1CLKINN, L0ACKO, L1ACKO, ACK, $\overline{\text{CPA}}$, $\overline{\text{DPA}}$, $\overline{\text{L0BCMPO}}$, $\overline{\text{L1BCMPO}}$, $\overline{\text{L0BCMPI}}$, $\overline{\text{L1BCMPI}}$, ID2–0, CTRL_IMPD1–0, SCLKRAT2–0, DS2–0, ENEDREG, TM2, TM3, TM4.
[12] JTAG system output timing clock reference is the falling edge of TCK.

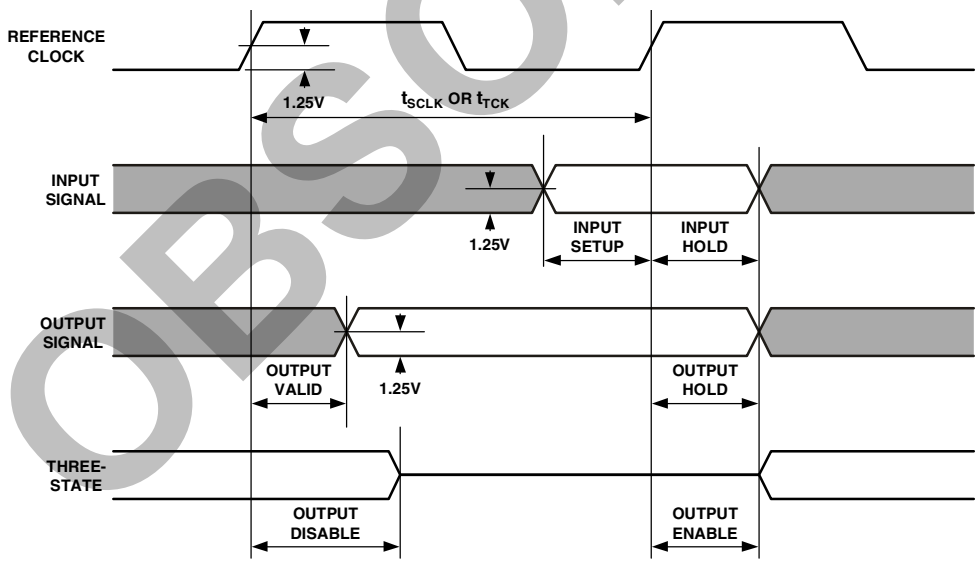


Figure 13. General AC Parameters Timing

Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing

Table 30 and Table 31 with Figure 14 provide the electrical characteristics for the LVDS link ports. The LVDS link port signal definitions represent all differential signals with a V_{OD} = 0 V level and use signal naming without N (negative) and P (positive) suffixes (see Figure 15).

Table 30. Link Port LVDS Transmit Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	Output Voltage High, V_{O_P} or V_{O_N}	R_L = 100 Ω		1.85	V
V_{OL}	Output Voltage Low, V_{O_P} or V_{O_N}	R_L = 100 Ω	0.92		V
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100 Ω	300	650	mV
I_{OS}	Short-Circuit Output Current	V_{O_P} or V_{O_N} = 0 V		+5/–55	mA
		V_{OD} = 0 V		±10	mA
V_{OCM}	Common-Mode Output Voltage		1.20	1.50	V

Table 31. Link Port LVDS Receive Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$\|V_{ID}\|$	Differential Input Voltage	$t_{LDIS}/t_{LDIH} \geq 0.20$ ns	250	850	mV
		$t_{LDIS}/t_{LDIH} \geq 0.25$ ns	217	850	mV
		$t_{LDIS}/t_{LDIH} \geq 0.30$ ns	206	850	mV
		$t_{LDIS}/t_{LDIH} \geq 0.35$ ns	195	850	mV
V_{ICM}	Common-Mode Input Voltage		0.6	1.57	V

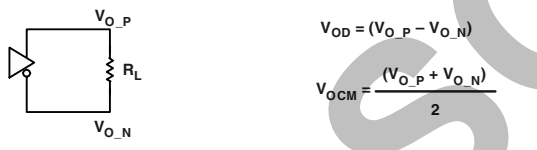


Figure 14. Link Ports—Transmit Electrical Characteristics

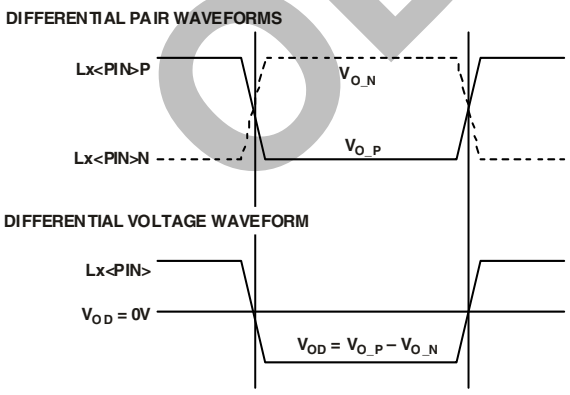


Figure 15. Link Ports—Signals Definition

Link Port—Data Out Timing

Table 32 with Figure 16, Figure 17, Figure 18, Figure 19, Figure 20, and Figure 21 provide the data out timing for the LVDS link ports.

Table 32. Link Port—Data Out Timing

Parameter	Description	Min	Max	Unit
Outputs				
t_{REO}	Rising Edge (Figure 17)		350	ps
t_{FEO}	Falling Edge (Figure 17)		350	ps
t_{LCLKOP}	LxCLKOUT Period (Figure 16)	Greater of 4.0 or $0.9 \times LCR \times t_{CCLK}$ [1, 2, 3]	Smaller of 12.5 or $1.1 \times LCR \times t_{CCLK}$ [1, 2, 3]	ns
t_{LCLKOH}	LxCLKOUT High (Figure 16)	$0.4 \times t_{LCLKOP}$ [1]	$0.6 \times t_{LCLKOP}$ [1]	ns
t_{LCLKOL}	LxCLKOUT Low (Figure 16)	$0.4 \times t_{LCLKOP}$ [1]	$0.6 \times t_{LCLKOP}$ [1]	ns
t_{COJT}	LxCLKOUT Jitter (Figure 16)		±150 [4, 5, 6]	ps
			±250 [7]	ps
t_{LDOS}	LxDATO Output Setup (Figure 18)	$0.25 \times LCR \times t_{CCLK} - 0.10 \times t_{CCLK}$ [1, 4, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.15 \times t_{CCLK}$ [1, 5, 6, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.30 \times t_{CCLK}$ [1, 7, 8]		ns
t_{LDOH}	LxDATO Output Hold (Figure 18)	$0.25 \times LCR \times t_{CCLK} - 0.10 \times t_{CCLK}$ [1, 4, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.15 \times t_{CCLK}$ [1, 5, 6, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.30 \times t_{CCLK}$ [1, 7, 8]		ns
t_{LACKID}	Delay from LxACKI rising edge to first transmission clock edge (Figure 19)		$16 \times LCR \times t_{CCLK}$ [1, 2]	ns
t_{BCMPOV}	$\overline{\text{LxBCMPO}}$ Valid (Figure 19)		$2 \times LCR \times t_{CCLK}$ [1, 2]	ns
t_{BCMPOH}	$\overline{\text{LxBCMPO}}$ Hold (Figure 20)	$3 \times TSW - 0.5$ [1, 9]		ns
Inputs				
t_{LACKIS}	LxACKI low setup to guarantee that the transmitter stops transmitting (Figure 20)			
	LxACKI high setup to guarantee that the transmitter continues its transmission without any interruption (Figure 21)	$16 \times LCR \times t_{CCLK}$ [1, 2]		ns
t_{LACKIH}	LxACKI High Hold Time (Figure 21)	0.51		ns

[1] Timing is relative to the 0 differential voltage ($V_{OD} = 0$).
[2] LCR (link port clock ratio) = 1, 1.5, 2, or 4. t_{CCLK} is the core period.
[3] For the cases of t_{LCLKOP} = 4.0 ns and t_{LCLKOP} = 12.5 ns, the effect of t_{COJT} specification on output period must be considered.
[4] LCR = 1.
[5] LCR = 1.5.
[6] LCR = 2.
[7] LCR = 4.
[8] The t_{LDOS} and t_{LDOH} values include LCLKOUT jitter.
[9] TSW is a short-word transmission period. For a 4-bit link, it is $2 \times LCR \times t_{CCLK}$. For a 1-bit link, it is $8 \times LCR \times t_{CCLK}$ ns.

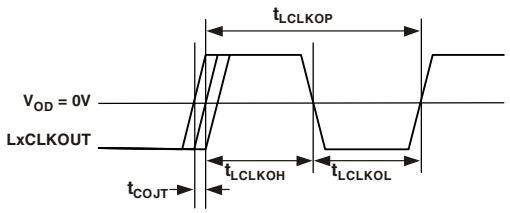


Figure 16. Link Ports—Output Clock

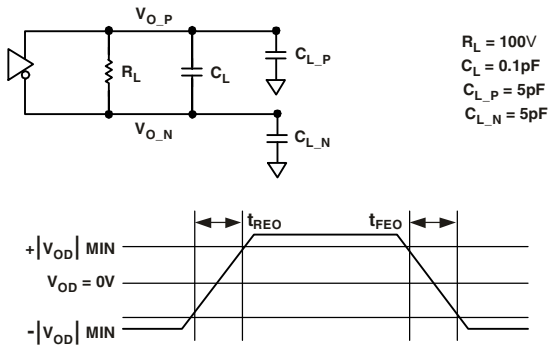


Figure 17. Link Ports—Differential Output Signals Transition Time

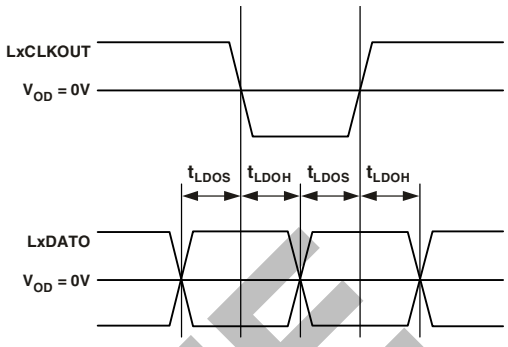


Figure 18. Link Ports—Data Output Setup and Hold[1]

[1] These parameters are valid for both clock edges.

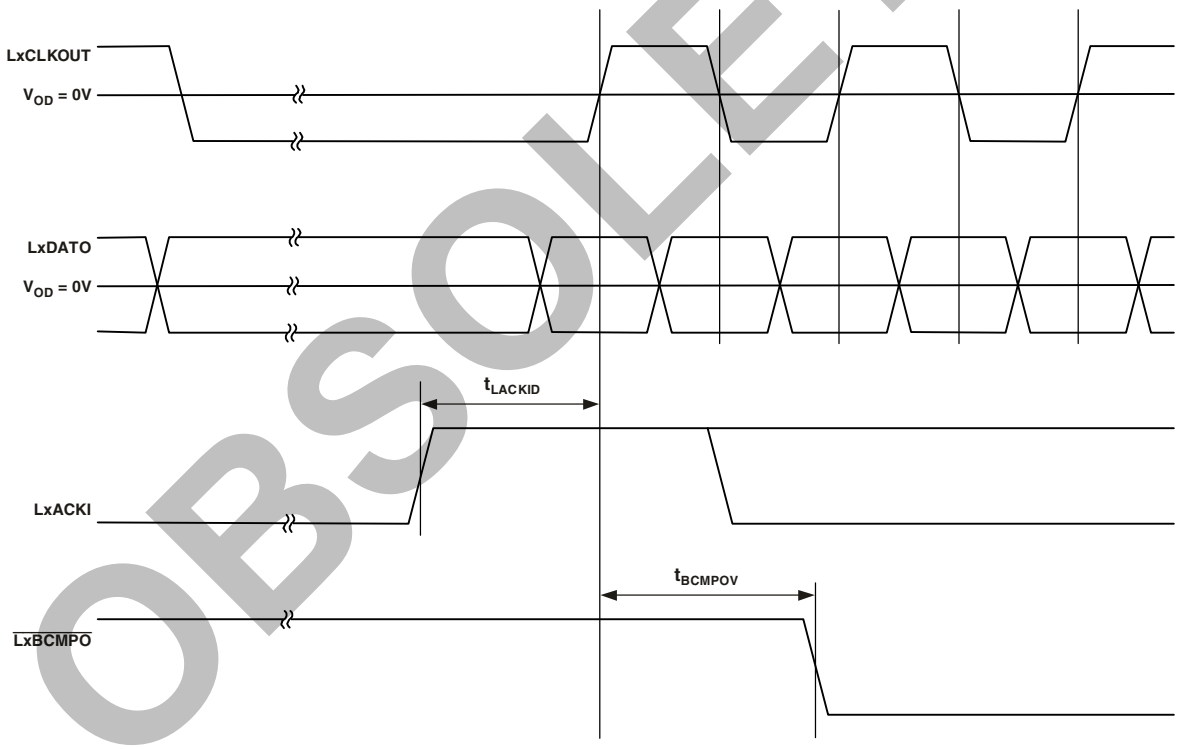


Figure 19. Link Ports—Transmission Start

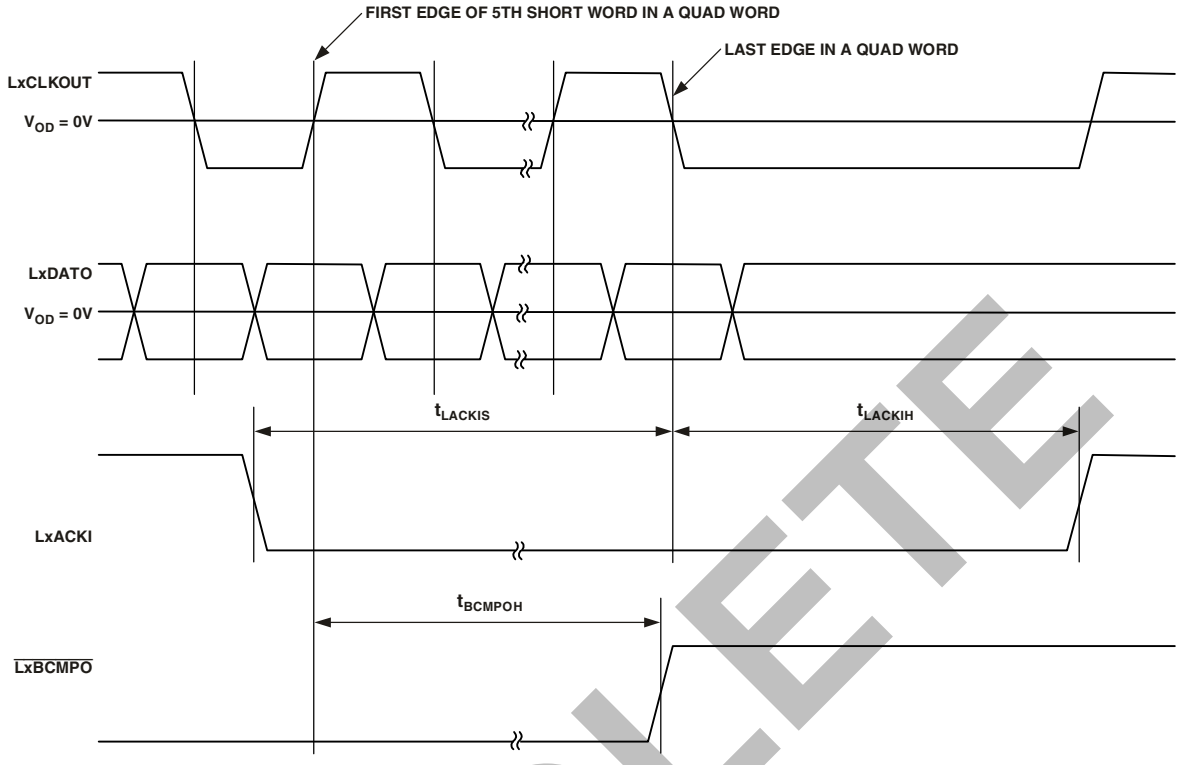


Figure 20. Link Ports—Transmission End and Stops

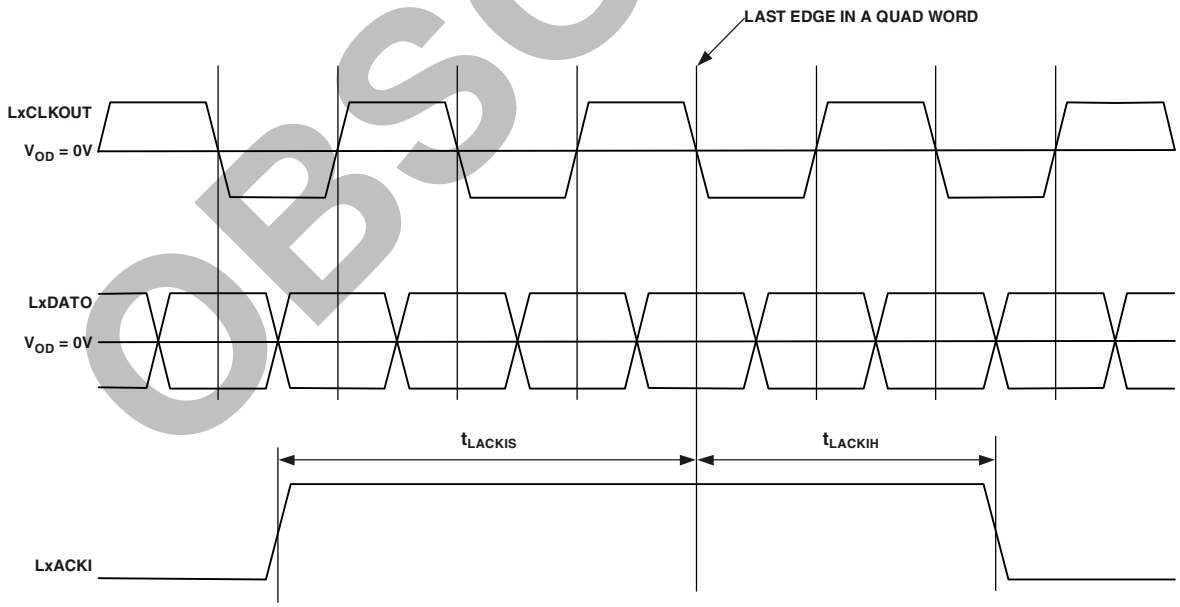


Figure 21. Link Ports—Back to Back Transmission

Link Port—Data In Timing

Table 33 with Figure 22 and Figure 23 provide the data in timing for the LVDS link ports.

Table 33. Link Port—Data In Timing

Parameter	Description	Min	Max	Unit
Inputs				
t_{LCLKIP}	LxCLKIN Period (Figure 23)	Greater of 1.8 or 0.9 × t_{CCLK}[1]	12.5	ns
t_{LDIS}	LxDATI Input Setup (Figure 23)	0.20[1, 2]		ns
		0.25[1, 3]		ns
		0.30[1, 4]		ns
		0.35[1, 5]		ns
t_{LDIH}	LxDATI Input Hold (Figure 23)	0.20[1, 2]		ns
		0.25[1, 3]		ns
		0.30[1, 4]		ns
		0.35[1, 5]		ns
t_{BCMPIS}	$\overline{\text{LxBCMPI}}$ Setup (Figure 22)	2 × t_{LCLKIP}[1]		ns
t_{BCMPIH}	$\overline{\text{LxBCMPI}}$ Hold (Figure 22)	2 × t_{LCLKIP}[1]		ns

[1] Timing is relative to the 0 differential voltage (V_{OD} = 0).
[2] $|V_{ID}|$ = 250 mV.
[3] $|V_{ID}|$ = 217 mV.
[4] $|V_{ID}|$ = 206 mV.
[5] $|V_{ID}|$ = 195 mV.

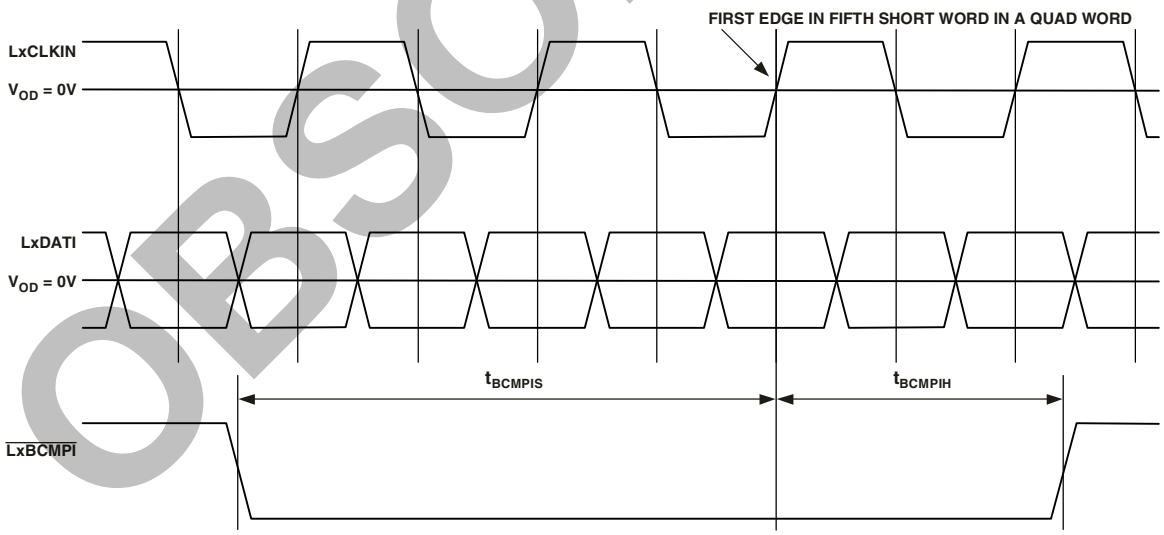


Figure 22. Link Ports—Last Received Quad Word

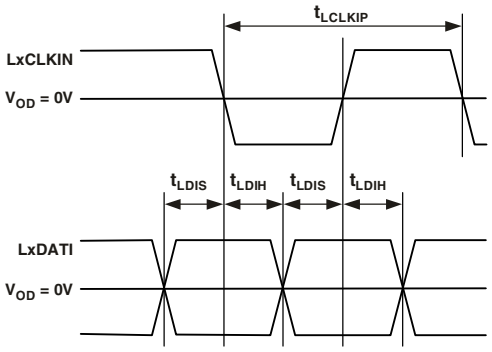


Figure 23. Link Ports—Data Input Setup and Hold[1]

[1] These parameters are valid for both clock edges.

OUTPUT DRIVE CURRENTS

Figure 24 through Figure 31 show typical I–V characteristics for the output drivers of the ADSP-TS203S processor. The curves in these diagrams represent the current drive capability of the output drivers as a function of output voltage over the range of drive strengths. For complete output driver characteristics, refer to the processor's IBIS models, available on the Analog Devices website (www.analog.com).

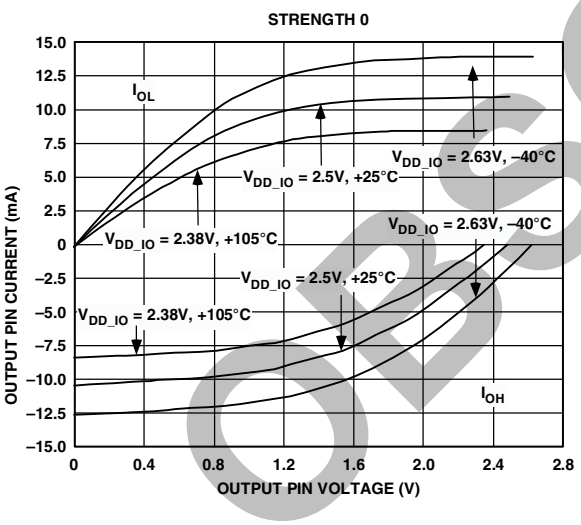


Figure 24. Typical Drive Currents at Strength 0

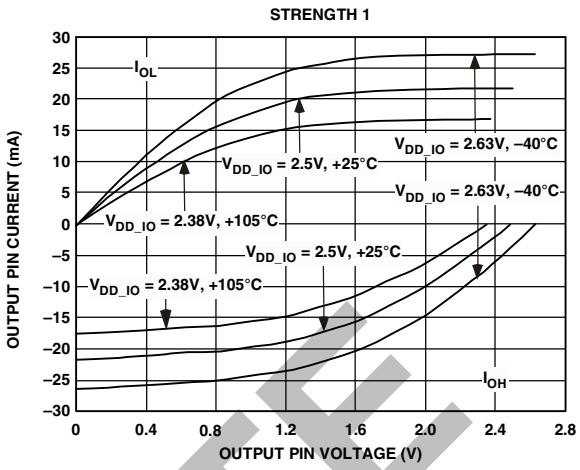


Figure 25. Typical Drive Currents at Strength 1

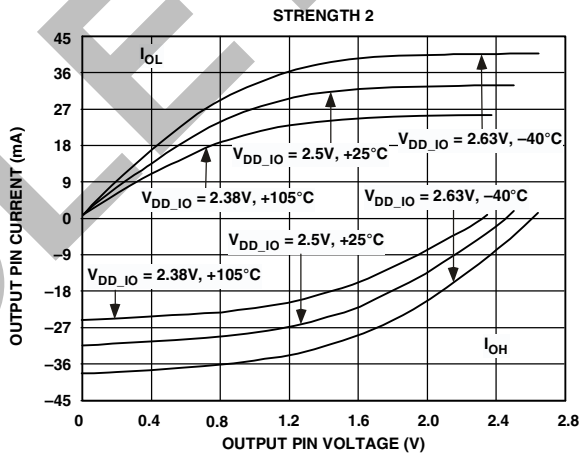


Figure 26. Typical Drive Currents at Strength 2

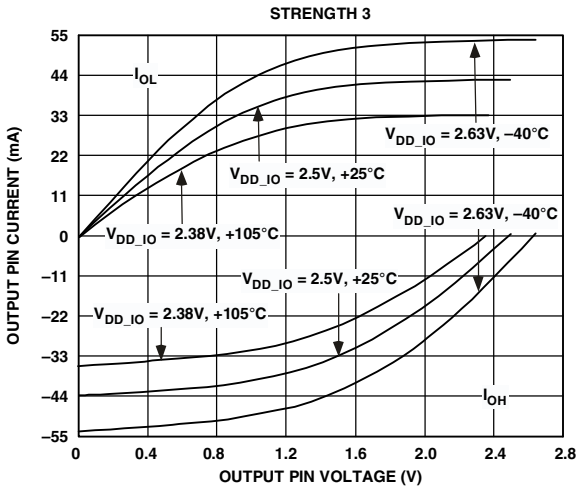


Figure 27. Typical Drive Currents at Strength 3

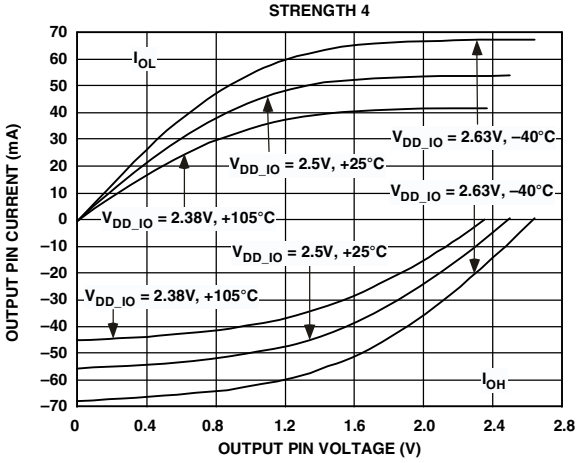


Figure 28. Typical Drive Currents at Strength 4

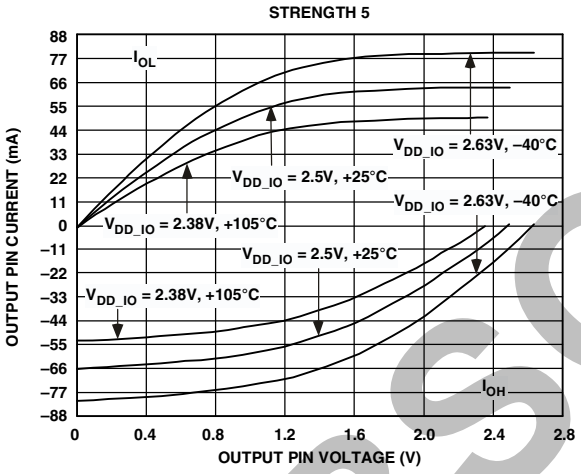


Figure 29. Typical Drive Currents at Strength 5

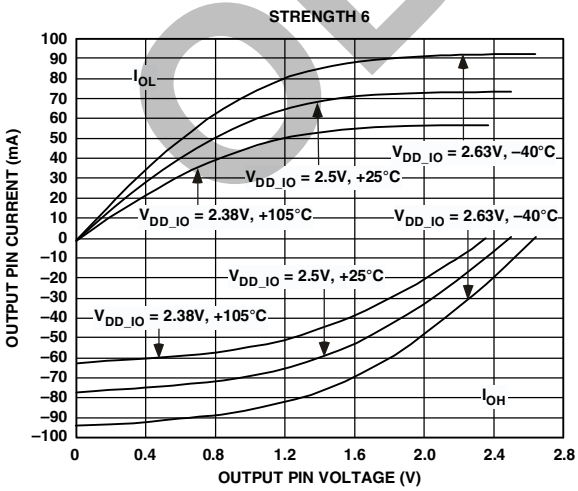


Figure 30. Typical Drive Currents at Strength 6

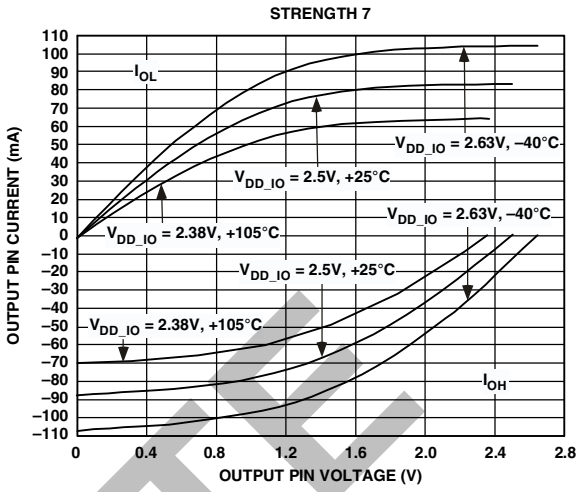


Figure 31. Typical Drive Currents at Strength 7

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 29 on Page 27. These include output disable time, output enable time, and capacitive loading. The timing specifications for the processor apply for the voltage reference levels in Figure 32.

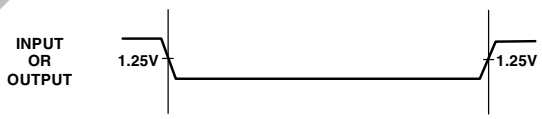


Figure 32. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED\_DIS}$ and t_{DECAY} as shown in Figure 33. The time $t_{MEASURED\_DIS}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.4 V.

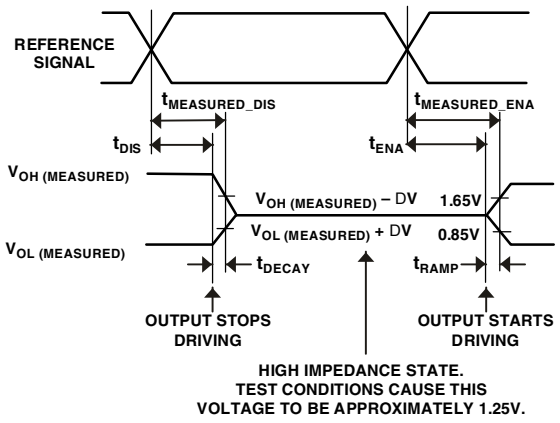


Figure 33. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The time for the voltage on the bus to ramp by ΔV is dependent on the capacitive load, C_L, and the drive current, I_D. This ramp time can be approximated by the following equation:

$$t_{RAMP} = (C_L \Delta V)/I_D$$

The output enable time t_{ENA} is the difference between $t_{MEASURED\_ENA}$ and t_{RAMP} as shown in Figure 33. The time $t_{MEASURED\_ENA}$ is the interval from when the reference signal switches to when the output voltage ramps ΔV from the measured three-stated output level. t_{RAMP} is calculated with test load C_L, drive current I_D, and with ΔV equal to 0.4 V.

Capacitive Loading

Output valid and hold are based on standard capacitive loads: 30 pF on all pins (see Figure 34). The delay and hold specifications given should be derated by a drive strength related factor for loads other than the nominal value of 30 pF. Figure 35 through Figure 42 show how output rise time varies with capacitance. Figure 43 graphically shows how output valid varies with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 35.) The graphs of Figure 35 through Figure 43 may not be linear outside the ranges shown.

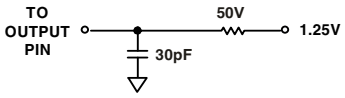


Figure 34. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

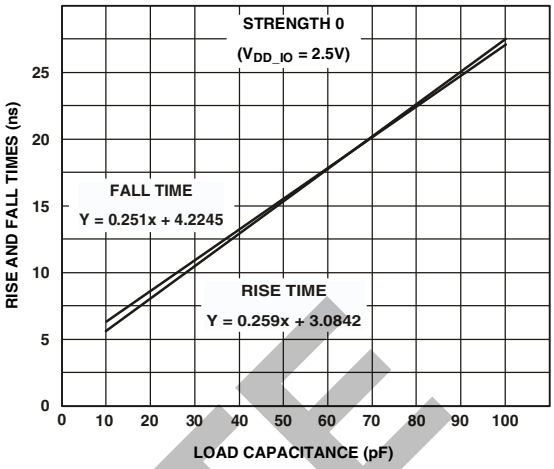


Figure 35. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 0

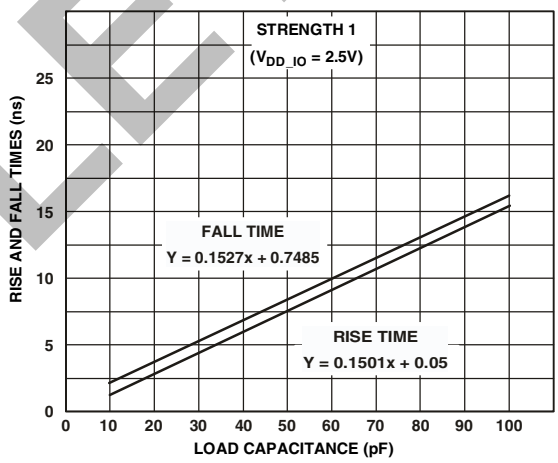


Figure 36. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 1

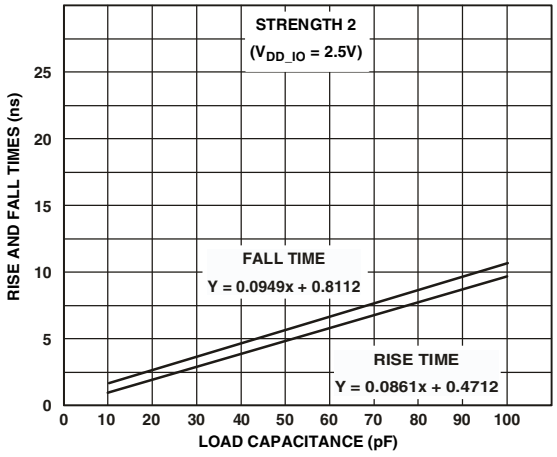


Figure 37. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 2

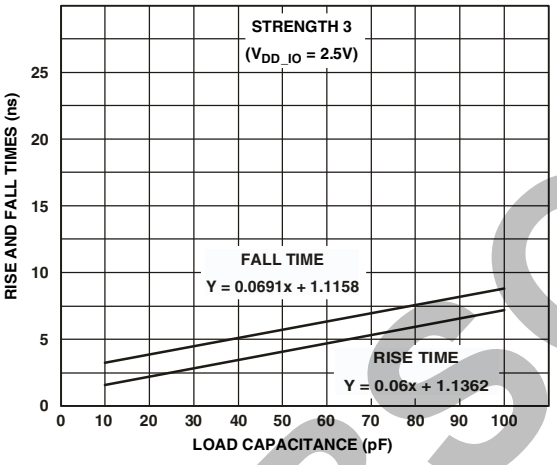


Figure 38. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 3

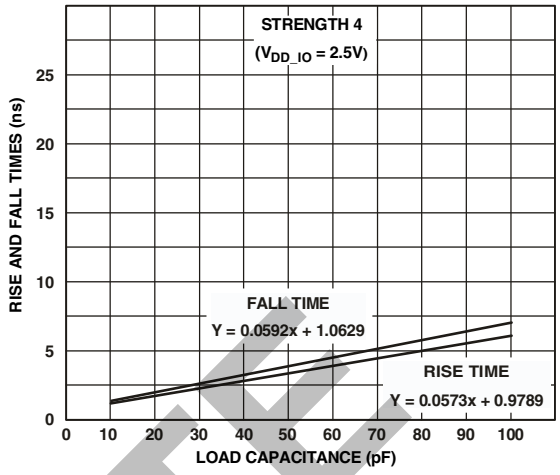


Figure 39. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 4

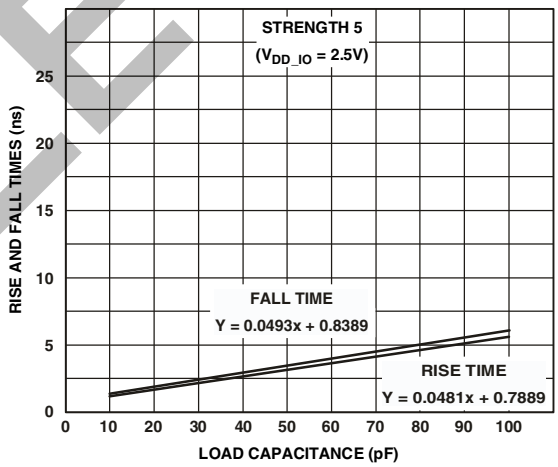


Figure 40. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 5

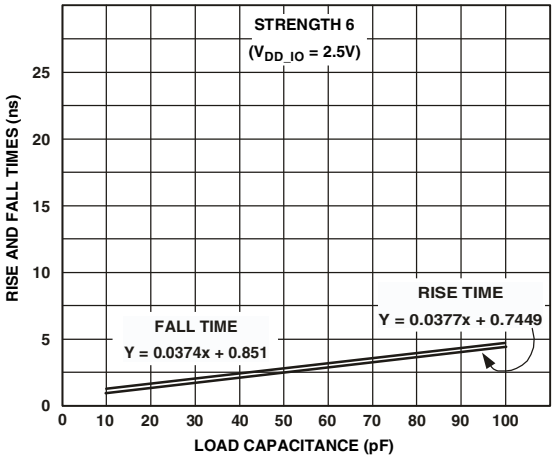


Figure 41. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 6

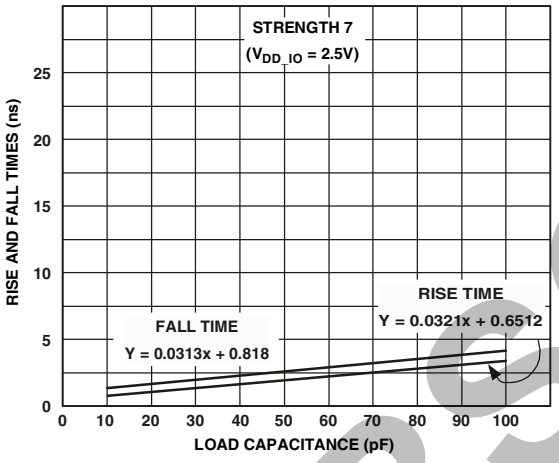


Figure 42. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 7

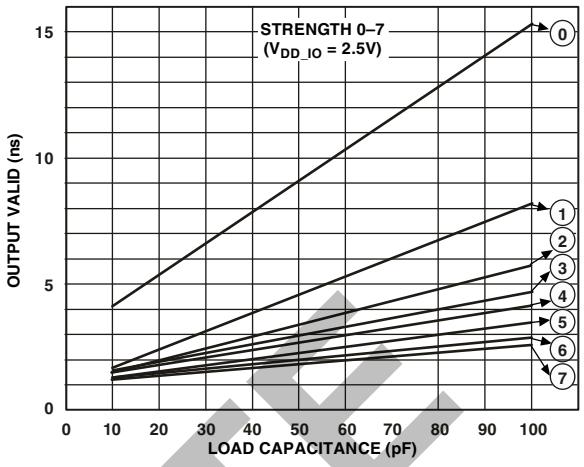


Figure 43. Typical Output Valid (V_{DD_IO} = 2.5 V) vs. Load Capacitance at Max Case Temperature and Strength 0 to 7[1]

[1] The line equations for the output valid vs. load capacitance are:
Strength 0: y = 0.0956x + 3.5662
Strength 1: y = 0.0523x + 3.2144
Strength 2: y = 0.0433x + 3.1319
Strength 3: y = 0.0391x + 2.9675
Strength 4: y = 0.0393x + 2.7653
Strength 5: y = 0.0373x + 2.6515
Strength 6: y = 0.0379x + 2.1206
Strength 7: y = 0.0399x + 1.9080

ENVIRONMENTAL CONDITIONS

The ADSP-TS203S processor is rated for performance under T_{CASE} environmental conditions specified in the Operating Conditions on Page 20.

Thermal Characteristics

The ADSP-TS203S processor is packaged in a 25 mm × 25 mm, thermally enhanced ball grid array (BGA_ED). The processor is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heat sink and/or an air flow source may be required. Table 34 shows the thermal characteristics of the BGA_ED package. All parameters are based on a JESD51-9 four-layer 2s2p board. All data are based on 3 W power dissipation.

Table 34. Thermal Characteristics

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow = 0 m/s	12.9[2]	°C/W
	Airflow = 1 m/s	10.2	°C/W
	Airflow = 2 m/s	9.0	°C/W
	Airflow = 3 m/s	8.0	°C/W
θ_{JB}[3]	—	7.7	°C/W
θ_{JC}[4]	—	0.7	°C/W

[1] θ_{JA} measured per JEDEC standard JESD51-6.
[2] θ_{JA} = 12.9°C/W for 0 m/s is for vertically mounted boards. For horizontally mounted boards, use 17.0°C/W for 0 m/s.
[3] θ_{JB} measured per JEDEC standard JESD51-9.
[4] θ_{JC} measured by cold plate test method (no approved JEDEC standard).

576-BALL BGA_ED PIN CONFIGURATIONS

Figure 44 shows a summary of pin configurations for the 576-ball BGA_ED package, and Table 35 lists the signal-to-ball assignments.

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	V_{SS}	B1	NC	C1	V_{SS}	D1	NC
A2	NC	B2	V_{SS}	C2	V_{SS}	D2	NC
A3	V_{SS}	B3	V_{SS}	C3	V_{SS}	D3	NC
A4	NC	B4	NC	C4	NC	D4	V_{SS}
A5	NC	B5	NC	C5	NC	D5	NC
A6	NC	B6	NC	C6	NC	D6	NC
A7	NC	B7	NC	C7	NC	D7	NC
A8	NC	B8	NC	C8	NC	D8	NC
A9	DATA29	B9	DATA30	C9	DATA31	D9	NC
A10	DATA25	B10	DATA26	C10	DATA27	D10	DATA28
A11	DATA23	B11	DATA24	C11	DATA21	D11	DATA22
A12	DATA19	B12	DATA20	C12	DATA17	D12	DATA18
A13	DATA15	B13	DATA16	C13	V_{SS}	D13	V_{SS}
A14	DATA11	B14	DATA12	C14	DATA13	D14	DATA14
A15	DATA9	B15	DATA10	C15	DATA7	D15	DATA8
A16	DATA5	B16	DATA6	C16	DATA3	D16	DATA4
A17	DATA1	B17	DATA2	C17	ACK	D17	DATA0
A18	$\overline{WRL}$	B18	TM4	C18	$\overline{RD}$	D18	$\overline{BRST}$
A19	ADDR30	B19	ADDR31	C19	ADDR26	D19	ADDR27
A20	ADDR28	B20	ADDR29	C20	ADDR24	D20	ADDR25
A21	ADDR22	B21	ADDR23	C21	ADDR20	D21	V_{SS}
A22	V_{SS}	B22	V_{SS}	C22	V_{SS}	D22	ADDR19
A23	ADDR21	B23	V_{SS}	C23	V_{DD_IO}	D23	ADDR17
A24	V_{SS}	B24	ADDR18	C24	V_{DD_IO}	D24	ADDR16

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
E1	NC	F1	NC	G1	$\overline{\text{MSSD1}}$	H1	V_{SS}
E2	NC	F2	$\overline{\text{MS1}}$	G2	V_{SS}	H2	$\overline{\text{MSH}}$
E3	NC	F3	NC	G3	$\overline{\text{MS0}}$	H3	$\overline{\text{MSSD3}}$
E4	NC	F4	NC	G4	$\overline{\text{BMS}}$	H4	SCLKRAT0
E5	V_{SS}	F5	V_{DD_IO}	G5	V_{SS}	H5	V_{DD_IO}
E6	V_{DD_IO}	F6	V_{DD}	G6	V_{DD}	H6	V_{DD}
E7	V_{SS}	F7	V_{DD}	G7	V_{DD}	H7	V_{DD}
E8	V_{DD_IO}	F8	V_{DD}	G8	V_{DD}	H8	V_{SS}
E9	V_{SS}	F9	V_{DD}	G9	V_{DD}	H9	V_{SS}
E10	V_{DD_IO}	F10	V_{DD}	G10	V_{DD}	H10	V_{SS}
E11	V_{DD_IO}	F11	V_{DD_DRAM}	G11	V_{DD_DRAM}	H11	V_{SS}
E12	V_{DD_IO}	F12	V_{DD_DRAM}	G12	V_{DD_DRAM}	H12	V_{SS}
E13	V_{DD_IO}	F13	V_{DD}	G13	V_{DD}	H13	V_{SS}
E14	V_{DD_IO}	F14	V_{DD}	G14	V_{DD}	H14	V_{SS}
E15	V_{DD_IO}	F15	V_{DD_DRAM}	G15	V_{DD_DRAM}	H15	V_{SS}
E16	V_{SS}	F16	V_{DD_DRAM}	G16	V_{DD_DRAM}	H16	V_{SS}
E17	V_{DD_IO}	F17	V_{DD}	G17	V_{DD}	H17	V_{SS}
E18	V_{SS}	F18	V_{DD}	G18	V_{DD}	H18	V_{DD}
E19	V_{DD_IO}	F19	V_{DD}	G19	V_{DD}	H19	V_{DD}
E20	V_{SS}	F20	V_{DD_IO}	G20	V_{DD_IO}	H20	V_{DD_IO}
E21	ADDR15	F21	ADDR13	G21	ADDR7	H21	ADDR3
E22	ADDR14	F22	ADDR12	G22	ADDR6	H22	ADDR2
E23	ADDR11	F23	ADDR9	G23	ADDR5	H23	ADDR1
E24	ADDR10	F24	ADDR8	G24	ADDR4	H24	ADDR0

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
J1	$\overline{RAS}$	K1	SDA10	L1	$\overline{SDWE}$	M1	$\overline{BR3}$
J2	$\overline{CAS}$	K2	SDCKE	L2	$\overline{BR0}$	M2	SCLKRAT1
J3	V_{SS}	K3	LDQM	L3	$\overline{BR1}$	M3	$\overline{BR5}$
J4	V_{REF}	K4	NC	L4	$\overline{BR2}$	M4	$\overline{BR6}$
J5	V_{SS}	K5	V_{DD_IO}	L5	V_{DD_IO}	M5	V_{DD_IO}
J6	V_{DD}	K6	V_{DD}	L6	V_{DD}	M6	V_{DD}
J7	V_{DD}	K7	V_{DD}	L7	V_{DD}	M7	V_{DD}
J8	V_{SS}	K8	V_{SS}	L8	V_{SS}	M8	V_{SS}
J9	V_{SS}	K9	V_{SS}	L9	V_{SS}	M9	V_{SS}
J10	V_{SS}	K10	V_{SS}	L10	V_{SS}	M10	V_{SS}
J11	V_{SS}	K11	V_{SS}	L11	V_{SS}	M11	V_{SS}
J12	V_{SS}	K12	V_{SS}	L12	V_{SS}	M12	V_{SS}
J13	V_{SS}	K13	V_{SS}	L13	V_{SS}	M13	V_{SS}
J14	V_{SS}	K14	V_{SS}	L14	V_{SS}	M14	V_{SS}
J15	V_{SS}	K15	V_{SS}	L15	V_{SS}	M15	V_{SS}
J16	V_{SS}	K16	V_{SS}	L16	V_{SS}	M16	V_{SS}
J17	V_{SS}	K17	V_{SS}	L17	V_{SS}	M17	V_{SS}
J18	V_{DD}	K18	V_{DD_DRAM}	L18	V_{DD_DRAM}	M18	V_{DD}
J19	V_{DD}	K19	V_{DD_DRAM}	L19	V_{DD_DRAM}	M19	V_{DD}
J20	V_{SS}	K20	V_{DD_IO}	L20	V_{DD_IO}	M20	V_{DD_IO}
J21	L0ACKO	K21	L0DATI1_N	L21	L0DATI3_N	M21	V_{SS}
J22	$\overline{L0BCMPI}$	K22	L0DATI1_P	L22	L0DATI3_P	M22	V_{SS}
J23	L0DATI0_N	K23	L0CLKINN	L23	L0DATI2_N	M23	L0DATO3_N
J24	L0DATI0_P	K24	L0CLKINP	L24	L0DATI2_P	M24	L0DATO3_P

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
N1	ID0	P1	SCLK	R1	V_{SS}	T1	$\overline{RST\_IN}$
N2	V_{SS}	P2	SCLK_VREF	R2	NC (SCLK)[1]	T2	SCLKRAT2
N3	V_{DD_A}	P3	V_{SS}	R3	NC (SCLK_VREF)[1]	T3	$\overline{BR4}$
N4	V_{DD_A}	P4	$\overline{BM}$	R4	$\overline{BR7}$	T4	DS0
N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD_IO}	T5	V_{SS}
N6	V_{DD}	P6	V_{DD}	R6	V_{DD}	T6	V_{DD}
N7	V_{DD}	P7	V_{DD}	R7	V_{DD}	T7	V_{DD}
N8	V_{SS}	P8	V_{SS}	R8	V_{SS}	T8	V_{SS}
N9	V_{SS}	P9	V_{SS}	R9	V_{SS}	T9	V_{SS}
N10	V_{SS}	P10	V_{SS}	R10	V_{SS}	T10	V_{SS}
N11	V_{SS}	P11	V_{SS}	R11	V_{SS}	T11	V_{SS}
N12	V_{SS}	P12	V_{SS}	R12	V_{SS}	T12	V_{SS}
N13	V_{SS}	P13	V_{SS}	R13	V_{SS}	T13	V_{SS}
N14	V_{SS}	P14	V_{SS}	R14	V_{SS}	T14	V_{SS}
N15	V_{SS}	P15	V_{SS}	R15	V_{SS}	T15	V_{SS}
N16	V_{SS}	P16	V_{SS}	R16	V_{SS}	T16	V_{SS}
N17	V_{SS}	P17	V_{SS}	R17	V_{SS}	T17	V_{SS}
N18	V_{DD}	P18	V_{DD_DRAM}	R18	V_{DD_DRAM}	T18	V_{DD}
N19	V_{DD}	P19	V_{DD_DRAM}	R19	V_{DD_DRAM}	T19	V_{DD}
N20	V_{DD_IO}	P20	V_{DD_IO}	R20	V_{DD_IO}	T20	V_{SS}
N21	L0DATO2_N	P21	L0DATO1_N	R21	NC	T21	L1DATI0_N
N22	L0DATO2_P	P22	L0DATO1_P	R22	V_{SS}	T22	L1DATI0_P
N23	L0CLKON	P23	L0DATO0_N	R23	$\overline{L0BCMPO}$	T23	L1ACKO
N24	L0CLKOP	P24	L0DATO0_P	R24	L0ACKI	T24	$\overline{L1BCMPI}$

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
U1	$\overline{\text{MSSD0}}$	V1	$\overline{\text{MSSD2}}$	W1	CONTROLIMP0	Y1	$\overline{\text{EMU}}$
U2	$\overline{\text{RST\_OUT}}$	V2	DS2	W2	ENEDREG	Y2	TCK
U3	ID2	V3	$\overline{\text{POR\_IN}}$	W3	TDI	Y3	TMR0E
U4	DS1	V4	CONTROLIMP1	W4	TDO	Y4	FLAG3
U5	V_{DD_IO}	V5	V_{SS}	W5	V_{DD_IO}	Y5	V_{SS}
U6	V_{DD}	V6	V_{DD}	W6	V_{DD}	Y6	V_{DD_IO}
U7	V_{DD}	V7	V_{DD}	W7	V_{DD}	Y7	V_{SS}
U8	V_{SS}	V8	V_{DD}	W8	V_{DD}	Y8	V_{DD_IO}
U9	V_{SS}	V9	V_{DD}	W9	V_{DD}	Y9	V_{SS}
U10	V_{DD}	V10	V_{DD}	W10	V_{DD}	Y10	V_{DD_IO}
U11	V_{DD_DRAM}	V11	V_{DD_DRAM}	W11	V_{DD_DRAM}	Y11	V_{DD_IO}
U12	V_{SS}	V12	V_{DD_DRAM}	W12	V_{DD_DRAM}	Y12	V_{DD_IO}
U13	V_{SS}	V13	V_{DD}	W13	V_{DD}	Y13	V_{DD_IO}
U14	V_{SS}	V14	V_{DD}	W14	V_{DD}	Y14	V_{DD_IO}
U15	V_{SS}	V15	V_{DD_DRAM}	W15	V_{DD_DRAM}	Y15	V_{DD_IO}
U16	V_{SS}	V16	V_{DD_DRAM}	W16	V_{DD_DRAM}	Y16	V_{SS}
U17	V_{SS}	V17	V_{DD}	W17	V_{DD}	Y17	V_{DD_IO}
U18	V_{DD}	V18	V_{DD}	W18	V_{DD}	Y18	V_{SS}
U19	V_{DD}	V19	V_{DD}	W19	V_{DD}	Y19	V_{DD_IO}
U20	V_{DD_IO}	V20	V_{DD_IO}	W20	V_{DD_IO}	Y20	V_{SS}
U21	L1CLKINN	V21	L1DATI3_N	W21	L1CLKON	Y21	L1DATO1_N
U22	L1CLKINP	V22	L1DATI3_P	W22	L1CLKOP	Y22	L1DATO1_P
U23	L1DATI1_N	V23	L1DATI2_N	W23	L1DATO3_N	Y23	L1DATO2_N
U24	L1DATI1_P	V24	L1DATI2_P	W24	L1DATO3_P	Y24	L1DATO2_P

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
AA1	FLAG2	AB1	V_{SS}	AC1	FLAG0	AD1	V_{SS}
AA2	FLAG1	AB2	V_{SS}	AC2	V_{SS}	AD2	ID1
AA3	$\overline{IRQ3}$	AB3	V_{SS}	AC3	V_{DD_IO}	AD3	V_{DD_IO}
AA4	V_{SS}	AB4	NC	AC4	TMS	AD4	$\overline{TRST}$
AA5	$\overline{IRQ0}$	AB5	$\overline{IRQ2}$	AC5	$\overline{IOWR}$	AD5	$\overline{IORD}$
AA6	$\overline{IOEN}$	AB6	$\overline{IRQ1}$	AC6	$\overline{DMAR2}$	AD6	$\overline{DMAR3}$
AA7	$\overline{DMAR0}$	AB7	$\overline{DMAR1}$	AC7	$\overline{CPA}$	AD7	$\overline{DPA}$
AA8	$\overline{HBR}$	AB8	$\overline{HBG}$	AC8	$\overline{BOFF}$	AD8	$\overline{BUSLOCK}$
AA9	TM3	AB9	V_{DD_IO}	AC9	NC	AD9	NC
AA10	NC	AB10	NC	AC10	NC	AD10	NC
AA11	NC	AB11	NC	AC11	NC	AD11	NC
AA12	V_{SS}	AB12	V_{SS}	AC12	V_{DD_IO}	AD12	V_{DD_IO}
AA13	V_{DD_IO}	AB13	V_{DD_IO}	AC13	V_{SS}	AD13	V_{DD_IO}
AA14	V_{DD_IO}	AB14	V_{DD_IO}	AC14	V_{DD_IO}	AD14	V_{DD_IO}
AA15	NC	AB15	V_{SS}	AC15	NC	AD15	V_{SS}
AA16	NC	AB16	NC	AC16	TM2	AD16	V_{DD_IO}
AA17	NC	AB17	NC	AC17	NC	AD17	NC
AA18	NC	AB18	NC	AC18	NC	AD18	NC
AA19	V_{SS}	AB19	V_{DD_IO}	AC19	V_{DD_IO}	AD19	V_{DD_IO}
AA20	V_{DD_IO}	AB20	V_{DD_IO}	AC20	V_{DD_IO}	AD20	V_{DD_IO}
AA21	V_{SS}	AB21	NC	AC21	V_{DD_IO}	AD21	V_{DD_IO}
AA22	$\overline{L1BCMPO}$	AB22	V_{SS}	AC22	V_{DD_IO}	AD22	V_{DD_IO}
AA23	L1DATO0_N	AB23	V_{DD_IO}	AC23	V_{SS}	AD23	V_{SS}
AA24	L1DATO0_P	AB24	V_{DD_IO}	AC24	L1ACKI	AD24	V_{SS}

[1] On revision 1.x silicon, the R2 and R3 balls are NC. On revision 0.x silicon, the R2 ball is SCLK, and the R3 ball is SCLK_V_{REF}. For more information on SCLK and SCLK_V_{REF} on revision 0.x silicon, see *EE-179: ADSP-TS20x TigerSHARC System Design Guidelines*.

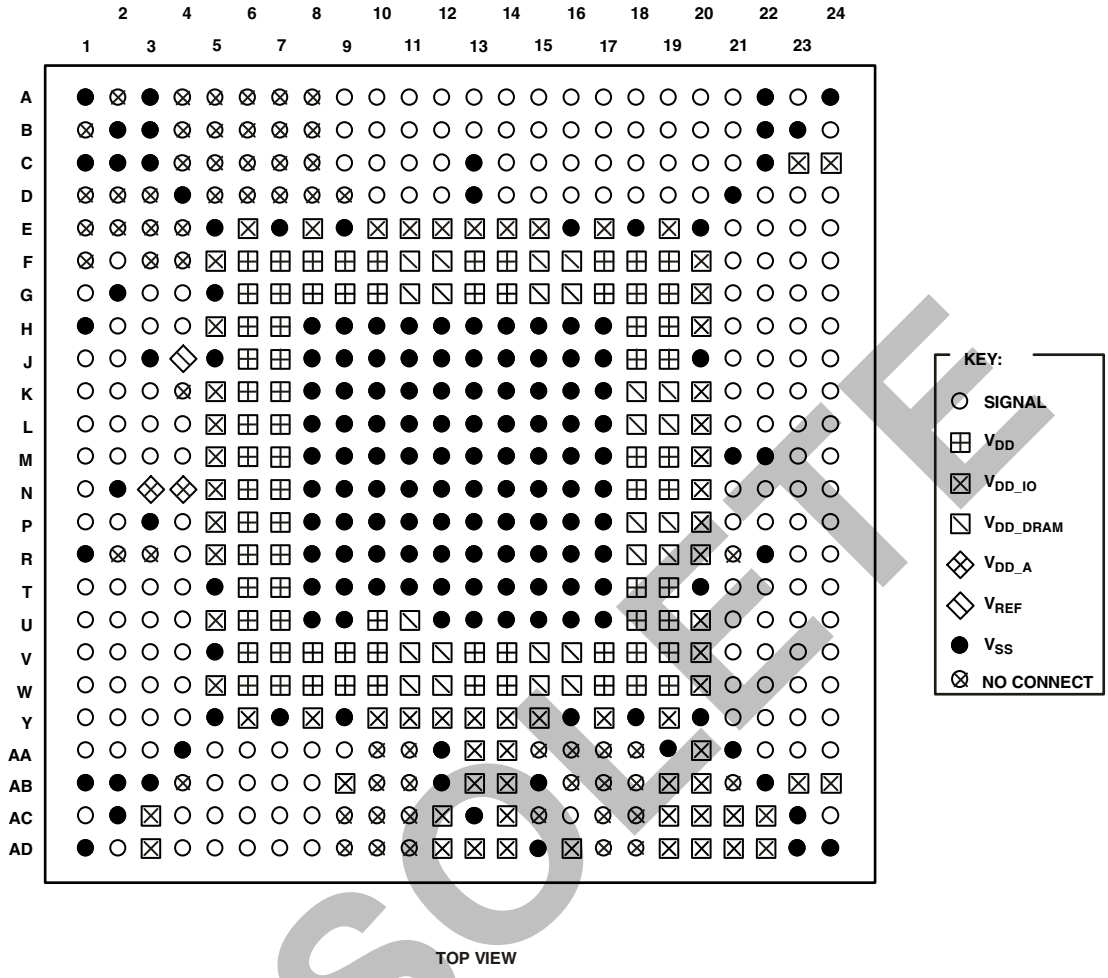


Figure 44. 576-Ball BGA_ED Pin Configurations[1] (Top View, Summary)

[1] For a more detailed pin summary diagram, see *EE-179: ADSP-TS20x TigerSHARC System Design Guidelines*.

OUTLINE DIMENSIONS

The ADSP-TS203S processor is available in a 25 mm × 25 mm, 576-ball metric thermally enhanced ball grid array (BGA_ED) package with 24 rows of balls (BP-576).

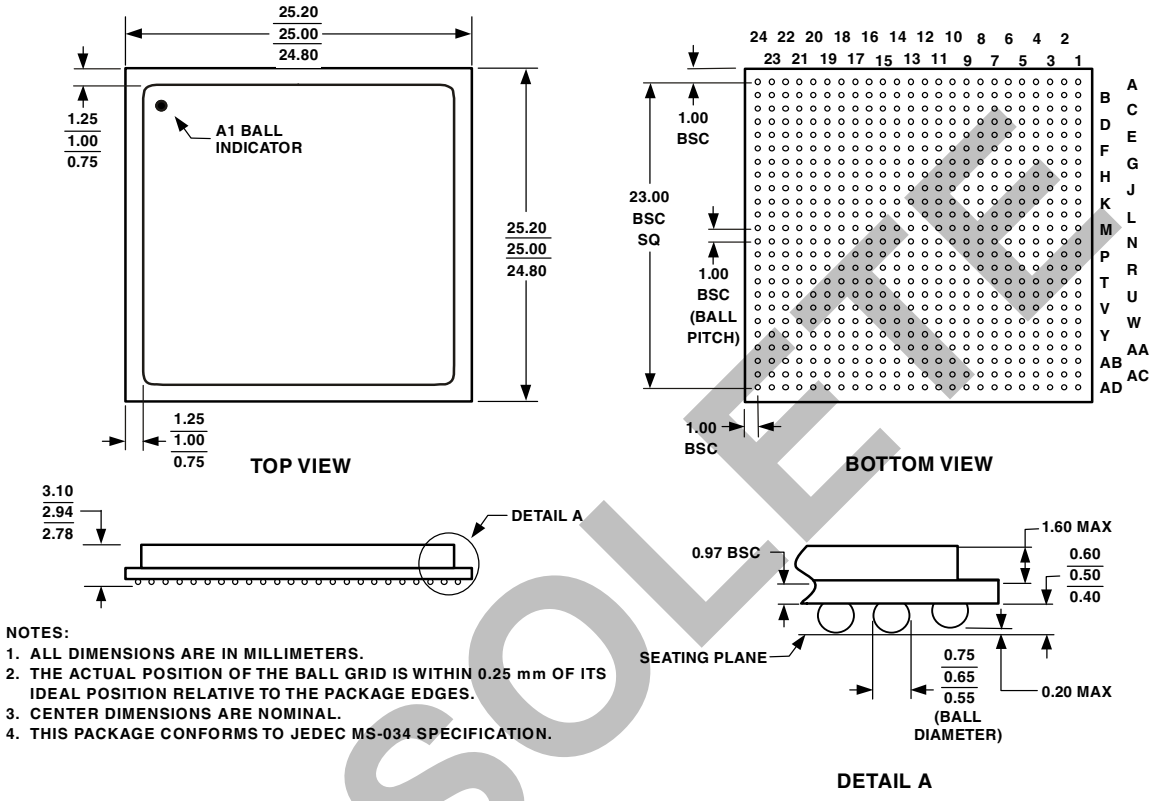


Figure 45. 576-Ball BGA_ED (BP-576)

SURFACE MOUNT DESIGN

The following table is provided as an aide to PCB design. The numbers listed in the table are for reference purposes and should not supersede the PCB design rules. Please reference IPC-7351, *Surface Mount Design and Land Pattern Standard*, for PCB design recommendations.

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
576-Ball BGA_ED (BP-576-1)	Nonsolder Mask Defined (NSMD)	0.69	0.56

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate[3]	On-Chip DRAM	Package Option	Package Description
ADSP-TS203SBBPZ050	0°C to +85°C	500 MHz	4M bit	BP-576	576-Ball BGA_ED
ADSP-TS203SABP-050	–40°C to +85°C	500 MHz	4M bit	BP-576	576-Ball BGA_ED
ADSP-TS203SABPZ050	–40°C to +85°C	500 MHz	4M bit	BP-576	576-Ball BGA_ED

[1] Z = RoHS complaint part.
[2] Represents case temperature.
[3] The instruction rate is the same as the internal processor core clock (CCLK) rate.