19-5248; Rev 0; 4/10

EVALUATION KIT AVAILABLE

100Mbps, 16-Channel LLTs

General Description

The MAX14548E/MAX14548AE 16-channel, bidirectional level translators (LLTs) provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a high-voltage logic signal on the V_{CC} side of the device and vice versa.

The devices feature a programming frequency input (PF) that adjusts the one-shot accelerator on-time to guarantee a bit rate of 100Mbps with a load capacitance < 15pF and V_L > 1.1V (MAX14548E) or V_L > 1.4V (MAX14548AE) when driven low. The MAX14548E can drive capacitive loads up to 50pF with a guaranteed bit rate of 40Mbps when $V_L \geq$ 1.1V and PF is driven high. The MAX14548AE can drive capacitive loads up to 50pF with a guaranteed bit rate of 40Mbps when $V_L \geq$ 1.1V and PF is driven high.

The device operate at full speed with external drivers that source as low as 4mA output current. Each I/O channel is pulled up to V_{CC} or V_L by an internal 35µA current source, allowing both devices to be driven by either push-pull or open-drain drivers.

The devices feature multiple power-saving features including an enable input (EN) that places the device into a low-power shutdown mode when driven low and an automatic shutdown mode that disables the part when V_{CC} is less than V_L. The MAX14548AE output driver is designed to operate at full speed (100Mbps) with V_L > 1.4V, which reduces the dynamic supply current vs. the MAX14548E. The state of I/O V_{CC}_and I/O V_L_are in high-impedance state during shutdown.

The devices operate with V_{CC} voltages from +1.7V to +3.6V and V_L voltages from +1.1V to +3.6V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The devices are available in a 40-bump WLP (2.16mm x 3.46mm) package with 0.4mm ball pitch, and operate over the extended -40°C to +85°C temperature range.

Features

- **Bidirectional Level Translation**
- **100Mbps Guaranteed Data Rate**
- **+1.7V to +3.6V Supply Voltage Range for V_{CC}**
- **+1.1V to +3.6V Supply Voltage Range for V_L (V_{CC} > V_L)**
- **-40°C to +85°C Extended Operating Temperature Range**

Applications

CMOS Logic-Level Translation

Low-Voltage ASIC Level Translation

Smart Card Readers

Portable Communication Devices

Cell Phones

GPS

Telecommunications Equipment

Typical Operating Circuit appears at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	BIT RATE (PF = LOW) LOAD CAPACITANCE < 15pF (Mbps)	BIT RATE (PF = HIGH) LOAD CAPACITANCE < 50pF (Mbps)	LOW DYNAMIC SUPPLY CURRENT
MAX14548EEWL+	40 WLP	100	40	—
MAX14548AEEWL+	40 WLP	100	40	Yes (V_L > 1.1V)

Note: *All devices operate over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, V_L, EN, PF.....-0.3V to +4V
I/O $V_{CC\_}$ ..... -0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$ ..... -0.3V to (V_L + 0.3V)
Short-Circuit Duration I/O $V_{L\_}$,
I/O $V_{CC\_}$ to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Bump WLP (derate 17.2mW/°C above +70°C) 1379mW
Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 1) .....58°C/W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.7V to +3.6V, V_L = +1.1V to +3.6V, V_{CC} > V_L, EN = V_L, C_{VCC} = 1µF, C_{VL} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
V_L Supply Range	V_L			1.1		3.6	V
V_{CC} Supply Range	V_{CC}			1.7		3.6	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L				40	µA
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L				20	µA
V_{CC} Shutdown Supply Current	$I_{SHDN-VCC}$	T_A = +25°C, EN = GND, unconnected I/O pins			0.1	1	µA
V_L Shutdown Mode Supply Current	$I_{SHDN-VL}$	T_A = +25°C, EN = GND, unconnected I/O pins			0.1	1	µA
		T_A = +25°C, EN = V_L, V_{CC} = GND, unconnected I/O pins			0.1	2	
Dynamic Supply Current	I_D	One I/O switching at 25MHz; all other I/O connected to V_{CC} or V_L; C_{LOAD} = 0pF	MAX14548E		2.9		mA
			MAX14548AE		2.6		
I/O $V_{CC\_}$, I/O $V_{L\_}$ Three-State Leakage Current	I_{LEAK}	T_A = +25°C, EN = GND			0.1	6	µA
EN, PF Input Leakage Current	$I_{LEAK\_EN\_PF}$	T_A = +25°C				1	µA
V_L Shutdown Threshold	V_{TH_VL}				0.3		V
V_L - V_{CC} Shutdown Threshold High	V_{TH_H}	V_{CC} rising (V_L = 3.6V) (Note 4)		0.05	0.3	0.65	V
V_L - V_{CC} Shutdown Threshold Low	V_{TH_L}	V_{CC} falling (V_L = 3.6V) (Note 4)		0.2	0.52	0.85	V
I/O $V_{L\_}$ Pullup Current	$I_{VL\_PU\_}$	I/O $V_{L\_}$ = GND, I/O $V_{CC\_}$ = GND		10		125	µA
I/O $V_{CC\_}$ Pullup Current	$I_{VCC\_PU\_}$	I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND		15		90	µA
I/O $V_{L\_}$ to I/O $V_{CC\_}$ DC Resistance	R_{IOVL_IOVCC}	(Note 5)			3		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.7V to +3.6V, V_L = +1.1V to +3.6V, V_{CC} > V_L, EN = V_L, C_{VCC} = 1µF, C_{VL} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ESD PROTECTION							
I/O V_{CC}_, I/O V_L_		Human Body Model, C_{VCC} = 1µF, C_{VL} = 1µF	Unpowered device		±12		kV
			Powered device		±5		
All Other Pins					±2		kV
LOGIC LEVELS							
I/O V_L_ Input-Voltage High Threshold	V_{IHL}	(Note 6)		V_L - 0.2			V
I/O V_L_ Input-Voltage Low Threshold	V_{ILL}	(Note 6)				0.15	V
I/O V_{CC}_ Input-Voltage High Threshold	V_{IHC}	(Note 6)		V_{CC} - 0.4			V
I/O V_{CC}_ Input-Voltage Low Threshold	V_{ILC}	(Note 6)				0.2	V
EN, PF Input-Voltage High Threshold	V_{IH}	1.1V < V_L < 1.3V		V_L - 0.25			V
		V_L = 1.8V		V_L - 0.4			
EN, PF Input-Voltage Low Threshold	V_{IL}	1.1V < V_L < 1.3V				0.4	V
		V_L = 1.8V				0.4	
I/O V_L_ Output-Voltage High	V_{OHL}	I/O V_L_ source current = 10µA		4/5 x V_L			V
I/O V_L_ Output-Voltage Low, Drop to GND	V_{OLL}	I/O V_L_ sink current = 20µA, I/O V_{CC}_ < 0.05V				1/3 x V_L	V
I/O V_{CC}_ Output-Voltage High	V_{OHC}	I/O V_{CC}_ source current = 10µA		4/5 x V_{CC}			V
I/O V_{CC}_ Output-Voltage Low, Drop to GND	V_{OLC}	I/O V_{CC}_ sink current = 20µA, I/O V_L_ < 0.05V				1/3 x V_{CC}	V
RISE/FALL TIME ACCELERATOR STAGE							
Accelerator Pulse Duration		PF = low	On rising edge		2.65		ns
			On falling edge		2.5		
		PF = high	On rising edge		4		ns
			On falling edge		3.7		
V_L Output Accelerator Source Impedance		V_L = 1.62V			7		Ω
		V_L = 3.2V			4.43		
V_{CC} Output Accelerator Source Impedance		V_{CC} = 2.2V			14.2		Ω
		V_{CC} = 3.6V			11.2		
V_L Output Accelerator Sink Impedance		V_L = 1.62V			15.3		Ω
		V_L = 3.2V			15.3		
V_{CC} Output Accelerator Sink Impedance		V_{CC} = 2.2V			20.3		Ω
		V_{CC} = 3.6V			19.5		

HIGH-SPEED TIMING CHARACTERISTICS—MAX14548E

(V_{CC} = +1.7V to +3.6V, V_L = +1.1V to +3.6V, V_{CC} > V_L, EN = V_L, PF = low, C_{VCC} = 1µF, C_{VL} = 1µF, C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 15pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Input rise time < 2ns, Figure 1			2	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Input fall time < 2ns, Figure 1			2	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}	Input rise time < 2ns, Figure 2			2	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	Input fall time < 2ns, Figure 2			2	ns
Propagation Delay (Driving I/O $V_{L\_}$)	$t_{PVL-VCC}$	Input rise time < 2ns, Figure 1		2.75		ns
Propagation Delay (Driving I/O $V_{CC\_}$)	$t_{PVCC-VL}$	Input rise time < 2ns, Figure 2		2.26		ns
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 2ns		0.2		ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ After EN	t_{EN-VCC}	R_{LOAD} = 1MΩ, Figure 3		27		µs
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ After EN	t_{EN-VL}	R_{LOAD} = 1MΩ, Figure 3		0.05		µs
Maximum Data Rate		Push-pull operation	100			Mbps
		Open-drain operation	0.3			

HIGH-SPEED TIMING CHARACTERISTICS—MAX14548AE

(V_{CC} = +1.7V to +3.6V, V_L = +1.4V to +3.6V, V_{CC} > V_L, EN = V_L, PF = low, C_{VCC} = 1µF, C_{VL} = 1µF, C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 15pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Input rise time < 2ns, Figure 1			2	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Input fall time < 2ns, Figure 1			2	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}	Input rise time < 2ns, Figure 2			2	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	Input rise time < 2ns, Figure 2			2	ns
Propagation Delay (Driving I/O $V_{L\_}$)	$t_{PVL-VCC}$	Input rise time < 2ns, Figure 1		2.75		ns
Propagation Delay (Driving I/O $V_{CC\_}$)	$t_{PVCC-VL}$	Input rise time < 2ns, Figure 2		2.26		ns
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 2ns		0.2		ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ After EN	t_{EN-VCC}	R_{LOAD} = 1MΩ, Figure 3		27		µs
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ After EN	t_{EN-VL}	R_{LOAD} = 1MΩ, Figure 3		0.05		µs
Maximum Data Rate		Push-pull operation	100			Mbps
		Open-drain operation	0.3			

LOW-SPEED TIMING CHARACTERISTICS—MAX14548E

(V_{CC} = +1.7V to +3.6V, V_L = +1.1V to +3.6V, V_{CC} > V_L, EN = V_L, PF = high, C_{VCC} = 1µF, C_{VL} = 1µF, C_{IOVL} ≤ 50pF, C_{IOVCC} ≤ 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Input rise time < 6ns, Figure 1			6	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Input fall time < 6ns, Figure 1			6	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}	Input rise time < 6ns, Figure 2			6	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	Input rise time < 6ns, Figure 2			6	ns
Propagation Delay (Driving I/O $V_{L\_}$)	$t_{PVL-VCC}$	Input rise time < 6ns, Figure 1		4		ns
Propagation Delay (Driving I/O $V_{CC\_}$)	$t_{PVCC-VL}$	Input rise time < 6ns, Figure 2		3.37		ns
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 6ns		0.2	0.5	ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ After EN	t_{EN-VCC}	R_{LOAD} = 1MΩ, Figure 3		27		µs
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ After EN	t_{EN-VL}	R_{LOAD} = 1MΩ, Figure 3		0.06		µs
Maximum Data Rate		Push-pull operation	40			Mbps
		Open-drain operation	0.3			

LOW-SPEED TIMING CHARACTERISTICS—MAX14548AE

(V_{CC} = +1.7V to +3.6V, V_L = +1.1V to +3.6V, V_{CC} > V_L, EN = V_L, PF = high, C_{VCC} = 1µF, C_{VL} = 1µF, C_{IOVL} ≤ 50pF, C_{IOVCC} ≤ 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.8V, V_L = +1.8V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Input rise time < 6ns, Figure 1			6	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Input fall time < 6ns, Figure 1			6	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}	Input rise time < 6ns, Figure 2			6	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	Input rise time < 6ns, Figure 2			6	ns
Propagation Delay (Driving I/O $V_{L\_}$)	$t_{PVL-VCC}$	Input rise time < 6ns, Figure 1		4		ns
Propagation Delay (Driving I/O $V_{CC\_}$)	$t_{PVCC-VL}$	Input rise time < 6ns, Figure 2		3.37		ns
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 6ns		0.2		ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ After EN	t_{EN-VCC}	R_{LOAD} = 1MΩ, Figure 3		27		µs
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ After EN	t_{EN-VL}	R_{LOAD} = 1MΩ, Figure 3		0.06		µs
Maximum Data Rate		Push-pull operation	40			Mbps
		Open-drain operation	0.3			

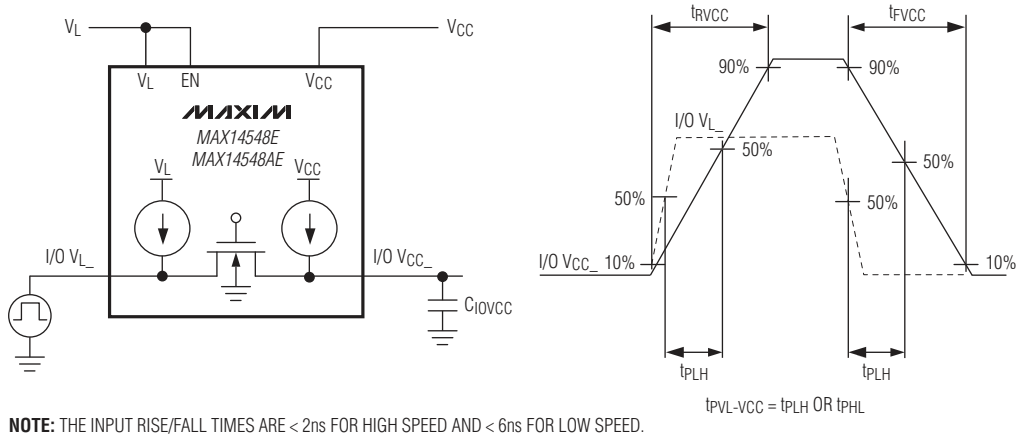
Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 4: When V_{CC} is below V_L by more than the V_L - V_{CC} shutdown threshold, the device turns off its pullup generators and I/O $V_{CC\_}$ and I/O $V_{L\_}$ enter their respective shutdown states.

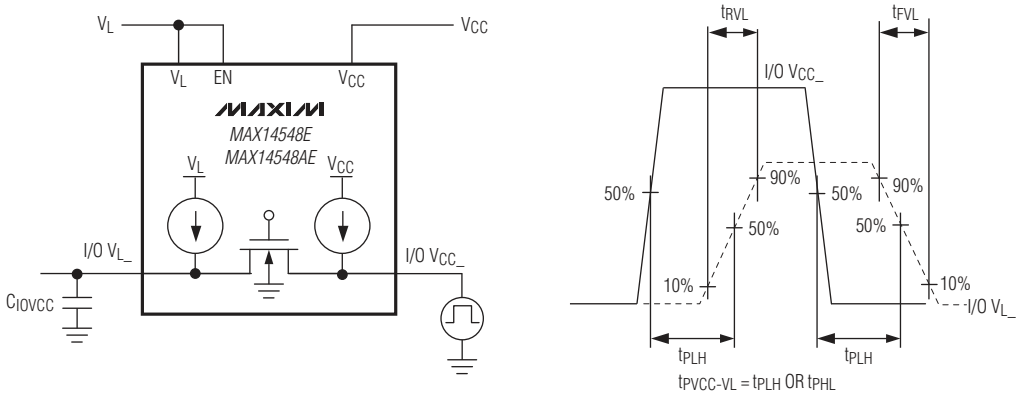
Note 5: Guaranteed by design.

Note 6: Input thresholds are referenced to the boost circuit.



NOTE: THE INPUT RISE/FALL TIMES ARE < 2ns FOR HIGH SPEED AND < 6ns FOR LOW SPEED.

Figure 1. Push-Pull Driving I/O VL_ Test Circuit and Timing



NOTE: THE INPUT RISE/FALL TIMES ARE < 2ns FOR HIGH SPEED AND < 6ns FOR LOW SPEED.

Figure 2. Push-Pull Driving I/O VCC_ Test Circuit and Timing

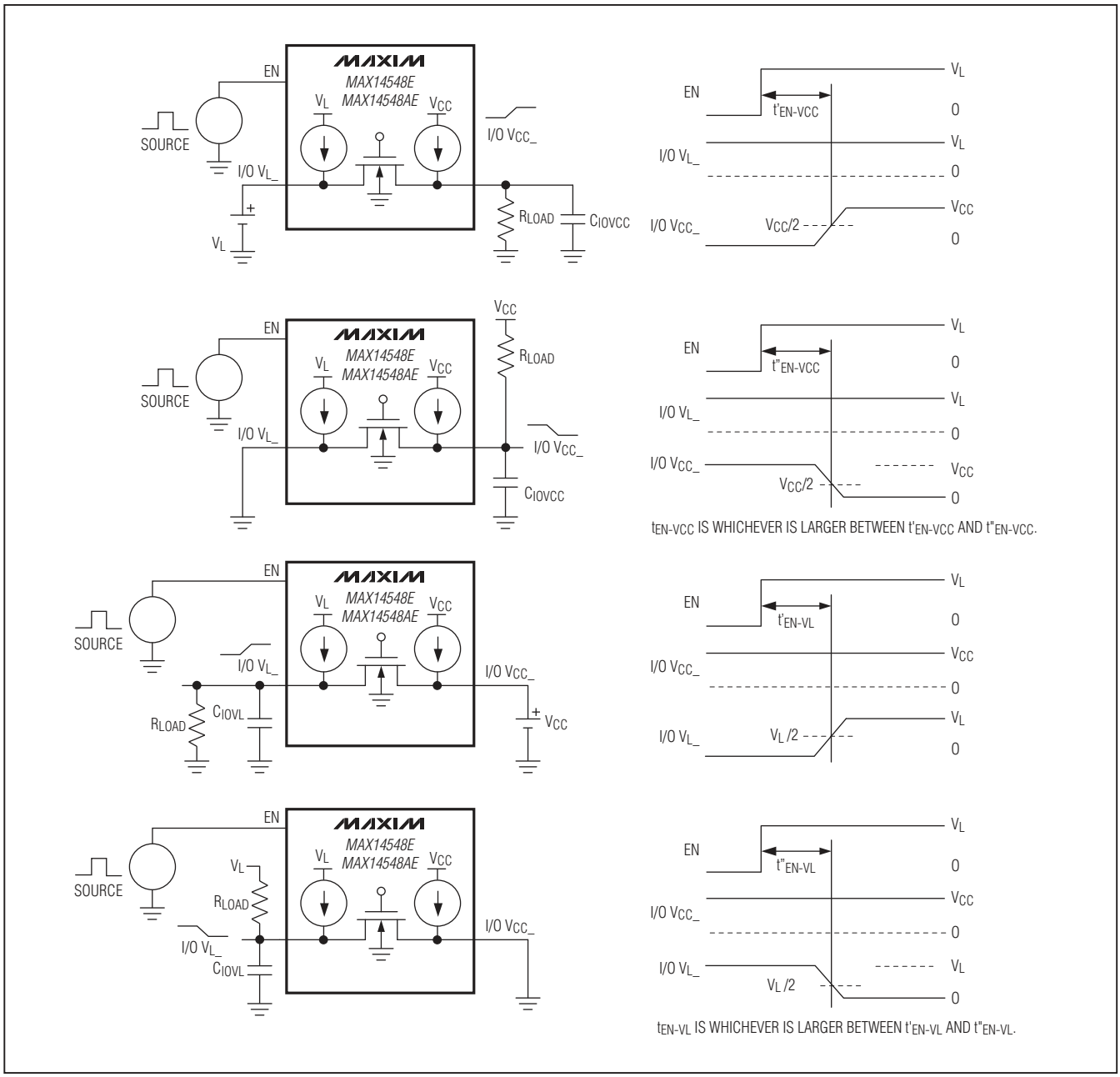


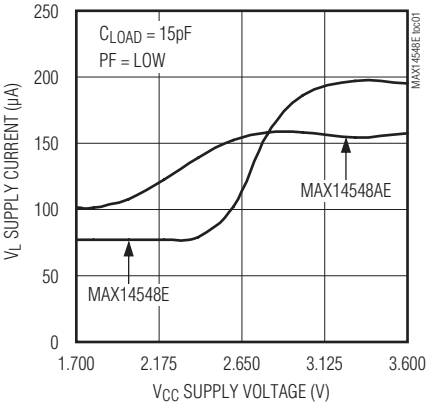
Figure 3. Enable Test and Timing

100Mbps, 16-Channel LLTs

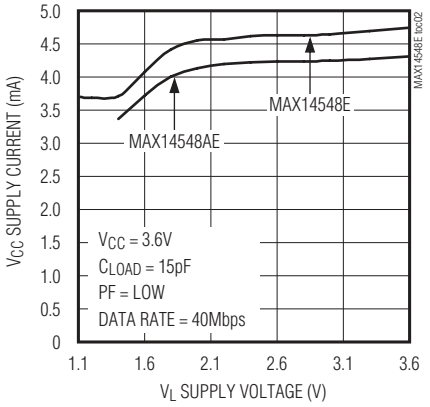
Typical Operating Characteristics

(V_{CC} = 1.8V, V_L = 1.4V, C_L = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

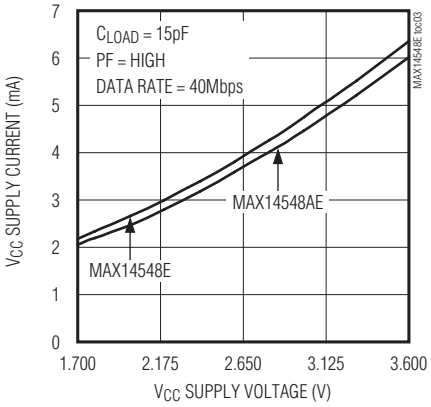
V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O V_L_)



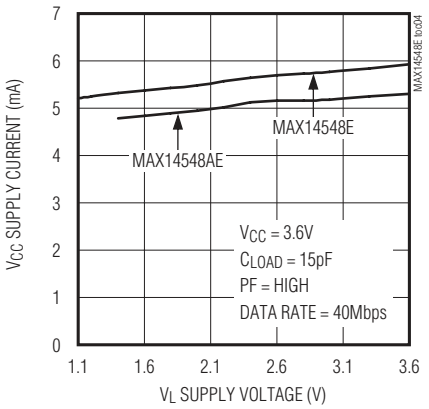
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O V_{CC}_)



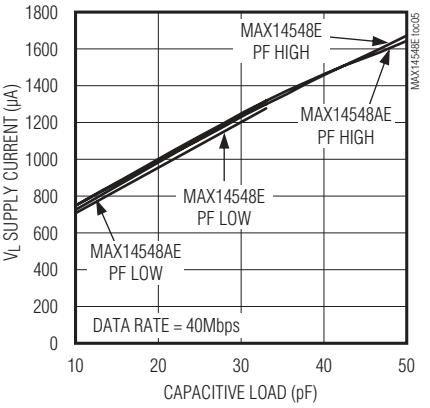
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O V_L_)



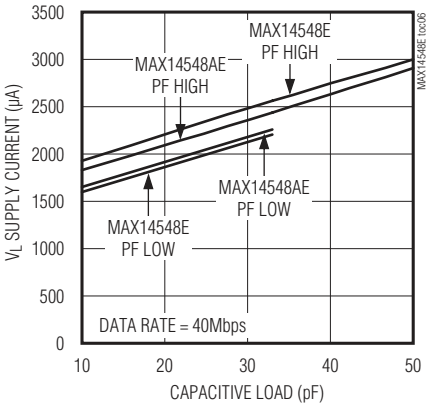
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O V_{CC}_)



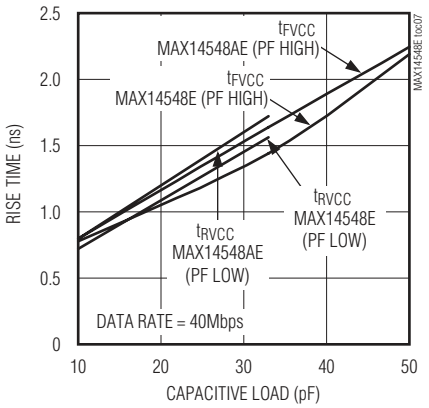
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD (DRIVING ONE I/O V_{CC})



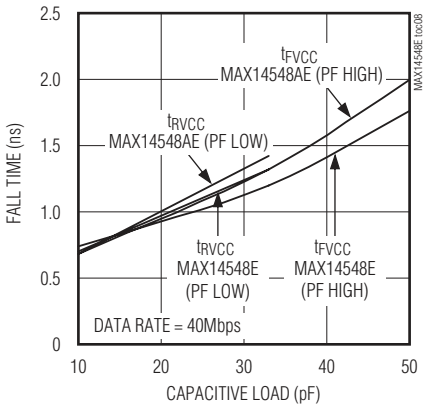
V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD (DRIVING ONE I/O V_L_)



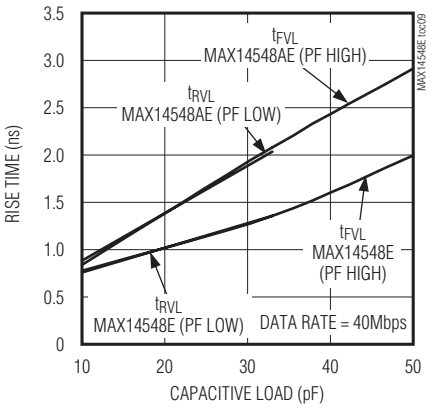
RISE TIME vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING ONE I/O V_L)



FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING ONE I/O V_L)



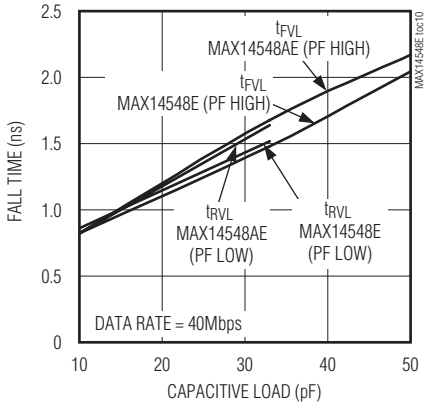
RISE TIME vs. CAPACITIVE LOAD ON I/O V_L (DRIVING ONE I/O V_{CC})



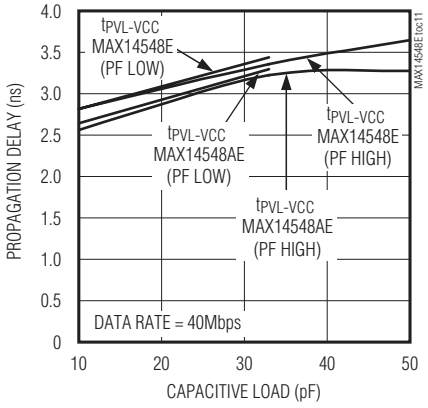
Typical Operating Characteristics (continued)

(V_{CC} = 1.8V, V_L = 1.4V, C_L = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

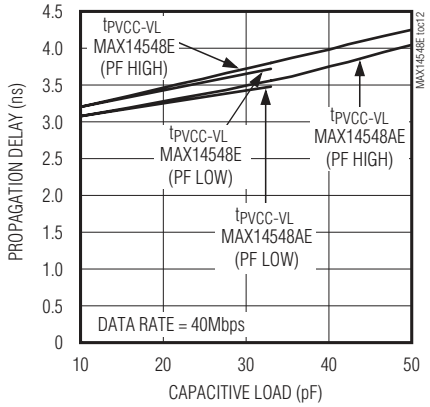
FALL TIME vs. CAPACITIVE LOAD ON I/O V_L (DRIVING ONE I/O V_{CC})



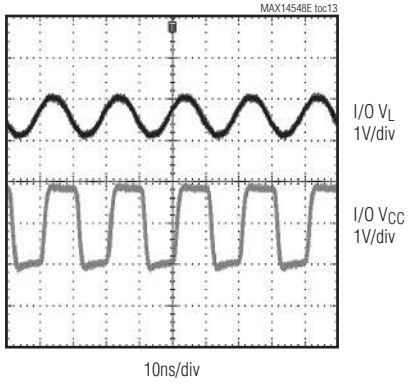
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING ONE I/O V_L)



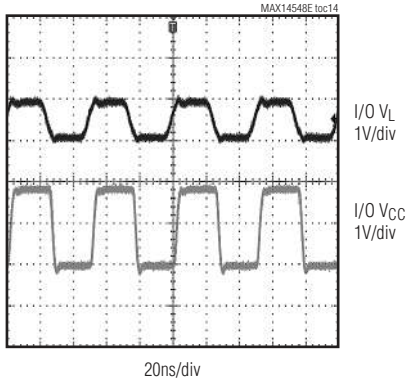
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L (DRIVING ONE I/O V_{CC})



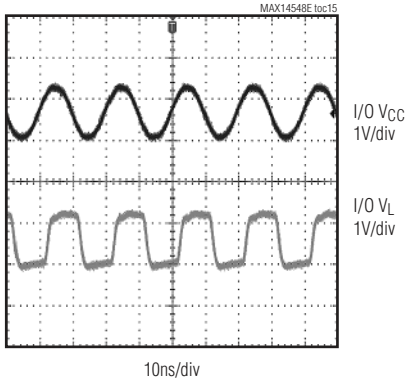
TYPICAL I/O $V_{L\_}$ DRIVING (DATA RATE = 100Mbps, C_{IOVCC} = 10pF), PF = LOW, MAX14548E



TYPICAL I/O $V_{L\_}$ DRIVING (DATA RATE = 40Mbps, C_{IOVCC} = 47pF), PF = HIGH, MAX14548E



TYPICAL I/O $V_{CC\_}$ DRIVING (DATA RATE = 100Mbps, C_{IOVL} = 10pF), PF = LOW, MAX14548E

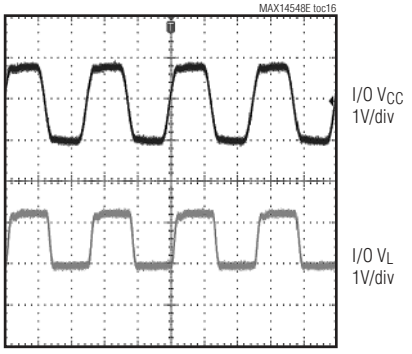


100Mbps, 16-Channel LLTs

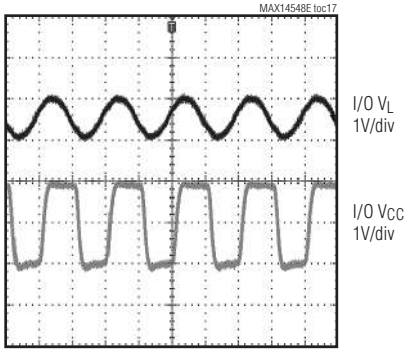
Typical Operating Characteristics (continued)

(V_{CC} = 1.8V, V_L = 1.4V, C_L = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

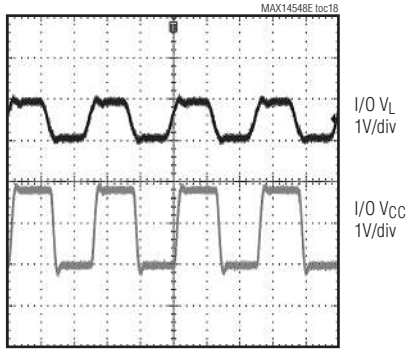
TYPICAL I/O $V_{CC\_}$ DRIVING (DATA RATE = 40Mbps, C_{IOVL} = 47pF), PF = HIGH, MAX14548E



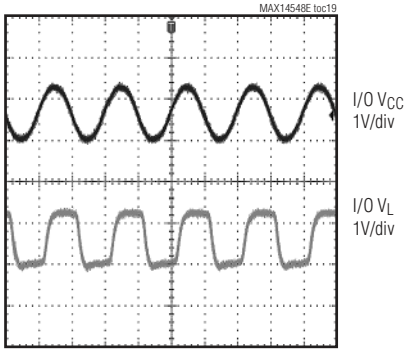
TYPICAL I/O $V_{L\_}$ DRIVING (DATA RATE = 100Mbps, C_{IOVCC} = 10pF), PF = LOW, MAX14548AE



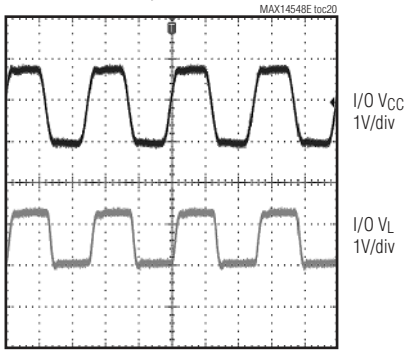
TYPICAL I/O $V_{L\_}$ DRIVING (DATA RATE = 40Mbps, C_{IOVCC} = 47pF), PF = HIGH, MAX14548AE



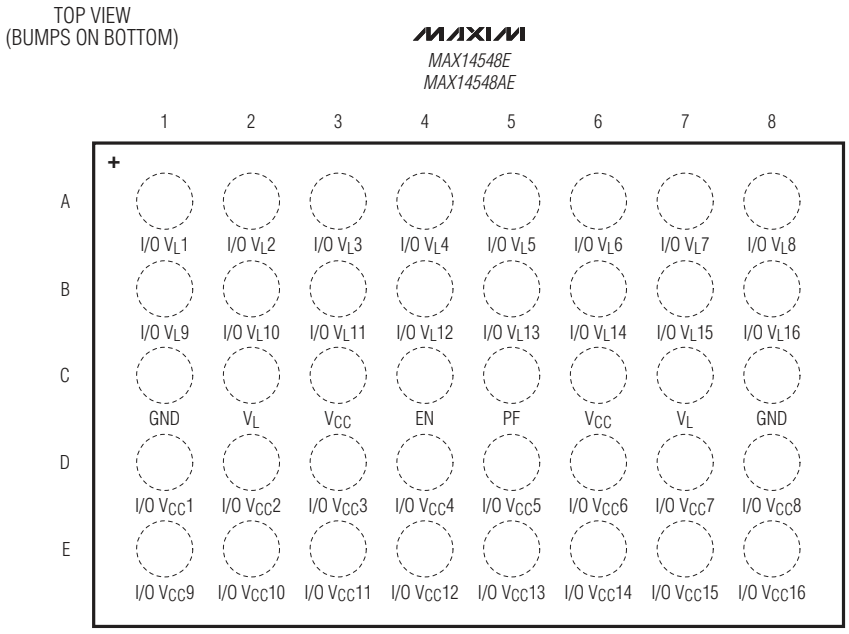
TYPICAL I/O $V_{CC\_}$ DRIVING (DATA RATE = 100Mbps, C_{IOVL} = 10pF), PF = LOW, MAX14548AE



TYPICAL I/O $V_{CC\_}$ DRIVING (DATA RATE = 40Mbps, C_{IOVL} = 47pF), PF = HIGH, MAX14548AE



Pin Configuration



WLP
(2.16mm × 3.46mm)

Pin Description

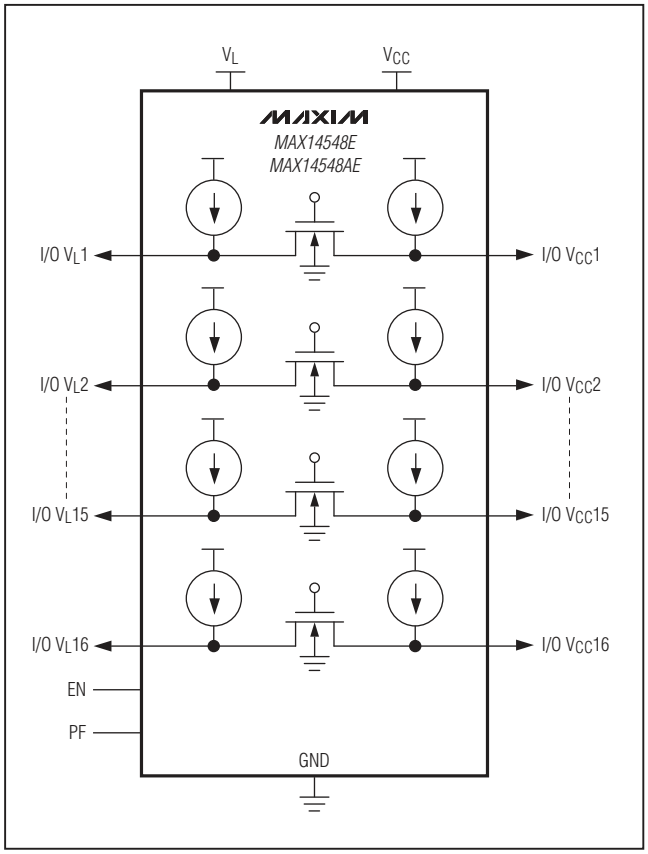
PIN	NAME	FUNCTION
A1	I/O V_L1	Input/Output 1. Referenced to V_L.
A2	I/O V_L2	Input/Output 2. Referenced to V_L.
A3	I/O V_L3	Input/Output 3. Referenced to V_L.
A4	I/O V_L4	Input/Output 4. Referenced to V_L.
A5	I/O V_L5	Input/Output 5. Referenced to V_L.
A6	I/O V_L6	Input/Output 6. Referenced to V_L.
A7	I/O V_L7	Input/Output 7. Referenced to V_L.
A8	I/O V_L8	Input/Output 8. Referenced to V_L.
B1	I/O V_L9	Input/Output 9. Referenced to V_L.
B2	I/O V_L10	Input/Output 10. Referenced to V_L.
B3	I/O V_L11	Input/Output 11. Referenced to V_L.
B4	I/O V_L12	Input/Output 12. Referenced to V_L.
B5	I/O V_L13	Input/Output 13. Referenced to V_L.
B6	I/O V_L14	Input/Output 14. Referenced to V_L.
B7	I/O V_L15	Input/Output 15. Referenced to V_L.
B8	I/O V_L16	Input/Output 16. Referenced to V_L.
C1, C8	GND	Ground

100Mbps, 16-Channel LLTs

Pin Description (continued)

PIN	NAME	FUNCTION
C2, C7	V_L	Logic Supply Voltage, +1.1V to +3.6V. Bypass V_L to GND with a 1µF capacitor placed as close as possible to the device.
C3, C6	V_{CC}	Power-Supply Voltage, +1.7V to +3.6V. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor. For full ESD protection, connect an additional 1µF ceramic capacitor from V_{CC} to GND as close as possible to the V_{CC} input.
C4	EN	Enable Input. Drive EN to GND for shutdown mode, or drive EN to V_L or V_{CC} for normal operation.
C5	PF	Programmable Frequency Input. Drive PF low for high-frequency operation. Drive PF high for lower frequency operation.
D1	I/O V_{CC}1	Input/Output 1. Referenced to V_{CC}.
D2	I/O V_{CC}2	Input/Output 2. Referenced to V_{CC}.
D3	I/O V_{CC}3	Input/Output 3. Referenced to V_{CC}.
D4	I/O V_{CC}4	Input/Output 4. Referenced to V_{CC}.
D5	I/O V_{CC}5	Input/Output 5. Referenced to V_{CC}.
D6	I/O V_{CC}6	Input/Output 6. Referenced to V_{CC}.
D7	I/O V_{CC}7	Input/Output 7. Referenced to V_{CC}.
D8	I/O V_{CC}8	Input/Output 8. Referenced to V_{CC}.
E1	I/O V_{CC}9	Input/Output 9. Referenced to V_{CC}.
E2	I/O V_{CC}10	Input/Output 10. Referenced to V_{CC}.
E3	I/O V_{CC}11	Input/Output 11. Referenced to V_{CC}.
E4	I/O V_{CC}12	Input/Output 12. Referenced to V_{CC}.
E5	I/O V_{CC}13	Input/Output 13. Referenced to V_{CC}.
E6	I/O V_{CC}14	Input/Output 14. Referenced to V_{CC}.
E7	I/O V_{CC}15	Input/Output 15. Referenced to V_{CC}.
E8	I/O V_{CC}16	Input/Output 16. Referenced to V_{CC}.

Functional Diagram



Detailed Description

The MAX14548E/MAX14548AE 16-channel, bidirectional level translators (LLTs) provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a high-voltage logic signal on the V_{CC} side of the device and vice versa.

The devices operate at full speed with external drivers that source as little as 4mA output current (min). Each I/O channel is pulled up to V_{CC} or V_L by an internal 35µA current source, allowing the devices to be driven by either push-pull or open-drain drivers.

The devices feature an enable input (EN) that places the device into a low-power shutdown mode when driven low. They also feature an automatic shutdown mode that disables the part when V_{CC} is less than V_L.

The devices feature a programmable frequency input (PF) that guarantees a bit rate of 100Mbps with a load capacitance < 15pF and V_L > 1.1V (MAX14548E) or V_L > 1.4V (MAX14548AE) when driven low. The MAX14548E can drive capacitive loads up to 50pF with a guaranteed bit rate of 40Mbps when $V_L \geq 1.1V$ and PF is driven high. The MAX14548AE can drive capacitive loads up to 50pF with a guaranteed bit rate of 40Mbps when $V_L \geq 1.1V$ and PF is driven high.

Level Translation

For proper operation, ensure that $1.7V \leq V_{CC} \leq 3.6V$, $1.1V \leq V_L \leq V_{CC}$. When power is supplied to V_L while V_{CC} is less than V_L, the devices automatically enter a low-power mode and the I/Os are in high-impedance mode. The devices also enter shutdown mode when EN = 0. In both conditions where EN = 0 or $V_L > V_{CC}$, there is a known high-impedance state on I/O V_L_ and I/O V_{CC}_. The maximum data rate depends heavily on the load capacitance (see the rise/fall time graphs in the *Typical Operating Characteristics*), output impedance of the driver, and the operating voltage range.

Input Driver Requirements

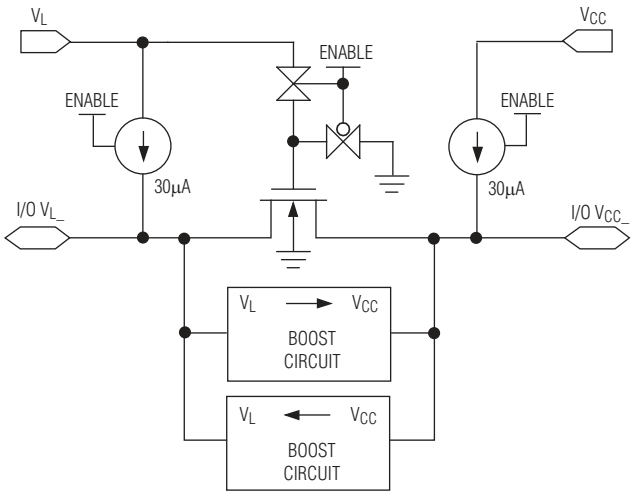
The device architecture is based on an nMOS pass gate and output accelerator stages (Figure 4). The accelerators are active only when there is a rising/falling edge on a given I/O. A short pulse is then generated where the output accelerator stages become active and charge/discharge the capacitances at the I/Os. Due to its architecture, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps speed up the transition on the driven side.

The devices have internal current sources capable of sourcing 35µA to pull up the I/O lines. These internal pullup current sources allow the inputs to be driven with open-drain drivers and push-pull drivers. It is not recommended to use external pullup resistors on the I/O lines. The architecture of the devices permit either side to be driven with a minimum of 4mA drivers or larger.

Output Load Requirements

The device I/Os are designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ and do not place an RC circuit at the input of these devices to slow down the edges. If a slower rise/fall time is required, refer to the MAX3000E/MAX3001E/MAX3002–MAX3012 data sheet.

100Mbps, 16-Channel LLTs



NOTE 1: THE MAX14548E/MAX14548AE ARE ENABLED WHEN $V_L < V_{CC}$ - 0.2V AND EN = V_L.

Figure 4. Simplified Functional Diagram for One I/O Line

Shutdown Mode

The EN input places the devices into a low-power shutdown mode when driven low. The automatic shutdown mode disables the devices when V_{CC} is unconnected or less than V_L. When V_{CC} is less than V_L or EN = GND, the devices enter shutdown mode.

Data Rate and Capacitive Load (PF Input)

The programmable frequency input (PF) adjusts the one-shot accelerator to guarantee a 100Mbps bit rate with a load capacitance <15pF and V_L > 1.1V (MAX14548E) or V_L > 1.4V (MAX14548AE) when driven low. The MAX14548E can drive capacitive loads up to 50pF with a guaranteed 40Mbps bit rate when V_L > 1.1V and PF is driven high. The MAX14548AE can drive capacitive loads up to 50pF with a guaranteed 40Mbps bit rate when V_L > 1.1V and PF is driven high.

Applications Information

Layout Recommendations

Use standard high-speed layout practices when laying out a board with the MAX14548E/MAX14548AE. For example, to minimize line coupling, place all other signal lines not connected to the devices at least 1x the substrate height of the PCB away from the input and output lines of the devices.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with 0.1µF ceramic capacitors. Place all capacitors as close as possible to the power-supply inputs. For full ESD protection, bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the V_{CC} input.

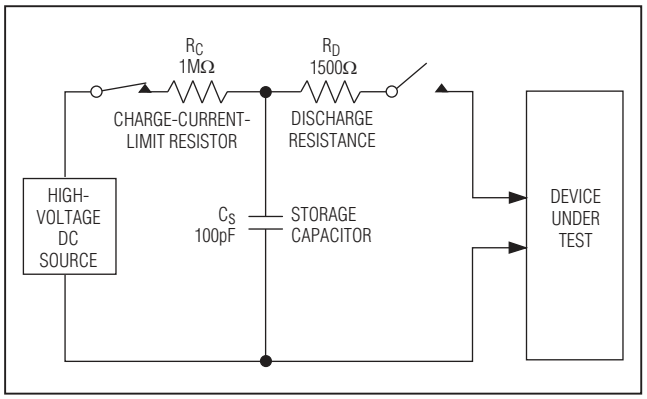


Figure 5a. Human Body ESD Test Model

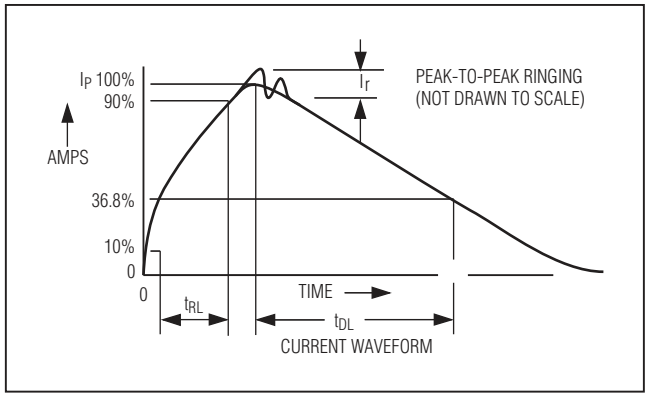


Figure 5b. Human Body Current Waveform

Unidirectional vs. Bidirectional Level Translator

The devices bidirectional level translators can operate as a unidirectional device by selecting one I/O as the input and the corresponding I/O as an output. These devices provide the smallest solution (WLP package) for level translation applications.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O $V_{L\_}$ and I/O $V_{CC\_}$ pins have extra protection against static electricity.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 5a shows the Human Body Model, and Figure 5b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Use with External Pullup/Pulldown Resistors

Due to the architecture of the devices, it is not recommended to use external pullup or pulldown resistors on the bus. In certain applications, the use of external pullup or pulldown resistors is desired to have a known bus state when there is no active driver on the bus. The devices include internal pullup current sources that set the bus state when the device is enabled. In shutdown mode, the state of I/O $V_{CC\_}$ and I/O $V_{L\_}$ is high impedance.

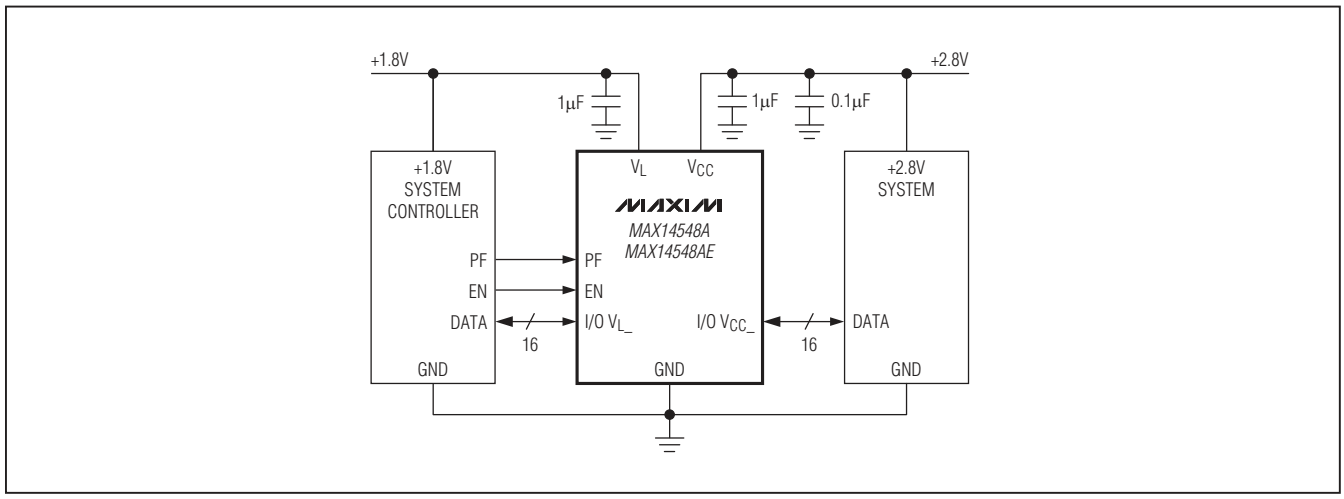
Open-Drain Signaling

The devices are designed to pass open-drain as well as CMOS push-pull signals. When used with open-drain signaling, the rise time is dominated by the interaction of the internal pullup current source and the parasitic load capacitance. The devices include internal rise time accelerators to speed up transitions, eliminating any need for external pullup resistors. For applications such as I^2C or 1-Wire® that require an external pullup resistor, refer to the MAX13046E and MAX13047E data sheets.

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

100Mbps, 16-Channel LLTs

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 WLP	W402B3+1	21-0437

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—