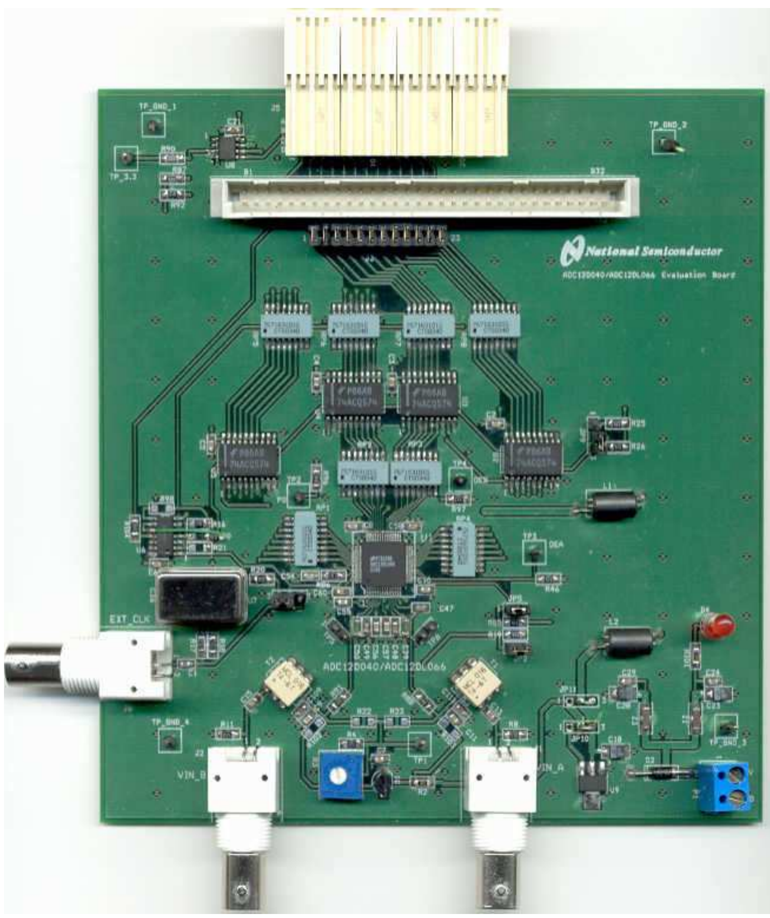
User's Guide

SNAU010A – December 2005 – Revised August 2014

ADC12D040, ADC11DL066, ADC12DL066 - A/D Converters with Internal Reference and Sample & Hold

Evaluation Board User's Guide
ADC12D040 Dual 12-Bit, 40 MSPS, 5 Volt, 600 mW
ADC11DL066 Dual 11-Bit, 66 MSPS 3.3 Volt, 862 mW
ADC12DL066 Dual 12-Bit, 66 MSPS 3.3 Volt, 862 mW



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1 Introduction

The ADC12D040EVAL, the ADC11DL066EVAL and the ADC12DL066EVAL Design Kits (consisting of the ADC12D040, ADC11DL066 or the ADC12DL066 Evaluation Board, this User's Guide and the WaveVision5 Data Capture Board and its User's Guide and WaveVision5 software) are designed to ease evaluation and design-in of Texas Instruments's ADC12D040 dual Analog-to-Digital Converter, which can operate at sample rates up to 40 Msps, the ADC11DL066 or the ADC12DL066 dual 12-bit Analog-to-Digital Converters, which operate at sample rates up to 66 Msps. Further reference in this User's Guide to the ADC12D040 is meant to also include the ADC11DL066 and the ADC12DL066 and references to the ADC12DL066 include the ADC11DL066, unless otherwise specified or implied.

The evaluation board can be used in either of two modes. In the Manual mode, suitable test equipment, such as a logic analyzer, can be used with the board to evaluate the ADC12D040 performance.

In the Computer or Automatic mode, evaluation is simplified by connecting the board to Texas Instruments Data Capture Boards (order number WAVEVSN BRD 4.0), which is connected through a USB communication port to a personal computer running WaveVision5 software. The WaveVision5 program can be downloaded free from the web at http://www.ti.com/adc.

The WaveVision5 software operates under Microsoft Windows. The signal at the two the Analog Inputs is digitized and can be captured and displayed on a PC monitor as a dynamic waveform schematic and is also available at the FutureBus connector J5. See Figure 2.

Upon command, the software will perform an FFT on the captured data. This FFT plot also shows dynamic performance in the form of SNR, SINAD, THD, SFDR and ENOB.

The Signal at the Analog Inputs (J1 for input VIN_A and J2 for input VIN_B) are available at differential Test Points TP6 and TP5 respectively. These signals can be viewed with a Differential Probe.

The ADC12D040 can operate with an external reference or with its internal reference. Accordingly, jumper JP2 is used to select use of the ADC internal reference or the separate reference provided on the evaluation board. The internal reference is used with a jumper on JP2. The external reference on the board is used when the jumper on J2 is removed. Provision is made for adjustment of the external Reference Voltage, V_{REF}, with R3. This voltage is regulated with an LM4040-2.5 reference for the ADC12D040, or an LM4140-1.2 reference for the ADC12DL066, and can be set to values between 0.8V to 2.5V for the ADC12D040 and to values between 0.4V and 1.2V for the ADC12DL066.

2 Board Assembly

The ADC12D040 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to Figure 1 for major component placement and to Figure 2 for the Evaluation Board schematic.

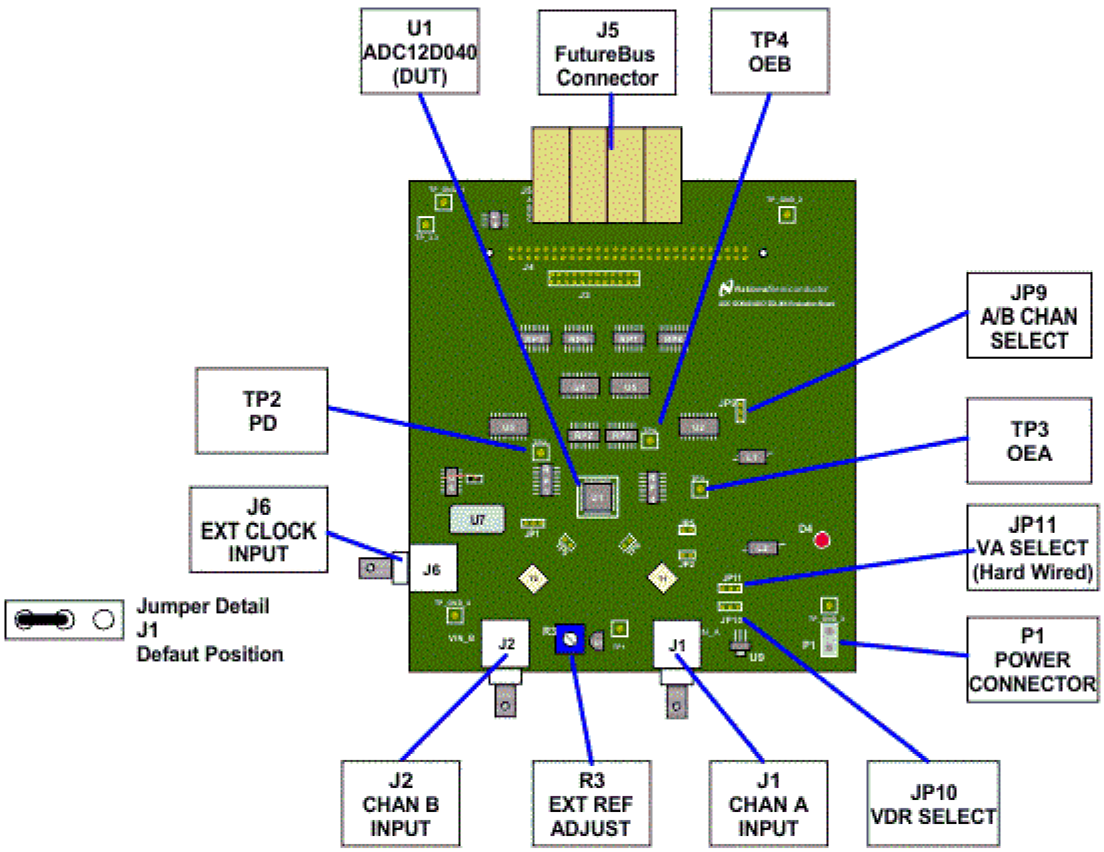

Figure 1. Component and Test Point Locations

3 Quick Start

Refer to Figure 1 for locations of test points and major components.

1. Connect a clean analog (not switching) +5V power source to Power Connector P1.
2. Set the output amplitude of the clock signal generator, if used, to 3 V_{P-P} for the ADC12D040 or to 2V_{P-P} for the ADC12DL066 and the frequency to the desired sample rate.
3. Use R3 to set the reference voltage (V_{REF}) at TP1 to +2.0V ±0.05 for the ADC12D040 or to 1.0V ±0.03V for the ADC12DL066. To use the ADC internal reference, verify a shorting jumper is placed on JP2.

4. Connect a signal source of 2.0 V_{P-P} amplitude for the ADC12D040 or 1.0 V_{P-P} for the ADC12DL066 from a suitable 50-Ω source (such as the Agilent 8644B synthesizer) to Analog Input BNC connector J1. The ADC input signal can be observed at TP6.
   Note: The signal to J1 should be applied through a bandpass filter to eliminate the noise and harmonics commonly associated with signal sources. Even the best signal generators can not do justice to a 12-bit ADC without such a filter. On the other hand, even a good bandpass filter will not eliminate noise near its center frequency.
5. Put a jumper on JP5 to get an offset binary output from the ADC12D040. Remove any jumper from JP5 for 2's complement output format.
6. Adjust the input signal amplitude as needed to ensure that the differential signal at TP6 is close to but does not exceed 2.0V_{P-P} for ADC12D040 or 1.0V_{P-P} for ADC12DL066 from each side of TP6 to ground.
7. Check to be sure the correct frequency TTL oscillator is in socket U7, or apply an external 50-Ω, low jitter, signal source to BNC J6. The amplitude of this signal should be between 2.5 and 3.3 V_{P-P}. If using an external source, remove the oscillator from U7. If using an oscillator at U7, remove the signal source from J6. The presence of a second oscillator source could add noise to the conversion process. Turn on the power.
8. The digitized signal is available at pins A4 through A18 and B4 through B15 of J5. See board schematic of Figure 2.
9. Open the WaveVision 5 software
10. Select the WaveVision data format (Offset Binary or 2's Complement) from the Signal Sources Tab on the right side of the screen.
11. The setup is now ready to capture data in the WaveVision 5 Software

4 Functional Description

Table 1 describes the function of the various jumpers on the ADC12D040 evaluation board. The Evaluation Board schematic is shown in Figure 2.

Table 1. Jumper Functions

Jumper	Pins 1 & 2
JP1	Short pins 2-3 to select the on-board XO (U7) as the sampling clock source Short pins 1-2 to select the signal source connected to J6 as the sampling clock source
JP2	Open to use external reference Short to use on-chip reference
JP5	Short for offset binary output Open for 2's complement
JP9	Should be hard-wired to short pins 1, 2, and 3 together
JP10	ADC12D040EVAL must have pins 1-2 shorted ADC12DL066EVAL must have pins 2-3 shorted
JP11	Short pins 1-2 for output driver supply to be same as the ADC12D040 core supply. Short pins 2-3 for 3.3V supply for the ADC12D040 output drivers. Hard- wired for ADC12DL066

4.1 Input (signal conditioning) Circuitry

The input signal to be digitized should be applied to BNC J1 for testing Channel A of the ADC or to BNC J2 for testing Channel B.

The 50 Ω inputs J1 and J2 are intended to accept low-noise sine wave signals of 2.0 Volt peak-to-peak amplitude for the ADC12D040 or 1.0 Volt peak-to-peak for the ADC12DL066. To accurately evaluate dynamic performance, the input test signal will have to come from a high quality signal source (such as the Agilent 8644B) and be passed through a high-quality bandpass filter with a 60 dB minimum stop band attenuation. Even the best generators available do not provide a pure enough sine wave to properly evaluate a high resolution ADC. Likewise, even with a good filter, apparent performance will still depend upon the signal source used.

Signal transformers T1 and T2 provide single-ended to differential conversion for the ADC12D040 inputs. The common mode voltage at the ADC input comes from the reference voltage on the evaluation board through R22 and R23.

Test points TP6 and TP5 may be used to observe the ADC input signals with differential probes. No scope or other test equipment should be connected to TP6 or to TP5 while gathering data.

NOTE: If input frequency components above 50 MHz are required, remove capacitors C14 & C19 and C17 & C20 at the ADC differential input pins. These capacitors are located on the back of the board.

4.2 ADC Reference Circuitry

These ADCs have an internal reference but can use an external reference as well. An adjustable reference circuit is provided on this board. To use the external voltage reference, leave JP2 open. To use the on-chip voltage reference, short the pins of JP2.

The evaluation board reference circuit will generate a reference voltage that can be adjusted within the nominal range of 0.8 to 2.5 Volts for the ADC12D040 or 0.4 to 1.3 Volts for the ADC12DL066. The ADC12D040 is will operate with V_{REF} in the range of 1.0 to 2.2 Volts, with a nominal value of 2.0 Volts while the ADC12DL066 is will operate with V_{REF} in the range of 0.8 to 1.2 Volts, with a nominal value of 1.0 Volt. The external reference voltage can be monitored at test point TP1 and is set with R3.

ADC Clock Circuit

The crystal oscillator provided on the evaluation board is selected by shorting pins 2 and 3 of JP1. It is best to remove any external signal generator when using this oscillator to reduce any unnecessary noise.

This board will also accept a clock signal from an external source by connecting that source to BNC J6 and shorting pins 1 and 2 of JP1. A very stable, low jitter source, such as the Agilent 8644B or equivalent, should be used for the clock signal. An a.c. coupled circuit together with a d.c. biased resistive divider is provided so the board can accept a 50 Ohm signal source in the range of 2.2 to $2.5V_{P-P}$ to drive this input. It is best to remove the oscillator at U7 when using an external clock source, or to remove the external source when using U7, to reduce any unnecessary noise.

4.3 Digital Data Output

When using this evaluation board with a WaveVision 5 Data Capture Bboard, the 12-bit ADC12D040 output on both channels may be monitored at J3.

To cause the ADC outputs to be straight binary, pins 1-2 of JP5 should be shorted together. To cause the ADC outputs to be 2's Complement, no jumper should be placed on JP5.

4.4 Power Supply Connections

Power for the EVM should be supplied to connector P1 from a low-noise bench power supply. Switching power supplies may add noise and degrade the performance of the ADC.

4.5 Power Requirements

Voltage and current requirements for the ADC12D040 Evaluation Board alone is +5V at 400 mA.

5 Software Operation and Settings

The latest version of the WaveVision 5 Software can be found online at www.ti.com.

6 Evaluation Board Specifications

Board Size:	5.9" x 6.18" (15.0 cm x 15.7 cm)
Power Requirements:	+5.0V, 340 mA
Clock Frequency Range:	1.0 MHz to 40 MHz (ADC12D040) 1.0 MHz to 66 MHz (ADC12DL066)
Analog Input	
Nominal Voltage:	2.0VP-P (ADC12D040) 1.0VP-P (ADC12DL066)
Impedance:	50 Ohms

7 Hardware Schematic

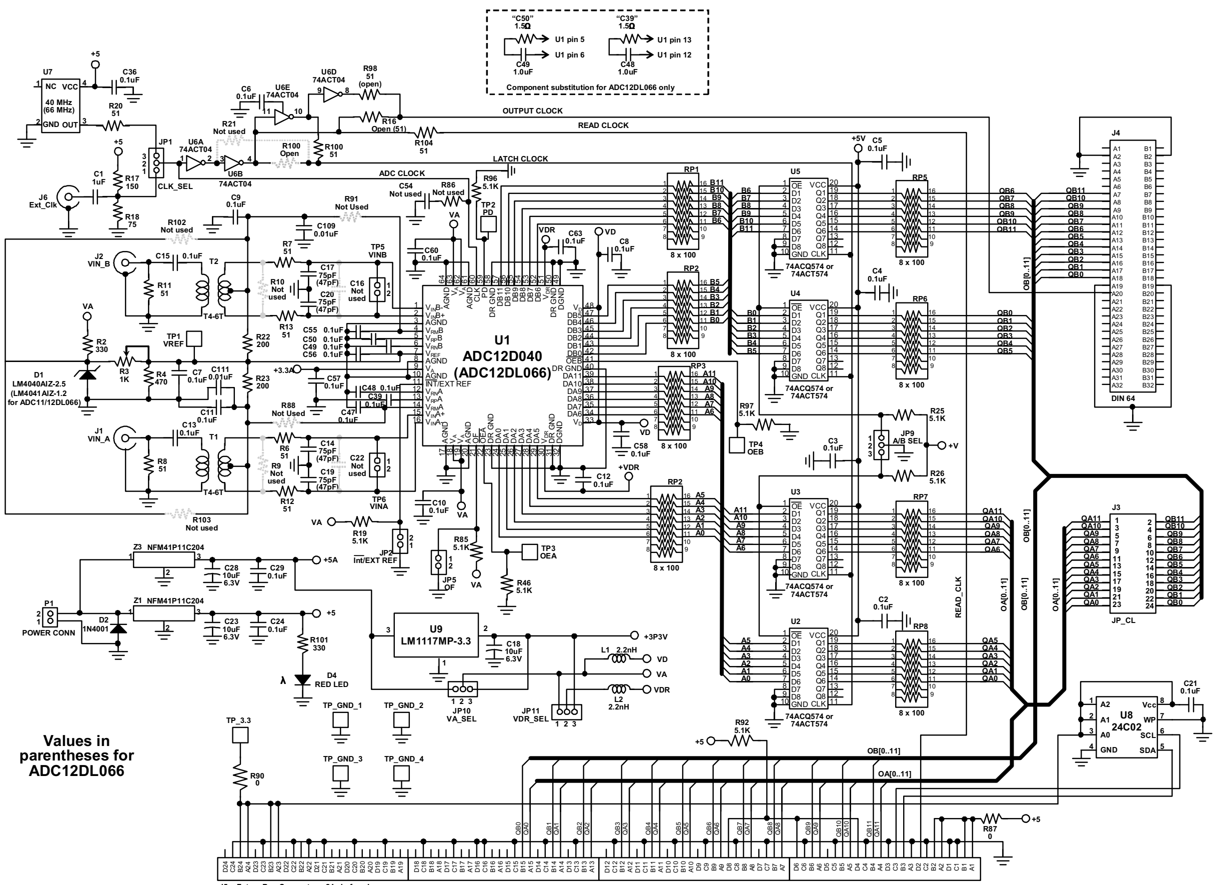

Figure 2. ADC12D040 / ADC12DL066 Evaluation Board Schematic

8 ADC12D040 / ADC12DL066 Evaluation Board Bill of Materials

Table 2. Bill of Materials

Qty	Reference	Part	
1	C1	1uF	Size 0805
2	C109, C111	0.01uF	Size 0805
24	C2–C13, C15, C21, C24, C29, C36, C47, C55–C58, C60, C63	0.1uF	Size 0805
4	C14, C17, C19, C20	75pF (ADC12D040) 47pF (ADC11/12DL066)	Size 0805
3	C18, C23, C28	10uF, 6.3V	Size 1206
–	C16, C22, C54	not populated	n/a
–	C25–C27, C30–C35, C40–C46, C51–C53, C59, C61, C62	Not used	n/a
2	C39, C50	0.1uF (ADC12D040) 1.5Ω resistor (ADC11/12DL066)	Size 0805
2	C48, C49	0.1uF (ADC12D040) 1.0uF (ADC11/12DL066)	Size 0805
1	D1	LM4040AIZ-2.5 (ADC12D040) LM4041AIZ-1.2 (ADC11/12DL066)	Texas Instruments
1	D2	1N4001 or 1N4002 or 1N4003	Various
1	D4	Red LED	Various
4	JP2, JP5, TP5, TP6	2-Pin Post Headers	DigiKey # A19351-ND
1	JP1	3-pin Post Headers	DigiKey # A19350-ND
1	JP9	Hard-Wired all together for ADC12D040 and ADC11/12DL066	
1	JP11	3-pin Post Header for ADC12D040 Hard-Wired for ADC11/12DL066	DigiKey # A19350-ND n/a
–	JP10	Hard wired	n/a
3	J1, J2, J6	BNC Connectors	DigiKey # ARF1177-ND
1	J3	24-pin Header	DigiKey # S2011-12-ND
-	J4	Not Populated	n/a
4	J5	Future Bus Connector	Amp # 223514-1
2	L1, L2	Wide-Band Choke	DigiKey # M2103-ND or JW Miller # FB20010-3B
1	P1	Terminal Block	DigiKey # ED1609-ND
1	R3	1K Pot	DigiKey # 3386P-102-ND
1	R90	0 Ohms	Size 1206
2	R2, R101	330, 5%	Size 1206
1	R4	470, 5%	Size 1206
10	R6–R8, R11–R13, R16, R20, R100, R104	51, 5%	Size 1206
1	R18	75, 5%	Size 1206
1	R17	150, 5%	Size 1206
2	R22, R23	200, 5%	Size 1206
8	R19, R25, R26, R46, R85, R92, R96, R97	5.1k, 5%	Size 1206
–	R9, R10, R21, R88, R86, R91, R98, R102, R103	Not populated	n/a
–	R87	Not Populated	n/a
–	R1, R5	Not used	n/a
8	RP1–RP8	Resistor Pack - 8 x 100	DigiKey # 766-163-R101-ND or DigiKey # 768-163-R101-ND

Table 2. Bill of Materials (continued)

1	TP–TP4, TP_GND_1, TP_GND_2, TP_GND_3, TP_GND_4, TP_3.3	Breakable Header	DigiKey # S1012-36-ND
2	T1, T2	Signal Transformer	MiniCircuits Type T4-6T
1	U1	ADC12D040CIVS, ADC11DL066CIVS or ADC12DL066CIVS	Texas Instruments
4	U2, U3, U4, U5	74AT574SC or 74ACT574SC	Fairchild Semiconductor
1	U6	74AC04SC or 74ACT04SC	Fairchild Semiconductor
1	U7	40MHz Osc (ADC12D040) 66MHz Osc (ADC11/12DL066)	Pletronics #P1145-3SD-40.00M or DigiKey # CTX120-ND (ADC12D040) or Pletronics #P1145-3SD-66.667M or DigiKey # CTX137-ND (ADC11/12L066)
1	U8	24C02	Various
1	U9	LM1117MP-3.3	Texas Instruments
2	Z1, Z3	Noise Filters	Murata # NFM41P11C204
1	--	4-Pin full-size oscillator socket	DigiKey # A462-ND

Appendix A

A.1 Summary Tables of Test Points, Connectors, and Connectors

Table 3. Test Points on the ADC12D040/ADC11DL066/ADC12DL066 Evaluation Board

TP1: V_{REF}	ADC Reference Voltage Test Point.
TP2: PD	Power Down control. Apply a logic high voltage here to power down the A/D Converter.
TP3: OEA	Output Enable for ADC "A". Apply a logic high voltage here to disable outputs "A".
TP4: OEB	Output Enable for ADC "B". Apply a logic high voltage here to disable outputs "B".
TP5: VINB	Differential input signal to ADC "B"
TP6: VINA	Differential input signal to ADC "A"
TP_3.3	3.3 Volt test point from the WaveVison4 Board.
TP_GND_1	Ground. Located in corner nearest TP_3.3
TP_GND_2	Ground. Located in corner nearest board identification silk screen.
TP_GND_3	Ground. Located in corner nearest Power Connector
TP_GND_4	Ground. Located in corner nearest BNC J2.

Connectors and Selection Jumpers on the ADC12D040/ADC11DL066/ADC12DL066 Evaluation Board

J1: BNC Connector	Single-Ended input to ADC "A"
J2: BNC Connector	Single-Ended input to ADC "B"
J3: JP_CL	Put jumpers on all 12 pin pairs to make output bus available on J4 available for converter selected by JP9.
J4: DIN 64	Not used.
J5: Future Bus connector	Future Bus connector for use with WaveVision 5 Data Capture Board
J6: BNC Connector	External Clock Input

Table 4. Selection Jumpers on the ADC12D040/ADC11DL066/ADC12DL066 Evaluation Board

JP1: CLK_SEL	Jumper pins 2-3 to select on-board oscillator at U7 or jumper pins 1-2 to select external clock at J6
JP2: INT/EXT REF	Place jumper on these pins to select the internal 1.0V reference; leave jumper off to use external reference.
JP3:	Not Used
JP4:	Not Used
JP5: OF	Place jumper on these pins to select Offset Binary output format; leave jumper off for 2's complement.
JP6:	Not Used
JP7:	Not Used
JP8:	Not Used
JP9: A/B SEL	Hard-wired together
JP10: VA_SEL	Hard-wired to +5.0V for ADC12D040. Hard-wired to 3.3V for ADC12DL066
JP11: V_{DR}_SEL	Jumper pins 2-3 to select 3.3V for V_{DR} (output driver supply) or jumper pins 1-2 to select ADC supply for V_{DR}. Hard-wired to 3.3V for ADC12DL066

Table 5. P1: Connector - Power Supply Connections

P1-1	+5V	Positive Supply voltage (+5V)
P1-2	GND	Power Supply Ground

Table 6. J3: Latch Outputs

J3 pin number	Signal (when channel enabled)
1, 2	B11(MSB) Ch A, B11(MSB) Ch B
3, 4	B10 Ch A, B10 Ch B
5, 6	B9 Ch A, B9 Ch B
7, 8	B8 Ch A, B8 Ch B
9, 10	B7 Ch A, B7 Ch B
11, 12	B6 Ch A, B6 Ch B
13, 14	B5 Ch A, B5 Ch B
15, 16	B4 Ch A, B4 Ch B
17, 18	B3 Ch A, B3 Ch B
19, 20	B2 Ch A, B2 Ch B
21, 22	B1 Ch A, B1 Ch B
23, 24	B0(LSB) Ch A, B0(LSB)

Table 7. J5: Future Bus connector for use with WAVEVSN BRD 4.0 Data Capture Board

J5 Pin Number	Signal
A1, B1, A2, B2	Not connected
C1 thru C24	Ground
A3, A22, B3, D1, D16	Ground
D2	READ_CLK to clock data into RAM
A4	QA11 - Bit 11 (MSB) output for ADC "A"
B4	QB11 - Bit 11 output for ADC "B"
A5	QA10 - Bit 10 output for ADC "A"
B5	QB10 - Bit 10 output for ADC "B"
A6	QA9 - Bit 9 output for ADC "A"
B6	QB9 - Bit 9 output for ADC "B"
A7	QA8 - Bit 8 output for ADC "A"
B7	QB8 - Bit 8 output for ADC "B"
A8	QA7 - Bit 7 output for ADC "A"
B8	QB7 - Bit 7 output for ADC "B"
A9	QA6 - Bit 7 output for ADC "A"
B9	QB6 - Bit 7 output for ADC "B"
A10	QA5 - Bit 7 output for ADC "A"
B10	QB5 - Bit 7 output for ADC "B"
A11	QA4 - Bit 7 output for ADC "A"
B11	QB4 - Bit 7 output for ADC "B"
A12	QA3 - Bit 7 output for ADC "A"
B12	QB3 - Bit 7 output for ADC "B"
A13	QA2 - Bit 7 output for ADC "A"
B13	QB2 - Bit 7 output for ADC "B"
A14	QA1 - Bit 7 output for ADC "A"
B14	QB1 - Bit 7 output for ADC "B"
A15	QA0 - Bit 7 output for ADC "A"
B15	QB0 - Bit 7 output for ADC "B"
D4, D6, D8	Board ID pins - not used
A23, B23, A24, B24	3.3V from WaveVision4 Data Capture Board
A16 thru A21	Not Used
B16 thru B21	Not Used
D5, D7, D9 thru D15	Not Used
D17 thru D24	Not Used

Revision History

Changes from Original (December 2005) to A Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Important Notice for Users of EVMs Considered “Radio Frequency Products” in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

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IMPORTANT NOTICE

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