2-/3-/4-Phase Synchronous Buck Controller for IMVP-5 CPUs

ADP3206

FEATURES

- **Selectable 2-, 3-, or 4-phase operation at up to 1 MHz per phase**
- **6-bit digitally programmable 0.8375 V to 1.6 V output**
- **±10 mV DAC accuracy over temperature**
- **Logic-level PWM outputs for interface to external high power drivers**
- **Active current/thermal balancing between phases**
- **Built-in power good/crowbar blanking supports on-the-fly VID code changes**
- **Programmable deep sleep offset and deeper sleep reference voltage**
- **Programmable soft transient control to minimize inrush currents during output voltage changes**
- **Programmable short circuit protection with programmable latch-off delay**

APPLICATIONS

- **Desk-note and notebook PC power supplies for IMVP-5 compliant Intel® processors**

GENERAL DESCRIPTION

The ADP3206 is a highly efficient multiphase synchronous buck-switching regulator controller optimized for converting the notebook main supply into the core supply voltage required by IMVP-5 Intel processors. It uses an internal 6-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.8375 V and 1.6 V, and uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation.

The ADP3206 includes programmable no-load offset and slope functions to adjust the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3206 also provides accurate and reliable short circuit protection, adjustable current limiting, deep sleep and deeper sleep programming inputs, and a delayed power good output that accommodates on-the-fly output voltage changes requested by the CPU.

ADP3206 is specified over the commercial temperature range of 0°C to 100°C and is available in a 40-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

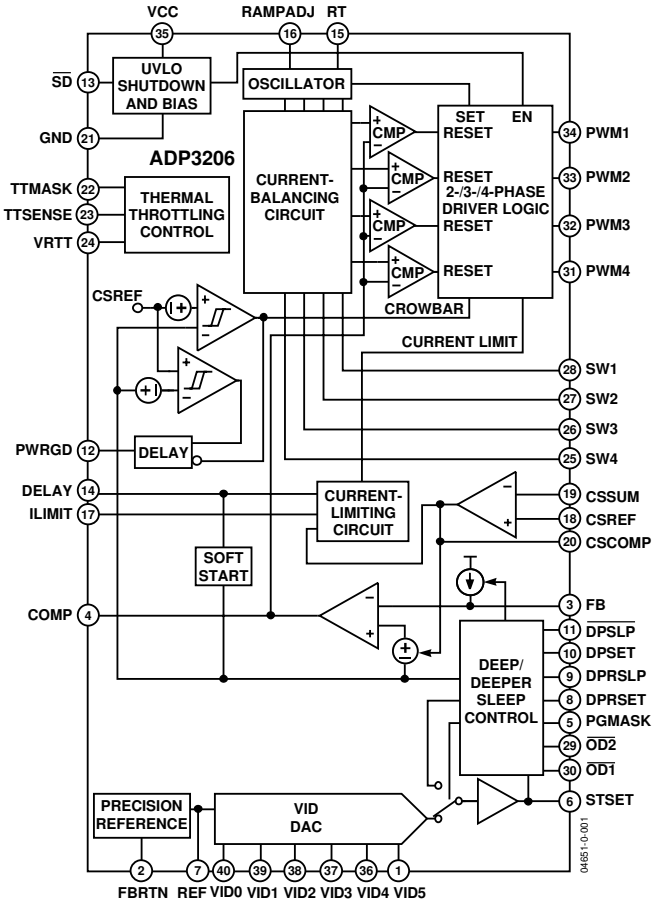

Figure 1.

Rev. 0

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REVISION HISTORY

4/04—Revision 0: Initial Version

SPECIFICATIONS

Table 1. VCC = 5 V, FBRTN = DPRSLP = GND, $\overline{SD}$ = 1.2 V, DPSLP = 3.3 V, T_A = 0°C to 100°C, unless otherwise noted.[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE and VID DAC						
Reference Output Voltage	V_{REF}	I_{REF} = 100 μA	2.95	3.0	3.05	V
		I_{REF} = 4 mA	2.93	3.0	3.07	V
Output Current Range	I_{REF}		0		4	mA
Normal Mode Output Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, DPRSLP = 0 V	−10		+10	mV
Deeper Sleep Output Accuracy	V_{STSET}	Relative to DPRSET input, referenced to FBRTN, DPRSLP = 3.3 V	−5		+5	mV
Input Low Voltage	$V_{IL(VID)}$				0.4	V
Input High Voltage	$V_{IH(VID)}$		0.8			V
Input Current, Input Voltage Low	$I_{IL(VID)}$	VID(X) = 0 V		−20	−30	μA
Input Current, Input Voltage High	$I_{IH(VID)}$	VID(X) = 1.25 V		5	15	μA
Pull-up resistance	R_{VID}		35	60		kΩ
Internal Pull-up Voltage			0.9	1.1	1.25	V
VID Transition Delay Time[1]		VID change to DACREF change	400			ns
No CPU Detection Turn-off Delay Time[2]		VID change to 1111 to PWM going low	400			ns
DEEPSLEEP/DEEPERSLEEP CONTROL						
DPSLP, DPRSLP						
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Current			−1		1	μA
OD1, OD2						
Output Voltage Low	V_{OL}	$I_{ODX(SINK)}$ = 400 μA		80	500	mV
Output Voltage High	V_{OH}	$I_{ODX(SOURCE)}$ = 400 μA	4.0	5.0		V
DPSET						
Output Voltage	V_{DPSET}	DPSET – Nominal VID output	−70		+70	mV
Output Current Range	I_{DPSET}		0		100	μA
DPRSET						
Input Voltage Range	V_{DPRSET}		0.5		1.0	V
Input Current	I_{DPRSET}		−1		1	μA
STSET						
Minimum Capacitance	C_{STET}		100			pF
Transient Time		DPSET = 0.75 V		100		μs
		Nominal VID output = 1.55 V, C_{STSET} = 1.5 nF				
Output Voltage Range			0.5		3	V
Output Current	I_{STSET}	DPSET = 0.75 V, DPRSLP – 3.3 V				
		V_{STSET} = 2 V	−19	−16	−13	μA
		V_{STSET} = 0.5 V	13	16	19	μA
THERMAL THROTTLING CONTROL						
TTSENSE Voltage Range			0		2	V
TTSENSE Threshold Voltage			1.46	1.5	1.54	V
TTSENSE Bias Current			−1		1	μA
TTMASK Threshold Voltage			1.45	1.5	1.55	V
TTMASK Output Low Voltage		TTSENSE static, $I_{TTMASK(SINK)}$ = 1 mA			200	mV
VRTT Output Voltage Low	V_{OL}	$I_{VRTT(SINK)}$ = 200 μA		100	500	mV
VRTT Output Voltage High	V_{OH}	$I_{VRTT(SOURCE)}$ = 200 μA	4.0	5.0		V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Output Voltage Range	V_{COMP}		0.8		3.3	V
Line Regulation	ΔV_{FB}	VCC = 4.5 V to 5.5 V		0.05		%
FB Input Bias Current	I_{FB}	DPSLP = 3.3 V	14	16	18	µA
		DPSLP = DRSLP = 0 V, I_{DPSET} = 60 µA	70	75	80	µA
FBRTN Current	I_{FBRTN}			85	120	µA
Output Current	$I_{O(ERR)}$	FB Forced to V_{OUT} = 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		C_{COMP} = 10 pF		50		V/µs
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		4	MHz
Frequency Variation	f_{PHASE}	T_A = +25°C, R_T = 250 kΩ, 4-Phase	155	200	245	kHz
		T_A = +25°C, R_T = 115 kΩ, 4-Phase		400		kHz
		T_A = +25°C, R_T = 75 kΩ, 4-Phase		600		kHz
Output Voltage	VRT	R_T = 100 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ = FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$				100	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF, see Figure 1	−1.5		+1.5	mV
Gain Bandwidth Product	$GBW_{(CSA)}$			10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		25		V/µs
Input Common Mode Range		CSSUM and CSREF	0		3	V
Positioning Accuracy	ΔV_{FB}	FB − V_{VID}, see Figure 2	−75	−80	−85	mV
CSSUM Bias Current	I_{CSSUM}			20	100	nA
CSREF Bias Current	I_{CSREF}			0.5	5	µA
Output Current[2]	I_{CSCOMP}	CSAMP unity gain				
		Sourcing	500			µA
		Sinking			−300	µA
CURRENT BALANCE CIRCUIT						
Common Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistant	$R_{SW(X)}$	$S_{W(X)}$ = 0 V	22	32	42	kΩ
Input Current	$I_{SW(X)}$	$S_{W(X)}$ = 0 V	4	7	10	µA
Input Current Matching	$\Delta I_{SW(X)}$	$S_{W(X)}$ = 0 V	−5		+5	%
CURRENT LIMIT COMPARATOR						
Output Voltage	V_{ILIMIT}	R_{ILIMIT} = 200 kΩ	0.95	1	1.05	V
Output Current	I_{ILIMIT}	R_{ILIMIT} = 200 kΩ		5		µA
Current Limit Threshold Voltage	V_{CL}	V_{CSREF} − V_{CSCOMP}, R_{ILIMIT} = 200 kΩ				
		4 Phase				
		DPRSLP = 0 V	105	120	145	mV
		DPRSLP = 3.3 V	15	30	45	mV
Latch-Off Delay Threshold	V_{DELAY}	In current limit	1.7	1.8	1.9	V
Latch-Off Delay Time	t_{DELAY}	R_{DELAY} = 250 kΩ C_{DELAY} = 4.7 nF		1.2		ms
SOFT START						
Output Current, Soft-Start Mode	$I_{DELAY(SS)}$	During start-up, delay < 2.8 V	15	20	25	µA
Output Voltage	V_{DELAY}			3		V
Soft-Start Delay Time	$t_{DELAY(SS)}$	R_{DELAY} = 250 kΩ, C_{DELAY} = 4.7 nF, VID code = 011111		600		µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SHUTDOWN INPUT						
Input Low Voltage	$V_{IL(SD)}$				0.4	V
Input High Voltage	$V_{IH(SD)}$		0.8			V
Input Current, Input Voltage Low	$I_{IL(SD)}$	$\overline{SD}$ = 0 V	−1		1	μA
Input Current, Input Voltage High	$I_{IH(SD)}$	$\overline{SD}$ = 1.25 V		10	25	μA
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal output	−200	−250	−300	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal output	100	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 4 mA		150	400	mV
Power Good Delay Time						
VID Code Changing		C_{PGMASK} = 150 pF		90		μs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to nominal output	100	150	200	mV
Crowbar Reset Point			350	450	550	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low				
VID Code Changing		C_{PGMASK} = 150 pF		90		μs
VID Code Static				400		ns
POWER GOOD MASKING						
Threshold Voltage			2.85	3	3.15	V
Output Current		DPRSLP or VID changing, V_{PGMASK} = 0 V	3.5	5	6.5	μA
		DPRSLP or VID static, V_{PGMASK} = 0.5 V	500			μA
PWM OUTPUTS						
Output Voltage Low	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400 μA		100	500	mV
Output Voltage High	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 μA	4.0	5.0		V
SUPPLY						
Supply Voltage Range	V_{CC}		4.5		5.5	V
Supply Current	I_{CC}			3.5	6	mA
UVLO Threshold Voltage	V_{UVLO}	VCC Rising	3.6	3.8	4.1	V
UVLO Hysteresis	ΔV_{UVLO}		50	100	150	mV

[1] All limits at temperature extremes are guaranteed via correlation using Standard Statistical Quality Control (SQC).
[2] Guaranteed by design or bench characterization, not production tested.

TEST CIRCUITS

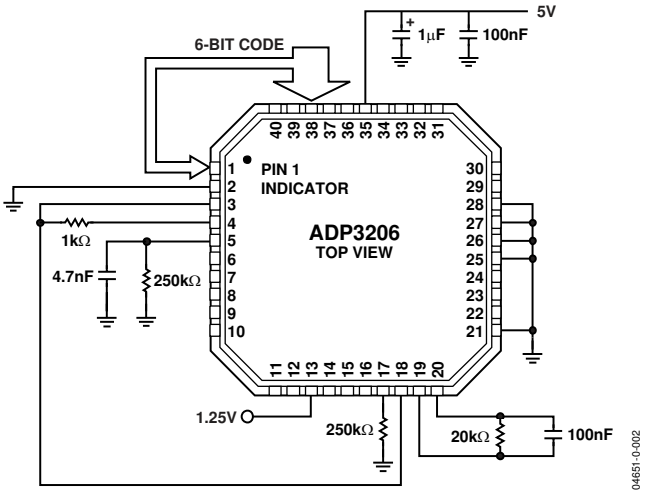


Figure 2. Closed-Loop Output Voltage Accuracy

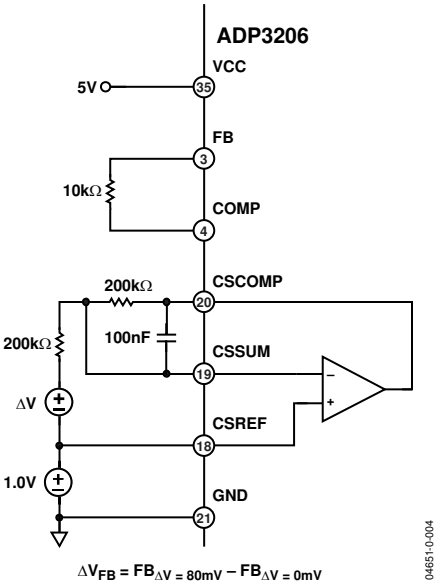


Figure 4. Positioning Voltage

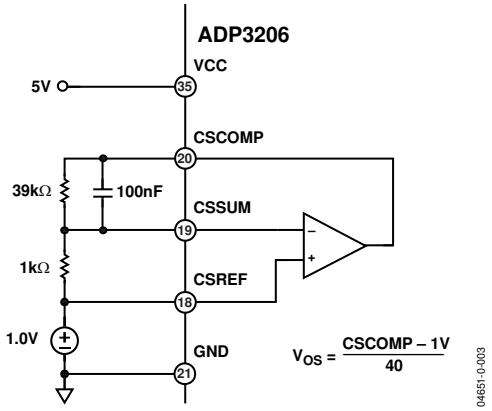


Figure 3. Current Sense Amplifier V_{OS}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	–0.3 V to + 6 V
FBRTN	–0.3 V to + 0.3 V
SW1 – SW4	–5 V to + 25 V
All other Inputs & Outputs	–0.3 V to + 6 V
Operating Ambient Temperature Range	0°C to +100°C
Operating Junction Temperature	125°C
Storage Temperature Range	–65°C to +150°C
θ_{JA}	100°C/W
Lead Temperature Range (Soldering 10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

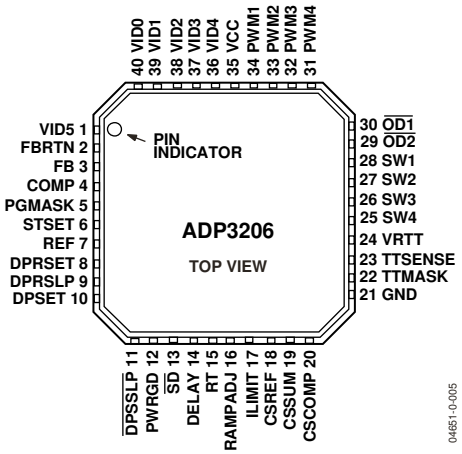


Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 36 to 40	VID5, VID4 to VID0	Voltage Identification DAC Inputs. These six pins are pulled up to an internal reference, providing a Logic 1 if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.8375 V to 1.6 V. Leaving all VID4 through VID0 open results in the ADP3206 going into a "No CPU" mode, shutting off its PWM outputs.
2	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
3	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no-load offset point.
4	COMP	Error Amplifier Output and Compensation Point.
5	PGMASK	Power Good Masking. A capacitor connected between this pin and GND sets the Power Good Comparator masking time during DPRSLP and VID pin transitions.
6	STSET	Soft Transient Setting Input. A capacitor connected between this pin and GND controls the slew rate of the output voltage during transitions between various operating modes.
7	REF	Internal 3 V Reference Output.
8	DPRSET	Deeper Sleep Voltage Setting Input used as the DAC reference voltage when DPRSLP is asserted.
9	DPRSLP	Deeper Sleep Control Input.
10	DPSET	Deep Sleep Offset Voltage Setting Input. The offset programmed by a resistor connected between this pin and GND is activated when DPSLP is asserted.
11	$\overline{\text{DPSLP}}$	Deep Sleep Control Input.
12	PWRGD	Power Good Output. Open drain output that signals when the output voltage is outside of the proper operating range.
13	$\overline{\text{SD}}$	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs.
14	DELAY	Soft-start Delay and Current Limit Latch-off Delay Setting Input. An external resistor/capacitor connected between this pin and GND sets the soft-start ramp-up time and the overcurrent latch-off delay time.
15	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
16	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
17	ILIMIT	Current Limit Set Point. An external resistor from this pin to GND sets the current limit threshold of the converter.
18	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power good and crowbar functions. This pin should be connected to the common point of the output inductors.
19	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.

Pin No.	Mnemonic	Description
20	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the slope of the load line and the positioning loop response time.
21	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
22	TTMASK	Thermal Throttling Masking Time Setting Input. An external resistor from this pin to VCC and an external capacitor to GND set the delay time during which the VRTT output is masked. This delay is triggered by the assertion or de-assertion of VRTT.
23	TTSENSE	VR Hot Thermal Throttling Sense Input. This pin monitors the common tap point of an external resistor-thermistor voltage divider network and causes VRTT output signal to go high if the remotely sensed hot spot temperature exceeds the programmed temperature threshold.
24	VRTT	Voltage Regulator Thermal Throttling Output. This logic output alerts the CPU that the temperature at one of the designated monitoring points has exceeded the programmed temperature threshold.
25-28	SW4 – SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
29	$\overline{OD2}$	This pin is actively pulled low under the same conditions as those of $\overline{OD1}$. In addition, this pin is actively pulled low when DPRSLP is asserted. This pin is normally connected to the $\overline{SD}$ input of the drivers for phases 2 through 4.
30	$\overline{OD1}$	This pin is actively pulled low when the ADP3206 $\overline{SD}$ input is low, or when VCC is below its UVLO threshold to signal to the driver IC that the driver high-side and low-side outputs should go low. This pin is normally connected to the $\overline{SD}$ input of the phase 1 driver.
31-34	PWM4 – PWM1	Logic-level PWM Outputs. Each output connects to the input of an external MOSFET driver. Connecting the PWM3 and/or PWM4 outputs to GND causes that phase to turn off, allowing the ADP3206 to operate as a 2-, 3-, or 4-phase controller.
35	VCC	Supply Voltage for the device.

TYPICAL PERFORMANCE CHARACTERISTICS

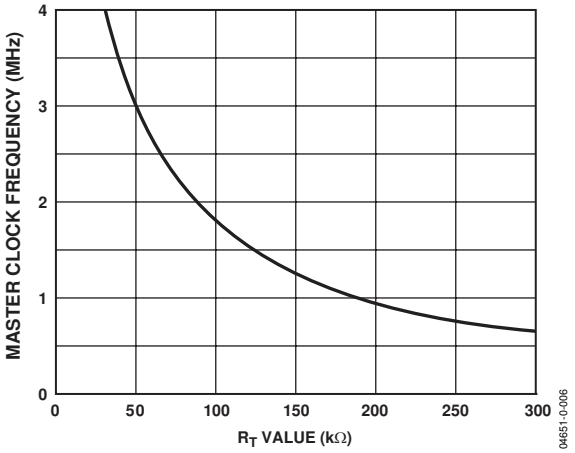


Figure 6. Master Clock Frequency vs. R_T

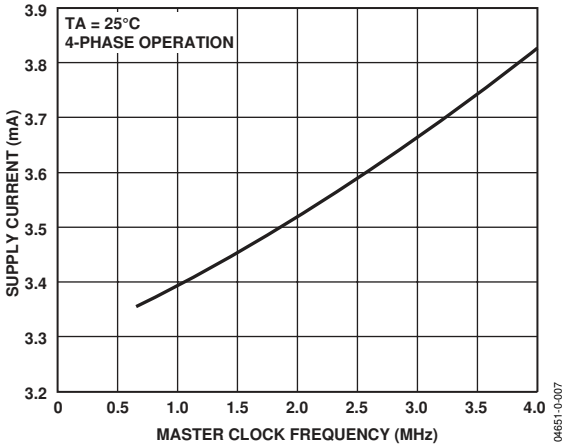


Figure 7. Supply Current vs. Oscillator Frequency

THEORY OF OPERATION

The ADP3206 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 2-, 3-, and 4-phase synchronous buck CPU core supply power converters. The internal 6-bit VID DAC conforms to Intel's IMVP-5 specifications. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter would place high thermal demands on the components in the system such as the inductors and MOSFETs.

The multimode control of the ADP3206 ensures a stable, high performance topology for

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- High current output from having up to 4 phase operation
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

NUMBER OF PHASES

The number of operational phases and their phase relationship is determined by internal circuitry that monitors the PWM outputs. Normally, the ADP3206 operates as a 4-phase PWM controller. Grounding the PWM4 pin programs 3-phase operation, and grounding the PWM3 and PWM4 pins programs 2-phase operation.

When the ADP3206 is enabled, the controller outputs a voltage on PWM3 and PWM4 that is approximately 550 mV. An internal comparator checks each pin's voltage versus a threshold of 300 mV. If the pin is grounded, then it is below the threshold and the phase is disabled. The output impedance of the PWM pin is approximately 5 kΩ during the phase detect. Any external pull-down resistance connected to the PWM pin should not be less than 25 kΩ to ensure proper phase detection. The phase detection is made during the first two clock cycles of the internal oscillator. After this time, if the PWM output was not grounded, then it switches between 0 V and 5 V. If the PWM output was grounded, then switching to the pin remains off.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3419. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at a time for overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3206 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 6. To determine the frequency per phase, the clock is to be divided by the number of phases in use. If PWM4 is grounded, then divide the master clock by 3 for the frequency of the remaining phases. If PWM3 and 4 are grounded, then divide by 2. If all phases are in use, divide by 4.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3206 combines differential sensing with a high accuracy VID DAC, precision REF output, and a low offset error amplifier to meet Intel's IMVP-5 specification. During normal mode, the VID DAC and error amplifier maintain a worst-case specification of ±10 mV over the full operating output voltage and temperature range. For Deeper Sleep operation, an external resistor divider from the REF pin to FBRTN creates the DPRSET voltage. This voltage is buffered by a low offset, slew rate limited amplifier that is used to drive the noninverting input of the error amplifier.

The core output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC, DPRSET voltage, and precision REF output are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing.

OUTPUT CURRENT SENSING

The ADP3206 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current and for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method then peak current detection or sampling the current across a sense element such as the low side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor ESR sensing without thermistor for lowest cost
- Output inductor ESR sensing with thermistor to improve accuracy for tracking inductor temperature
- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor to set the load line required by the microprocessor. The current information is then given as the difference of CSREF − CSCOMP. This difference signal is used internally to offset the error amplifier for voltage positioning and as a differential input for the current limit comparator.

To provide the best accuracy for current sensing, the CSA has been designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors so that it can be made extremely accurate.

ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the CSCOMP pin can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the error amplifier offset voltage to tell the error amplifier where the output voltage should be. This differs from previous implementations and allows enhanced feed-forward response

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3206 has individual inputs for each phase which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It is also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the applications section.

External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase may have better cooling and can support higher currents. Resistors R_{SW1} through R_{SW4} (see the typical application circuit in Figure 1) can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, so make sure placeholders are provided in the layout.

To increase the current in any given phase, make R_{SW} for that phase larger (make $R_{SW} = 0$ for the hottest phase and do not change during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain-bandwidth error amplifier is used for the voltage-mode control loop. During normal mode, the noninverting input voltage is set via the 6-bit VID logic code listed in Table 4, while during Deeper Sleep operation, it is set to track the buffered DPRSET voltage. The noninverting input voltage is also offset by the droop voltage for offsetting the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with a resistor R_B and is used for sensing and controlling the output voltage at this point. During normal mode, a current source from the FB pin flowing through R_B is used for setting the no-load offset voltage from the VID voltage. The no-load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated in the feedback network between FB and COMP.

Table 4. Output Voltage vs. VID Code (X = Don't Care)

VID4	VID3	VID2	VID1	VID0	VID5	$V_{OUT(NOM)}$
0	1	0	1	0	0	0.8375 V
0	1	0	0	1	1	0.850 V
0	1	0	0	1	0	0.8625 V
0	1	0	0	0	1	0.875 V
0	1	0	0	0	0	0.8875 V
0	0	1	1	1	1	0.900 V
0	0	1	1	1	0	0.9125 V
0	0	1	1	0	1	0.925 V
0	0	1	1	0	0	0.9375 V
0	0	1	0	1	1	0.950 V
0	0	1	0	1	0	0.9625 V
0	0	1	0	0	1	0.975 V
0	0	1	0	0	0	0.9875 V
0	0	0	1	1	1	1.000 V
0	0	0	1	1	0	1.0125 V
0	0	0	1	0	1	1.025 V
0	0	0	1	0	0	1.0375 V
0	0	0	0	1	1	1.050 V
0	0	0	0	1	0	1.0625 V
0	0	0	0	0	1	1.075 V
0	0	0	0	0	0	1.0875 V
1	1	1	1	0	1	1.100 V
1	1	1	1	0	0	1.1125 V
1	1	1	0	1	1	1.125 V
1	1	1	0	1	0	1.1375 V
1	1	1	0	0	1	1.150 V
1	1	1	0	0	0	1.1625 V
1	1	0	1	1	1	1.175 V
1	1	0	1	1	0	1.1875 V
1	1	0	1	0	1	1.200 V
1	1	0	1	0	0	1.2125 V
1	1	0	0	1	1	1.225 V
1	1	0	0	1	0	1.2375 V
1	1	0	0	0	1	1.250 V
1	1	0	0	0	0	1.2625 V
1	0	1	1	1	1	1.275 V
1	0	1	1	1	0	1.2875 V
1	0	1	1	0	1	1.300 V
1	0	1	1	0	0	1.3125 V
1	0	1	0	1	1	1.325 V
1	0	1	0	1	0	1.3375 V
1	0	1	0	0	1	1.350 V
1	0	1	0	0	0	1.3625 V
1	0	0	1	1	1	1.375 V
1	0	0	1	1	0	1.3875 V
1	0	0	1	0	1	1.400 V
1	0	0	1	0	0	1.4125 V
1	0	0	0	1	1	1.425 V
1	0	0	0	1	0	1.4375 V
1	0	0	0	0	1	1.450 V
1	0	0	0	0	0	1.4625 V
0	1	1	1	1	1	1.475 V
0	1	1	1	1	0	1.4875 V
0	1	1	1	0	1	1.500 V
0	1	1	1	0	0	1.5125 V
0	1	1	0	1	1	1.525 V
0	1	1	0	1	0	1.5375 V
0	1	1	0	0	1	1.550 V
0	1	1	0	0	0	1.5625 V
0	1	0	1	1	1	1.575 V
0	1	0	1	1	0	1.5875 V
0	1	0	1	0	1	1.600 V
1	1	1	1	1	X	No CPU

DEEP SLEEP AND DEEPER SLEEP SETTINGS

The ADP3206 includes circuitry to perform both Deep Sleep and Deeper Sleep functions. During Deep Sleep, the IMVP-5 specification requires that the core output voltage be decreased by a fixed percentage. This decrease is user programmable. The ADP3206 accomplishes this function by forcing the programmed DAC voltage on the DPSET pin. An external resistor between this pin and ground generates a current that is proportional to the DAC voltage. This Deep Sleep offset current is then mirrored and forced out of the FB pin along with the no-load offset current. This causes the core output voltage to be negative with respect to the VID DAC. To enter Deep Sleep operation, $\overline{\text{DPSLP}}$ and DPRSLP must be low.

The ADP3206 also provides a soft transient function to reduce inrush current during transitions into and out of Deeper Sleep. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors due to added stress. The slew rate for the soft transient is set by the external capacitor on the STSET pin and the 15 µA output current of the low offset buffer. During normal and Deep Sleep modes, the output of the VID DAC is connected to the buffer, thereby forcing the STSET voltage to the nominal DAC voltage. When the DPRSLP signal is forced high, the ADP3206 enters into Deeper Sleep mode. First, the Deep Sleep offset current is shut off. Next, the VID DAC output is disconnected from the noninverting input of the Error Amplifier, while the STSET pin is connected. The DPRSET pin is then connected to the input of the buffer, which causes the STSET voltage to slew from the nominal DAC voltage to the DPRSET voltage. Because the core voltage follows the noninverting input of the error amplifier, the output voltage transitions to the Deeper Sleep voltage. To exit Deeper Sleep, the DPRSLP pin must be forced low. The DPRSET pin is then disconnected from the buffer and the VID DAC signal is connected. This causes the STSET voltage to slew from the DPRSET voltage to the programmed DAC voltage. The core voltage follows this transition. After the STSET voltage

reaches the programmed DAC voltage, the STSET pin is disconnected from noninverting input of the error amplifier, while the VID DAC output is connected.

During transitions into/out of Deeper Sleep, the Power Good circuit is masked to prevent false triggering of the PWRGD signal. The masking time is set by an external capacitor, which is placed between the PGMASK pin and ground. This capacitor is discharged to ground during normal operation. During a transition of the DPRSLP pin, the masking time begins and the capacitor is charged up by a current source. Once the voltage on the PGMASK pin reaches 3V, the masking time has ended and the PGMASK capacitor is reset to ground. If a DPRSLP transition occurs during a masking event, the capacitor on PGMASK is reset to ground to restart the masking time.

To minimize power dissipation during Deeper Sleep, the ADP3206 switches over to single-phase operation. This is accomplished by taking the $\overline{OD2}$ and PWM2, 3, and 4 outputs low upon the completion of the Power Good masking time. This allows for all phases to aid in discharging the core output during the soft transient into Deeper Sleep. When DPRSLP goes low, the $\overline{OD2}$ signal immediately goes high, followed by the normal operation of the PWM2 through PWM4 signals. This allows all phases to aid in the charging of the core output back to the Deep Sleep voltage.

SOFT-START

The power-on ramp up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch-off time as explained in the following section. In UVLO or when $\overline{SD}$ is a logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and $\overline{SD}$ is asserted, the DELAY cap is charged up with an internal 20 µA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush current. The soft-start time depends on the value of VID DAC and C_{DLY}, with a secondary effect from R_{DLY}. Refer to the applications section for detailed information on setting C_{DLY}.

When the PWRGD threshold is reached, the soft-start cycle is stopped and the DELAY pin is pulled up to 3 V. This ensures that the output voltage is at the VID voltage when the PWRGD signals to the system that the output voltage is good. If either $\overline{SD}$ is taken low or VCC drops below UVLO, the DELAY cap is reset to ground to be ready for another soft-start cycle.

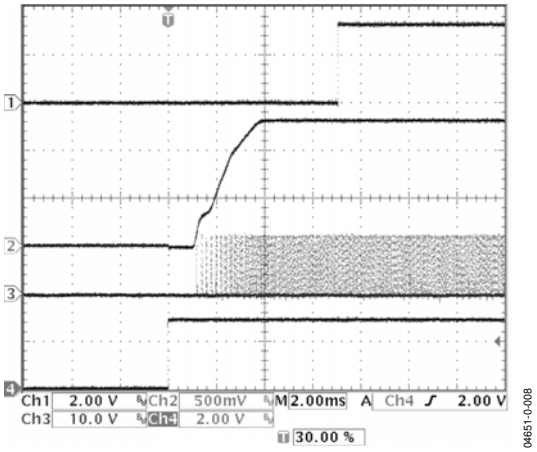


Figure 8. Typical Start-Up Waveforms
Channel 1: PWRGD, Channel 2: V_{CORE},
Channel 3: Phase 2 Switch Node, Channel 4: $\overline{SD}$

CURRENT LIMIT, SHORT CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3206 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The nominal voltage on the ILIMIT pin is 1 V. The level of current limit is set with a resistor from the ILIMIT pin to ground. For four-phase operation during normal mode, the current through the external resistor is internally scaled to give a current limit threshold of 24 mV/µA. During Deeper Sleep mode, the current limit threshold is scaled down to a fraction of the normal mode threshold where the scaling factor is the number of operational phases. For example, a four-phase design scales the current limit threshold to 6 mV/µA. During any mode of operation, if the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current limit latch-off delay time is therefore set by the RC time constant discharging from 3 V to 1.8 V.

Because the controller continues to cycle the phases during the latch-off delay time, if the current limit is removed before the 1.8 V threshold is reached, the controller returns to normal operation. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if current limit has caused the output voltage to drop below the PWRGD threshold, then a soft-start cycle is initiated.

The latch-off function can be reset by both removing and reapplying VCC to the ADP3206, or by pulling the $\overline{SD}$ pin low for a short time. To disable the current limit latch-off function, the external resistor on the DELAY pin to ground should be left open. This prevents the DELAY capacitor from discharging so the 1.8 V threshold is never reached.

During start-up when the output voltage is below 200 mV, a secondary current limit is active because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This limits the voltage drop across the low side MOSFETs through the current balance circuitry.

There is also an inherent per phase current limit that protects individual phases in the case where one or more phases may stop functioning because of a faulty component. This limit is based on the maximum normal-mode COMP voltage.

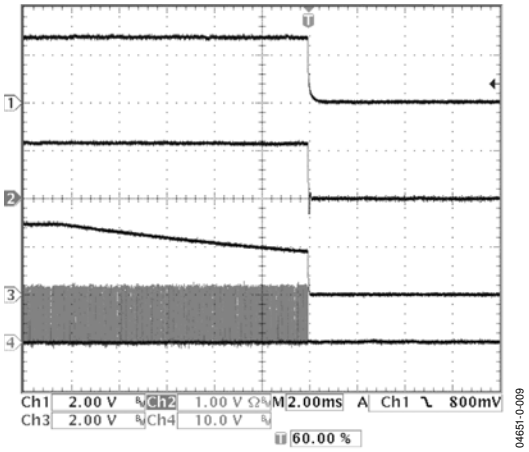


Figure 9. Overcurrent Latch-Off Waveforms
Channel 1: PWRGD, Channel 2: V_{CORE},
Channel 3: Delay, Channel 4: Phase 2 Switch Node

DYNAMIC VID

The ADP3206 incorporates the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID-on-the-fly (OTF). A VID-OTF can occur under either light load or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be either positive or negative.

When a VID input changes state, the ADP3206 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time is to prevent a false code due to logic skew while the6 VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR masking functions to prevent a false PWRGD or CROWBAR event. Each VID change resets the voltage on the PGMASK capacitor.

POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open drain output whose high level (i.e., when it is connected to a pull-up resistor) indicates that the output voltage is within the nominal limits based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range. PWRGD is masked during a VID-OTF event for a period determined by the PGMASK capacitor.

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper power good threshold. This crowbar action stops once the output voltage has fallen below the release threshold of approximately 450 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short of the high side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from destruction.

OUTPUT ENABLE AND UVLO

The input supply (VCC) to the controller must be higher than the UVLO threshold and the $\overline{SD}$ pin must be higher than its logic threshold for the ADP3206 to begin switching. If UVLO is less than the threshold or the SD pin is a logic low, the ADP3206 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the $\overline{OD1}$and $\overline{OD2}$ pins at ground.

Proper power supply sequencing must be adhered to during start-up and shutdown of the ADP3206. All input pins must be at ground prior to applying VCC. During the power down sequence, all input pins must be forced to ground prior to VCC ramping down to ground. All output pins should be left in a high impedance state when VCC is off.

THERMAL THROTTLING CONTROL

The ADP3206 includes a thermal monitoring and masking circuit to detect when a point on the VR has exceeded a user-defined temperature. The thermal monitoring circuit requires an external resistor divider connected between the REF pin and GND. This divider uses a NTC thermistor and a resistor. The midpoint of the divider is connected to the TTSENSE pin in order to generate a voltage that is proportional to temperature.

An internal circuit compares this voltage to a 1.5 V threshold and outputs a logic level signal at the VRTT output. The VRTT output is designed to drive an external transistor. This transistor should be connected to the processors thermal control circuit.

In order to provide temperature hysteresis, a timer is provided to mask the VRTT output. The time is programmed with an external series RC circuit connected between REF and GND. The midpoint of the RC circuit is connected to the TTMASK pin. During shutdown, the TTMASK voltage is forced to ground while the VRTT output is forced low.

Once $\overline{SD}$ goes high, the voltage on TTSENSE is compared to an internal threshold of 1.5 V. If the voltage on TTSENSE rises above the threshold, the VRTT output goes high. During this transition, the masking timer starts. The TTMASK voltage now increases based upon the RC time constant. During this charging time, the VRTT signal is latched and remains high regardless of changes in the TTSENSE voltage. Once the TTMASK voltage reaches the 1.5 V threshold, the TTMASK pin is forced to ground to reset the timer and complete the masking time. In the event that the TTSENSE voltage goes below the threshold, the above masking time and latching of the new VRTT signal occurs again.

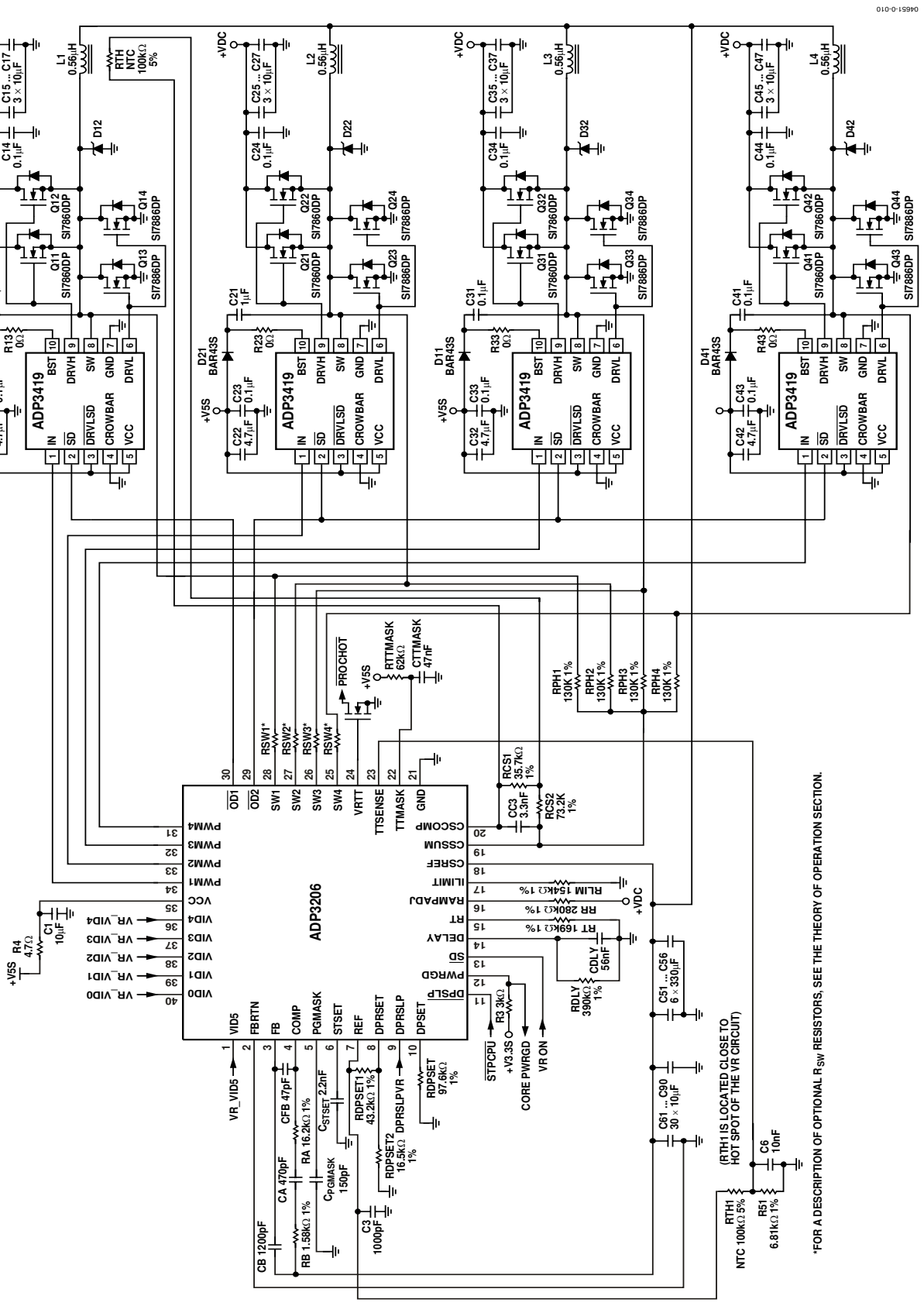


Figure 10. Typical IMVP-5 Application Circuit

APPLICATION INFORMATION

The design parameters for a typical Intel IMVP5-compliant CPU Core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 8 V
- Output voltage by VID setting (V_{VID}) = 1.350 V
- Nominal output voltage at No Load (V_{ONL}) = 1.325 V
- Offset voltage (V_{OFFSET}) = 1.350 V-1.325 V = 0.025 V
- Nominal output voltage at 80 A Load (V_{OFL}) = 1.221 V
- Duty cycle at maximum input voltage (D_{MIN}) = 0.070
- Duty cycle at minimum input voltage (D_{MAX}) = 0.166
- Load line slope (R_O) = 1.3 mΩ
- Static output voltage drop from no load to full load (V_Δ) = V_{ONL} - V_{OFL} = 1.325 V - 1.221 V = 104 mV
- Maximum output current (I_O) = 80 A
- Maximum output current step (ΔI_O) = 56 A
- Number of phases (n) = 4
- Switching frequency per phase (f_{SW}) = 280 kHz
- Deepersleep voltage at no load (V_{DPRSLP}) = 0.8V
- Deepsleep offset percentage (k_{OS}%) = -1.7%

SETTING THE CLOCK FREQUENCY

The ADP3206 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and input and output capacitors. In case of a four-phase design, a clock frequency of 1.12 MHz sets the switching frequency to 280 kHz per phase. This selection represents trade-off between the switching losses and the minimum sizes of the output filter components. Figure 6 shows that to achieve a 1.12 MHz oscillator frequency, R_T has to be 169 kΩ. Alternatively, the value for R_T can be calculated using:

$$R_T = \frac{1}{\left(n \times f_{SW} \times 5.83\ \text{pF}\right) - \frac{1}{1.5\ \text{M}\Omega}} \quad (1)$$

where 5.83 pF and 1.5 MΩ are internal IC component values. For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

SOFT-START, POWER GOOD, AND CURRENT LIMIT LATCH-OFF DELAY TIMES

The soft-start and current limit latch-off delay functions share the DELAY pin, consequently, these two parameters must be considered together. The first step is to set C_{DLY} for the soft-start ramp. This ramp is generated with a 20 µA internal current source. The value of R_{DLY} has a second-order impact on the soft-start time by sinking a portion of the current to ground. However, as long as R_{DLY} is kept greater than 200 kΩ, this effect is negligible. The value for C_{DLY} can be approximated using:

$$C_{DLY} = \left(20\ \text{mA} - \frac{V_{VID}}{2 \times R_{DLY}}\right) \times \frac{t_{SS}}{V_{VID}} \quad (2)$$

Where t_{SS} is the desired soft-start time. Assuming an R_{DLY} of 390 kΩ and a desired a soft-start time of 2.2 ms, C_{DLY} is 56 nF.

Once C_{DLY} has been chosen, R_{DLY} can be recalculated for the current limit latch off time using:

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}} \quad (3)$$

If the result for R_{DLY} is less than 200 kΩ, then a smaller soft-start time or longer latch-off time should be considered when C_{DLY} is recalculated. In no case should R_{DLY} be less than 200 kΩ. In this example, a delay time of 10 ms gives R_{DLY} = 371 kΩ. The closest standard 5% value is 390 kΩ.

The PWRGD delay, defined as the time period between the V_{CORE} voltage reaching VID voltage and the assertion of PWRGD signal, is also controlled by the DELAY pin. The ADP3206 does not assert the PWRGD signal until DELAY pin voltage reaches about 2.2 V. Given the previously calculated values for R_{DELAY} and C_{DELAY}, the PWRGD delay is in the range of 2.4 ms to 4 ms. This satisfies the specification range of 1 ms to 10 ms.

INDUCTOR SELECTION

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and also the conduction losses in the MOSFETs. However, this allows the use of smaller-size inductors, and for a specified peak-to-peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. In multiphase converter, the practical value for peak-to-peak inductor ripple current is less than 50% of the maximum DC current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency,

and peak-to-peak ripple current. Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage:

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \quad (4)$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - (n \times D_{MIN})) \times (1 - D_{MIN})}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for a 10 mV peak-to-peak output ripple voltage yields

$$L \geq \frac{1.350\ \text{V} \times 1.3\ \text{m}\Omega \times (1 - (4 \times 0.07)) \times (1 - 0.07)}{280\ \text{kHz} \times 10\ \text{mV}} = 417\ \text{nH}$$

If the ripple voltage ends up being less than the initially selected value was, then the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 560 nH inductor is a good choice for a starting point, and it gives a calculated ripple current of 8.0 A. The inductor should not saturate at the peak current of 24 A, and should be able to handle the sum of the power dissipation caused by the average current of 20 A in the winding and also the AC core loss.

Another important factor in regarding the inductor design is the DCR, which is used for measuring the phase currents. A large DCR causes excessive power losses, while too small of a value leads to increased measurement error. A good rule of thumb is to have the DCR to be about 1 to 1½ times of the droop resistance (R_O). For our example, we are using an inductor with a DCR of 1.7 mΩ.

SELECTING A STANDARD INDUCTOR

Once the inductance and DCR are known, the next step is to select a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to keep the accuracy of the system controlled. Using 20% tolerance for the inductance and 8% for the DCR (at room temperature) are reasonable assumptions that most manufacturers can meet.

POWER INDUCTOR MANUFACTURERS

The following companies provide surface mount power inductors optimized for high power applications upon request.

- Vishay Dale Electronics, Inc.
  (605) 665-9301
  http://www.vishay.com
- Panasonic
  (714) 373-7334
  http://www.panasonic.com
- Sumida Electric Company
  (847) 545-6700
  http://www.sumida.com
- NEC Tokin Corporation
  (510) 324-4110
  http://www.nec-tokin.com/

OUTPUT DROOP RESISTANCE

The design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a DC output resistance (R_O).

The output current is measured by summing the currents of the resistors monitoring the voltage across each inductor and by passing the signal through a low-pass filter. This summer-filter is implemented by the CS amplifier that is configured with resistors $R_{PH(X)}$ (summers), and R_{CS} and C_{CS} (filter). The output resistance of the regulator is set by the following equations, where R_L is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \times R_L \quad (6)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (7)$$

One has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. Due to the current drive ability of CSCOMP pin, the R_{CS} resistance should be larger than 100 kΩ. For example, select R_{CS} to be equal to 100 kΩ, then solve for $R_{PH(X)}$ by rearranging Equation 6.

$$R_{PH(X)} = \frac{1.7\ \text{m}\Omega}{1.3\ \text{m}\Omega} \times 150\ \text{k}\Omega = 196\ \text{k}\Omega$$

Next, use Equation 7 to solve for C_{CS}:

$$C_{CS} = \frac{560\ \text{nH}}{1.7\ \text{m}\Omega \times 150\ \text{k}\Omega} = 2.2\ \text{nF}$$

For this example, C_{CS} calculates to 3.3 nF, which is a standard capacitance. In case that the calculated C_{CS} is not a standard value, adjust R_{CS} until standard C_{CS} capacitor value is achieved. For best accuracy, C_{CS} should be a 5% NPO capacitor. The standard 1% value for $R_{PH(X)}$ is 130 kΩ.

INDUCTOR DCR TEMPERATURE CORRECTION

With the inductor's DCR being used as sense element, and copper wire being the source of the DCR, one needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite sign but equal percentage change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors, R_{CS1} and R_{CS2} (see Figure 11) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

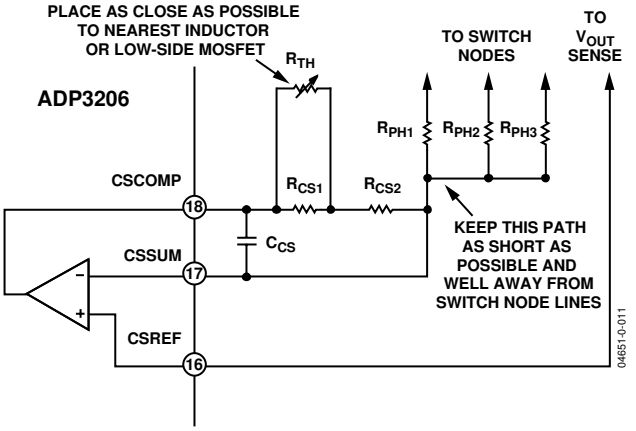


Figure 11. Temperature Compensation Circuit Values

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on type and value. Because we do not have a value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.

2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures to use that work well are 50°C and 90°C. We call these resistance values A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the NTC's relative value is always 1 at 25°C.

3. Next, find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which we initially make 0.39%/°C. We call these r_1 (r_1 is $1/(1+ TC \times (T_1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T_2 - 25))$), where TC=0.0039, T1 = 50°C and T2 = 90°C.

4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using:

$$r_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)}$$

$$r_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}} \quad (8)$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (9)$$

6. Finally, calculate values for R_{CS1} and R_{CS2} using:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$

$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2})) \quad (10)$$

For this example, we start with a thermistor value of 100 kΩ. Looking through available 0603 size thermistors, we can find a Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these data we compute r_{CS1} = 0.3796, r_{CS2} = 0.7195 and r_{TH} = 1.0751. Solving for R_{TH} yields 107.5 kΩ, so we choose 100 kΩ, making k = 0.9302. Finally, we find R_{CS1} and R_{CS2} to be 35.3 kΩ and 73.9 kΩ. Choosing the closest 1% resistor values yields a choice of 35.7 kΩ and 73.2 kΩ.

OUTPUT OFFSET

Intel's specification requires that at no load the nominal output voltage of the regulator to be offset to a lower value than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (I_{FB}) and flowing through R_B. The value of R_B can be found using the following equation. The closest standard 1% resistor value is 1.58 kΩ.

$$R_B = \frac{V_{OFFSET}}{I_{FB}} \quad (11) \qquad R_B = \frac{0.025\ \text{V}}{15\ \mu\text{A}} = 1.67\ \text{k}\Omega$$

C_{OUT} SELECTION

The required output decoupling for processors and platforms is typically recommended by Intel. The following guidelines can also be used if there are both bulk and ceramic capacitors in the system.

The first thing is to select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramics is inside the socket; 12 to 18 pieces of size 1206 being the physical limit. Others can be placed along the outer edge of the socket as well.

Combined ceramic values of 200 to 300 µF are recommended, and are usually made up of multiple 10 µF or 22 µF capacitors. Select the number of ceramics and find the total ceramic capacitance (C_Z).

Next, there is an upper limit imposed on the total amount of bulk capacitance (C_X) when one considers the VID on-the-fly output voltage stepping (voltage step V_V in time t_V with error of V_{ERR}), and also a lower limit based on meeting the critical capacitance for load release at a given maximum load step ΔI_O. The IMVP-5 specification allows a maximum Vcore overshoot (V_{OSMAX}) of 50 mV over VID voltage for a step-off load current.

$$C_{X(MIN)} \geq \frac{L \times \Delta I_O}{n \times V_{VID} \times \left(R_O + \frac{V_{OSMAX} + V_{OFFSET}}{\Delta I_O} \right)} - C_Z \quad (12)$$

$$C_{X(MAX)} \leq \frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_V \frac{V_{VID}}{V_V} \times \frac{nkR_O}{L} \right)^2} - 1 \right) - C_Z$$

$$\text{where } K = 1n\left(\frac{V_{VERR}}{V_V} \right)$$

To meet the conditions of these expressions and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system does not meet the VID on-the-fly and/or Deepersleep exit specification and may require a smaller inductor or more phases (the switching frequency may also have to be increased to keep the output ripple the same).

For our example, we use thirty pieces of 10 µF 0805 MLC capacitors (C_Z = 300 µF). The largest VID voltage change is the exit of Deepersleep, V_{CORE} change is 525 mV in 100 µs with a setting error of 20 mV. Where K = 3.3, solving for the bulk capacitance yields:

$$C_{X(MIN)} \geq \frac{560\ \text{nH} \times 56\ \text{A}}{4 \times 1.350 \times \left(1.3\ \text{m}\Omega + \frac{50\ \text{mV} + 25\ \text{mV}}{56\ \text{A}} \right)} - 300\ \mu\text{F} = 1.9\ \text{mF}$$

Using six 330 µF Panasonic SP capacitors with a typical ESR of 7 mΩ each yields C_X = 1.98 mF with an R_X = 1.2 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the initial high-frequency transient spike. This is tested using:

$$L_X \leq C_Z \times R_O^2$$
$$L_X \leq 300\ \mu\text{F} \times (1.3\ \text{m}\Omega)^2 = 507\ \text{pH} \quad (14)$$

In this example, L_X is about 150 pH for the six SP cap capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of capacitors must be increased. One should note, for this multimode control technique, an all-ceramic capacitor design can be used as long as the conditions of Equations 12, 13 and 14 are satisfied.

POWER MOSFETS

For normal 20 A per phase application, the N-channel power MOSFETs are selected for two high-side switches and two or three low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS} and $R_{DS(ON)}$. Because the gate drive voltage (the supply voltage to the ADP3419) is 5 V, logic-level threshold MOSFETs must be used.

The maximum output current I_O determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. In the ADP3206, currents are balanced between phases; the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O):

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n\, I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (15)$$

Knowing the maximum output current and the maximum allowed power dissipation, one can find the required $R_{DS(ON)}$ for the MOSFET. For SO-8 or SO-8 compatible packaged MOSFETs, the junction to ambient (PCB) thermal impedance is 50°C/W. In worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, a safe limit for P_{SF} is 0.8 W~1.0 W at 120°C junction temperature. Thus, for our example (80 A maximum), we find $R_{DS(SF)}$ (per MOSFET) < 8.5mΩ for two pieces of low-side MOSFET. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C, therefore, the $R_{DS(SF)}$ (per MOSFET) should be lower than 6 mΩ at room temperature, which gives 8.5 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

The high-side (main) MOSFET has to be able to handle two main power dissipation components; conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (16)$$

Here, R_G is the total gate resistance (1.5 Ω for the ADP3419 and about 0.5 Ω for two pieces of typical high speed switching MOSFETs, making R_G = 2 Ω) and C_{ISS} is the input capacitance of the main MOSFET. The best thing to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the ON-resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (17)$$

Typically, for main MOSFETs, one wants the highest speed (low C_{ISS}) device, but these usually have higher ON-resistance. One must select a device that meets the total power dissipation (0.8~1.0 W for a single SO-8 package) when combining the switching and conduction losses.

For our example, we have selected a Vishay SI7860 device as the main MOSFET (eight in total; i.e., n_{MF} = 8), with about C_{ISS} = 1560 pF (max) and $R_{DS(MF)}$ = 15 mΩ (max at Tj = 120°C) and a Vishay SI7889 device as the synchronous MOSFET (eight in total; i.e., n_{SF} = 8), $R_{DS(SF)}$ = 7.9 mΩ (max at Tj = 120°C). Solving for the power dissipation per MOSFET at I_O = 80 A and I_R = 8.0 A yields 700 mW for each synchronous MOSFET and 730 mW for each main MOSFET. A 3rd synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

One last thing to look at is the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad (18)$$

Also shown is the standby dissipation (I_{CC} times the V_{CC}) of the driver. For the ADP3419, the maximum dissipation should be less than 300 mW, considering its thermal impedance 220°C/W and the maximum temperature increase is 50°C. For our example, with I_{CC} = 2 mA, Q_{GMF} = 22.8 nC and Q_{GSF} = 84 nC, we find 160 mW dissipation in each driver, which is below the 300 mW dissipation limit. See the ADP3419 data sheet for details.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use this expression to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (19)$$

$$R_R = \frac{0.2 \times 600 \text{ nH}}{3 \times 5 \times 4.2 \text{ m}\Omega \times 5 \text{ pF}} = 381\text{k}\Omega$$

where A_R is the internal ramp amplifier gain, A_D is the current balancing amplifier gain, R_{DS} is the total low-side MOSFET ON-resistance, and C_R is the internal ramp capacitor value. Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 20). For stability and noise immunity, keep this ramp size larger than 0.5 V. Taking this into consideration, the value of R_R is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated using:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (20)$$

$$V_R = \frac{0.2 \times (1 - 0.125) \times 1.5\text{V}}{383 \text{ k}\Omega \times 5 \text{ pF} \times 267 \text{ kHz}} = 0.51\text{mV}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improves, but thermal balance degrades. Likewise, if the ramp is made smaller, thermal balance improves at the sacrifice of transient response and stability. The factor of three in the denominator of equation 19 sets a minimum ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP PIN RAMP

There is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input.

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O} \right)} \quad (21)$$

For this example, the overall ramp signal is found to be 1.1V.

CURRENT LIMIT SETPOINT

To select the current limit set point, we need to find the resistor value for R_{LIM}. The current limit threshold for the ADP3206 is set with a 1 V source (V_{LIM}) across R_{LIM} with a gain of 6 mV/µA per phase. R_{LIM} can be found using the following:

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM} \times n}{I_{LIM} \times R_O} \quad (22)$$

For values of R_{LIM} greater than 500 kΩ, the current limit may be lower than expected, so some adjustment of R_{LIM} may be needed. Here, I_{LIM} is the average current limit for the output of the supply. For our example, choosing 120 A for I_{LIM}, we find R_{LIM} to be 154 kΩ, which is a standard 1% resistance.

The per phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} - \frac{I_R}{2} \quad (23)$$

For the ADP3206, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage (V_{BIAS}) is 1.2 V, and the current balancing amplifier gain (A_D) is 5. Using V_R of 1.1 V, and $R_{DS(MAX)}$ of 4.2 mΩ (low-side ON-resistance at 150°C), we find a per-phase limit of 66 A.

This limit can be adjusted by changing the ramp voltage V_R. But make sure not to set the per-phase limit lower than the average per-phase current (I_{LIM}/n).

The per phase initial duty cycle limit at maximum input voltage is:

$$D_{LIM} = D_{MIN} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \quad (24)$$

For this example, the duty cycle limit at maximum input voltage is found to be 0.23 when D is 0.07.

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3206 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate; this ensures the optimal positioning and allows the minimization of the output decoupling.

With the multimode feedback structure of the ADP3206, one needs to set the feedback compensation to make the converter's output impedance work in parallel with the output decoupling. There are several poles and zeros created by the output inductor and decoupling capacitors (output filter) that need to be compensated for.

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. The expressions given below are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects.(See Tuning Guide)

The first step is to compute the time constants for all of the poles and zeros in the system:

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \quad (25)$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad (26)$$

$$T_B = (R_X + R' - R_O) \times C_X \quad (27)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}} \right)}{V_{VID} \times R_E} \quad (28)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad (29)$$

where, for the ADP3206, R' is the PCB resistance from the bulk capacitors to the ceramics and where R_{DS} is the total low-side MOSFET ON-resistance per phase. For this example, A_D is 5, V_{RT} equals 1.1V, R' is approximately 0.4 mΩ (assuming an 8-layer motherboard) and L_X is 150 pH for the six Panasonic SP capacitors.

The compensation values can be solved using the following:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad (30)$$

$$R_A = \frac{T_C}{C_A} \quad (31)$$

$$C_B = \frac{T_B}{R_B} \quad (32)$$

$$C_{FB} = \frac{T_D}{R_A} \quad (33)$$

The standard values for these components are subject to the tuning procedure, as introduced in the next section.

C_{IN} SELECTION AND INPUT CURRENT DI/DT REDUCTION

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × V_{OUT}/V_{IN} and an amplitude of one-nth of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current happens at the lowest input voltage, and is given by

$$I_{CRMS} = D_{MAX} \times I_O \times \sqrt{\frac{1}{N \times D_{MAX}} - 1}$$
$$I_{CRMS} = 01.66 \times 80\ \text{A} \times \sqrt{\frac{1}{4 \times 0.166} - 1} = 9.4\ \text{A} \quad (34)$$

In a typical notebook system, the battery rail decouplings are MLCC capacitors or a mixture of MLCC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by 12 pieces of 10 µF, 25 V MLCC capacitors with a ripple current rating of about 1A each.

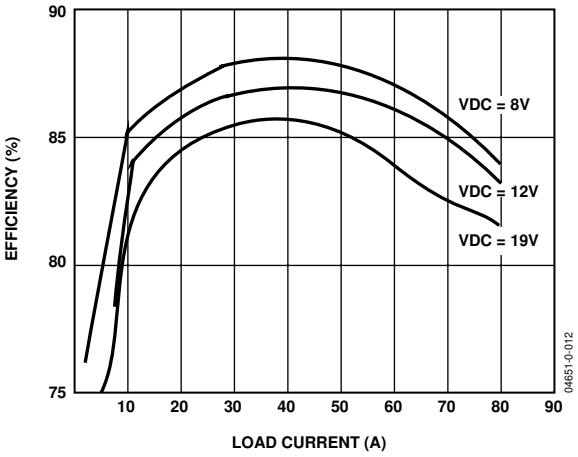


Figure 12. Efficiency of Power Conversion vs. Output Current and Input Voltage

DEEPERSLEEP VOLTAGE AND TRANSIENT SETTING

The Deepersleep voltage is set on the DPRSET pin via a resistor divider from V_{REF} voltage, which is 3.0 V. The voltage set on the DPRSET pin is used as the reference voltage for the error amplifier when DPRSLP is asserted. Considering there is a zero load offset voltage, the voltage on the DPRSET pin should be

$$V_{DPRSET} = V_{OFFSET} + V_{DPRSLP} \quad (35)$$

With V_{DPRSLP} = 0.8 V and V_{OFFSET} = 25 mV, V_{DPRSET} = 0.825 V.

The suggested current for the DPRSET pin resistor divider is I_{DPRSET}=50 µA. Therefore, the divider resistors are:

$$R_{DPRSET1} = \frac{V_{REF} - V_{DPRSET}}{I_{DPRSLP}} = 43.5\ \text{k}\Omega \quad (36)$$

$$R_{DPRSET2} = \frac{V_{DPRSET}}{I_{DPRSLP}} = 16.5\ \text{k}\Omega \quad (37)$$

The closest 1% resistors are 43.2 kΩ and 16.5 kΩ.

During the transient of entering and exiting Deepersleep, the slew-rate of V_{CORE} reference voltage change is controlled by the STSET pin capacitance, which can be calculated as below.

$$C_{STSET} = \frac{0.8 \times T_{DPRSLP} \times I_{STSET}}{V_{VIDHFM} - V_{OFFSET} - V_{DPRSLP}} \quad (38)$$

T_{DPRSLP} is the longest duration of Deepersleep exit, specified as 100 µs in IMVP-5. I_{STSET} is the charge and discharge current of the STSET pin, and has a value of ±15 µA. V_{VIDHFM} is the highest possible VID voltage the system returns when it exits from Deepersleep. It is specified as 1.350 V in IMVP-5. Therefore, C_{STSET} is calculated as 2.4 nF, with the closest standard capacitance 2.2 nF.

Figure 4 shows the transition from active mode to Deepersleep mode. As soon as DPRSLP is asserted, the V_{CORE} voltage is gradually discharged to Deepersleep voltage (0.8 V). Once the transition is completed, the PWM outputs of phase 2, 3, and 4 are disabled, switching the converter to single-phase operation.

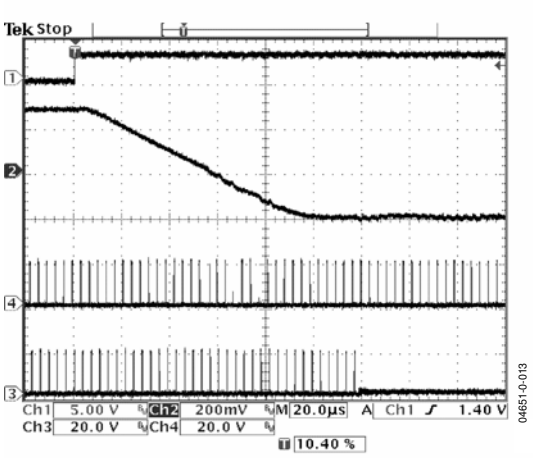


Figure 13. Transient to Deepersleep Mode
Channel 1–DPRSLP, Channel 2–VCORE (with 1 V Offset),
Channel 3–Switch Node of Phase 2, Channel 4–SW node of Phase 1.

Figure 5 shows the power conversion efficiency improvement of single-phase operation during Deepersleep.

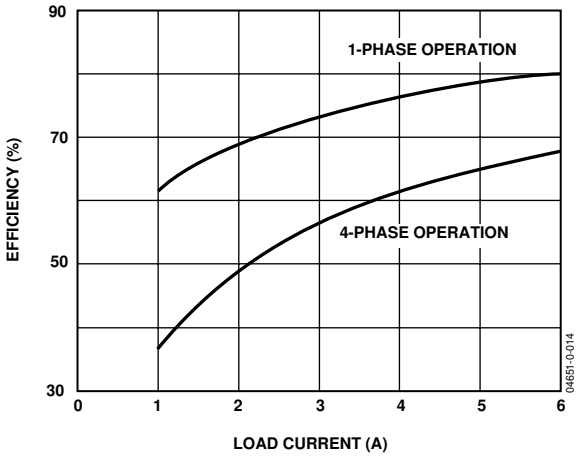


Figure 14. Efficiency Improvement in Deepersleep Mode

DEEPSLEEP OFFSET VOLTAGE SETTING

The Deepsleep offset voltage is programmed by a resistor on the DPSET pin. The voltage on the DPSET pin is equal to the VID voltage. When $\overline{\text{DPSLP}}$ is asserted, the current programmed on the DPSET pin is sourced on the FB pin, resulting in an additional negative offset voltage. The DPSET pin resistor should be:

$$R_{DPSET} = \frac{V_{OFFSET}}{V_{OS\%} I_{FB}} \quad (39)$$

where $V_{OS\%}$ is the Deepsleep offset percentage, specified as 1.7% in IMVP-5. The V_{OFFSET} over I_{FB} term is actually the R_B resistance (see Output Offset section). Thus, R_{DPSET} is calculated as 98 kΩ, with the closest standard resistance 97.6 kΩ.

PWRGD MASK TIMER SETTING

The PWRGD (Power Good) mask is programmed by the capacitance on the PGMASK pin. During the period of PWRGD masking, there is a source current (I_{PGMASK} = 5 μA) out of the PGMASK pin, to charge a capacitor, C_{PGMASK}. PWRGD masking is terminated when the voltage on the PGMASK pin reaches V_{PGMASK} = 3.0 V.

Thus, the capacitance on the PGMASK pin can be calculated as:

$$C_{PGMASK} = \frac{T_{PGMASK} \times I_{PGMASK}}{V_{PGMASK}} \quad (40)$$

In IMVP-5, the PWRGD mask time is defined as

T_{PGMASK} = 100 μs

resulting in C_{PGMASK} = 167 pF. Because the specified T_{PGMASK} is the maximum length of masking time, please select the next lower standard capacitance: 150 pF.

SELECTING THERMAL MONITOR COMPONENTS

For single-point hot spot thermal monitoring, simply set R_{TTSET1} equal to the NTC thermistor's resistance at the alarm temperature. For example, if VRTT alarm temperature is 100°C and we use a Vishay thermistor (NTHS-0603N011003J), whose resistance is 100 kΩ at 25°C, and 6.8 kΩ at 100°C, then we simply can set $R_{TTSET1} = R_{TH1}$(100°C) to 6.8 kΩ.

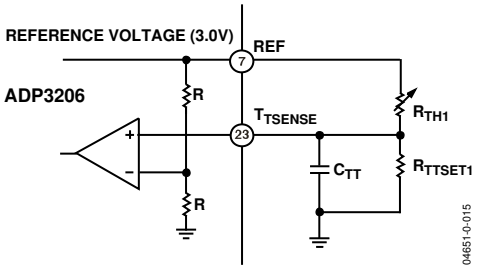


Figure 15. Single-Point Thermal Monitoring

Multiple-point hot spots thermal monitoring can be implemented as shown in Figure 16. If any of the monitored hot spots reaches alarm temperature, VRTT signal is asserted. The following calculation sets the alarm temperature:

$$R_{TTSET1} = \frac{\frac{1}{2} + \frac{V_{FD}}{V_{REF}}}{\frac{1}{2} - \frac{V_{FD}}{V_{REF}}} R_{TH1\ Alarm\ Temperature} \quad (41)$$

where V_{FD} is the forward drop voltage of the parallel diode.

Because the forward current is very small, the forward drop voltage is very low, i.e., 100 mV. Assuming the same 100°C alarm temperature used in the single-spot thermal monitoring example, and the same Vishay thermistor, then the above formula leads to R_{TTSET} = 7.8 kΩ, whose closest standard resistor is 7.87 kΩ (1%).

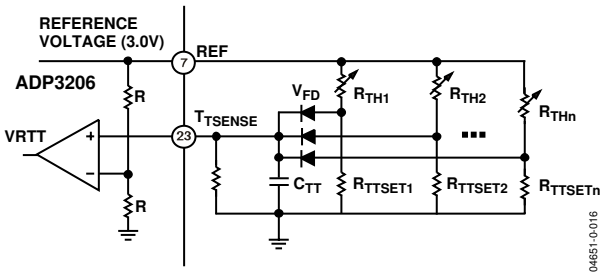


Figure 16. Multiple-Point Thermal Monitoring

The number of hot spots monitored is not limited as long as the current limit of REF pin (4 mA) is not exceeded. The alarm temperature of each hot spot can be set differently by playing different RTTSET1, RTTSET2, …$RTTSET_n$.

According to IMVP-5, the shortest duration of assertion and de-assertion of VRTT single is 1 ms (T_{VRTT} = 1 ms). This VRTT duration is programmed by the RC timer (R_{TTMASK}, C_{TTMASK}) on the TTMASK pin. If the RC timer is charged by the VCC voltage (5.0 V), then the RC timer can be set according to the following formula:

$$R_{TTMASK} \times C_{TTMASK} = 2.8 \times T_{VRTT} \quad (42)$$

Select a standard capacitance C_{TTMASK} = 47 nF, and then the above formula leads to R_{TTMASK} = 59.6 kΩ, whose next larger standard resistor is 62 kΩ (5%).

TUNING PROCEDURE FOR ADP3206

1. Build circuit based on compensation values computed from design spreadsheet.
2. Hook-up dc load to circuit, turn on and verify operation. Check for jitter at no-load and full-load.

DC Loadline Setting

3. Measure output voltage at no-load (V_{NL}). Verify it is within tolerance.
4. Measure output voltage at full-load and at cold (V_{FLCOLD}). Let board set for ~10 minutes at full-load and measure output (V_{FLHOT}). If there is a change of more than a few millivolts, adjust R_{CS1} and R_{CS2} using Equations 43 and 44.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{(V_{NL} - V_{FLCOLD})}{(V_{NL} - V_{FLHOT})} \quad (43)$$

5. Repeat Step 4 until cold and hot voltage measurements remain the same.
6. Measure output voltage from no-load to full-load using 5 A steps. Compute the load line slope for each change and then average to get overall load line slope (R_{OMEAS}).
7. If R_{OMEAS} is off from R_O by more than 0.05 mΩ, use the following to adjust the R_{PH} values;

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (45)$$

8. Repeat steps 6-7 to check load line and repeat adjustments if necessary.
9. Once complete with dc load line adjustment, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for rest of procedure.
10. Measure output ripple at no-load and full-load with scope and make sure it is within spec.

AC Loadline Setting

11. Remove dc load from circuit and hook up dynamic load.
12. Hook up scope to output voltage and set to dc coupling with time scale at 100 µs/div.
13. Set dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
14. Measure output waveform (may have to use dc offset on scope to see waveform). Try to use vertical scale of 100 mV/div or finer.
15. You see a waveform that looks something like Figure 17. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP} as shown. ***Do not measure the undershoot or overshoot that happens immediately after the step.***

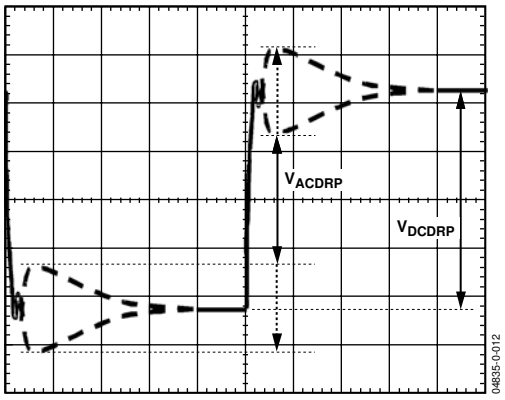


Figure 17. AC Loadline Waveform

16. If the V_{ACDRP} and V_{DCDRP} are different by more than a couple of millivolts, use the following to adjust C_{CS}. You may need to parallel different values to get the right one because there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this).

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (46)$$

17. Repeat steps 15-16 and repeat adjustments if necessary. Once complete, do not change C_{CS} for the rest of the procedure.
18. Set dynamic load step to maximum step size (do not use a step size larger than you need) and verify output waveform is square (which means V_{ACDRP} and V_{DCDRP} are equal).

    Note: Makes sure load step slew rate and turn-on are set for a slew rate of ~150-250 A/µs (for example, a load step of 50 A should take 200-300 ns) with no overshoot. Some dynamic loads have an excessive turn-on overshoot if a minimum current is not set properly (this is an issue if you are using a VTT tool).

Initial Transient Setting

19. With dynamic load still set at maximum step size, expand scope time scale to see 2-5 µs/div. You see a waveform that may have two overshoots and one minor undershoot (see Figure 18). Here, V_{DROOP} is the final desired value.

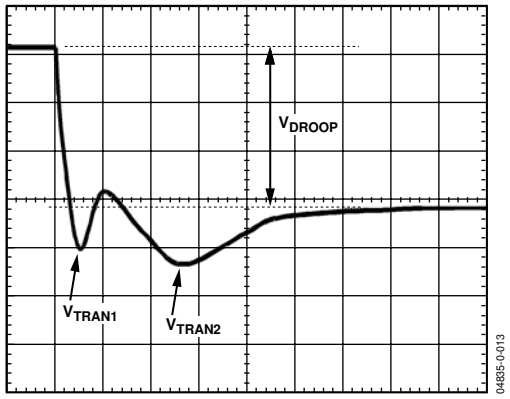


Figure 18. Transient Setting Waveform, Load Step

20. If both overshoots are larger than desired, try making the following adjustments in this order (NOTE—if these adjustments do not change the response, you are limited by the output decoupling). Check the output response each time you make a change as well as the switching nodes (to make sure it is still stable).

    a. Make ramp resistor larger by 25% (R_{RAMP}).

    b. For V_{TRAN1}, increase C_B or increase switching frequency.

    c. For V_{TRAN2}, increase R_A and decrease C_A both by 25%.

21. For load release (see Figure 19), if $V_{TRANREL}$ is larger than the IMVP-5 specification, you do not have enough output capacitance. You either need more capacitance or to make the inductor values smaller (if you change inductors, you need to start the design over using the spreadsheet and this tuning guide).

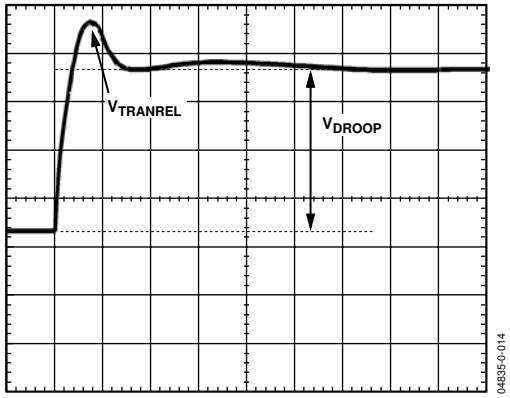
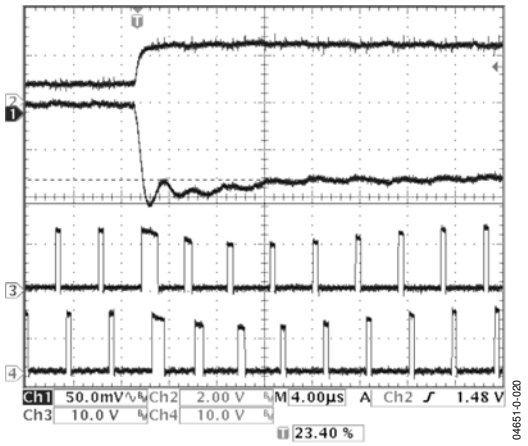
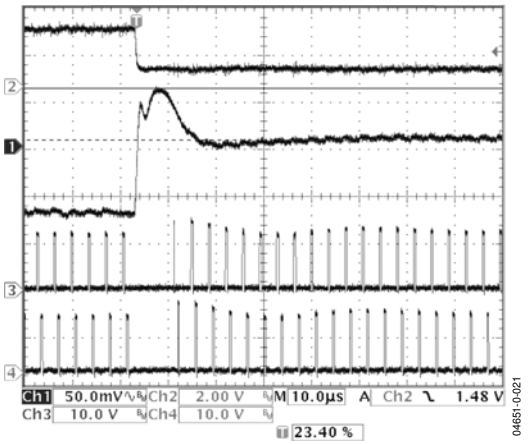


Figure 19. Transient Setting Waveform, Load Release

Figure 20 shows the typical transient response using these compensation values.



(a)



(b)

Figure 20. Typical Transient Response for Design Example (a) Load Step, (b) Load Release

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

GENERAL RECOMMENDATIONS

For good results, at least a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input, and output power, and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3206) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3206 for referencing the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the ADP3206 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. See Figure 2 for details on layout for the CSSUM node.

The output capacitors should be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop, described below.

POWER CIRCUITRY

The switching power path should be routed on the PCB to encompass the shortest possible length in order to minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.

Whenever a power dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias, and improved thermal performance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, the largest possible pad area should be used.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

SIGNAL CIRCUITRY

The output voltage is sensed and regulated between the FB pin and the FBRTN pin (which connects to the signal ground at the load). In order to avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus the FB and FBRTN traces should be routed adjacent to each other atop the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar which is the V_{CORE} common node for the inductors of all the phases.

The ADP3206 has a metal pad in the back side of the package. This metal pad is not a ground node. Do not ground this metal pad. In addition, vias under the ADP3206 are not recommended, because the metal pad may short between vias.

OUTLINE DIMENSIONS

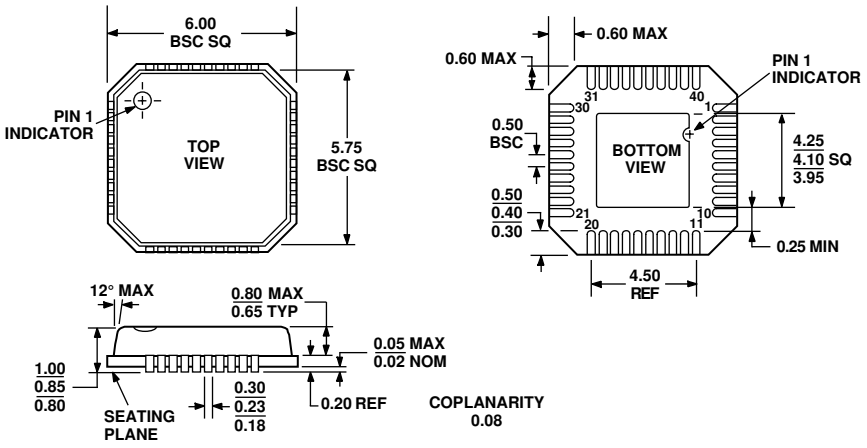


Figure 21. 40-Lead Frame Chip Scale Package [LFCSP]
(CP-40)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Option
ADP3206JCPZ-REEL[1]	0°C to +100°C	Lead Frame Chip Scale Package	CP-40

[1] Z = Pb-free part.

NOTES

NOTES

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