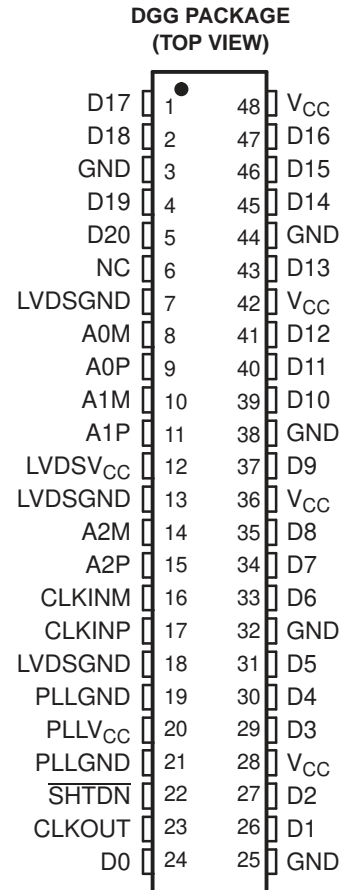


## FlatLink™ RECEIVER

Check for Samples: [SN65LVDS86A-Q1](#)

### FEATURES

- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply**
- **Tolerates 4-kV Human-Body Model (HBM) ESD**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Standard Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the SN75LVDS86 and NSC DS90C364**
- **Improved Jitter Tolerance**
- **Qualified for Automotive Applications**



NC – Not connected

### DESCRIPTION

The SN65LVDS86A FlatLink™ receiver contains three serial-in 7-bit parallel-out shift registers and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage LVTTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit wide LVTTTL parallel bus at the CLKIN rate. The SN65LVDS86A presents valid data on the falling edge of the output clock (CLKOUT).

The SN65LVDS86A requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN65LVDS86A is characterized for operation over the full automotive temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

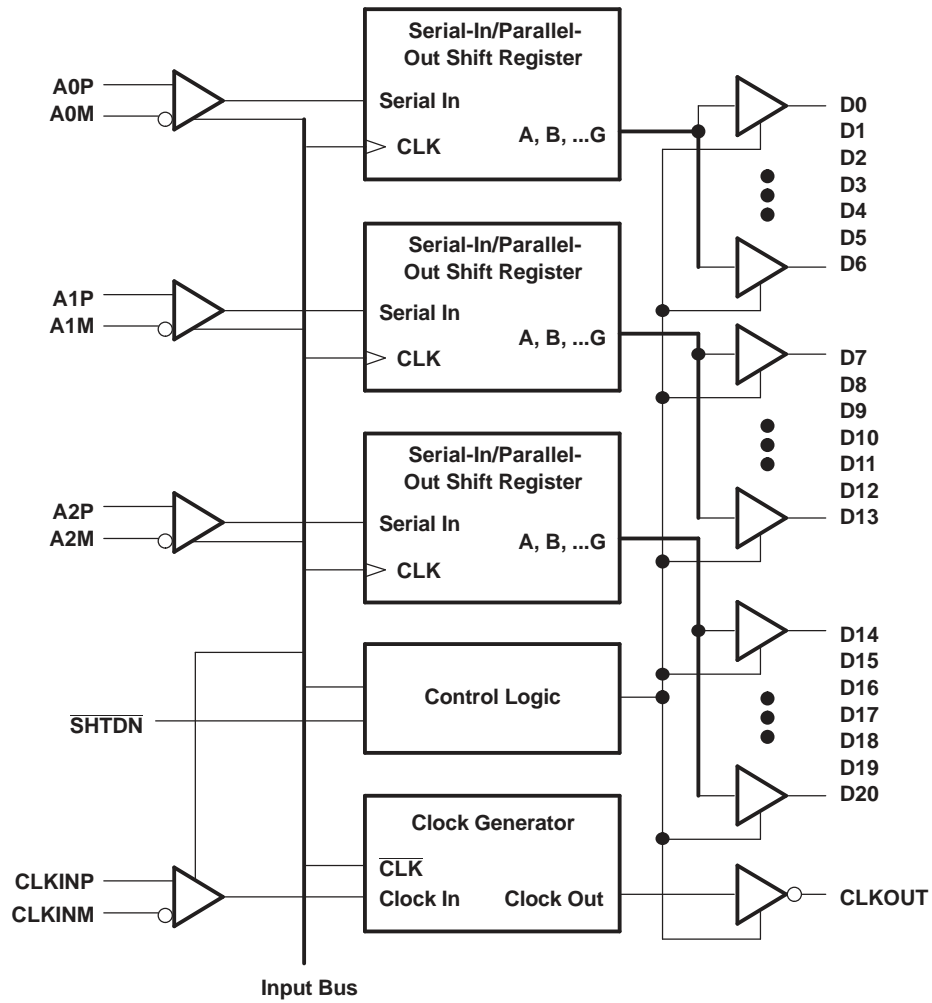
FlatLink is a trademark of Texas Instruments.

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP – DGG	Reel of 2000	SN65LVDS86ADGGRQ1	65LVDS86AQ

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTIONAL BLOCK DIAGRAM**



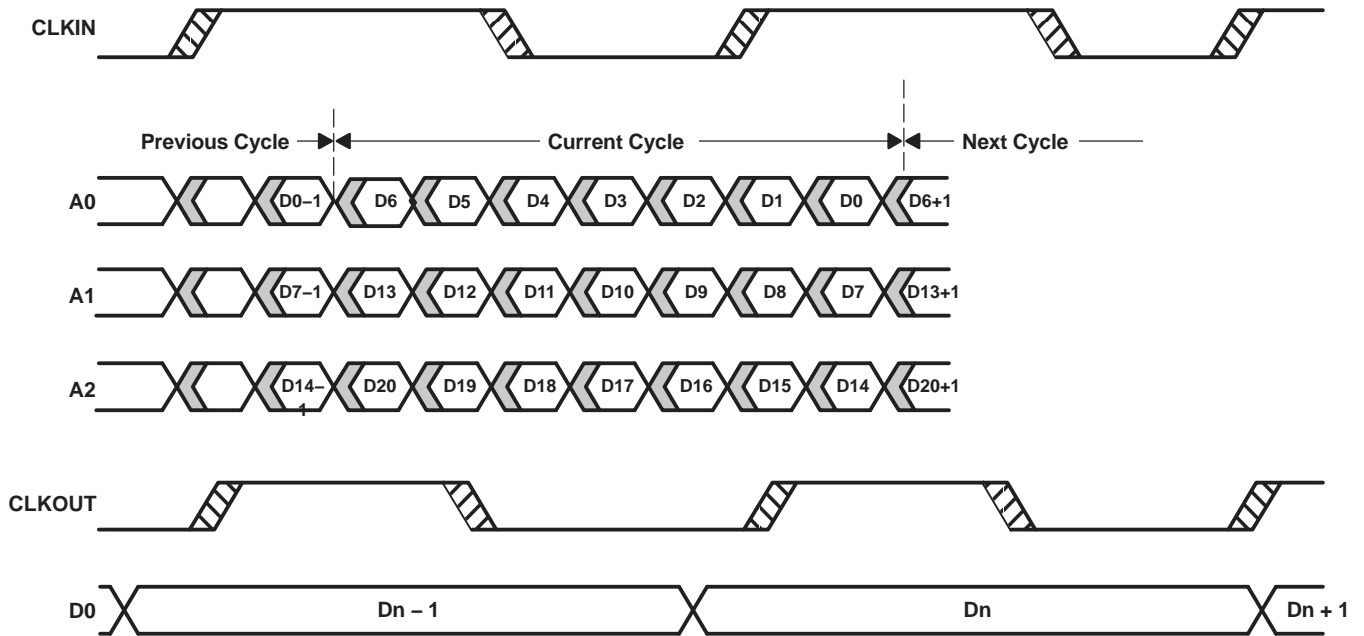
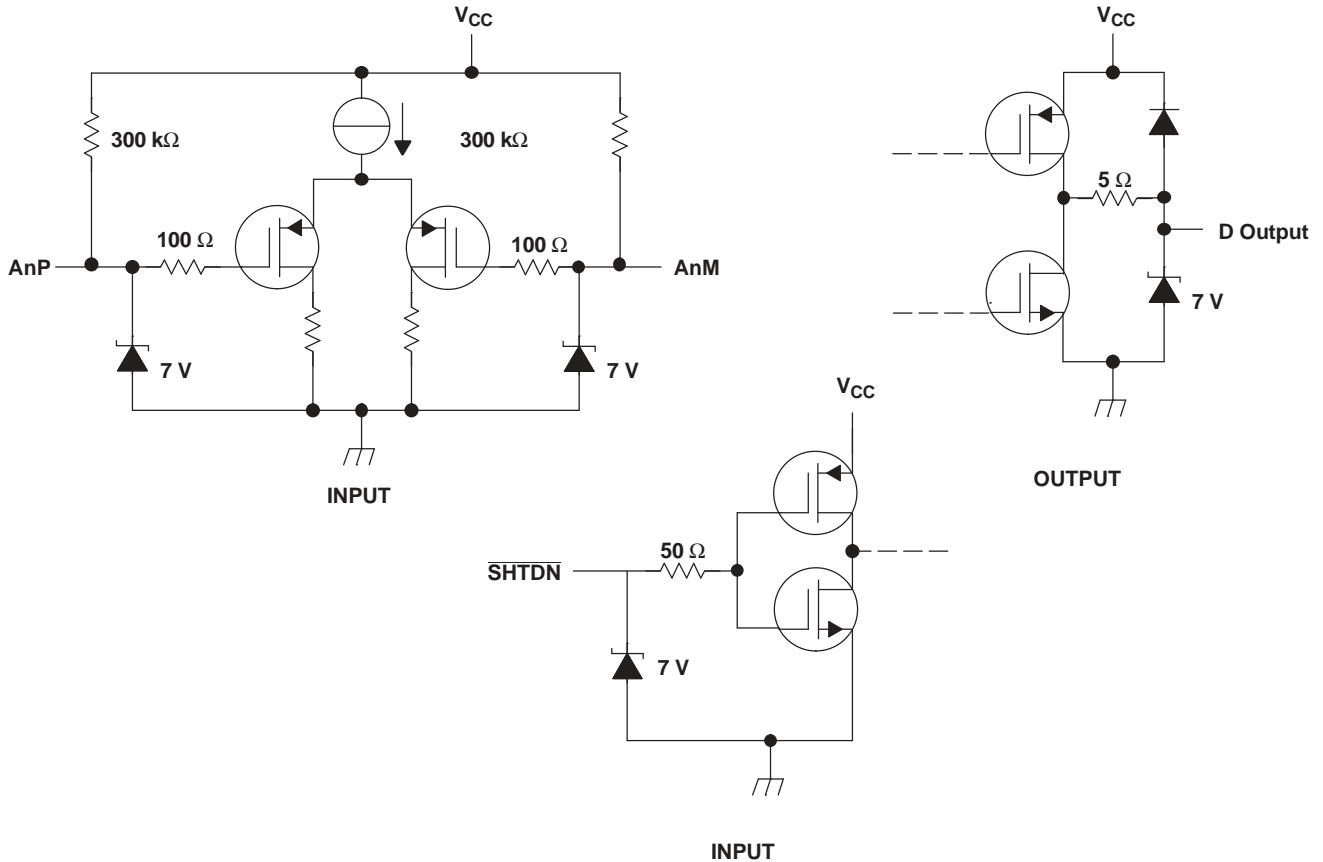


Figure 1. SN65LVDS86A Load and Shift Timing Sequences

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.5	4	V	
	Voltage range at any terminal	-0.5	V <sub>CC</sub> + 0.5	V	
	Electrostatic discharge <sup>(3)</sup>	All pins (Class 3A)		4	kV
		All pins (Class 2B)		200	V
	Continuous total power dissipation	See Dissipation Rating Table			
T <sub>J</sub>	Operating virtual junction temperature range	-40	150	°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals unless otherwise noted.
- (3) This rating is measured using MIL-STD-883C Method, 3015.7.

## Dissipation Rating Table

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
DGG	1637 mW	13.1 mW/°C	1048 mW	327 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

## Recommended Operating Conditions

See Figure 2

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
V <sub>IH</sub>	High-level input voltage (SHTDN)	2			V
V <sub>IL</sub>	Low-level input voltage (SHTDN)			0.8	V
V <sub>ID</sub>	Magnitude differential input voltage	0.1		0.6	V
V <sub>IC</sub>	Common-mode input voltage	$\frac{ V_{ID} }{2}$	2.4	$\frac{ V_{ID} }{2}$	V
T <sub>A</sub>	Operating free-air temperature	-40		125	°C

## Timing Requirements

		MIN	NOM	MAX	UNIT
t <sub>c</sub> <sup>(1)</sup>	Cycle time, input clock	14.7	t <sub>c</sub>	32.4	ns

- (1) Parameter t<sub>c</sub> is defined as the mean duration of a minimum of 32000 clock cycles.

## Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going differential input threshold voltage				100	mV
V <sub>IT-</sub>	Negative-going differential input threshold voltage <sup>(2)</sup>		-100			mV
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA	2.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA			0.4	V
I <sub>CC</sub>	Quiescent current (average)	Disabled, All inputs to GND			280	μA
		Enabled, AnM = 1.4 V, AnP = 1 V, t <sub>c</sub> = 15.38 ns		33	40	mA
		Enabled, Grayscale pattern (see Figure 3), C <sub>L</sub> = 8 pF, t <sub>c</sub> = 15.38 ns		43		
		Enabled, Worst-case pattern (see Figure 4), C <sub>L</sub> = 8 pF, t <sub>c</sub> = 15.38 ns		68		
I <sub>IH</sub>	High-level input current ( $\overline{\text{SHTDN}}$ )	V <sub>IH</sub> = V <sub>CC</sub>			±20	μA
I <sub>IL</sub>	Low-level input current ( $\overline{\text{SHTDN}}$ )	V <sub>IL</sub> = 0			±25	μA
I <sub>I</sub>	Input current A inputs	0 ≤ V <sub>I</sub> ≤ 2.4 V			±20	μA
I <sub>OZ</sub>	High-impedance output current	V <sub>O</sub> = 0 or V <sub>CC</sub>			±10	μA

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

## Switching Characteristics

over recommended operating conditions (unless otherwise noted)

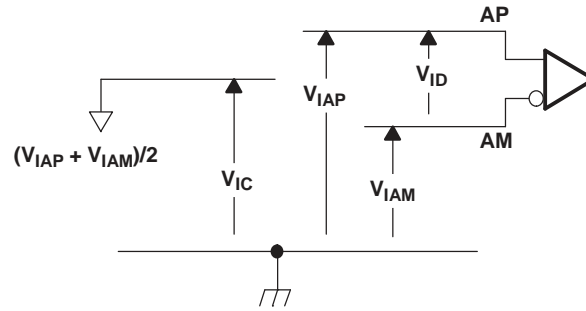
PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>su</sub>	Setup time, D0–D20 to CLKOUT↓	C <sub>L</sub> = 8 pF, See Figure 5	5			ns
t <sub>h</sub>	Data hold time, CLKOUT↓ to D0–D20		5			ns
t <sub>(RSKM)</sub>	Receiver input skew margin <sup>(2)</sup> (see Figure 7)	t <sub>c</sub> = 15.38 ns (±0.2%),  Input clock jitter  < 50 ps, <sup>(3)</sup>	550	700		ps
t <sub>d</sub>	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	V <sub>CC</sub> = 3.3 V, t <sub>c</sub> = 15.38 ns (±0.2%), T <sub>A</sub> = 25°C	3	5	7	ns
t <sub>en</sub>	Enable time, $\overline{\text{SHTDN}}$ to phase lock	See Figure 7		1		ms
t <sub>dis</sub>	Disable time, $\overline{\text{SHTDN}}$ to off state	See Figure 8		400		ns
t <sub>t</sub>	Transition time, output (10% to 90% t <sub>r</sub> or t <sub>f</sub> ) (data only)	C <sub>L</sub> = 8 pF		3		ns
t <sub>t</sub>	Transition time, output (10% to 90% t <sub>r</sub> or t <sub>f</sub> ) (clock only)	C <sub>L</sub> = 8 pF		1.5		ns
t <sub>w</sub>	Pulse duration, output clock			0.50 t <sub>c</sub>		ns

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

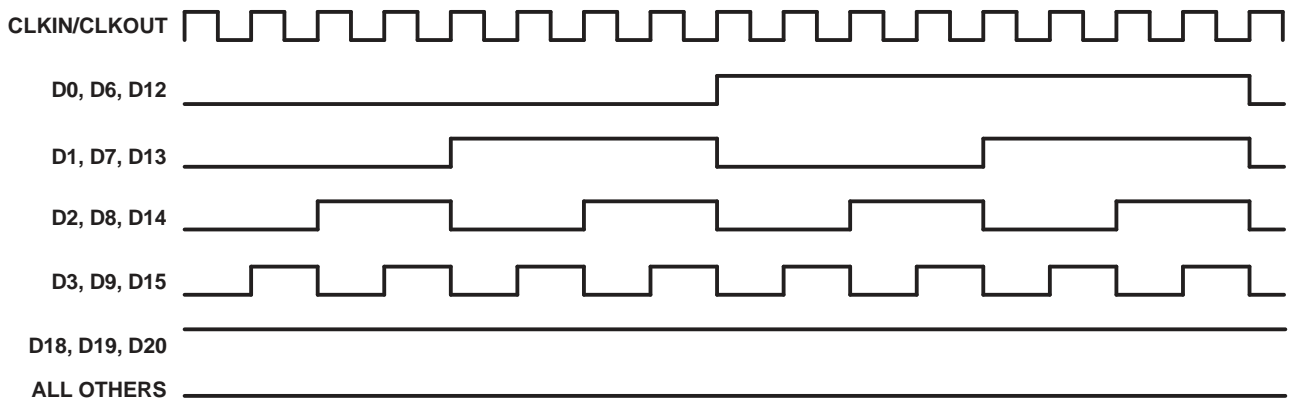
 (2) The parameter t<sub>(RSKM)</sub> is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from t<sub>(RSKM)</sub> = tc/14 – 550 ps.

(3) |Input clock jitter| is the magnitude of the change in input clock period.

**PARAMETER MEASUREMENT INFORMATION**

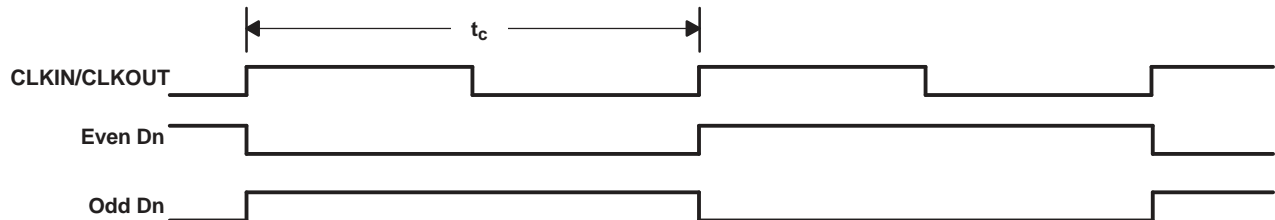


**Figure 2. Voltage Definitions**



A. The 16-grayscale test-pattern test device power consumption for a typical display pattern.

**Figure 3. 16-Grayscale Test-Pattern Waveforms**



A. The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTTL outputs.

**Figure 4. Worst-Case Test-Pattern Waveforms**

PARAMETER MEASUREMENT INFORMATION (continued)

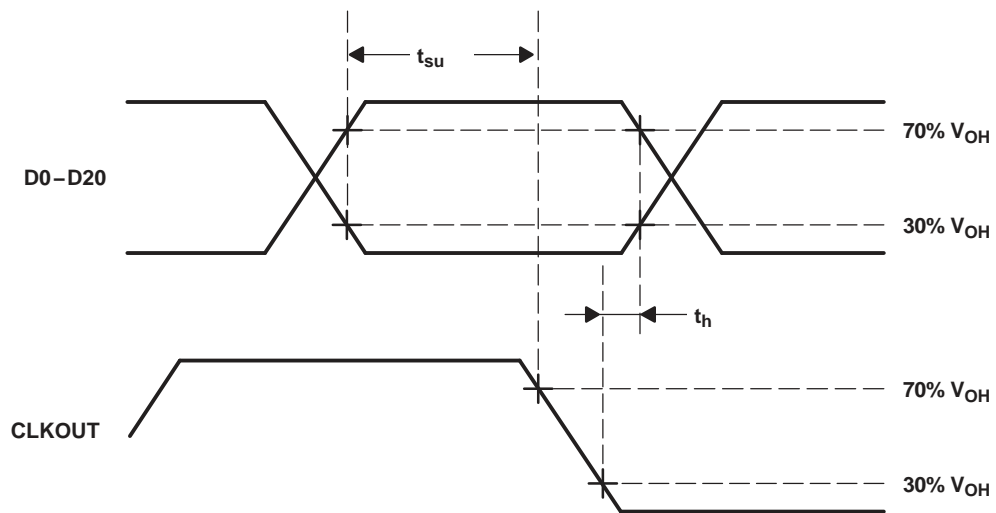
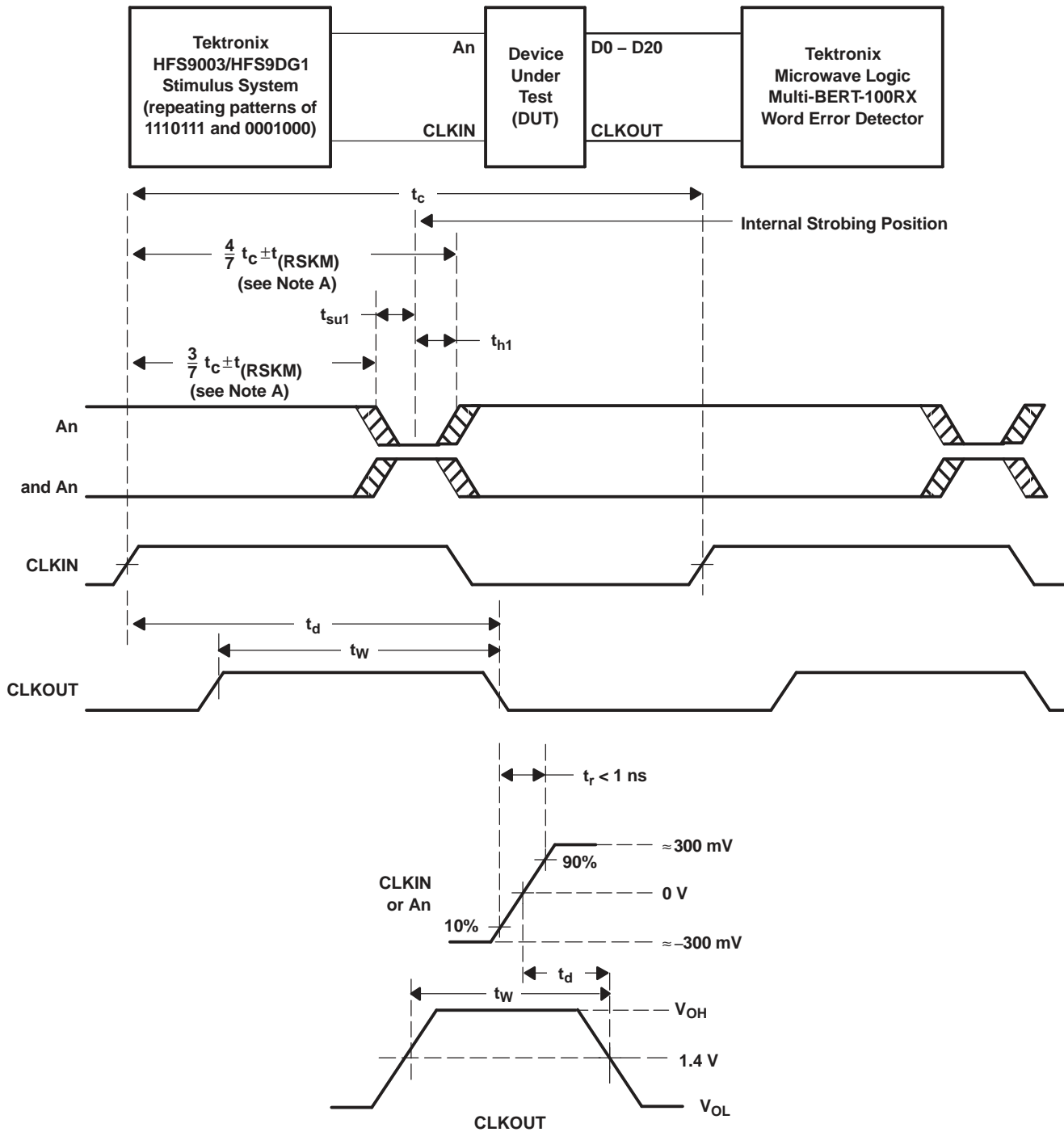


Figure 5. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



- A. CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is  $t_{(RSKM)}$ .

Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions



PARAMETER MEASUREMENT INFORMATION (continued)

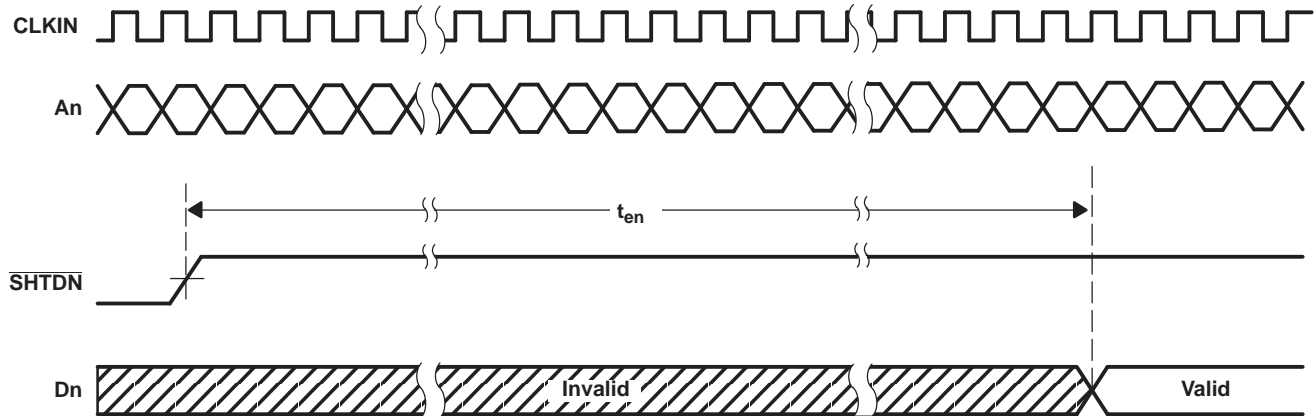


Figure 7. Enable Time Waveforms

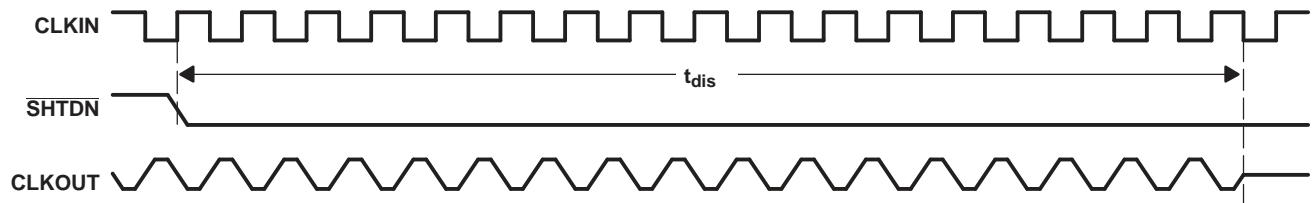


Figure 8. Disable Time Waveforms

TYPICAL CHARACTERISTICS

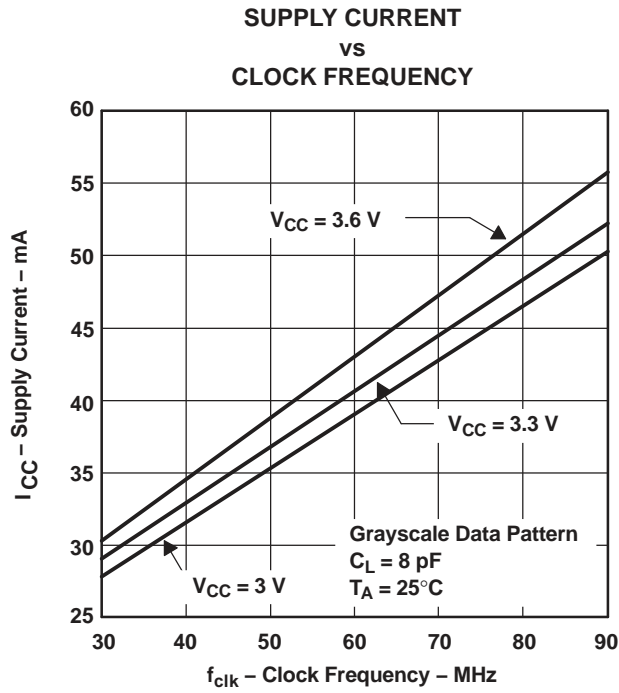
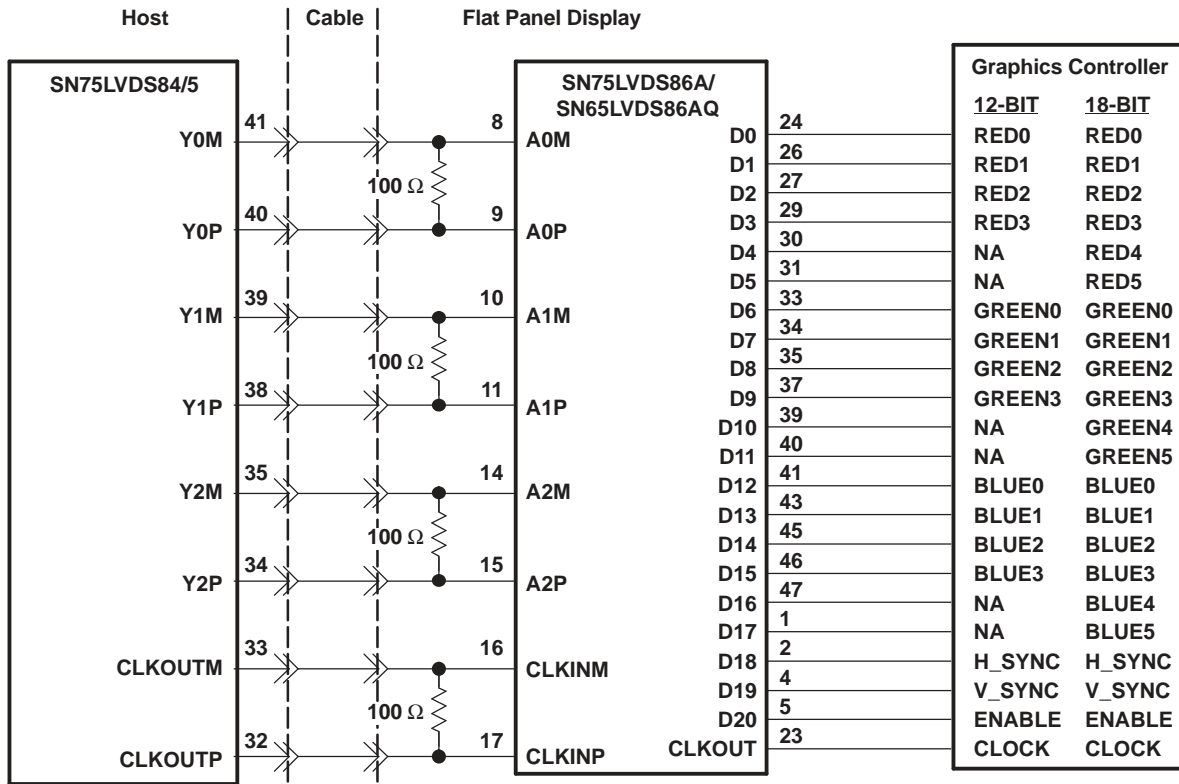


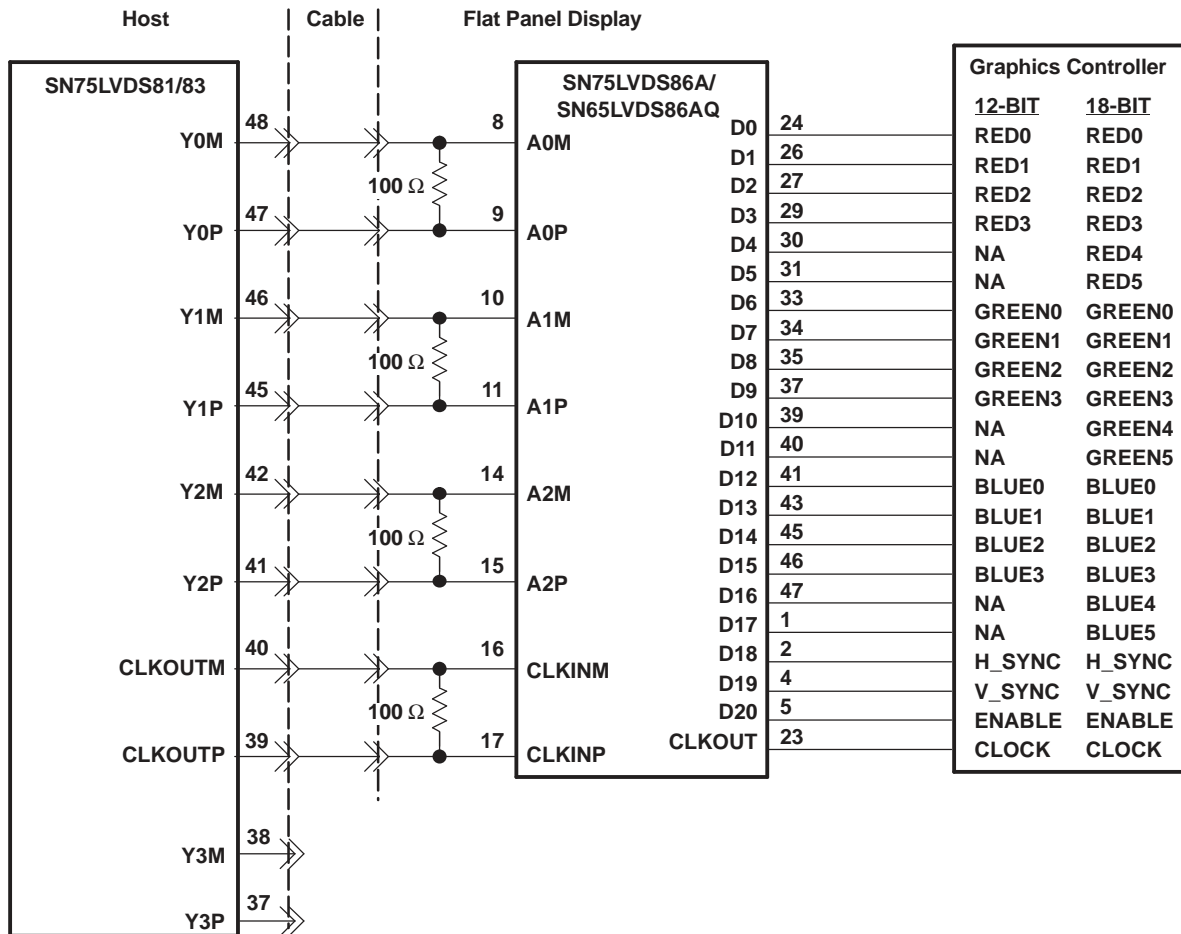
Figure 9. RMS Grayscale I<sub>CC</sub> vs Clock Frequency

APPLICATION INFORMATION



- A. The four 100-Ω terminating resistors are recommended to be 0603 types.
- B. NA – not applicable, these unused inputs should be left open.

Figure 10. 18-Bit Color Host to Flat Panel Display Application



- A. The four 100-Ω terminating resistors are recommended to be 0603 types.
- B. NA – not applicable, these unused inputs should be left open.

**Figure 11. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application**

See the *FLatLink Designer's Guide* (literature number SLLA012) for more application information.

---

**Changes from Original (August 2006) to Revision A****Page**

- 
- Changed Wide Phase-Lock Input Frequency Range lower limit from 10 MHz to 31 MHz ..... 1
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS86AQDGGG4	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	<a href="#">Samples</a>
SN65LVDS86AQDGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	<a href="#">Samples</a>
SN65LVDS86AQDGGRQ1	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN65LVDS86A-Q1 :**

- Catalog: [SN65LVDS86A](#)

NOTE: Qualified Version Definitions:

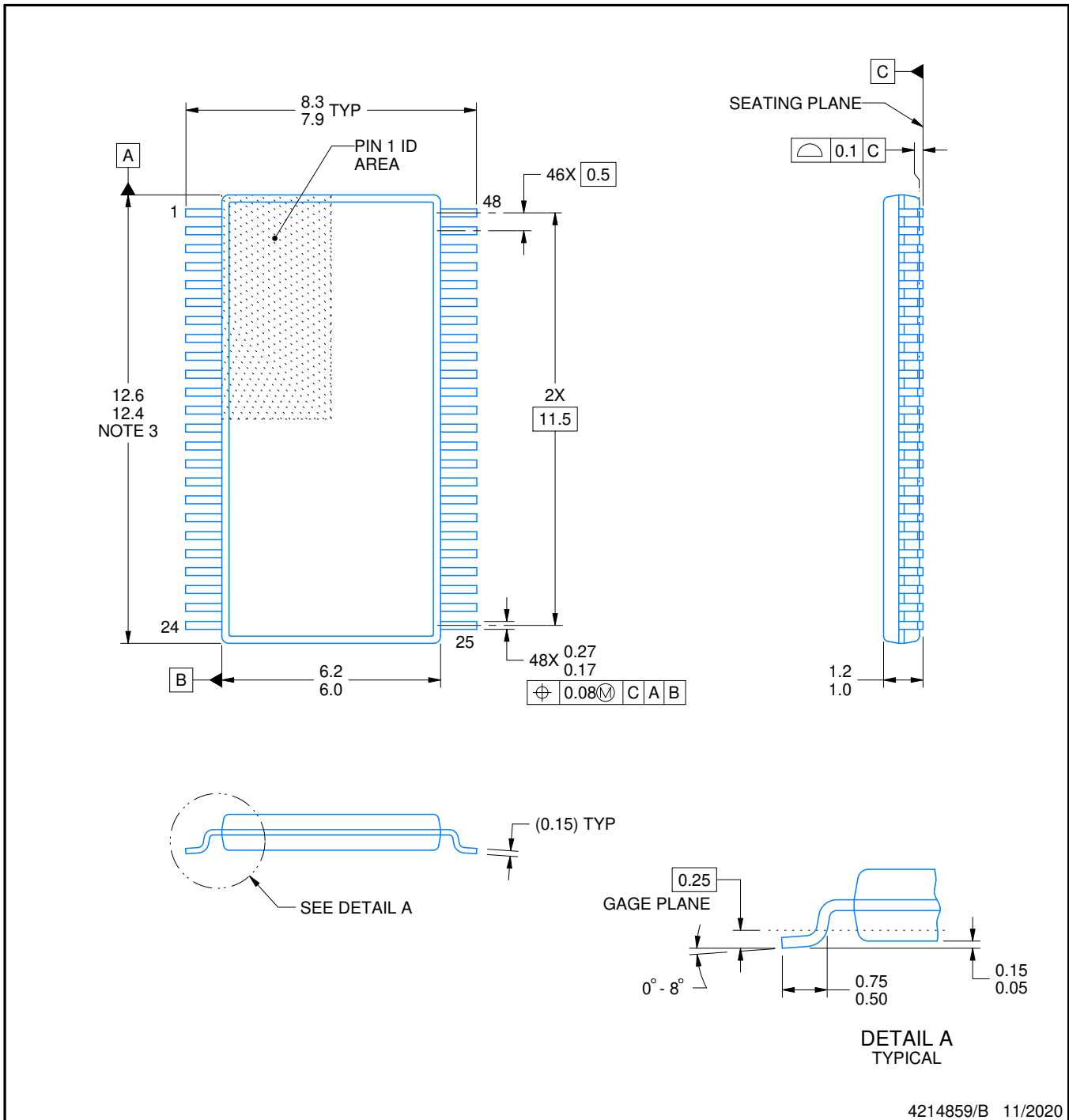
- Catalog - TI's standard catalog product

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVDS86AQDGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9





4214859/B 11/2020

NOTES:

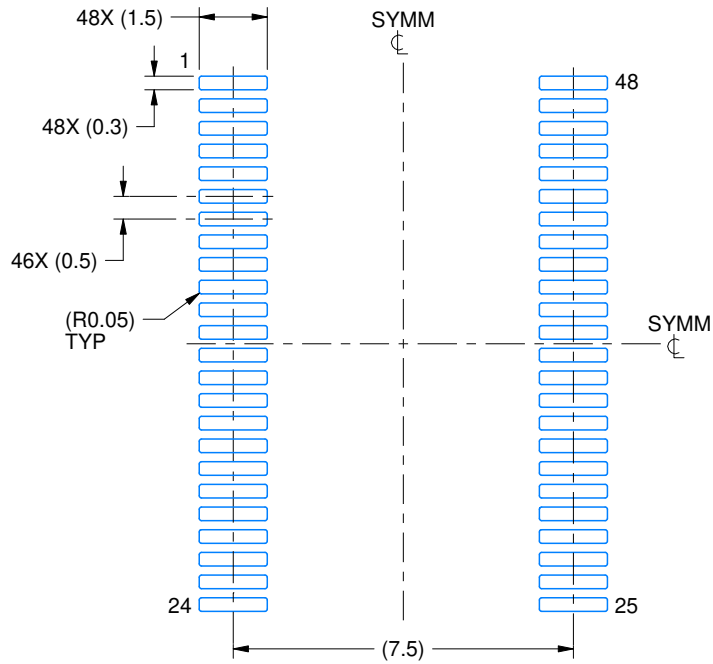
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

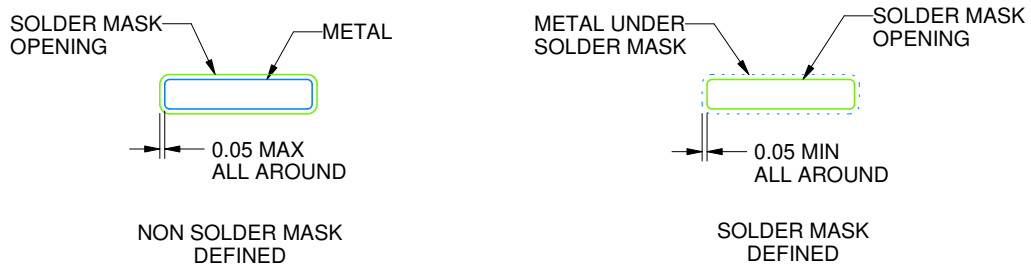
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

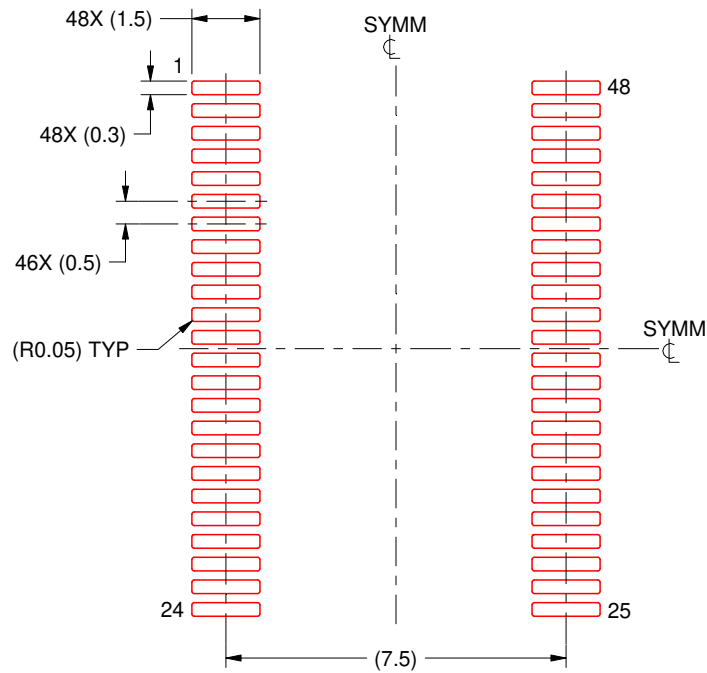
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

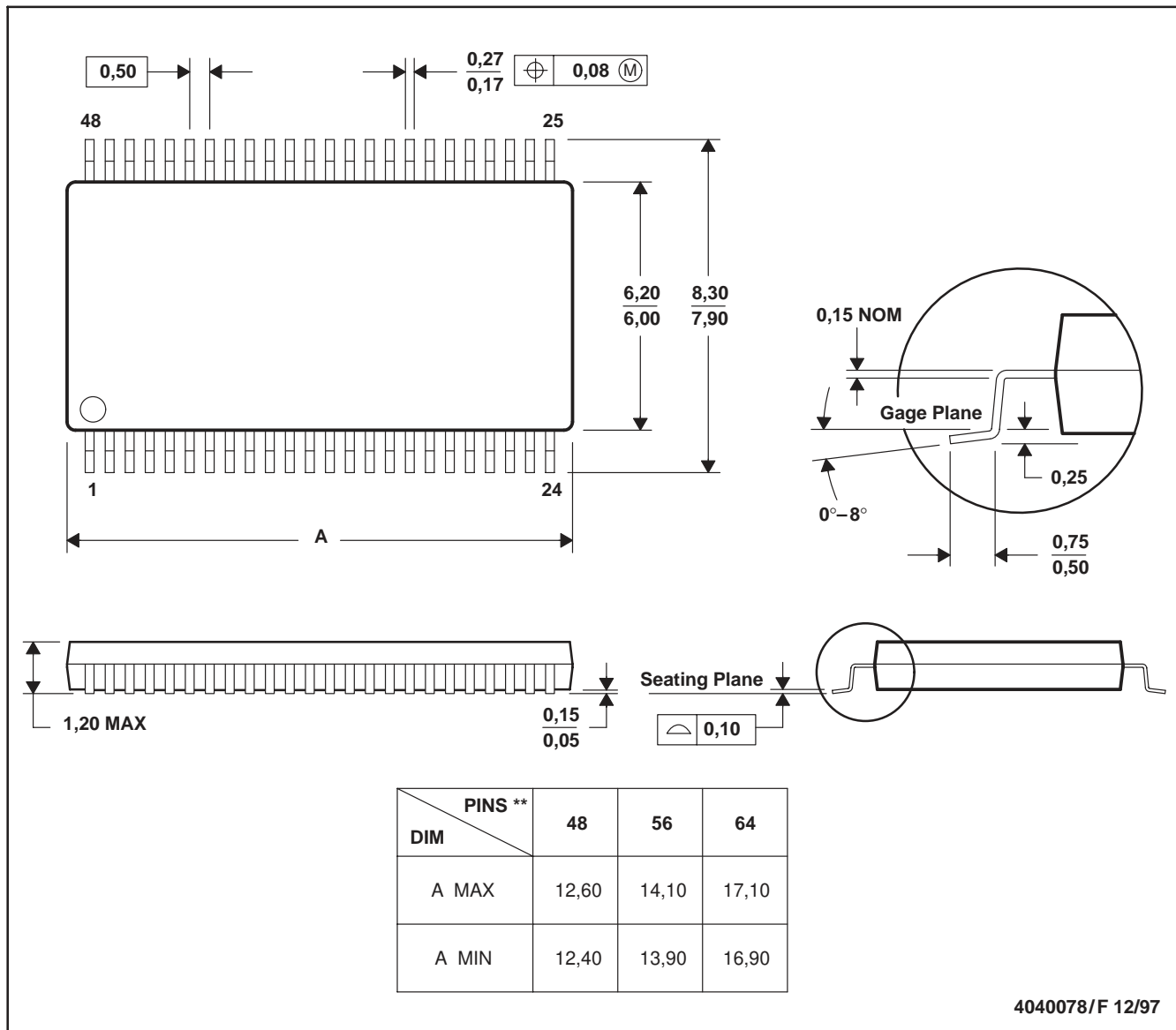
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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