# Low Cost, Voltage Output, High-Side, Current-Sense Amplifier

# ADM4073

## FEATURES

- Low cost, compact, current-sense solution
- 3 available gain versions
  - 20 V/V (ADM4073T)
  - 50 V/V (ADM4073F)
  - 100 V/V (ADM4073H)
- Typical ±1.0% full-scale accuracy
- Supply current: 500 µA
- Wide bandwidth: 1.8 MHz
- Operating supply: 3 V to 28 V
- Wide common-mode range: 2 V to 28 V
  - Independent of supply voltage
- Operating temperature range: −40°C to +125°C
- Available in a 6-lead SOT-23 package
- Pin-to-pin compatibility with the MAX4073

## APPLICATIONS

- Cell phones
- PDAs
- Notebook computers
- Portable, battery-powered systems
- Smart battery packs and chargers
- Automotive
- Power management systems
- PA bias control
- General system-level, board-level current monitoring
- Precision current sources

## FUNCTIONAL BLOCK DIAGRAM

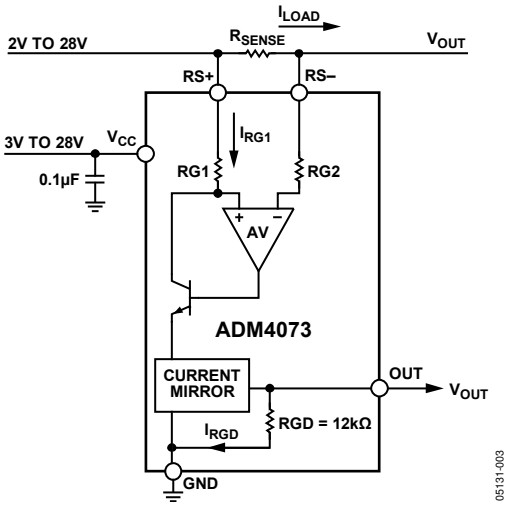


*Figure 1.*

## APPLICATION DIAGRAM

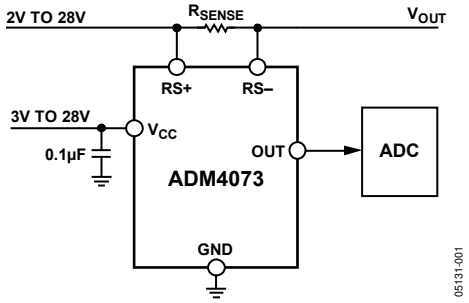


*Figure 2.*

## GENERAL DESCRIPTION

The ADM4073 is a low cost, high-side, current-sense amplifier ideal for small portable applications, such as cell phones, notebook computers, PDAs, and other systems where current monitoring is required. The device is available in three different gain models, eliminating the need for gain-setting resistors. Because the ground path is not interrupted, the ADM4073 is particularly useful in rechargeable battery-powered systems, while its wide 1.8 MHz bandwidth makes it suitable for use inside battery-charger control loops. The input common-mode range of 2 V to 28 V is independent of the supply voltage.

The voltage on the output pin is determined by the current flowing through the selectable external sense resistor and the gain of the version selected. The operating range is 3 V to 28 V with a typical supply current of 500 µA.

The ADM4073 is available in a 6-lead SOT-23 package and is specified over the automotive operating temperature range (−40°C to +125°C).

**Rev. A**



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113 

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**10/08—Rev. 0 to Rev. A**

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**7/06—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{RS+}$ = 2 V to 28 V, $V_{SENSE}$ = ($V_{RS+}$ − $V_{RS-}$) = 0 V, $V_{CC}$ = 3 V to 28 V, $T_A$ = −40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = 25°C.[1]

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Voltage Range, $V_{CC}$ | 3 | | 28 | V | Inferred from PSRR test |
| Common-Mode Input Range, $V_{CMR}$ | 2 | | 28 | V | Inferred OUT voltage error test |
| Common-Mode Input Rejection, CMR | | 90 | | dB | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V |
| Supply Current, $I_{CC}$ | | 0.5 | 1.2 | mA | $V_{CC}$ = 28 V |
| Leakage Current, $I_{RS+}/I_{RS-}$ | | 0.05 | 2 | µA | $V_{CC}$ = 0 V, $V_{RS+}$ = 28 V, $T_A$ = 85°C |
| Input Bias Current, $I_{RS+}$ | | 20 | 60 | µA | |
| Input Bias Current, $I_{RS-}$ | | 40 | 120 | µA | |
| Full-Scale Sense Voltage, $V_{SENSE}$ | | 150 | | mV | $V_{SENSE}$ = ($V_{RS+}$ − $V_{RS-}$) |
| Total Output Voltage Error[2] | | ±1 | | % | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 2 V |
| | | ±1.0 | ±5.0 | % | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $T_A$ = +25°C |
| | | | ±5.0 | % | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V, $V_{RS}$ = 12V, $T_A$ = −40°C to +125°C |
| | | ±1.0 | ±5.0 | % | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 28 V, $V_{RS}$ = 28 V, $T_A$ = +25°C |
| | | | ±5.0 | % | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 28 V, $V_{RS}$ = 28 V, $T_A$ = −40°C to +125°C |
| | | ±7.5 | | % | $V_{SENSE}$ = 6.25 mV,[3] $V_{CC}$ = 12 V, $V_{RS}$ = 12 V |
| Extrapolated Input Offset Voltage, $V_{OS}$ | | 1.0 | | mV | $V_{CC}$ = $V_{RS+}$ = 12 V, $V_{SENSE}$ > 10 mV |
| Output High Voltage ($V_{CC}$ − $V_{OH}$) | | 0.8 | 1.2 | V | $V_{CC}$ = 3 V, $V_{SENSE}$ = 150 mV (ADM4073T) |
| | | 0.8 | 1.2 | V | $V_{CC}$ = 7.5 V, $V_{SENSE}$ = 150 mV (ADM4073F) |
| | | 0.8 | 1.2 | V | $V_{CC}$ = 15 V, $V_{SENSE}$ = 150 mV (ADM4073H), $T_A$ = 25°C |
| DYNAMIC CHARACTERISTICS | | | | | |
| Bandwidth, BW | | 1.8 | | MHz | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $C_{LOAD}$ = 5 pF (ADM4073T) |
| | | 1.7 | | MHz | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $C_{LOAD}$ = 5 pF (ADM4073F) |
| | | 1.6 | | MHz | $V_{SENSE}$ = 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $C_{LOAD}$ = 5 pF (ADM4073H) |
| | | 600 | | kHz | $V_{SENSE}$ = 6.25 mV,[3] $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $C_{LOAD}$ = 5 pF (ADM4073T/F/H) |
| Gain, $A_V$ | | 20 | | V/V | ADM4073T |
| | | 50 | | V/V | ADM4073F |
| | | 100 | | V/V | ADM4073H |
| Gain Accuracy | | ±1.0 | ±2.0 | % | $V_{SENSE}$ = 10 mV to 150 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $T_A$ = +25°C (ADM4073T/F) |
| | | | ±2.0 | % | $V_{SENSE}$ = 10 mV to 150 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $T_A$ = −40°C to +125°C (ADM4073T/F) |
| | | ±1.0 | ±1.5 | % | $V_{SENSE}$ = 10 mV to 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $T_A$ = +25°C (ADM4073H) |
| | | | ±3.0 | % | $V_{SENSE}$ = 10 mV to 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $T_A$ = −40°C to +125°C (ADM4073H) |
| OUT Settling Time to 1% of Final Value | | 400 | | ns | $V_{SENSE}$ = 6.25 mV to 100 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $C_{LOAD}$ = 5 pF |
| | | 800 | | ns | $V_{SENSE}$ = 100 mV to 6.25 mV, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V, $C_{LOAD}$ = 5 pF |
| Output Resistance, $R_{OUT}$ | | 12 | | kΩ | |
| Power Supply Rejection Ratio, PSRR | | 78 | | dB | $V_{SENSE}$ = 60 mV, $V_{CC}$ = 3 V to 28 V (ADM4073T) |
| | | 85 | | dB | $V_{SENSE}$ = 24 mV, $V_{CC}$ = 3 V to 28 V (ADM4073F) |
| | | 90 | | dB | $V_{SENSE}$ = 12 mV, $V_{CC}$ = 3 V to 28 V (ADM4073H) |
| Power-Up Time[4] | | 5 | | µs | $C_{LOAD}$ = 5 pF, $V_{SENSE}$ = 100 mV |
| Saturation Recovery Time[5] | | 5 | | µs | $C_{LOAD}$ = 5 pF, $V_{CC}$ = 12 V, $V_{RS+}$ = 12 V |

[1] 100% production tested at $T_A$ = 25°C. Specifications over temperature limit are guaranteed by design.
[2] The sum of the gain and offset errors is the total OUT voltage error.
[3] 6.25 mV = 1/16$^{th}$ of 100 mV full-scale sense voltage.
[4] Output settles to within 1% of final value.
[5] When overdriven, this device does not experience phase reversal.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ to GND | −0.3 V to +30 V |
| RS+, RS− to GND | −0.3 V to +30 V |
| OUT to GND | −0.3 V to ($V_{CC}$ + 0.3 V) |
| OUT Short-Circuit to GND | Continuous |
| Differential Input Voltage ($V_{RS+} - V_{RS-}$) | ±5 V |
| Current into Any Pin | ±20 mA |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +125°C |
| Lead Temperature, Soldering (10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 6-Lead SOT-23 | 169.5 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

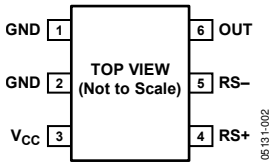



*Figure 3. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | GND | Chip Ground Pin. |
| 2 | GND | Chip Ground Pin. |
| 3 | $V_{CC}$ | Chip Power Supply. Requires a 0.1 µF capacitor to ground. |
| 4 | RS+ | Power-Side Connection to the External Sense Resistor. |
| 5 | RS– | Load-Side Connection to the External Sense Resistor. |
| 6 | OUT | Voltage Output. $V_{OUT}$ is proportional to $V_{SENSE}$. Output impedance is approximately 12 kΩ. |

# TYPICAL PERFORMANCE CHARACTERISTICS

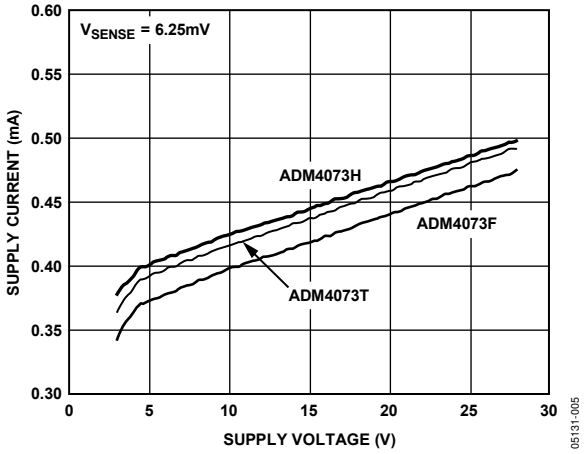



*Figure 4. Supply Current vs. Supply Voltage ($V_{SENSE}$ = 6.25 mV)*

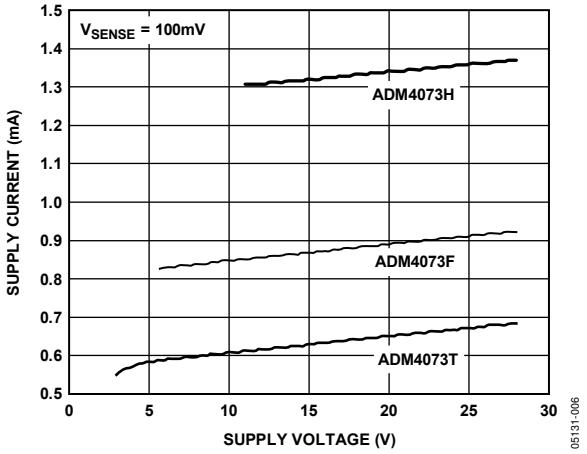



*Figure 5. Supply Current vs. Supply Voltage ($V_{SENSE}$ = 100 mV)*

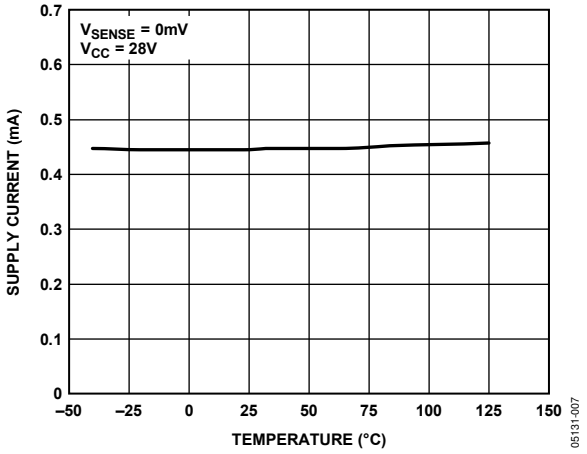



*Figure 6. Supply Current vs. Temperature*

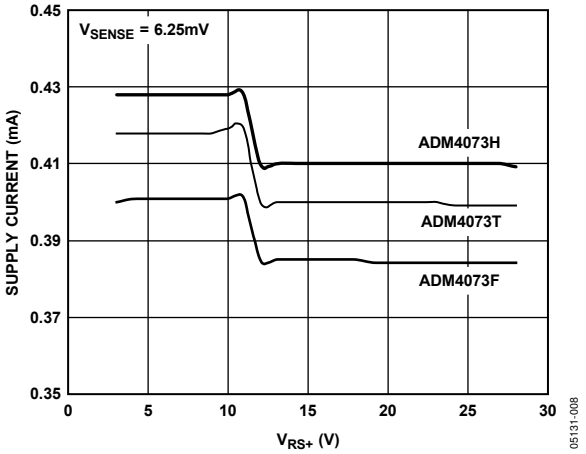



*Figure 7. Supply Current vs. RS+ Voltage ($V_{SENSE}$ = 6.25 mV)*

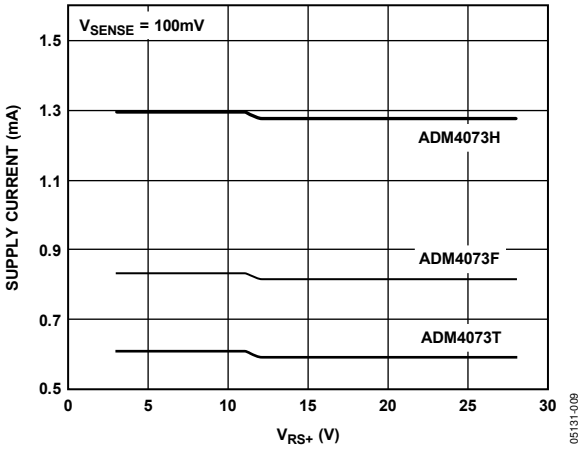



*Figure 8. Supply Current vs. RS+ Voltage ($V_{SENSE}$ = 100 mV)*

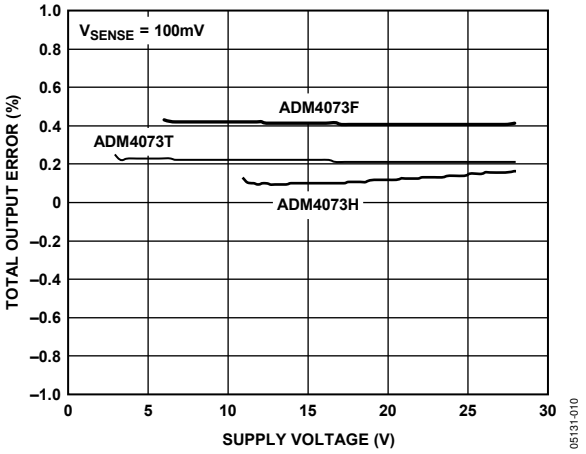



*Figure 9. Total Output Error vs. Supply Voltage ($V_{SENSE}$ = 100 mV)*

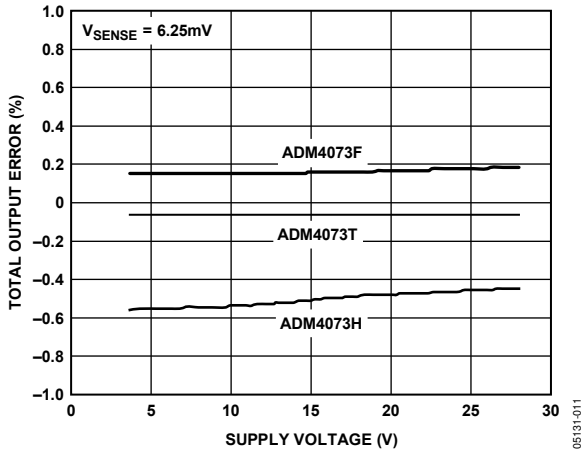



Figure 10. Total Output Error vs. Supply Voltage ($V_{SENSE}$ = 6.25 mV)

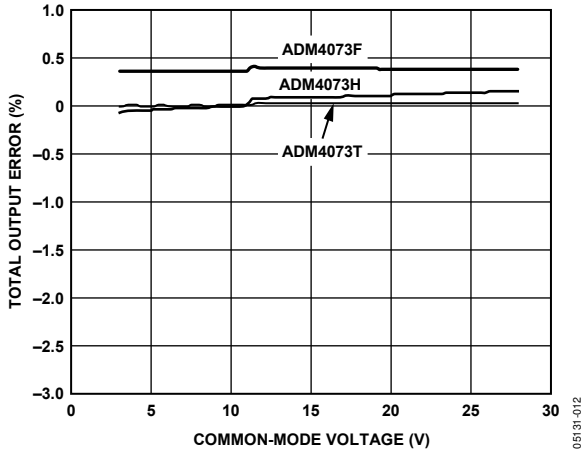



Figure 11. Total Output Error vs. Common-Mode Voltage

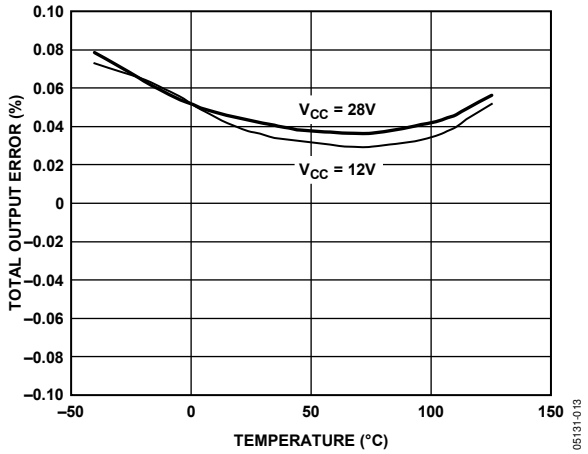



Figure 12. Total Output Error vs. Temperature

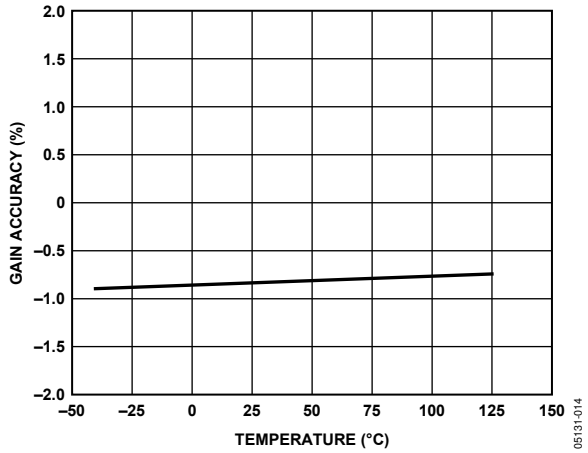



Figure 13. Gain Accuracy vs. Temperature

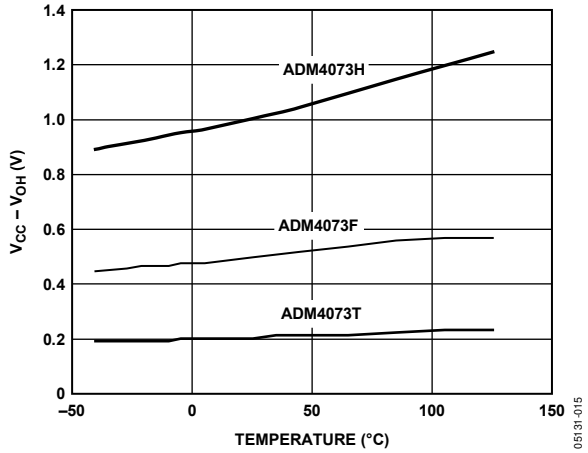



Figure 14. Output High Voltage ($V_{CC}$ – $V_{OH}$) vs. Temperature

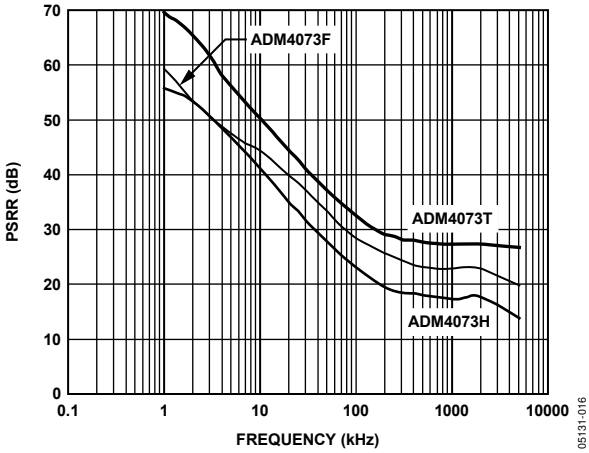



Figure 15. PSRR vs. Frequency

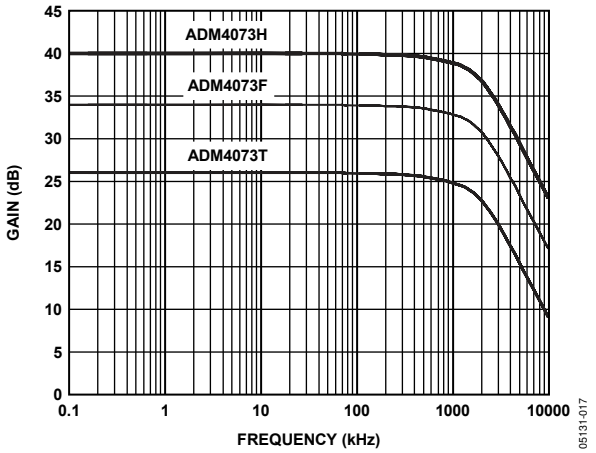



Figure 16. Small Signal Gain vs. Frequency

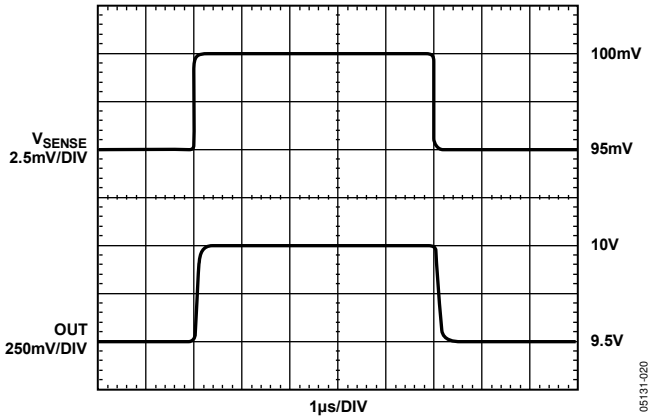



Figure 19. ADM4073H Small Signal Transient Response

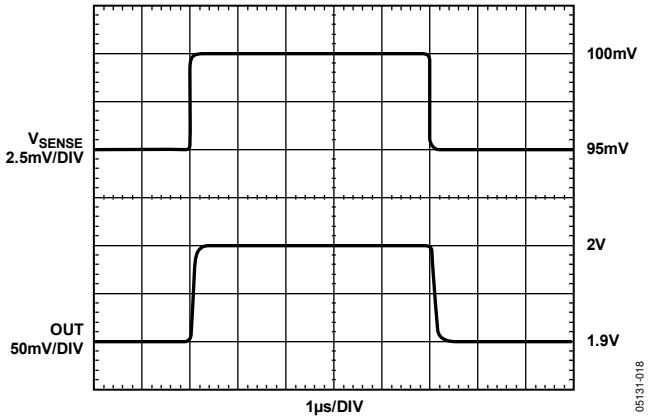



Figure 17. ADM4073T Small Signal Transient Response

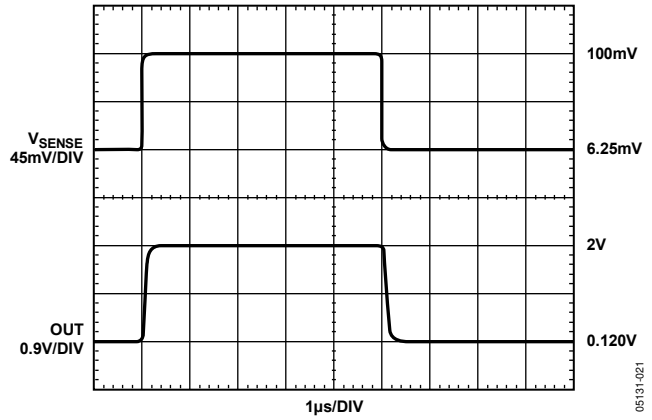



Figure 20. ADM4073T Large Signal Transient Response

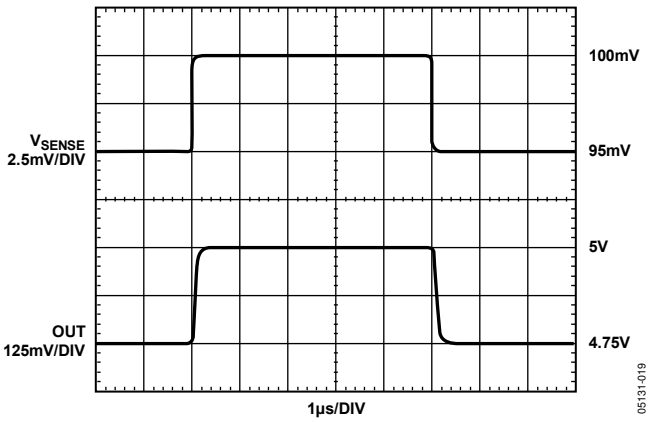



Figure 18. ADM4073F Small Signal Transient Response

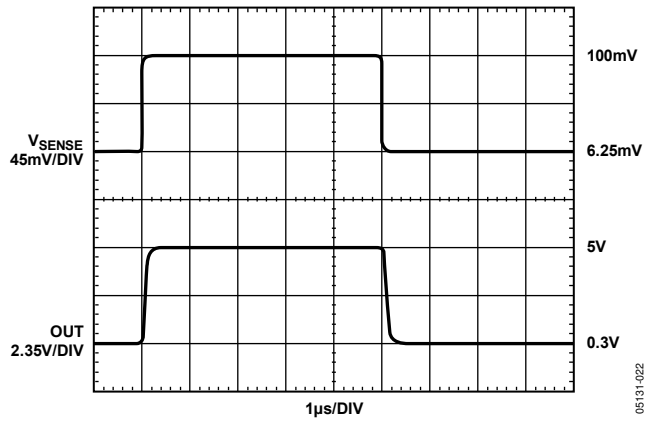



Figure 21. ADM4073F Large Signal Transient Response

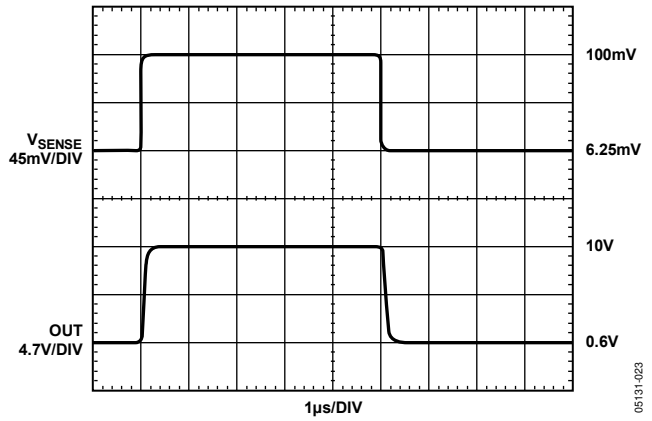



*Figure 22. ADM4073H Large Signal Transient Response*

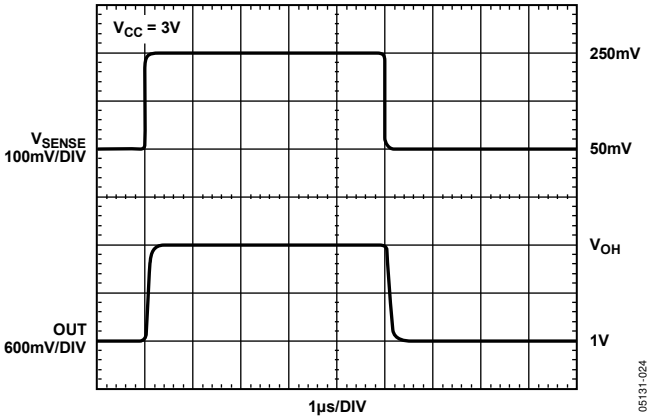



*Figure 23. ADM4073T Overdrive Response*

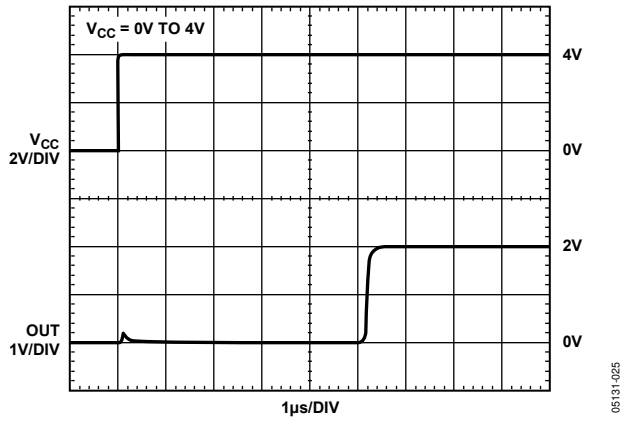



*Figure 24. ADM4073T Start-Up Delay*

# THEORY OF OPERATION

The current from the source flows through $R_{SENSE}$, which generates a voltage drop, $V_{SENSE}$, across the RS+ and RS− terminals of the sense amplifier. The Input Stage Amplifier A1 regulates its inputs to be equal, thereby shunting a current proportional to $V_{SENSE}/R_{G1}$ to the output current mirror. This current is then multiplied by a gain factor of b in the output stage current mirror and flows through $R_{GD}$ to generate $V_{OUT}$. Therefore, $V_{OUT}$ is related to $V_{SENSE}$ by the ratio of $R_{G1}$ to $R_{GD}$ and the current gain of b.

$$V_{OUT} = A_V \times V_{SENSE}$$

where:
$A_V = R_{GD}/R_{G1} \times b$

$A_v$ is equal to different voltages depending upon the model of the device.

- 20 V/V for ADM4073T.
- 50 V/V for ADM4073F.
- 100 V/V for ADM4073H.

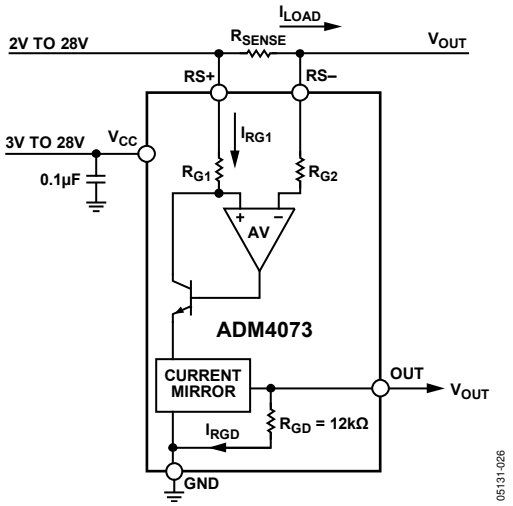



*Figure 25. Functional Block Diagram*

## $R_{SENSE}$

The ADM4073 has the ability to sense a wide variety of currents by selecting a particular sense resistor. Select a suitable output voltage for full-scale current, such as 10 V for 10 A. Then, select a gain model that gives the most efficient use of the sense voltage range (150 mV max).

In the example above, using the ADM4073H (gain of 100) gives an output voltage of 10 V when the sense voltage is 100 mV. Use the following equation to determine what value of sense resistor gives 100 mV with 10 A flowing through it:

$R_{SENSE}$ = 100 mV/10 A

$R_{SENSE}$ = 10 mΩ

$V_{OUT} = (I_{LOAD} \times R_{SENSE}) \times A_V$

To measure lower currents accurately, use as large a sense resistor as possible to utilize the higher end of the sense voltage range. This reduces the effects of the offset voltage errors in the internal amplifier.

When currents are very large, it is important to take the $I^2R$ power losses across the sense resistor into account. If the sense resistor's rated power dissipation is not sufficient, its value can drift, giving an inaccurate output voltage or it could fail altogether. This, in turn, causes the voltage across the RS+ and RS− pins to exceed the absolute maximum ratings.

If the monitored supply rail has a large amplitude high frequency component, choose a sense resistor with low inductance.

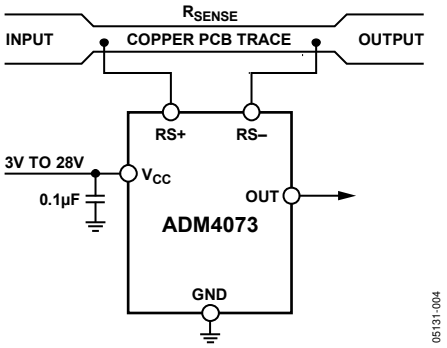



*Figure 26. Using PCB Trace for Current Sensing*

## OUTPUT (OUT)

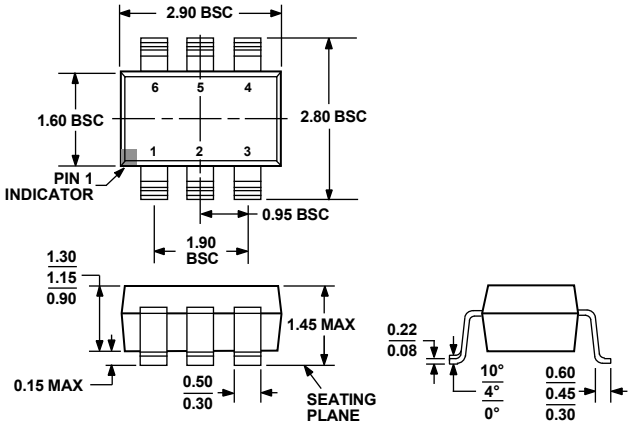
The output stage of the ADM4073 is a current source driving a pull-down resistance. To ensure optimum accuracy, care must be taken not to load this output externally. To minimize output errors, ensure OUT is connected to a high impedance input stage. If this is not possible, output buffering is recommended.

The percent error introduced by output loading is determined with the following formula:

$$\%\ Error = 100\left(1 - R_{LOAD}/\left(R_{OUT\_INT} + R_{LOAD}\right)\right)$$

where:
$R_{LOAD}$ is the external load applied to OUT.
$R_{OUT\_INT}$ is the internal output resistance (12 kΩ).

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-178-AB

*Figure 27. 6-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-6)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Gain | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|
| ADM4073TWRJZ-REEL7[1] | 20 | –40°C to +125°C | 6-Lead SOT-23 | RJ-6 | M2E |
| ADM4073FWRJZ-REEL7[1] | 50 | –40°C to +125°C | 6-Lead SOT-23 | RJ-6 | M2C |
| ADM4073HWRJZ-REEL7[1] | 100 | –40°C to +125°C | 6-Lead SOT-23 | RJ-6 | M2D |
| ADM4073WFWRJZ-RL7[1, 2] | 50 | –40°C to +125°C | 6-Lead SOT-23 | RJ-6 | M2C |

[1] Z = RoHS Compliant Part.
[2] Automotive Grade.

## NOTES


D05131-0-10/08(A)