PROFET™ Load Guard
Smart high-side power switch

RoHS

AEC Qualified

ISO 26262 ready

Features

- High-side switch with diagnosis and embedded protection
- Part of PROFET™ Load Guard family
- Switch ON capability while inverse current condition (InverseON)
- Capacitive load switching mode
- Green product (RoHS compliant)

Potential applications

- Replaces electromechanical relays, fuses and discrete circuits
- Protection of system supply
- Main switch for ECU power supply
- Suitable for driving resistive, inductive and capacitive loads
- Suitable for driving heating elements
- Suitable for driving ADAS & AD modules, e.g. cameras, radar, ultrasonic, and LIDAR modules
- Suitable for driving sub modules, e.g. displays

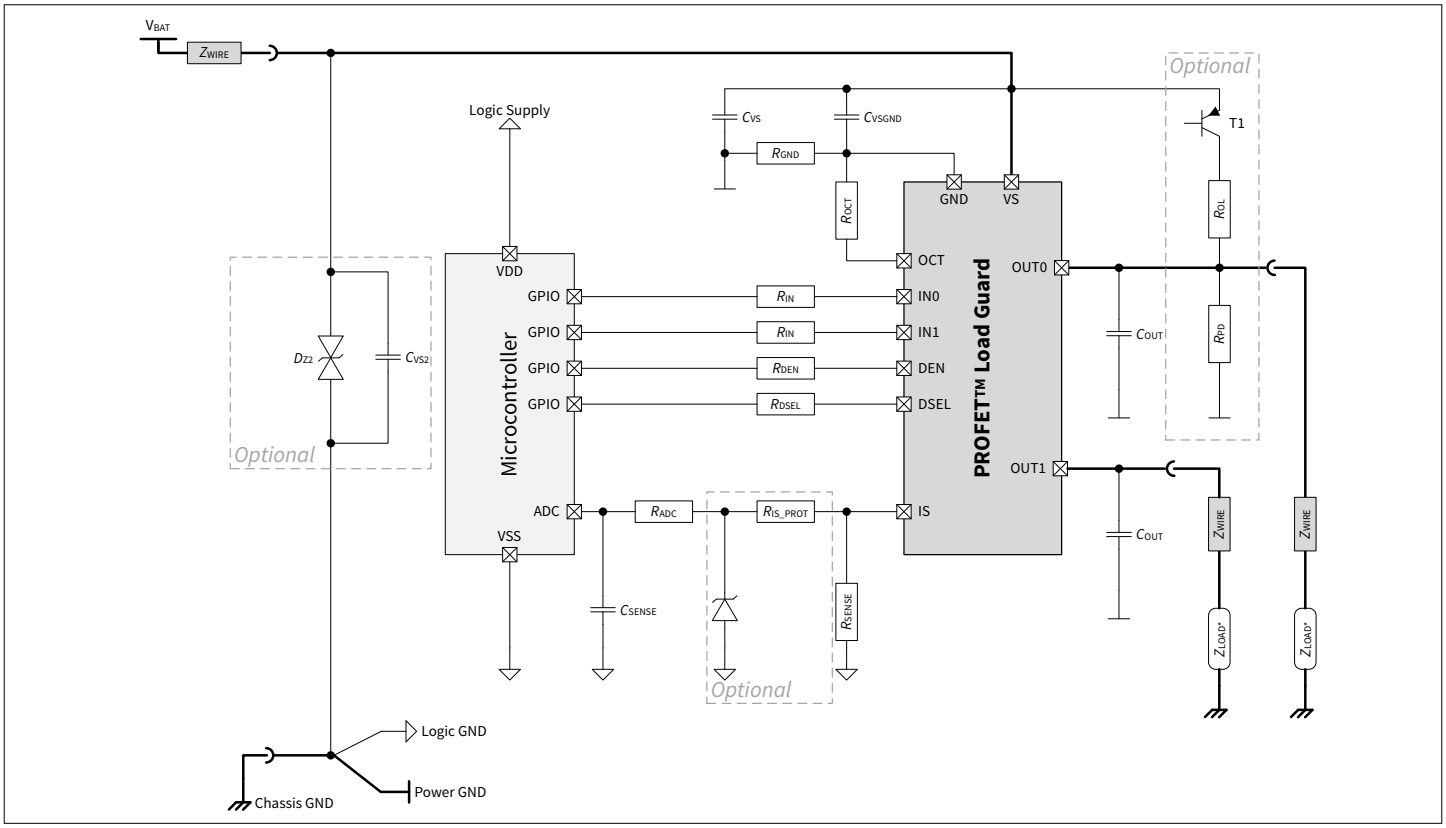
Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100, Grade 1.

Description

The PROFET™ Load Guard is a Smart High Side Switch, providing protection functions and enhanced diagnosis capabilities. The device offers an adjustable current limitation to offer higher reliability for protecting the system. In case of an short circuit to ground the PCB traces, connectors, as well as loads, can be protected. Furthermore, the PROFET™ Load Guard has an capacitive load switching mode implemented to charge capacitors.



Further information in Chapter 9

Parameter	Symbol	Values
Minimum operating voltage	$V_{S(OP)}$	3 V
Minimum operating voltage (cranking)	$V_{S(UV)}$	2.7 V
Maximum operating voltage	V_S	28 V
Minimum overvoltage protection ($T_J \geq 25°C$)	$V_{DS(CLAMP)\_25}$	35 V
Maximum current in sleep mode ($T_J \leq 85°C$)	$I_{VS(SLEEP)\_85}$	0.5 µA
Maximum operative current	$I_{GND(ACTIVE)}$	4.5 mA
Typical ON-state resistance ($T_J = 25°C$)	$R_{DS(ON)\_25}$	50 mΩ
Maximum ON-state resistance ($T_J = 150°C$)	$R_{DS(ON)\_150}$	100 mΩ
Nominal load current ($T_A = 85°C$)	$I_{L(NOM)}$	3 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	k_{ILIS}	2030
Adjustable overcurrent limitation	I_{LIM}	0.79 A - 8.86 A

Diagnostic features

- Proportional load current sense
- Open load in ON and OFF state
- Short circuit to ground and battery

Protection features

- Absolute and dynamic temperature protection with restart control
- Adjustable overcurrent limitation
- Overvoltage protection

Type	Package	Marking
BTG7050-2EPL	PG-TSDSO-14	7050-2L

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1 Block diagram and terms

1.1 Block diagram

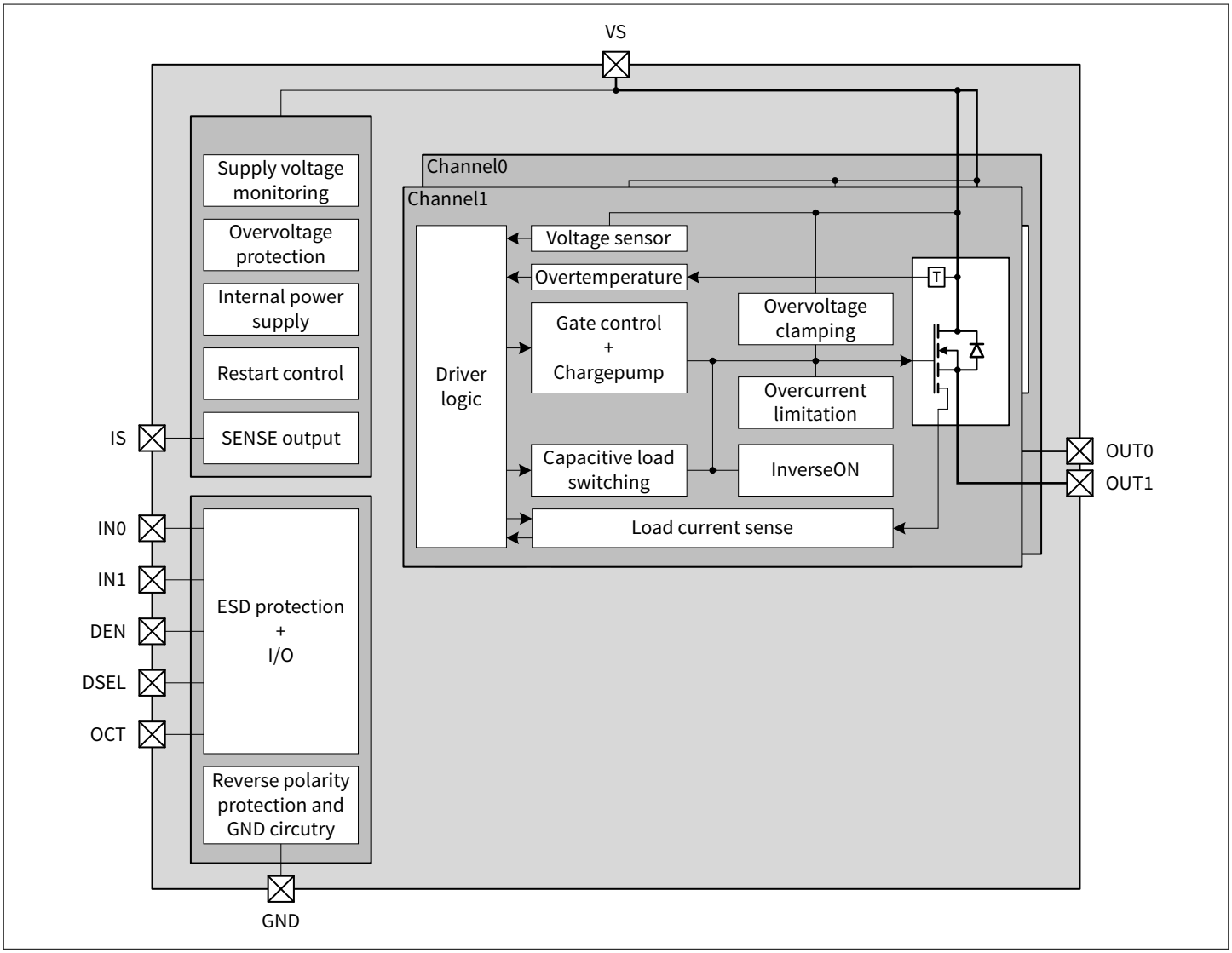


Figure 2 Block diagram of BTG7050-2EPL

1.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

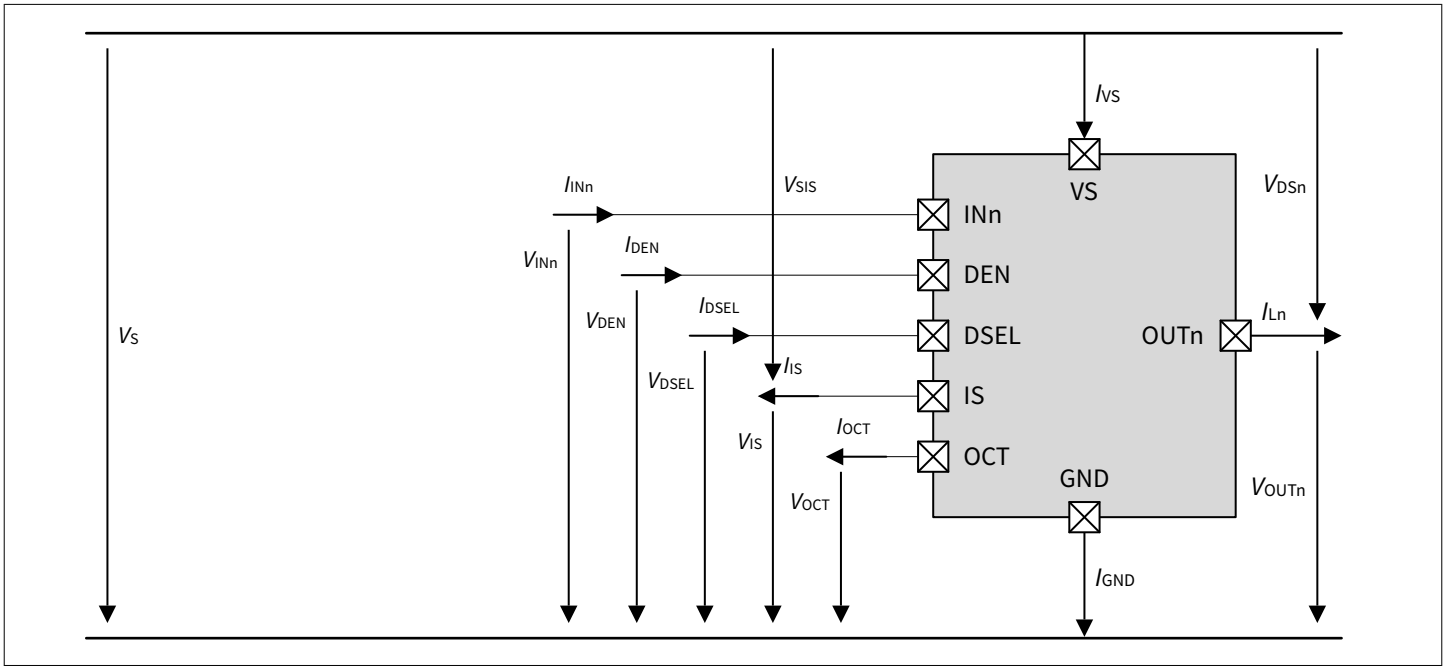


Figure 3 Voltage and current convention

2 Pin configuration

2.1 Pin assignment

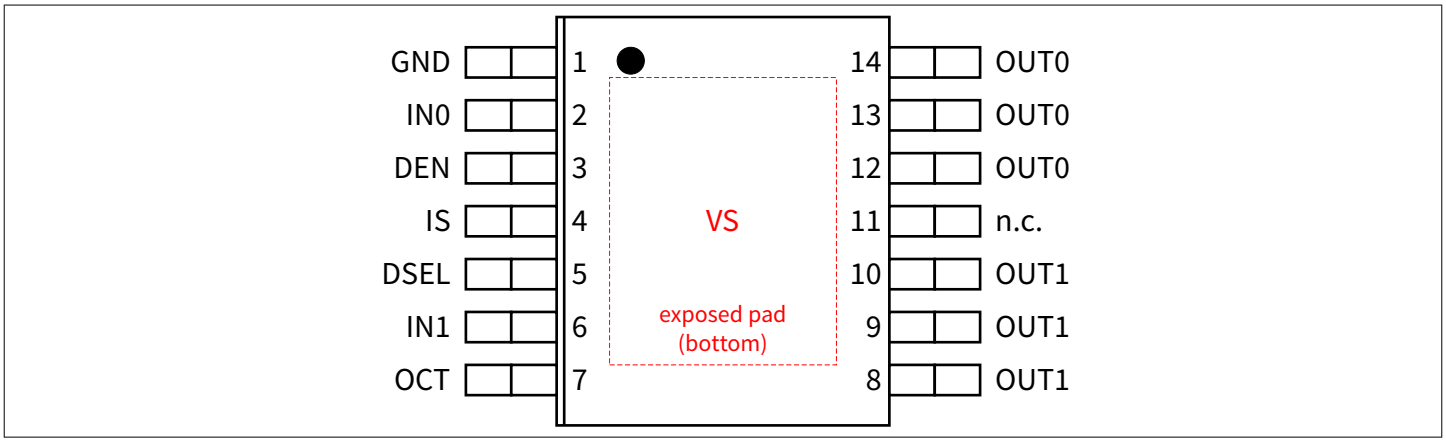


Figure 4 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definition

Pin	Symbol	Function
EP	VS (exposed pad)	**Supply Voltage** Battery voltage
1	GND	**Ground** Ground connection for the internal logic
2, 6	INn	**Input Channel n** Digital signal to switch ON channel n ("high" active) If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
3	DEN	**Diagnostic Enable** Digital signal to enable device diagnosis ("high" active) and to clear the protection counter of channel selected with DSEL pin. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
4	IS	**SENSE current output** Analog/digital signal for diagnosis If not used: Left open
5	DSEL	**Diagnosis Selection** Digital signal to toggle between the channels. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
7	OCT	**Adjustable overcurrent threshold** A resistor R_{OCT} needs to be connected between OCT pin and GND pin to adjust the overcurrent threshold If not used: Threshold selection as described in Chapter 7.1.1
11	n.c.	Not connected, internally not bonded

(table continues...)

Table 1 (continued) Pin definition

Pin	Symbol	Function
8-10, 12-14	OUTn	**Output n** Protected high-side power output channel n [1)]

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

3 General product characteristics

3.1 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	28	V	2) -	PRQ-34
Load dump voltage	$V_{BAT(LD)}$	–	–	35	V	2) suppressed load dump acc. to ISO16750-2 (2010). R_i = 2 Ω	PRQ-36
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	24	V	2) Setup acc. to AEC-Q100-012	PRQ-38
Reverse polarity voltage	$-V_{BAT(REV)}$	–	–	16	V	2) $t \leq$ 2min T_A = +25°C Setup as described in Chapter 9	PRQ-40
Current through GND pin	I_{GND}	-50	–	50	mA	2) R_{GND} according to Chapter 9	PRQ-44
Logic & control pins (Digital Input = DI) **DI = INn, DEN, DSEL**							
Current through DI pin	I_{DI}	-1	–	2	mA	2) 1)	PRQ-47
Current through DI pin - Reverse battery condition	$I_{DI(REV)}$	-1	–	10	mA	2) 1) $t \leq$ 2 min	PRQ-48
Analog & control pin (Analog Input = AI) **AI = OCT**							
Current through AI pin	I_{AI}	-1	–	2	mA	2) 1)	PRQ-60
Current through AI pin - Reverse battery condition	$I_{AI(REV)}$	-1	–	10	mA	2) 1) $t \leq$ 2 min	PRQ-61

(table continues...)

Table 2 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IS pin							
Voltage at IS pin	V_{IS}	-1.5	–	V_S	V	2) I_{IS} = 10 µA	PRQ-50
Current through IS Pin	I_{IS}	-25	–	$I_{IS(SAT),MAX}$	mA	2) -	PRQ-52
Temperatures							
Junction temperature	T_J	-40	–	+150	°C	2) -	PRQ-53
Storage temperature	T_{STG}	-55	–	+150	°C	2) -	PRQ-54
ESD susceptibility							
ESD Susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	2) HBM[3]	PRQ-55
ESD Susceptibility OUTn vs GND and VS connected (HBM)	$V_{ESD(HBM)\_OUT}$	-4	–	4	kV	2) HBM[3]	PRQ-56
ESD Susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	2) CDM[4]	PRQ-57
ESD Susceptibility corner pins (CDM) - (pins 1, 7, 8, 14)	$V_{ESD(CDM)\_CRN}$	-750	–	750	V	2) CDM[4]	PRQ-58
Power stage							
Maximum energy dissipation - single pulse	E_{AS}	–	–	12	mJ	2) $I_L = 2 \cdot I_{L(NOM)}$ $T_{J(0)}$ = 150°C V_S = 28 V	PRQ-615
Maximum energy dissipation - repetitive pulse	E_{AR}	–	–	2.5	mJ	2) $I_L = I_{L(NOM)}$ $T_{J(0)}$ = 85°C V_S = 13.5 V 1M cycles	PRQ-616
Load current	$\|I_L\|$	–	–	$I_{LIM,MAX}$	A	2) –	PRQ-617

1) Maximum V_{DI} to be considered for Latch-Up tests: 5.5 V
2) Not subject to production test - specified by design
3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(NOR)}$	4	13.5	20	V	1) –	PRQ-66
Lower extended supply voltage range for operation (normal)	$V_{S(EXT,LOW)}$	2.7	–	4	V	1) 2) 3) (parameter deviations possible)	PRQ-67
Upper extended supply voltage range for operation	$V_{S(EXT,UP)}$	20	–	28	V	1) 3) (parameter deviations possible)	PRQ-68
Junction temperature	T_J	-40	–	+150	°C	1) –	PRQ-69

1) Not subject to production test - specified by design
2) In case of V_S voltage decreasing refer to the maximum voltage of $V_{S(UV)}$, in case of V_S voltage increasing refer to the maximum voltage of $V_{S(OP)}$
3) Protection functions still operative

Note

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified by the conditions given in the Electrical Characteristics tables.

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction-top	Ψ_{JTOP}	–	4.4	7.5	K/W	1) 2)	PRQ-623

(table continues...)

Table 4 (continued) Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction-to-case	R_{thJC}	–	5.1	8.6	K/W	1) 2) simulated at exposed pad	PRQ-624
Thermal resistance junction-to-ambient	R_{thJA}	–	33.5	–	K/W	1) 2)	PRQ-625

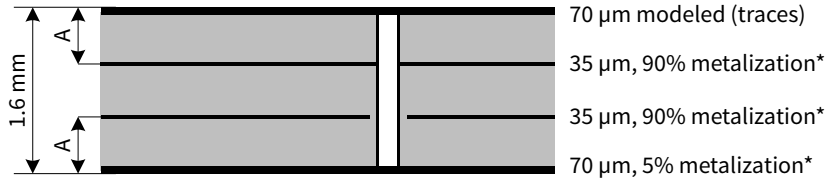
1) Not subject to production test - specified by design
2) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_A = 105°C, $P_{DISSIPATION}$ = 1 W

Note
This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

3.3.1 PCB setup

*: means percentual Cu metalization on each layer

Figure 5 1s0p PCB cross section



0.25mm ≤ A ≤ 0.5 mm *: means percentual Cu metalization on each layer

Figure 6 2s2p PCB cross section

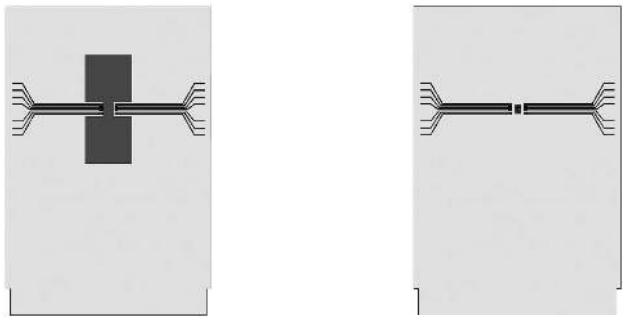


Figure 7 PCB setup for thermal simulations

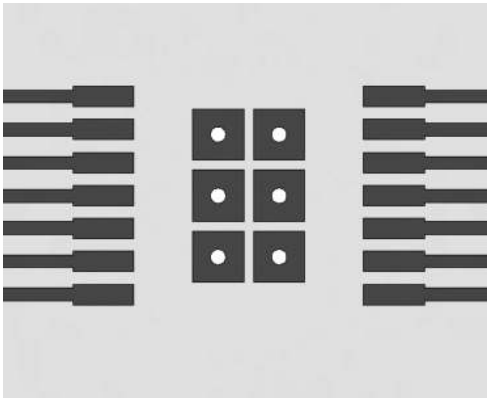


Figure 8 Thermal vias on PCB for 2s2p PCB setup

3.3.2 Thermal impedance

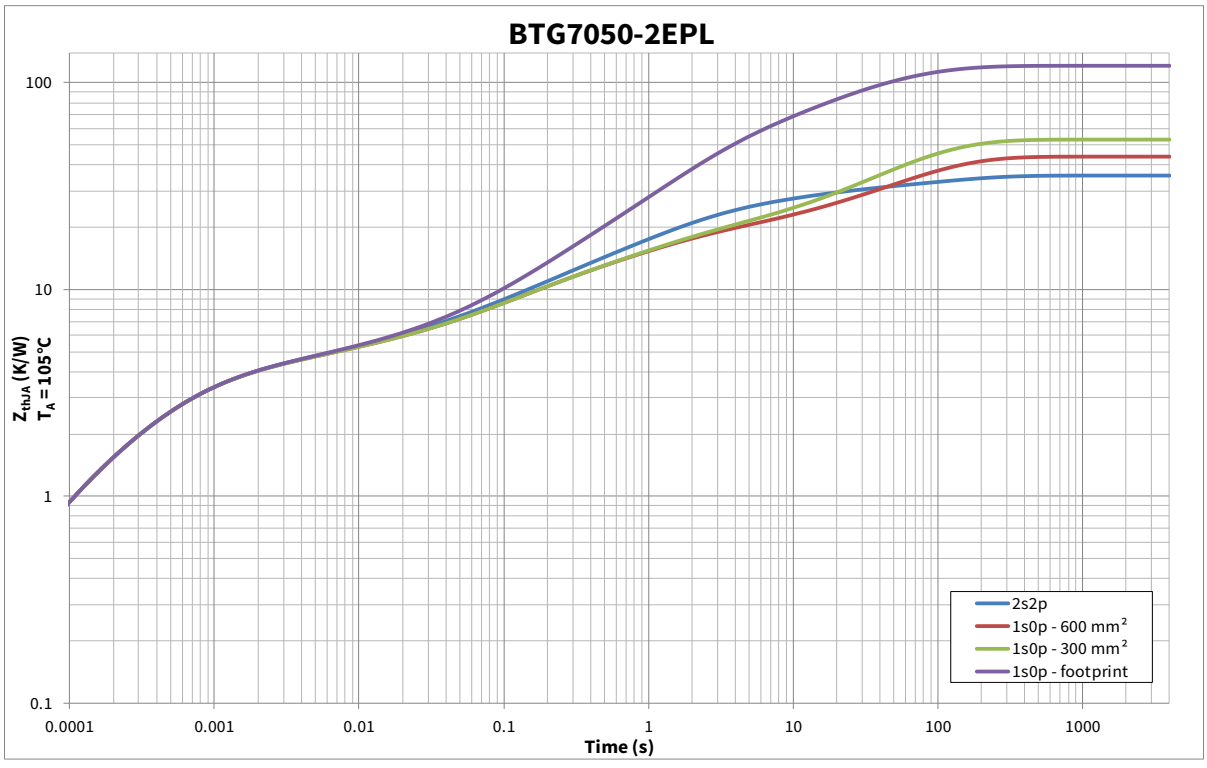


Figure 9 Typical thermal impedance. PCB setup according to PCB setup

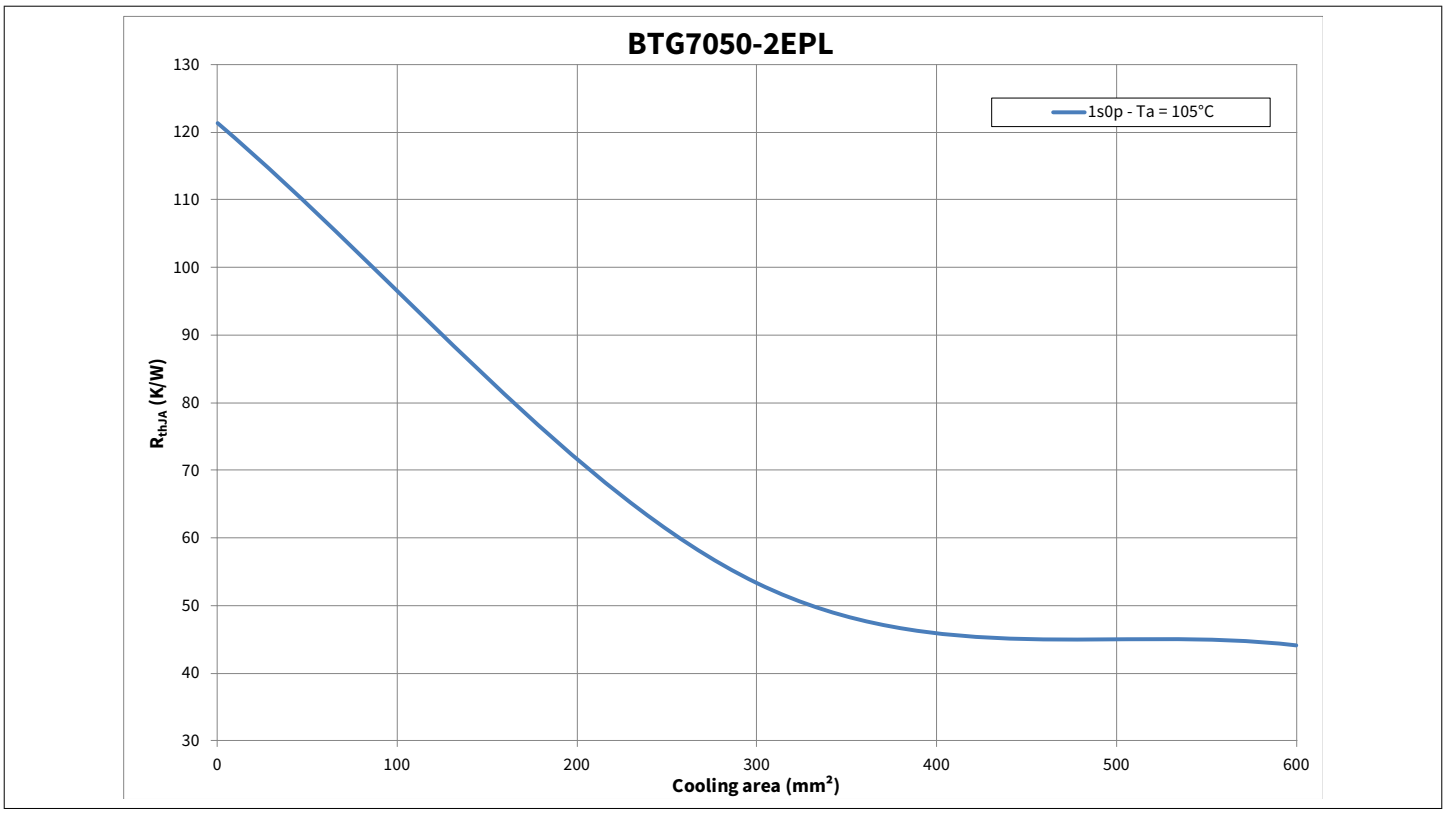


Figure 10 Thermal resistance on 1s0p PCB with various cooling surfaces

4 I/O pins

The device has four digital pins for direct control.

4.1 Digital I/O pins

Digital input (DI) pins = INn, DEN, DSEL

4.1.1 Input pins

The input pins IN0 and IN1 activate the corresponding output channel. The input circuitry is compatible with 3.3 V and 5 V microcontroller. The electrical equivalent of the input circuitry is shown in Figure 11. In case a pin is not used, it must be connected by a 10 kΩ resistor either to GND pin or to module ground.

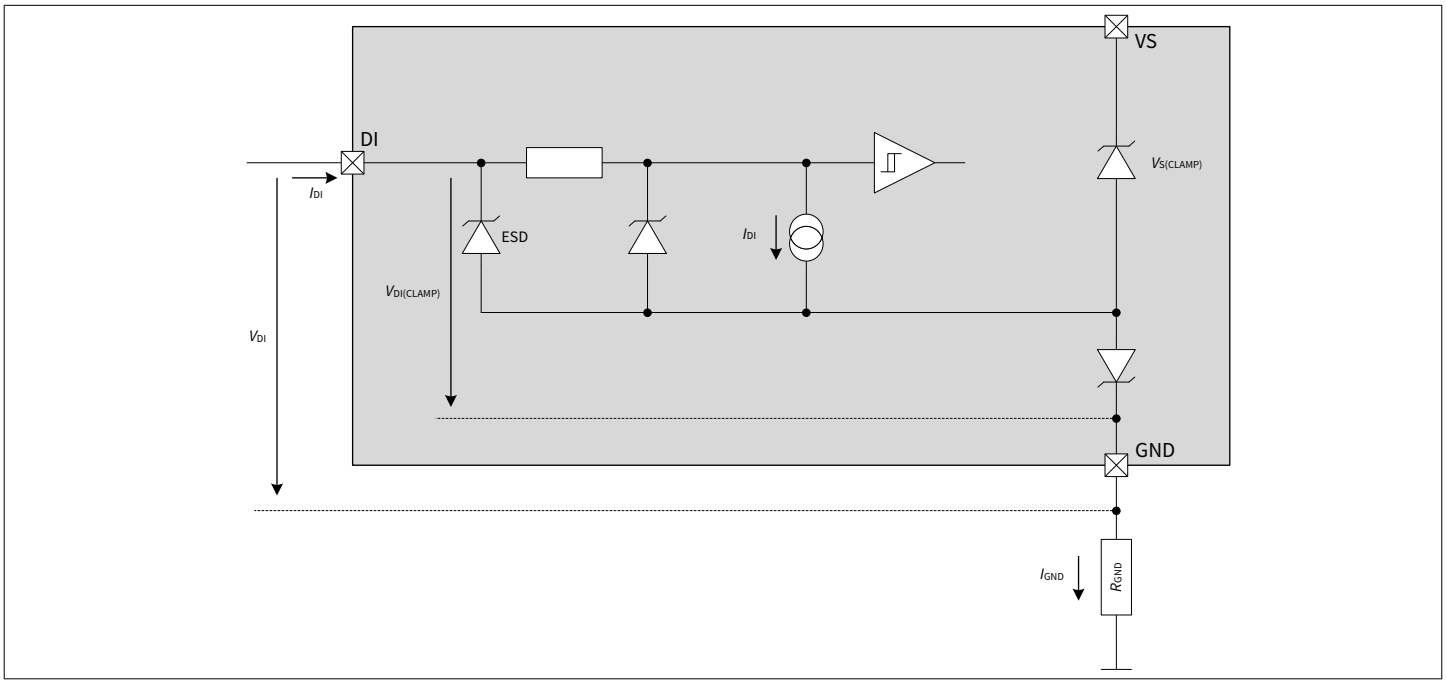


Figure 11 Input circuitry

The logic thresholds for “low” and “high” states are defined by parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in Figure 12.

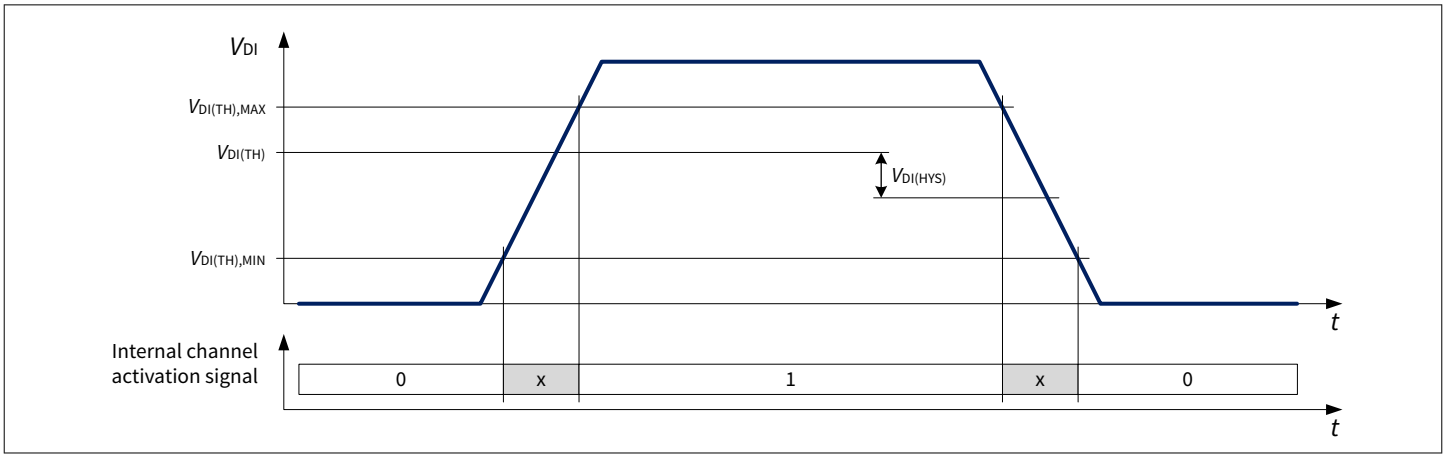


Figure 12 Input threshold voltages and hysteresis

4.1.2 Diagnosis pins

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and the protection circuitry. When DEN pin is set to “high”, the diagnosis is enabled (see Chapter 8.2 for more details). When it is set to “low”, the diagnosis is disabled (IS pin is set to high impedance). The Diagnosis Selection (DSEL) pin selects the channel where the diagnosis is performed (see Table 12). See Figure 12 for more details.

The transition from “high” to “low” of DEN pin clears the protection latch of the channel selected with DSEL pin depending on the logic state of IN pin and DEN pulse length (see Chapter 7.3 for more details).

4.2 Analog I/O pins

Analog input (AI) pins = OCT

4.2.1 Adjustable overcurrent threshold pin

To be able to adjust the overcurrent limitation for the OUTx pins, the device offers an OCT pin. The pin needs to be connected to device ground via an external resistor R_{OCT}. The adjustable current limit allows the flexibility to adjust the overcurrent limitation as defined in Table 10. This improves the reliability of the system by limiting the inrush or overload current. The electrical equivalent of the overcurrent pin circuit circuitry is shown in Figure 13.

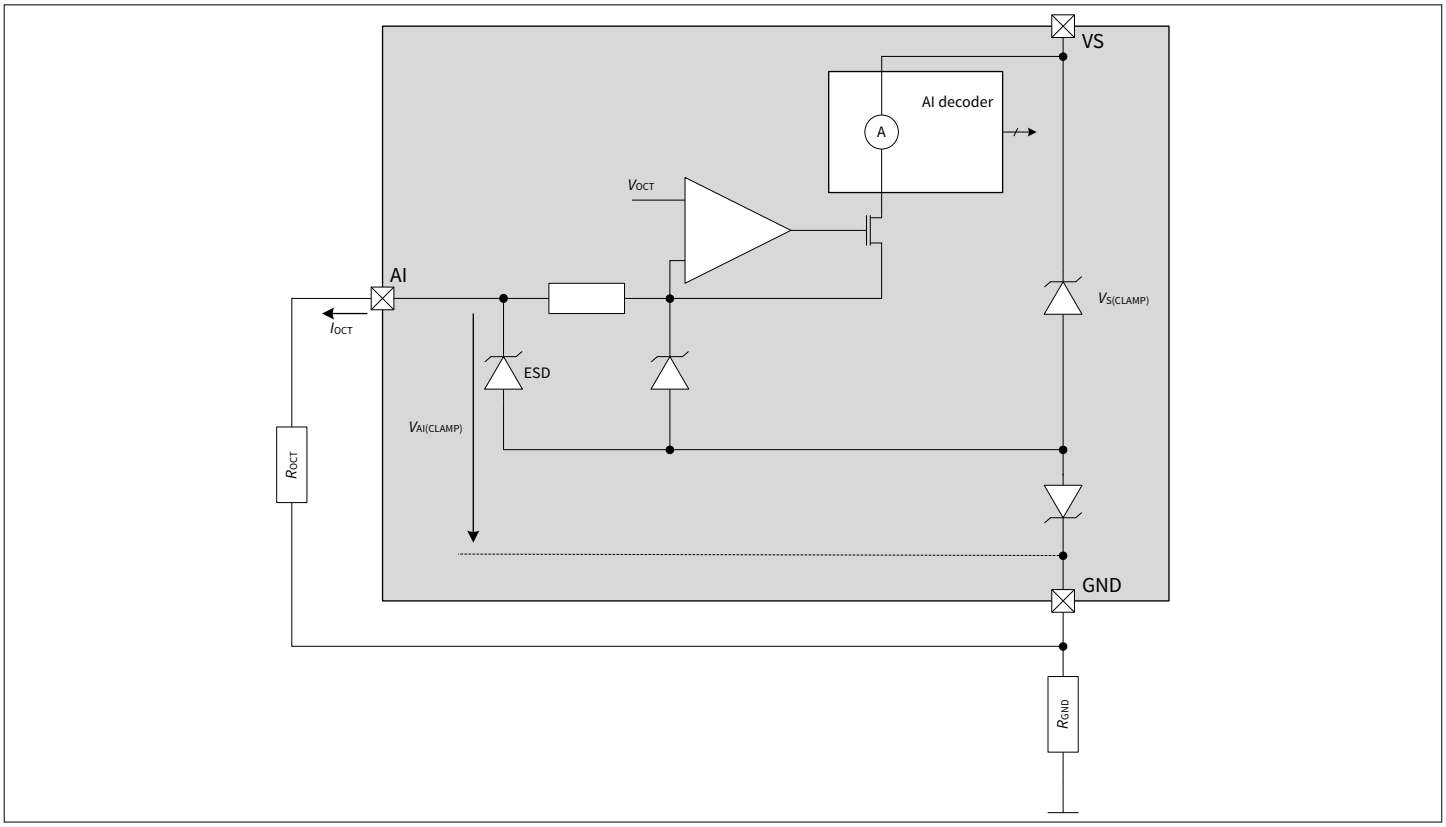


Figure 13 Adjustable overcurrent threshold pin circuitry

4.3 Electrical characteristics I/O pins

V_S = 4 V to 20 V, T_J = -40°C to +150°C

Unless otherwise specified typical values: V_S = 13.5 V, T_J = 25°C

Digital input (DI) pins = INn, DEN, DSEL

Analog input (AI) pins = OCT

Table 5 Electrical characteristics I/O pins

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DI pins							
Digital input voltage threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See Figure 11 and Figure 12	PRQ-76
Digital input clamping voltage	$V_{DI(CLAMP1)}$	–	7	–	V	1) I_{DI} = 1 mA See Figure 11 and Figure 12	PRQ-77
Digital input clamping voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	I_{DI} = 2 mA See Figure 11 and Figure 12	PRQ-78
Digital input hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	1) See Figure 11 and Figure 12	PRQ-80
Digital input current ("high")	$I_{DI(H)}$	2	10	25	µA	V_{DI} = 2 V See Figure 11 and Figure 12	PRQ-81
Digital input current ("low")	$I_{DI(L)}$	2	10	25	µA	V_{DI} = 0.8 V See Figure 11 and Figure 12	PRQ-82
AI pins							
Analog input clamping voltage	$V_{AI(CLAMP1)}$	–	7	–	V	1) I_{OCT} = 1 mA See Figure 13	PRQ-88
Analog input clamping voltage	$V_{AI(CLAMP2)}$	6.5	7.5	8.5	V	I_{OCT} = 2 mA See Figure 13	PRQ-630
Analog overcurrent voltage threshold	V_{OCT}	0.44	0.5	0.56	V	1) $I_{OCT,MIN} \le I_{OCT} \le I_{OCT,MAX}$ INn = "high" or DEN = "high"	PRQ-628
Analog linear overcurrent range	I_{OCT}	20	–	228	µA	1) INn = "high" or DEN = "high"	PRQ-89
OCT short to device ground detection current	$I_{OCT(SHORT2GND)}$	320	–	–	µA	2) DEN = "high" INn = "low"	PRQ-91

(table continues...)

Table 5 (continued) Electrical characteristics I/O pins

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCT open detection current	$I_{OCT(OPEN)}$	–	–	5	µA	2) DEN = "high" INn = "low"	PRQ-619

1) Not subject to production test - specified by design
2) Functional test only

5 Power Supply

The device is supplied by VS, which is used to supply the internal logic as well as to supply the power output stages. In case of an undervoltage condition, the device has an detection circuit, which prevents the activation of the power output stage as well as the diagnosis.

5.1 Operation modes and transitions

5.1.1 Operation modes

The device has the following operation modes:

- Sleep
- Inactive with diagnosis
- Active with diagnosis
- Active without diagnosis
- Capacitive load switching mode with diagnosis
- Capacitive load switching mode without diagnosis

The transition between operation modes is determined according to these variables:

- Logic level at INn pins
- PWM signal at INn pins
- Logic level at DEN pin

The state diagram including the possible transitions is shown in Figure 14. The behavior of the device as well as some parameters may change independent from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S supply voltage, some changes within the same operation mode can be seen accordingly.

Table 6 shows the correlation between operation modes, V_S supply voltage, and the state of the most important functions (channel status).

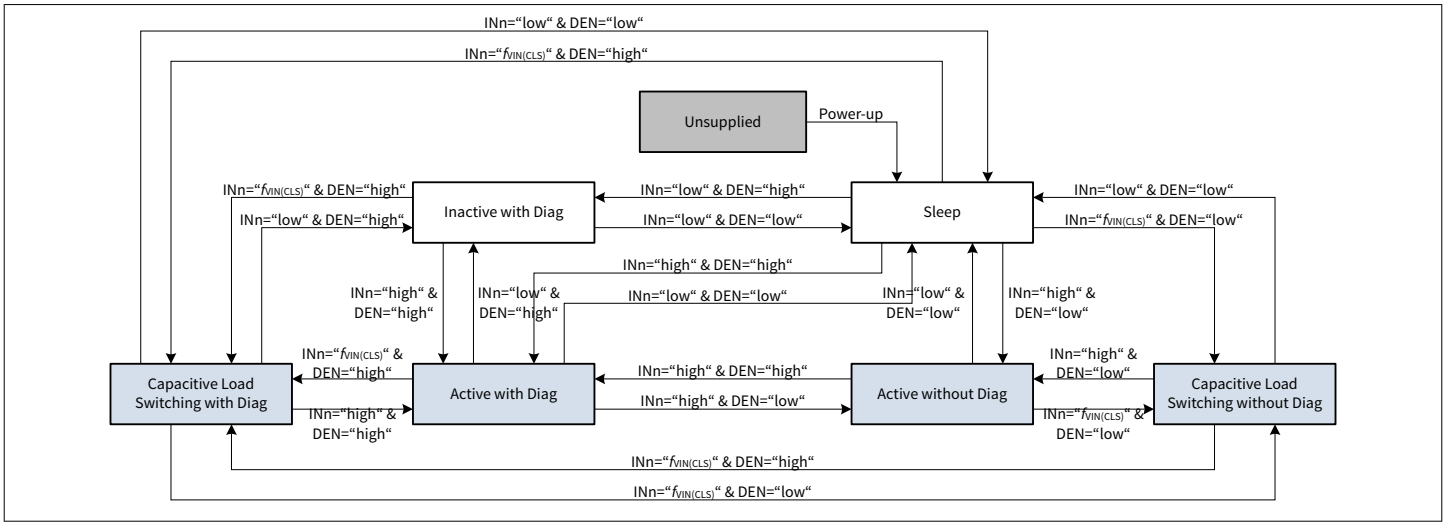


Figure 14 Operation mode state diagram

Table 6 Operation mode, device function and VS voltage

Operation mode	Function	$V_S > V_{S(OP)}$	$V_S < V_{S(OP)}$
Sleep	Channels	OFF	OFF
	Diagnosis	OFF	OFF

(table continues...)

Table 6 (continued) Operation mode, device function and VS voltage

Operation mode	Function	$V_S > V_{S(OP)}$	$V_S < V_{S(OP)}$
Inactive with diagnosis	Channels	OFF	OFF
	Diagnosis	ON	OFF
Active with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Active without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF
Capacitive load switching mode with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Capacitive load switching mode without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF

5.1.1.1 Unsupplied

In this state the device supply voltage is below the undervoltage threshold $V_{S(UV)}$.

5.1.1.2 Power-up

The power-up transition is entered when the supply voltage (V_S) is applied to the device. The supply rises until it exceeds the undervoltage threshold $V_{S(OP)}$.

5.1.1.3 Sleep

The device is in sleep mode when digital input (DI) pins are set to "low". While in sleep mode the current consumption is at $I_{VS(SLEEP)}$. Overtemperature, overload protection and undervoltage mechanism are disabled. The device can go in sleep mode only if the protection is not active ($n_{RESTART(CR)} = 0$, $T_J < T_{J(ABS)}$ and (T_J - $T_{J(REF)}$) < $T_{J(DYN)}$ (including hysteresis)), see Chapter 7.3.

5.1.1.4 Inactive with diagnosis

The device is in inactive with diagnosis mode while DEN pin is set to “high” and input pins are set to “low”. The channels are OFF, therefore open load in OFF diagnosis is possible. Depending on the load condition, either a fault current $I_{IS(FAULT)}$ or an open load in OFF current $I_{IS(OLOFF)}$ may be present at IS pin. During such condition, the current consumption of the device is increased.

5.1.1.5 Active with diagnosis

Active with diagnosis mode is the normal operation mode of of the device. The device enters active with diagnosis mode for the related channel when INn = "high" and DEN = "high", in this condition one or more outputs are switched ON with diagnosis. Device current consumption is specified by parameter $I_{GND(ACTIVE)}$.

5.1.1.6 Active without diagnosis

The device is in active without diagnosis mode when INn = "high" and DEN = "low", in this condition, one or more outputs are switched ON without diagnosis.

5.1.1.7 Capacitive load switching mode with diagnosis

The device has a capacitive load switching mode implemented to drive capacitive loads. The capacitive load switching mode with diagnosis can be activated with INn = "$f_{VIN(CLS)}$" and DEN = "high", in this condition one or more outputs are switched ON with diagnosis. Device current consumption is specified by parameter $I_{GND(ACTIVE)}$.

5.1.1.8 Capacitive load switching mode without diagnosis

The device is in capacitive load switching mode without diagnosis when INn = "$f_{VIN(CLS)}$" and DEN = "low", in this condition, one or more outputs are switched ON without diagnosis.

5.2 Undervoltage on VS

Between $V_{S(OP)}$ and $V_{S(UV)}$ the undervoltage mechanism is triggered.

The power output stage follows the input logic as long as $V_S > V_{S(OP)}$.

If the device is Active or in Capacitive Load Switching Mode, with or without Diagnosis and the supply voltage V_S drops below the undervoltage threshold $V_{S(UV)}$, the internal logic switches OFF the output channel.

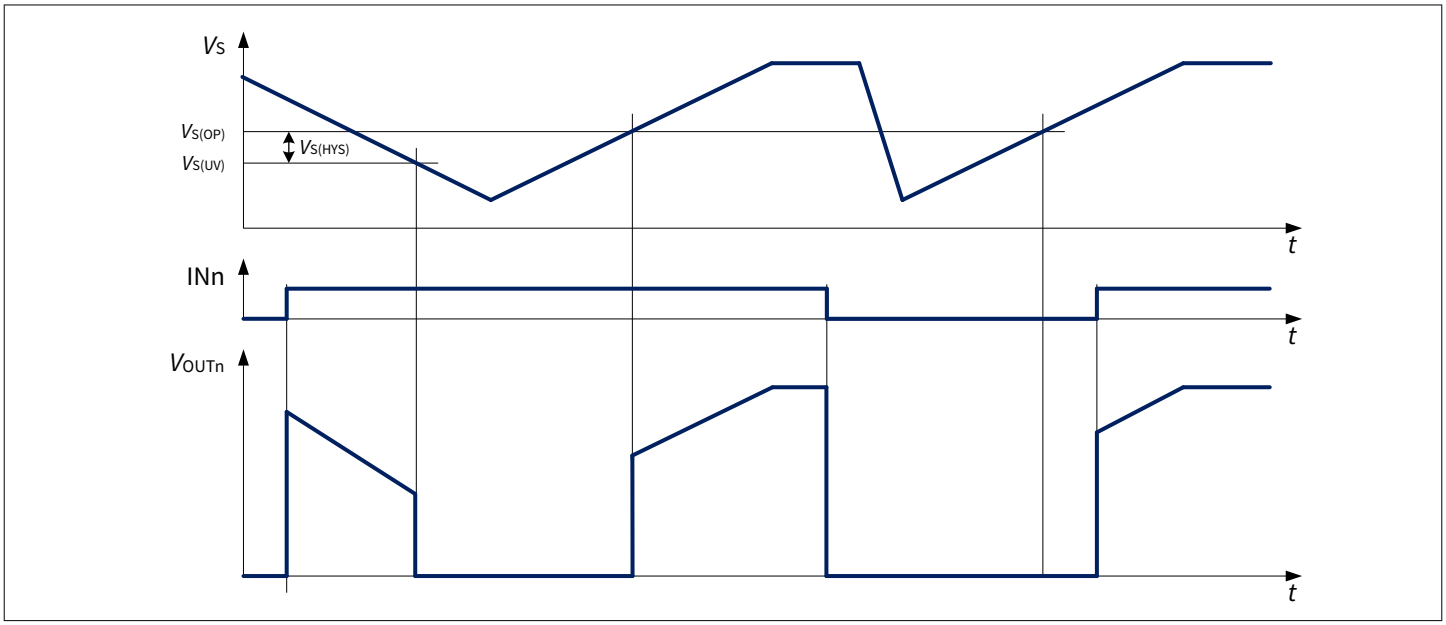


Figure 15 V_S undervoltage behavior

5.3 Electrical characteristics power supply

V_S = 4 V to 20 V, T_J = -40°C to +150°C

Unless otherwise specified typical values: V_S = 13.5 V, T_J = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTG7050-2EPL: R_L = 4.7 Ω

Table 7 Electrical characteristics power supply

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VS pin							
Power supply undervoltage shutdown	$V_{S(UV)}$	1.8	2.2	2.7	V	V_S decreasing INn = “high” From 0 ≤ V_{DS} ≤ 0.5 V to V_{DS} ~ V_S See Figure 15	PRQ-98

(table continues...)

Table 7 (continued) Electrical characteristics power supply

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply minimum operating voltage	$V_{S(OP)}$	2.1	2.5	3	V	V_S increasing INn = “high” From $V_{DS} \sim V_S$ to $0 \le V_{DS} \le 0.5$ V See Figure 15	PRQ-99
Power supply undervoltage shutdown hysteresis	$V_{S(HYS)}$	–	0.3	–	V	1) $V_{S(OP)}$ - $V_{S(UV)}$ See Figure 15	PRQ-100
Breakdown voltage between GND and VS pins in reverse battery	$-V_{S(REV)}$	16	–	30	V	1) $I_{GND(REV)}$ = 7 mA T_J = 150°C	PRQ-101
Power supply current consumption in sleep mode with loads at TJ ≤ 85°C	$I_{VS(SLEEP)\_85}$	–	0.03	0.5	µA	1) V_S = 20 V V_{OUT} = 0 V INn = DEN = DSEL = “low” $T_J \le 85$°C	PRQ-610
Power supply current consumption in sleep mode with loads at TJ = 150°C	$I_{VS(SLEEP)\_150}$	–	3.5	14	µA	V_S = 20 V V_{OUT} = 0 V INn = DEN = DSEL = “low” T_J = 150°C	PRQ-611
Operating current in active with diagnosis mode	$I_{GND(ACTIVE)}$	–	3.7	4.5	mA	V_S = 20 V INn = DEN = DSEL = “high”	PRQ-612
Operating current in inactive with diagnosis mode	$I_{GND(INACTIVE)}$	–	1.8	2.2	mA	V_S = 20 V INn = "low" DEN = DSEL = “high” $I_{OCT} = I_{OCT,MAX}$	PRQ-613

1) Not subject to production test - specified by design

6 Power Stage

The high-side power stages are built using a N-channel vertical power MOSFET with charge pump.

6.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J. Figure 16, shows the variation of $R_{DS(ON)}$ across the whole T_J range. The value “2” on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at T_J = 150°C.

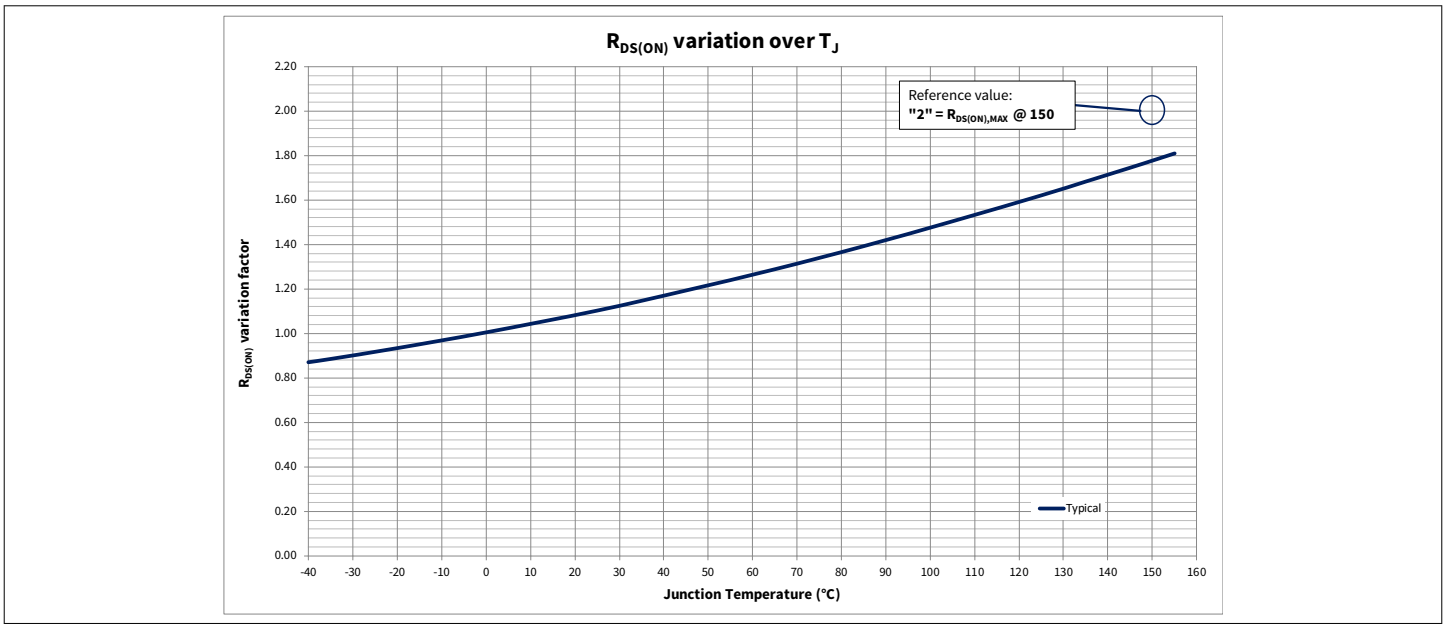


Figure 16 $R_{DS(ON)}$ variation factor

The behavior in reverse polarity is described in Chapter 7.4.1.

6.2 Switching loads

6.2.1 Switching resistive loads

When switching resistive loads, the switching times and slew rates shown in Figure 17 can be considered. The switching energy values E_{ON} and E_{OFF} are proportional to load resistance and times t_{ON} and t_{OFF}.

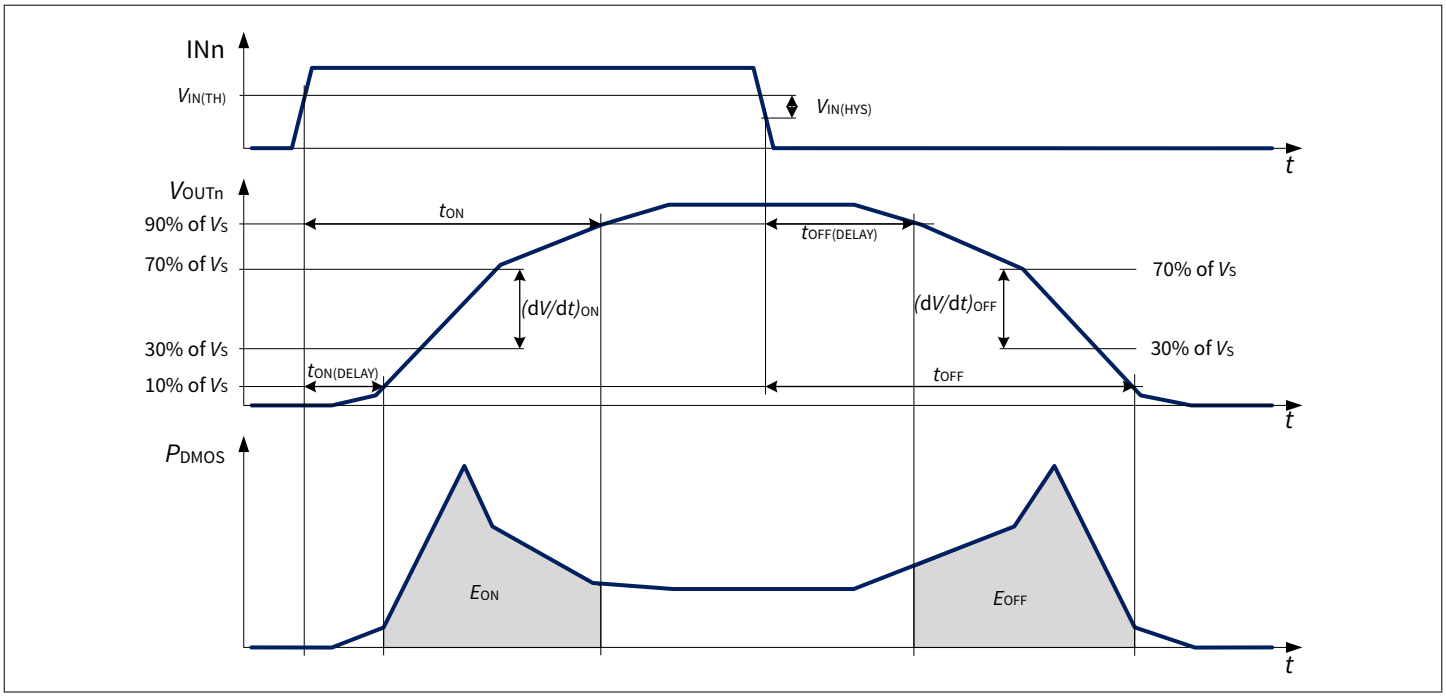


Figure 17 Switching a resistive load

6.2.2 Switching inductive loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the output voltage so that $V_{DS} \leq V_{DS(CLAMP)}$. Chapter 6.2.2 shows a concept drawing of the implementation.

The clamping structure is active in all operation modes listed in Chapter 5.1.

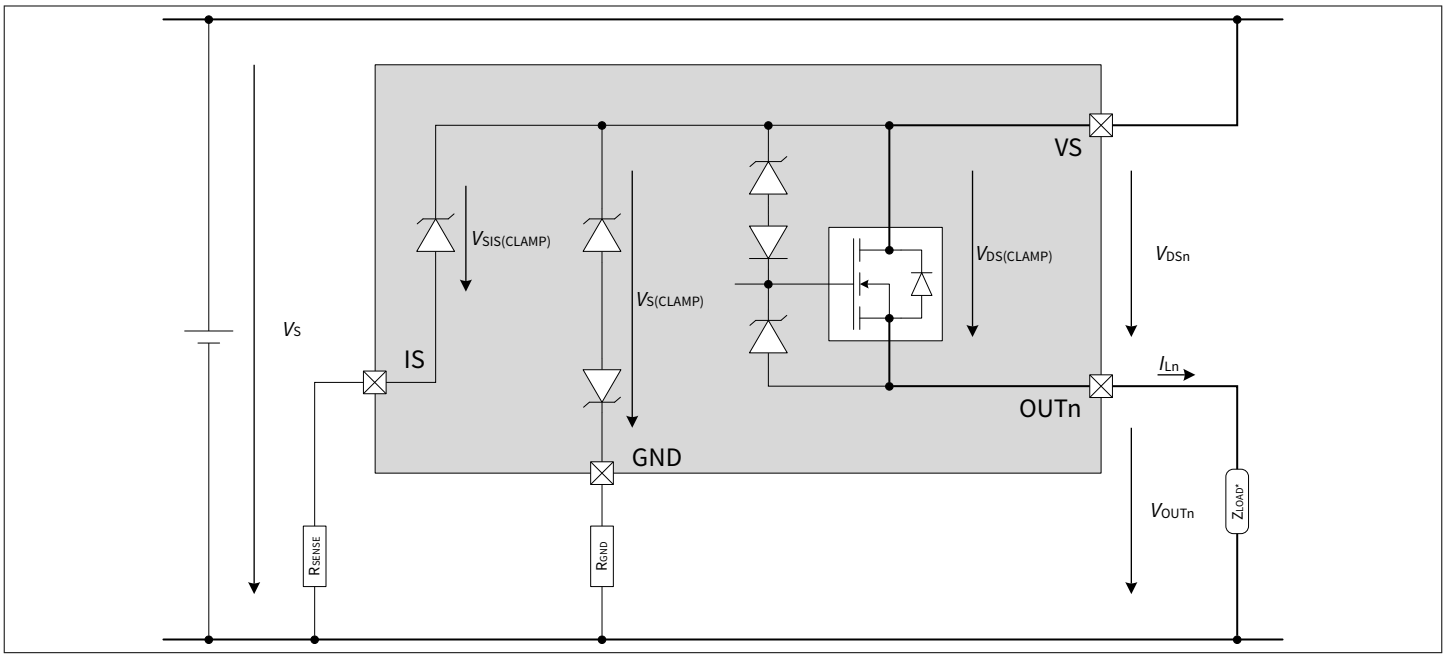


Figure 18 Output clamping concept

During demagnetization of inductive loads, energy has to be dissipated in the device. The energy can be calculated with:

$$E = V_{DS(CLAMP)} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}}\right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

The maximum energy the device can sustain is limited by the thermal design. Please refer to Table 2 for the maximum allowed values of E_{AS} (single pulse energy) and E_{AR} (repetitive energy).

6.2.3 Switching capacitive loads

When $f_{VIN(CLS)}$ is applied the device enters CLS mode after $t_{ON\_CLS(DELAY)}$ as shown in Figure 19. A pumping mode is applied to charge the capacitor while the overcurrent limitation is active using the overcurrent limitation setting as set by the OCT pin, as shown in Figure 20. During CLS mode, protection and diagnosis functions are active.

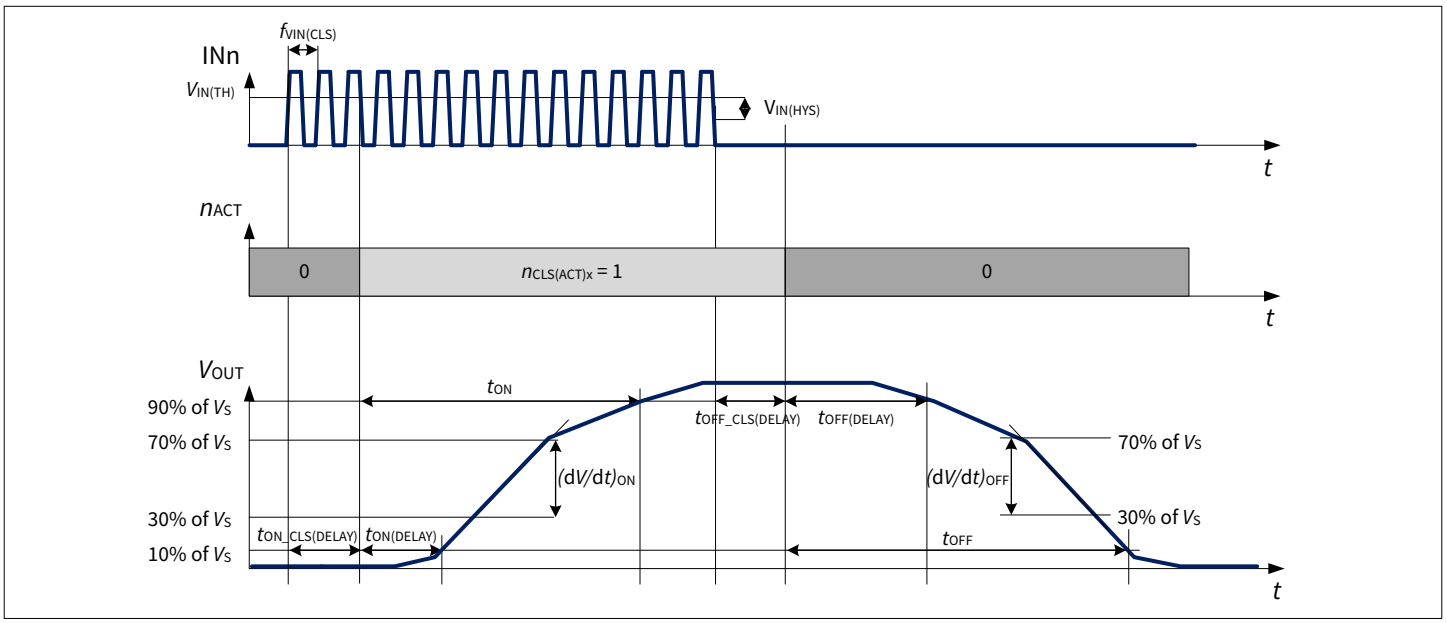


Figure 19 Switching a capacitive load

When the device is in CLS mode, the dynamic overtemperature protection is reduced to $T_{J(DYN)\_CLS}$ with continuous restart.

A transition from CLS mode to Active mode is performed automatically when $V_{DS} \leq V_{DS(OLOFF)}$.

On the contrary, when $V_{DS} > V_{DS(OLOFF)}$, the CLS mode has to be left after a maximum time of t_{CLSx} by setting input to "low" or "high".

A transition from capacitive load switching mode to active mode shall be performed only if there is no short circuit at the output. To distinguish between short circuit and normal load, a current sense measurement must be performed before leaving. If the current measurement delivers an expected value, the transition from CLS mode to active mode may be performed. If the current measurement delivers an open load value (no output current), it has to be assumed that there is either an open load or a short circuit at the output. Additionally, a short circuit condition could be excluded by an external voltage measurement at the output.

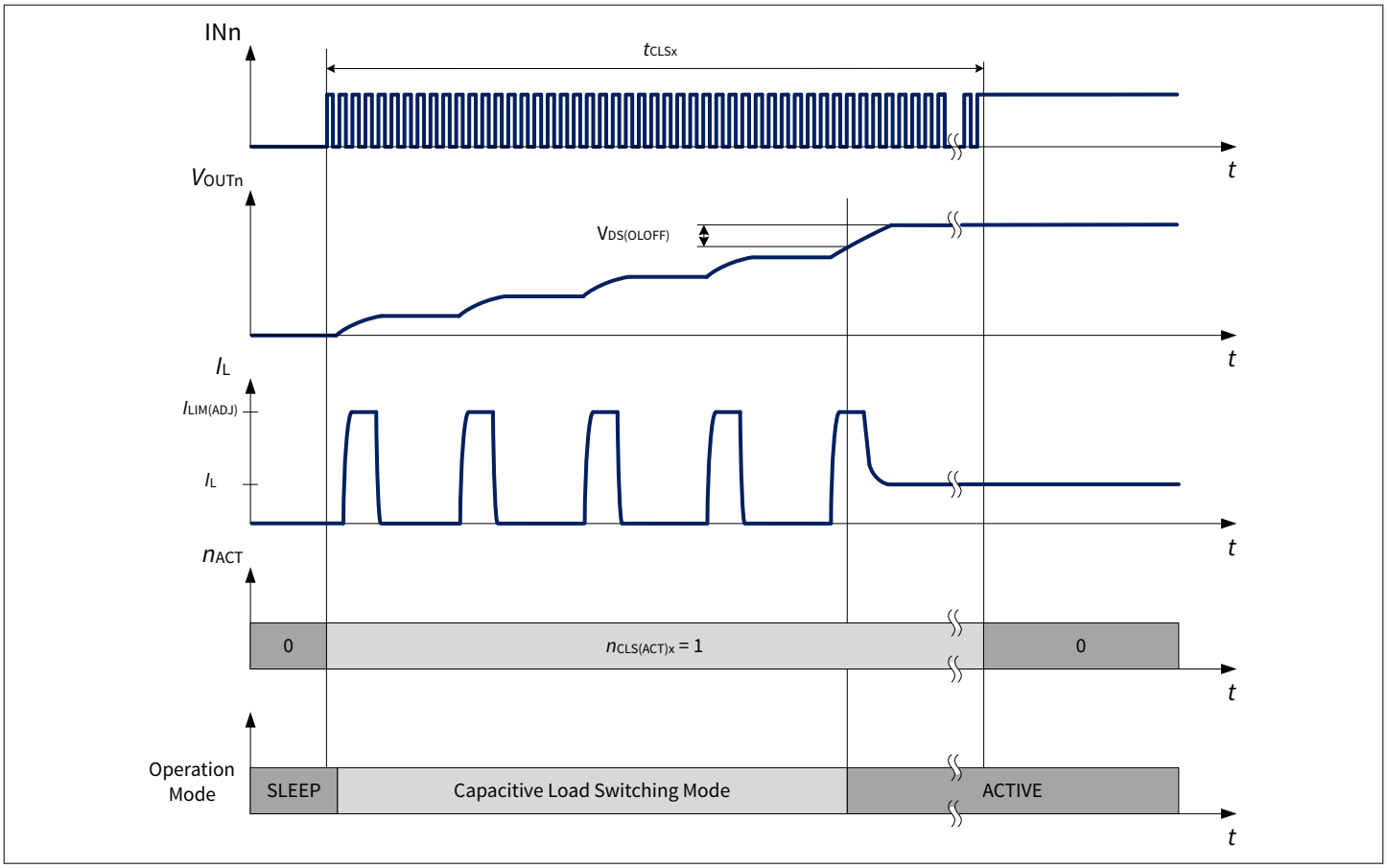


Figure 20 Capacitive load switching activations

6.3 Advanced switching characteristics

6.3.1 Inverse current behavior

When $V_{OUT} > V_S$, a current $I_{L(INV)}$ flows into the power output transistor (see Figure 21). This condition is known as "Inverse Current".

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses, therefore, an increase of overall device temperature. This may lead to a switch OFF of unaffected channels due to overtemperature. If the channel is in ON state, $R_{DS(INV)}$ can be expected and power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

During inverse current condition, the channel remains in ON or OFF state as long as $|-I_L| < |-I_{L(INV)}|$.

The feature of InverseON allows to switch ON the channel during Inverse Current condition as long as $|-I_L| < |-I_{L(INV)}|$, see Figure 22.

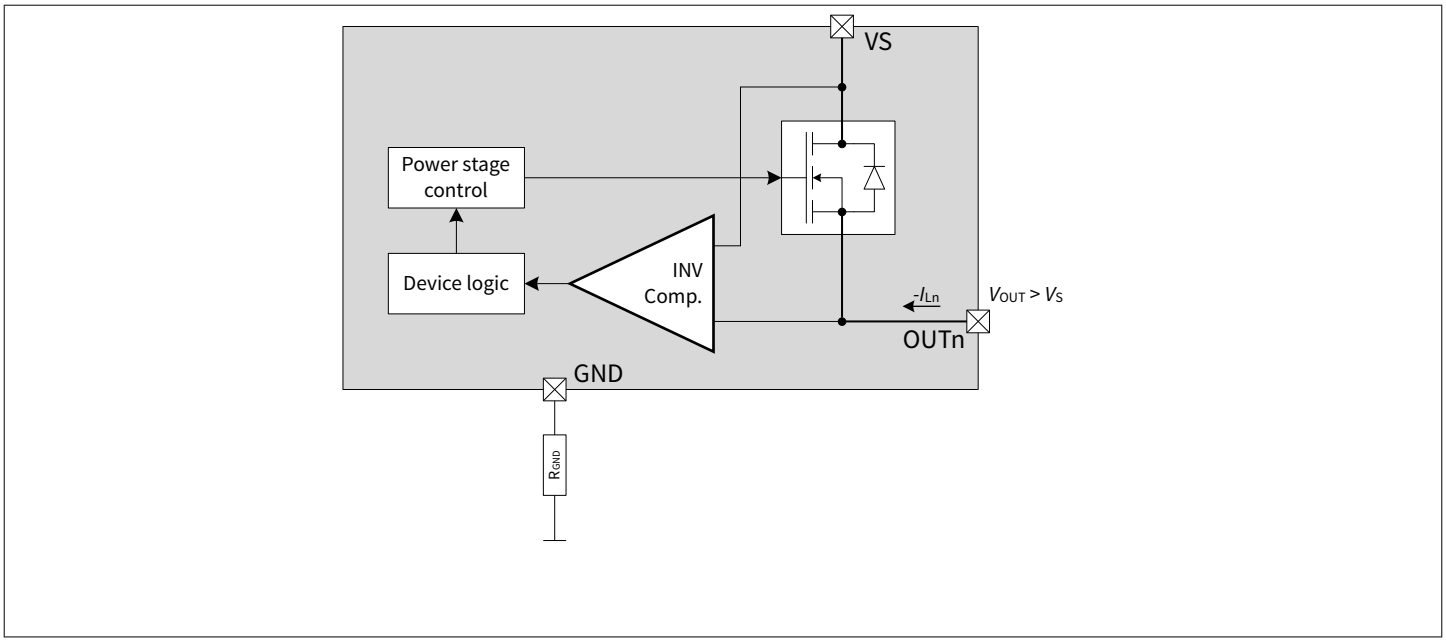


Figure 21 Inverse current circuitry

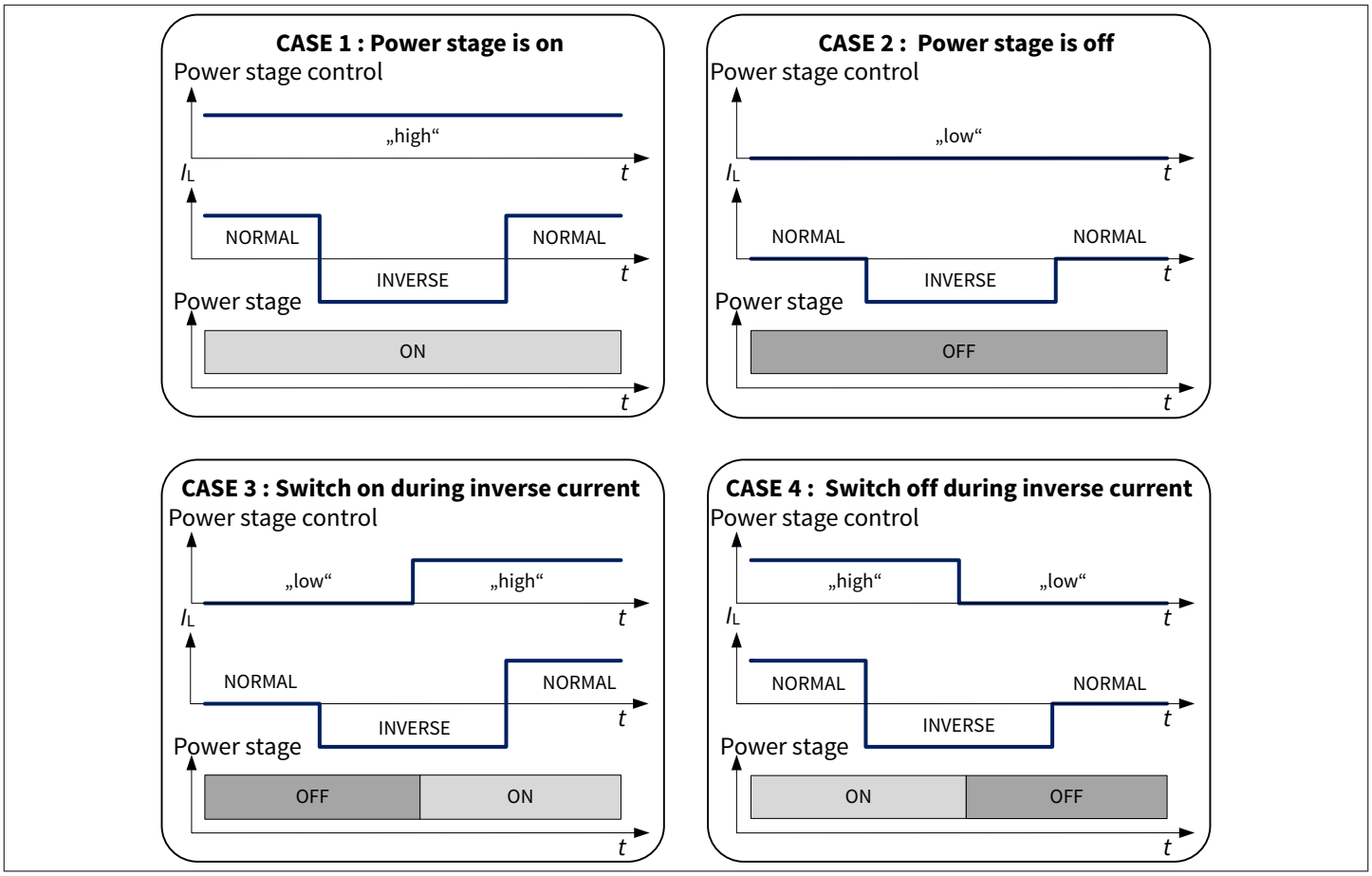


Figure 22 InverseON - Channel behavior in case of applied inverse current

6.4 Electrical characteristics power stage

V_S = 4 V to 20 V, T_J = -40°C to +150°C

Unless otherwise specified typical values: V_S = 13.5 V, T_J = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):
BTG7050-2EPL: R_L = 4.7 Ω

Table 8 Electrical characteristics power stage

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Drain to source clamping voltage at TJ = -40°C	$V_{DS(CLAMP)\_-40}$	33	36.5	42	V	I_L = 5 mA T_J = -40°C See Chapter 6.2.2	PRQ-110
Drain to source clamping voltage at TJ ≥ 25°C	$V_{DS(CLAMP)\_25}$	35	38	44	V	1) I_L = 5 mA T_J ≥ 25°C See Chapter 6.2.2	PRQ-111
Timings							
Switch-ON delay	$t_{ON(DELAY)}$	10	70	130	µs	V_S = 13.5 V V_{OUT} = 10% V_S I_{OCT} = $I_{OCT,MAX}$ See Figure 17	PRQ-112
Switch-OFF delay	$t_{OFF(DELAY)}$	10	50	160	µs	V_S = 13.5 V V_{OUT} = 90% V_S I_{OCT} = $I_{OCT,MAX}$ See Figure 17	PRQ-113
Switch-ON time	t_{ON}	50	130	210	µs	V_S = 13.5 V V_{OUT} = 90% V_S I_{OCT} = $I_{OCT,MAX}$ See Figure 17	PRQ-114
Switch-OFF time	t_{OFF}	30	100	220	µs	V_S = 13.5 V V_{OUT} = 10% V_S I_{OCT} = $I_{OCT,MAX}$ See Figure 17	PRQ-115
CLS activation delay	$t_{ON\_CLS(DELAY)}$	10	70	200	µs	V_S = 13.5 V I_{OCT} = $I_{OCT,MAX}$ See Figure 19	PRQ-664
CLS de-activation delay	$t_{OFF\_CLS(DELAY)}$	20	40	90	µs	V_S = 13.5 V I_{OCT} = $I_{OCT,MAX}$ See Figure 19	PRQ-665
Switch-ON/OFF Matching - tON - tOFF	Δt_{SW}	-60	25	90	µs	V_S = 13.5V I_{OCT} = $I_{OCT,MAX}$	PRQ-116

(table continues...)

Table 8 (continued) Electrical characteristics power stage

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage slope							
Switch-ON slew rate	$(dV/dt)_{ON}$	0.16	0.27	0.39	V/µs	V_S = 13.5 V $I_{OCT} = I_{OCT,MAX}$ V_{OUT} = 30% to 70% of V_S	PRQ-117
Switch-OFF slew rate	$(dV/dt)_{OFF}$	-0.39	-0.27	-0.16	V/µs	V_S = 13.5V $I_{OCT} = I_{OCT,MAX}$ V_{OUT} = 70% to 30% of V_S	PRQ-118
Slew rate matching - (dV/dt)ON + (dV/dt)OFF	$\Delta(dV/dt)_{SW}$	-0.15	0	0.15	V/µs	V_S = 13.5V $I_{OCT} = I_{OCT,MAX}$	PRQ-119
CLS mode							
Input frequency for capacitive load switching mode activation	$f_{VIN(CLS)}$	22	30	38	kHz	2) $DC_{VIN(CLS)}$ = 50%	PRQ-353
Duty cycle for capacitive load switching mode activation	$DC_{VIN(CLS)}$	30%	50%	70%	–	2) $f_{VIN(CLS)}$ = 30 kHz	PRQ-354
Maximum time in CLS mode	t_{CLS1}	–	–	25	ms	2) See Chapter 6.2.3	PRQ-355
Maximum time in CLS mode	t_{CLS2}	–	–	90	ms	2) See Chapter 6.2.3	PRQ-813
Maximum number of CLS mode activations	n_{CLS_ACT1}	–	–	500	kcycles	2) See Chapter 6.2.3	PRQ-812
Maximum number of CLS mode activations	n_{CLS_ACT2}	–	–	50	kcycles	2) See Chapter 6.2.3	PRQ-814
Output characteristics							
ON-state resistance at TJ = 25°C	$R_{DS(ON)\_25}$	–	50	–	mΩ	2) T_J = 25°C	PRQ-542
ON-state resistance at TJ = 150°C	$R_{DS(ON)\_150}$	–	–	100	mΩ	T_J = 150°C I_L = 2 A	PRQ-543
ON-state resistance in cranking at TJ = 150°C	$R_{DS(ON)\_CRANK\_150}$	–	–	110	mΩ	T_J = 150°C V_S = 3.1 V I_L = 1 A	PRQ-544

(table continues...)

Table 8 (continued) Electrical characteristics power stage

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ON-state resistance in inverse current at TJ = 25°C	$R_{DS(INV)\_25}$	–	50	–	mΩ	2) T_J = 25°C V_S = 13.5 V I_L = -2 A See Figure 21	PRQ-545
ON-state resistance in inverse current at TJ = 150°C	$R_{DS(INV)\_150}$	–	–	110	mΩ	T_J = 150°C V_S = 13.5 V I_L = -2 A See Figure 21	PRQ-546
Nominal load current per channel (all channels active) at TA = 85°C	$I_{L(NOM)\_85}$	–	3	–	A	2) T_A = 85°C $T_J \leq$ 150°C	PRQ-547
Output leakage current at TJ ≤ 85°C	$I_{L(OFF)\_85}$	–	0.01	0.5	µA	2) V_{OUT} = 0 V INn = "low" $T_A \leq$ 85°C	PRQ-548
Output leakage current at TJ = 150°C	$I_{L(OFF)\_150}$	–	1.2	4	µA	V_{OUT} = 0 V INn = "low" T_A = 150°C	PRQ-549
Inverse current capability	$I_{L(INV)}$	–	3	–	A	2) $V_S < V_{OUT}$ INn = "high" See Figure 21	PRQ-550
Voltages							
Drain source diode voltage	$\lvert V_{DS(DIODE)} \rvert$	–	550	700	mV	I_L = -190 mA T_J = 150°C	PRQ-552
Switch-ON energy	E_{ON}	–	1.2	–	mJ	1) V_S = 20V See Figure 17	PRQ-553
Switch-OFF energy	E_{OFF}	–	1.25	–	mJ	1) V_S = 20V See Figure 17	PRQ-554

1) Tested at T_J = 150°C
2) Not subject to production test - specified by design

7 Protection

The device is protected against overload, overtemperature and overvoltage.

Overtemperature and overload protection are operational in all operation modes, except when in sleep mode.

Overload protection is not active during inverse current condition.

Overtemperature and overload protection during inverse current condition is inactive on the channel which is in inverse condition.

Overvoltage protection is active in all operation modes.

7.1 Overcurrent protection

7.1.1 Adjustable overcurrent threshold

The device is protected in case of overload and short circuit to ground.

The device offers an adjustable overcurrent limitation range from $I_{LIM,MIN}$ to $I_{LIM,MAX}$. This feature offers protection against overstress for the load as well as for the power output stage. In case of DMOS temperature increase exceeding the device safe operating environment, overtemperature and dynamic temperature protection mechanism will be triggered as shown in Figure 24 and Figure 25.

For the adjustment of the current limitation for both output channels, the following equation can be considered:

$$I_{LIM} = (k_{ILIOCT} \cdot I_{OCT}) + \Delta I_{LIM} \quad where, \quad I_{OCT} = \frac{(I_{LIM} - \Delta I_{LIM})}{k_{ILIOCT}} \tag{2}$$

To select the proper resistor value R_{OCT} connected between the OCT pin and device ground, the following equation can be considered:

$$R_{OCT} = \frac{(V_{OCT} \cdot k_{ILIOCT})}{(I_{LIM} - \Delta I_{LIM})} \tag{3}$$

In case of an OCT pin open with the current not exceeding $I_{OCT(OPEN)}$ the device will set the current limit value to $I_{LIMOCT(OPEN)}$. In case of an OCT pin short to ground with the current exceeding $I_{OCT(SHORT2GND)}$ the device will set the current limit value to $I_{LIMOCT(SHORT2GND)}$. The behavior of how I_{OCT} is related to I_{LIM} is described in Figure 23. However, due to the maximum rating of the allowed current through OCT pin I_{OCT}, it is not recommended to shorten the OCT pin to device GND. In the case of reverse battery condition, this could lead to violations of the maximum ratings, therefore $I_{AI(REV)}$ needs to be considered.

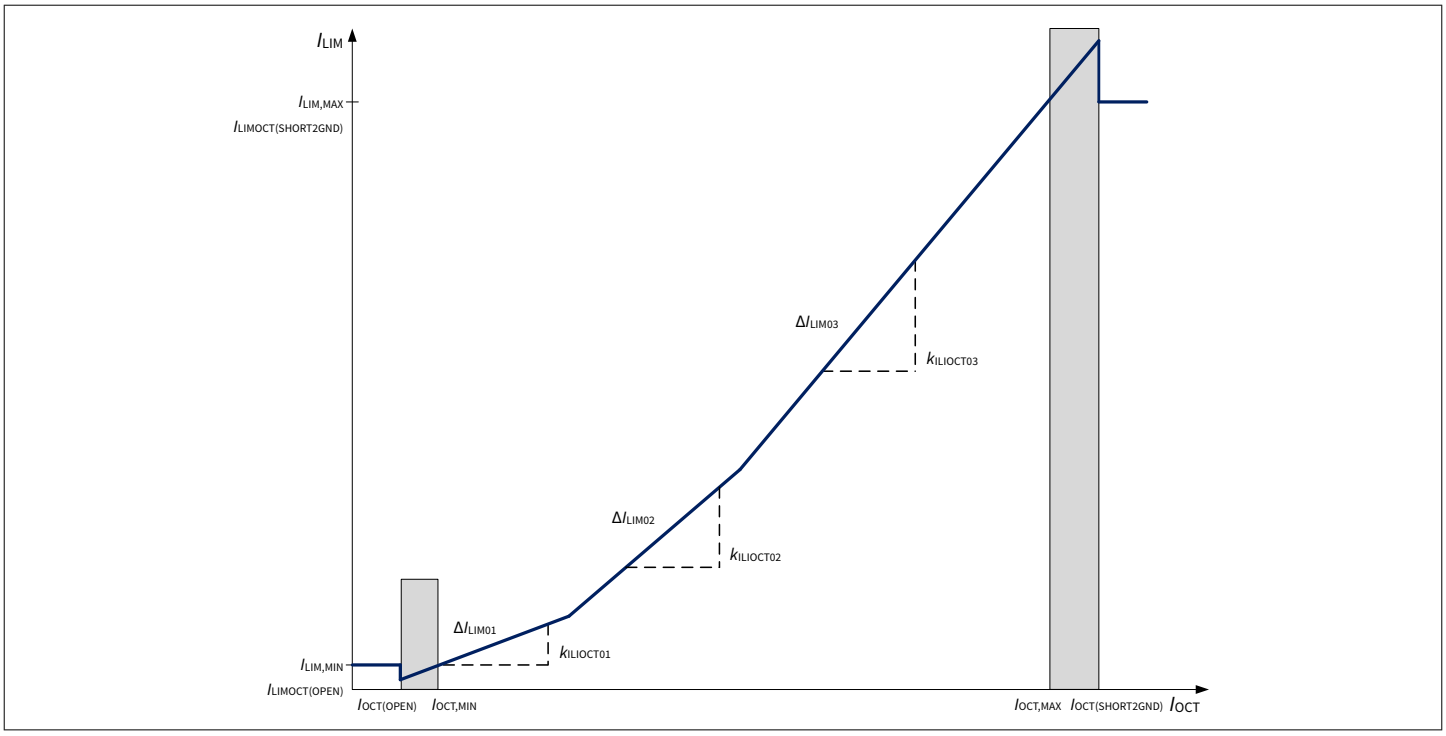


Figure 23 Adjustable overcurrent limitation behavior

7.2 Overtemperature protection

The device incorporates both an absolute ($T_{J(ABS)}$) and a dynamic ($T_{J(DYN)}$) temperature protection circuitry for each channel.

An increase in junction temperature T_J above either one of the two thresholds ($T_{J(ABS)}$ or $T_{J(DYN)}$) switches OFF the overheated channel. The affected channel will perform automatic restart attempts. The channel remains switched OFF until the junction temperature has reached the restart condition described in Table 9 according to Chapter 7.3.1. If the number of automatic restart attempts exceeds $n_{RESTART(CR),TYP}$, the affected channel latches OFF to prevent destruction. The behavior is shown in Figure 24 and Figure 25. $T_{J(REF)}$ is the reference temperature used for dynamic temperature protection.

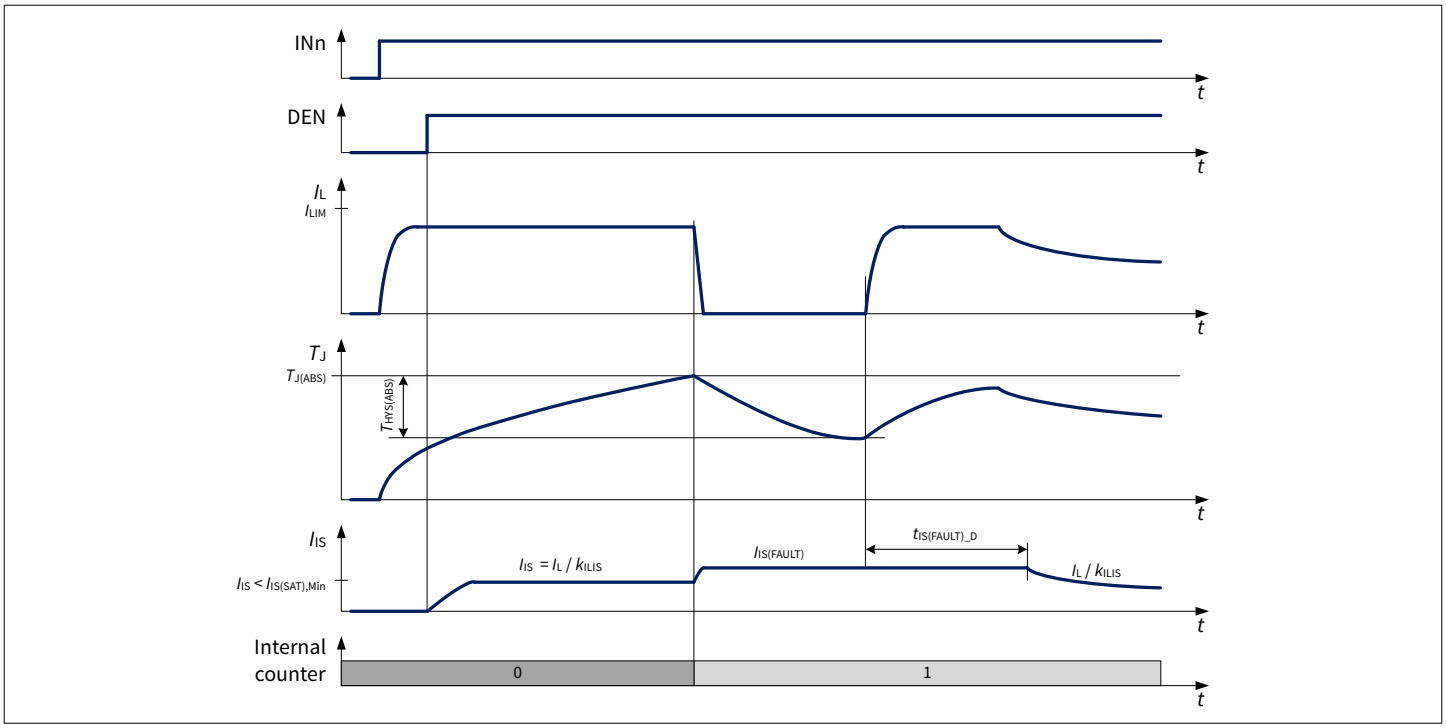


Figure 24 Overtemperature protection (absolute)

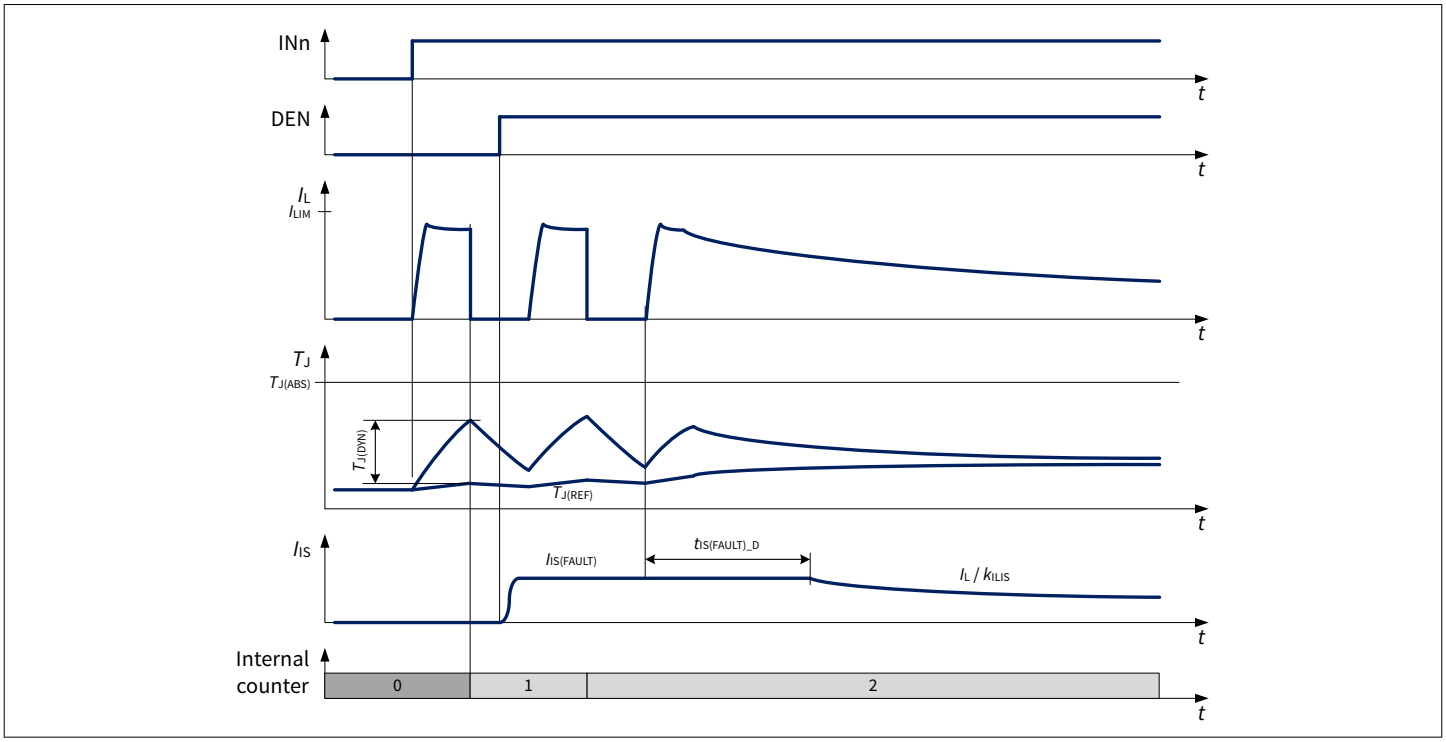


Figure 25 Overtemperature protection (dynamic)

When the overtemperature protection circuitry allows the channel to be switched ON again, the retry strategy described in Chapter 7.3 is followed.

7.3 Protection and diagnosis in case of fault

Any event that triggers overtemperature protection has two consequences:

- The affected channel switches OFF according to Chapter 7.3.1.
- If the diagnosis is active for the affected channel, a current $I_{IS(FAULT)}$ is provided by IS pin (see Chapter 8.2.2 for further details).

The channel can be switched ON again if all the protection mechanisms fulfill the “restart” conditions described in Table 9 and $n_{RESTART(CR)} < n_{RESTART(CR),typ}$.

Table 9 Protection "restart" condition

Fault condition	Switch OFF event	"Restart" condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)

7.3.1 Retry strategy

When INn is set to “high”, the related power output stage is switched ON. If a fault condition is detected the power output stage is switched OFF. The device will apply the restart strategy and return to normal operation or latches OFF if the fault remains to be present after $n_{RESTART(CR),TYP}$.

The device has an internal retry counter $n_{RESTART(CR)}$ (one for each channel) to maximize the robustness in case of fault.

The channel is allowed to switch ON for $n_{RESTART(CR)}$ times before switching OFF. After $n_{RESTART(CR),TYP}$ consecutive “restart” cycles, the channel latches OFF. To de-latch the power output stage and reset the internal counter it is necessary to set the input pin to “low” for a time longer than $t_{DELAY(CR)}$.

If the fault is no longer present and $t_{DELAY(CR)}$ is observed the device will enter normal operation. In case the fault is still present, the device will trigger again the retry strategy.

The retry strategy is shown in Figure 26.

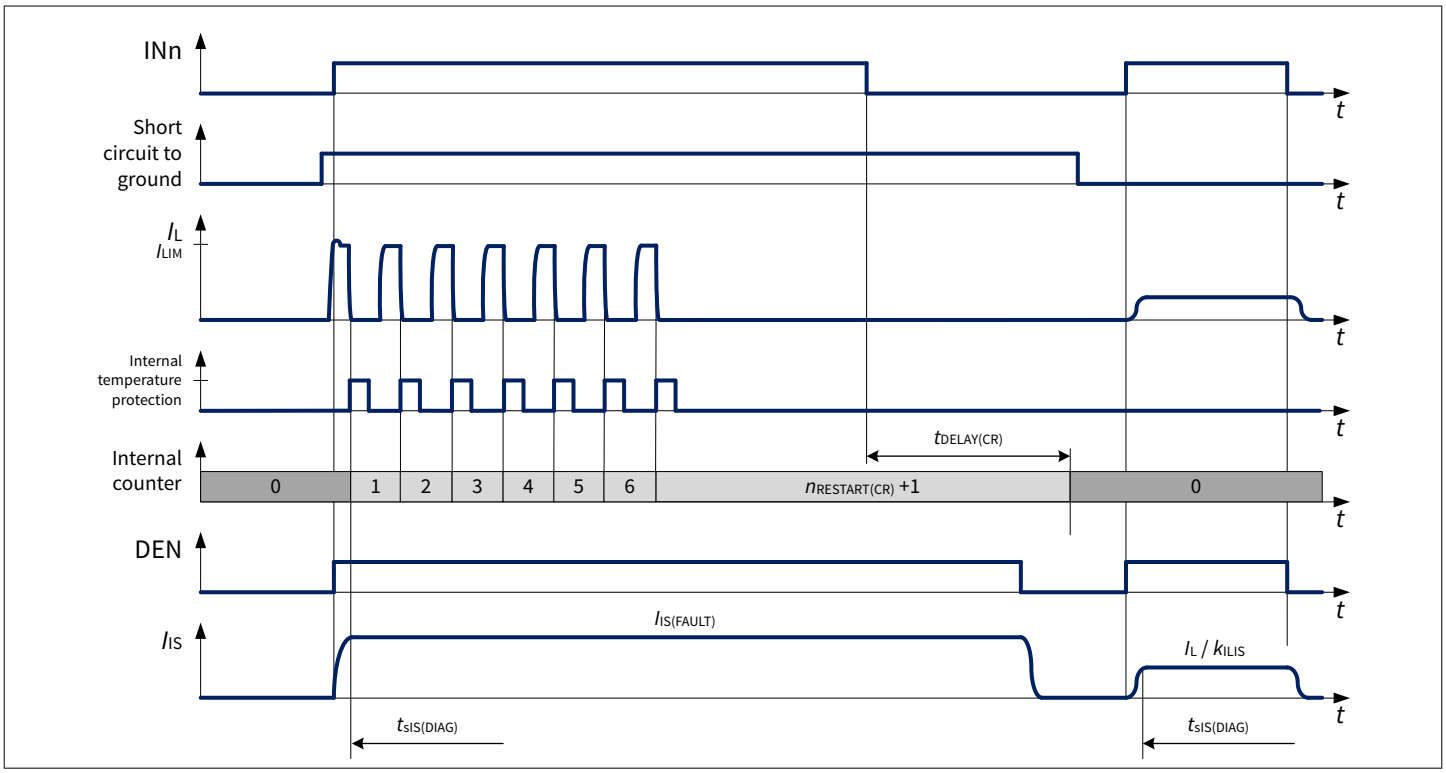


Figure 26 Retry strategy timing diagram

It is possible to “force” a reset of the internal counter without waiting for $t_{DELAY(CR)}$ by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is “low”. The pulse applied to DEN pin must have a duration longer than $t_{DEN(CR)}$ to ensure a reset of the internal counter. The DSEL pin must select the channel that has to be de-latched and keep the same logic value while DEN pin toggles twice (rising edge followed by a falling edge).

The timings are shown in Figure 27.

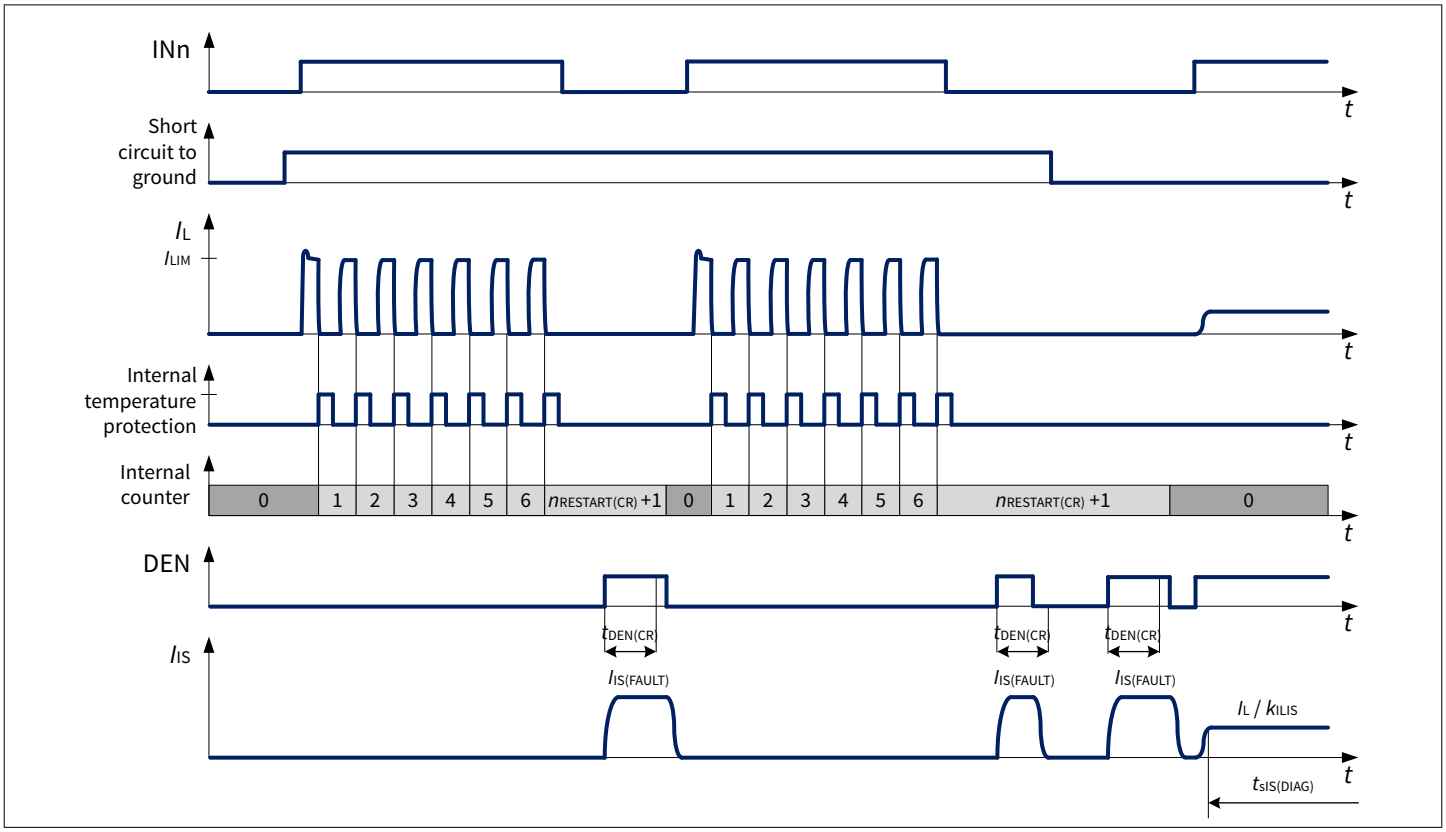


Figure 27 Retry strategy timing diagram with forced reset

7.4 Additional protection

7.4.1 Reverse polarity protection

In reverse polarity condition (also known as reverse battery), power dissipation is caused by the intrinsic body diode of the DMOS channel. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stages must be limited by the connected loads. The current through digital input pins has to be limited by an external resistor (please refer to the absolute maximum ratings listed in Table 2 and to Application Information in Chapter 9).

7.4.2 Overvoltage protection

In the case of supply voltages between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the output transistors are still operational and follow the input pin.

In addition to the output clamp for inductive loads as described in Chapter 6.2.2, there is a clamp mechanism available for overvoltage protection for the logic and the output channels, monitoring the voltage between V_S and GND pins ($V_{S(CLAMP)}$).

7.4.3 Loss of battery and loss of load

The loss of connection to the battery or the load does not influence device robustness as long as load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled.

The device can handle the inductivity of the wire harness up to 10 µH with $I_{L(NOM)\_85}$.

In case of applications where currents and/or the aforementioned inductivity are exceeded, an external suppressor diode (like diode D_{Z2} shown in Chapter 9) is recommended to handle the energy and to provide a well-defined path for the load current.

7.4.4 Loss of ground

It is recommended to have a resistor connected between any digital input pin and the microcontroller to ensure a channel switch OFF in case of a loss of device ground event (as described in Chapter 9).

Note

In case any digital input pin is pulled to ground (either by a resistor or active) a parasitic ground path is present, which could keep the device operational during a loss of device ground.

7.5 Electrical characteristics protection

V_S = 4 V to 20 V, T_J = -40°C to +150°C

Unless otherwise specified typical values: V_S = 13.5 V, T_J = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTG7050-2EPL: R_L = 4.7 Ω

Table 10 Electrical characteristics protection

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown temperature (absolute)	$T_{J(ABS)}$	150	175	200	°C	*1) 2)* See Figure 24	PRQ-174
Thermal shutdown hysteresis (absolute)	$T_{HYS(ABS)}$	–	30	–	K	*3)* See Figure 24	PRQ-356
Thermal shutdown temperature (dynamic)	$T_{J(DYN)}$	–	80	–	K	*3)* See Figure 24	PRQ-357
Thermal shutdown temperature (dynamic) in capacitive load switching mode	$T_{J(DYN)\_CLS}$	–	40	–	K	*3)*	PRQ-177
Power supply clamping voltage at TJ = -40°C	$V_{S(CLAMP)\_-40}$	33	36.5	42	V	I_{VS} = 5 mA T_J = -40°C See Chapter 6.2.2	PRQ-179
Power supply clamping voltage at TJ ≥ 25°C	$V_{S(CLAMP)\_25}$	35	38	44	V	*2)* I_{VS} = 5 mA T_J ≥ 25°C See Chapter 6.2.2	PRQ-184
Automatic restarts in case of fault after counter reset	$n_{RESTART(CR)}$	–	6	–	–	*1)* See Figure 26	PRQ-186
Counter reset delay time after fault condition	$t_{DELAY(CR)}$	40	70	100	ms	*1)* See Figure 26	PRQ-188
Minimum DEN pulse duration for counter reset	$t_{DEN(CR)}$	50	100	150	µs	*3)* See Figure 27	PRQ-190

(table continues...)

Table 10 (continued) Electrical characteristics protection

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Adjustable overcurrent limitation							
Adjustable overcurrent limitation accuracy (low)	$I_{LIM(ACCURACY)}$	-22.5%	–	+22.5%	–	3) 0.79 A ≤ I_{LIM} < 1.67 A V_{DS} = 3 V	PRQ-633
Adjustable overcurrent limitation d-factor (low)	ΔI_{LIM01}	–	0.102	–	A	3) 0.79 A ≤ I_{LIM} < 1.67 A	PRQ-646
Adjustable overcurrent limitation k-factor (low)	$k_{ILIOCT01}$	–	34449	–	–	3) 0.79 A ≤ I_{LIM} < 1.67 A	PRQ-658
Adjustable overcurrent limitation accuracy (medium)	$I_{LIM(ACCURACY)}$	-16%	–	+16%	–	3) 1.67 A ≤ I_{LIM} < 3.27 A V_{DS} = 3 V	PRQ-644
Adjustable overcurrent limitation d-factor (medium)	ΔI_{LIM02}	–	-0.042	–	A	3) 1.67 A ≤ I_{LIM} < 3.27 A	PRQ-647
Adjustable overcurrent limitation k-factor (medium)	$k_{ILIOCT02}$	–	37301	–	–	3) 1.67 A ≤ I_{LIM} < 3.27 A	PRQ-659
Adjustable overcurrent limitation accuracy (high)	$I_{LIM(ACCURACY)}$	-18%	–	+18%	–	3) 3.27 A ≤ I_{LIM} ≤ 8.86 A V_{DS} = 3 V	PRQ-634
Adjustable overcurrent limitation d-factor (high)	ΔI_{LIM03}	–	-0.374	–	A	3) 3.27 A ≤ I_{LIM} ≤ 8.86 A	PRQ-648
Adjustable overcurrent limitation k-factor (high)	$k_{ILIOCT03}$	–	40512	–	–	3) 3.27 A ≤ I_{LIM} ≤ 8.86 A	PRQ-660
Current limitation value in case OCT pin open	$I_{LIMOCT(OPEN)}$	0.52	0.74	0.97	A	4) I_{OCT} ≤ $I_{OCT(OPEN)}$	PRQ-661
Current limitation value in case OCT pin short to device ground	$I_{LIMOCT(SHORT2GND)}$	7.45	9.48	11.5	A	4) I_{OCT} ≥ $I_{OCT(SHORT2GND)}$	PRQ-662

1) Functional test only
2) Tested at T_J = 150°C only
3) Not subject to production test - specified by design
4) Tested at T_J = -40°C only

8 Diagnosis

For the purpose of diagnosis, the device provides a proportional sense current signal (I_{IS}) at pin IS. In case of disabled diagnostic (DEN pin set to “low”), IS pin becomes high impedance.

A sense resistor R_{SENSE} must be connected between IS pin and module ground if the current sense diagnosis is used.

R_{SENSE} value has to be higher than 820 Ω (or 400 Ω when a central Reverse Battery protection is present on the battery feed) to limit the power losses in the sense circuitry.

A typical value is R_{SENSE} = 1.2 kΩ.

Due to the internal connection between IS pin and V_S supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed.

See Figure 28 for details as an overview.

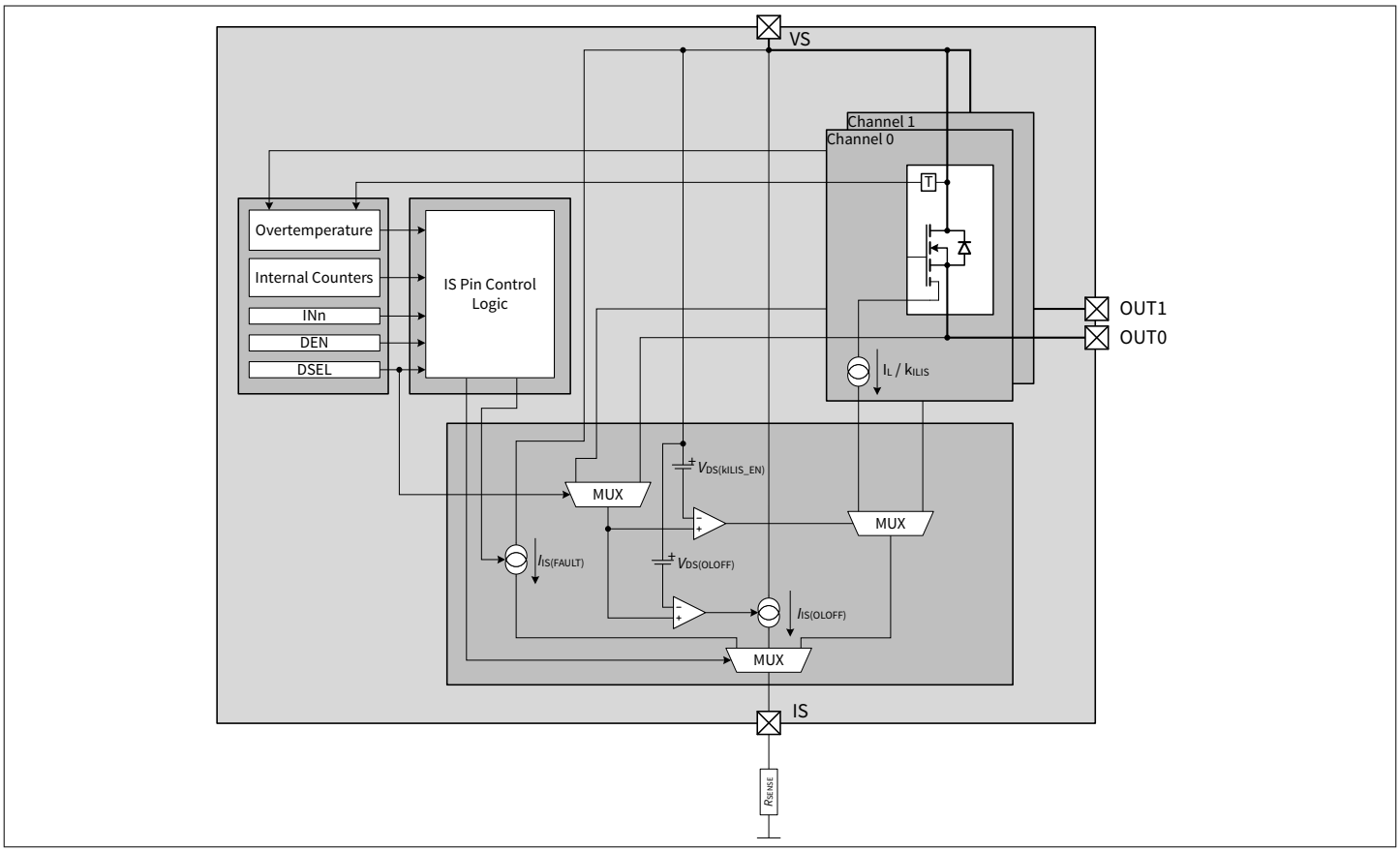


Figure 28 Diagnosis block diagram

8.1 Overview

Table 11 gives a quick reference to the state of the IS pin during the device operation.

Table 11 SENSE signal as a function of application condition

Operation mode	Input level	DEN level	V_{OUT}	Diagnostic output
Normal operation	LOW/OFF	HIGH	~ GND	Z $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$
Short circuit to GND			~ GND	Z $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$

(table continues...)

Table 11 (continued) SENSE signal as a function of application condition

Operation mode	Input level	DEN level	V_{OUT}	Diagnostic output
Thermal shutdown temperature (absolute)			Z	$I_{IS(FAULT)}$
Thermal shutdown temperature (dynamic)			Z	$I_{IS(FAULT)}$
Short circuit to V_S			= V_S	$I_{IS(OLOFF)}$ $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$
Open load			< V_S - $V_{DS(OLOFF)}$ > V_S - $V_{DS(OLOFF)}$ [1]	Z $I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$ for both cases
Overcurrent pin fault			< V_S - $V_{DS(OLOFF)}$ > V_S - $V_{DS(OLOFF)}$ [1]	$I_{IS(OCT\_PIN\_FAULT)}$ $I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$ for both cases
Inverse current			~ V_{INV} = V_{OUT} > V_S	$I_{S(OLOFF)}$ or $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$
Normal operation	HIGH/ON or CLS		< V_S - $V_{DS(kILIS\_EN)}$	$I_{IS} = I_L / k_{ILIS}$
Short circuit to GND			~ GND	$I_{IS(FAULT)}$
Thermal shutdown temperature (absolute)			Z	$I_{IS(FAULT)}$
Thermal shutdown temperature (dynamic)			Z	$I_{IS(FAULT)}$
Short circuit to V_S			= V_S	$I_{IS} < I_L / k_{ILIS}$
Open load			~ V_S [2]	$I_{IS} = I_{IS(EN)}$
Inverse current			~ V_{INV} = V_{OUT} > V_S	$I_{IS} = I_{IS(EN)}$
Current limitation			< V_S	$I_{IS(FAULT)}$
Underload			~ V_S [3]	$I_{IS(EN)} < I_{IS} < I_{L(NOM)} / k_{ILIS}$
All conditions	n.a.	LOW	n.a.	Z

1) With additional pull up resistor

2) The output current has to be smaller than $I_{L(OL)}$

3) The output current has to be higher than $I_{L(OL)}$

8.1.1 SENSE signal truth table

Diagnosis can be activated or deactivated using the DEN pin. Channel selection is done with DSEL pin according to Table 12.

Table 12 Diagnostic truth table

DEN	DSEL	IS
"low"	not relevant	Z

(table continues...)

Table 12 (continued) Diagnostic truth table

DEN	DSEL	IS
"high"	"low"	SENSE output 0
"high"	"high"	SENSE output 1

8.2 Diagnosis in ON state

A current proportional to the load current ($I_{IS} = I_L/k_{ILIS}$) is provided at pin IS when the following conditions are fulfilled:

- The power output stage is switched ON with $V_{DS} < V_{DS(kILIS\_EN)}$
- The diagnosis is enabled for that channel
- No fault (as described in Chapter 7.3) is present or was present and not cleared yet (see Chapter 8.2.2 for further details)

As long as a fault is present or was present and not cleared yet a current $I_{IS(FAULT)}$ is provided at IS pin.

8.2.1 Current sense (kILIS)

I_{IS} increases linearly with I_L output current until it reaches the saturation current $I_{IS(SAT)}$. In case of open load at the output stage (I_L close to 0 A), the maximum sense current $I_{IS(EN)}$ (no load, diagnosis enabled) is specified. This condition is shown in Figure 29. The center line represents the ideal k_{ILIS}, while the outer lines show the behavior of a typical product. An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1 µs for the RC filter is recommended). The k_{ILIS} factor is specified with limits that take into account effects due to temperature, supply voltage, and manufacturing process.

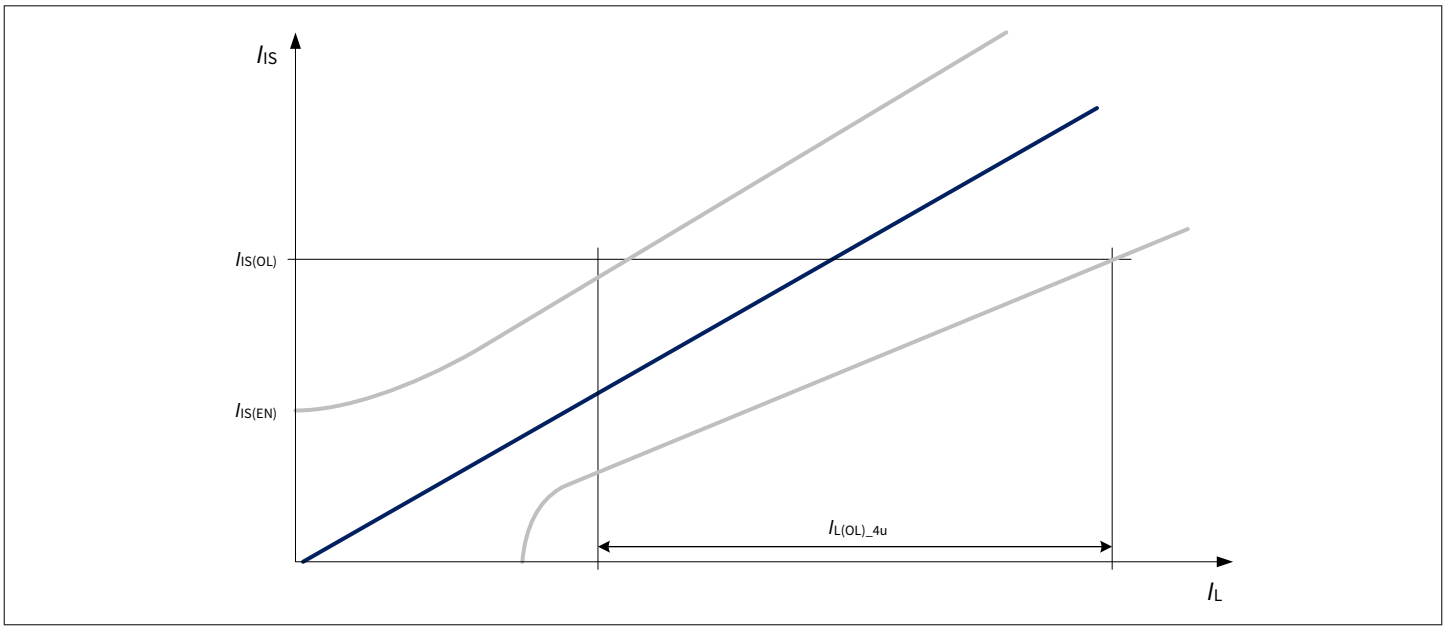


Figure 29 Current sense ratio in open load at ON condition

8.2.2 Fault current (IIS(FAULT))

In case a fault is present and DEN is set to “high” and the affected channel is selected by DSEL, a current $I_{IS(FAULT)}$ is provided.

The following situations may occur:

- If the channel is ON and the number of restarts is less than "$n_{RESTART(CR),TYP}$", the current $I_{IS(FAULT)}$ is provided for a time $t_{IS(FAULT)\_D}$ after the channel is allowed to restart, and thereafter $I_{IS} = I_L/k_{ILIS}$ (as shown in Figure 30). During a restart cycle the current $I_{IS(FAULT)}$ is provided each time the channel diagnosis is checked.
- If the channel is ON and the number of restarts is equal to "$n_{RESTART(CR),TYP}$", the current $I_{IS(FAULT)}$ is provided until the internal counter is reset. The internal counter can be cleared either by INn = "low" for $t_{DELAY(CR)}$ or by INn = "low" and DEN pin pulse for $t_{DEN(CR)}$, as described in Chapter 7.3.1.
- While the channel is OFF and the internal counter value is not reset, the current $I_{IS(FAULT)}$ is provided.

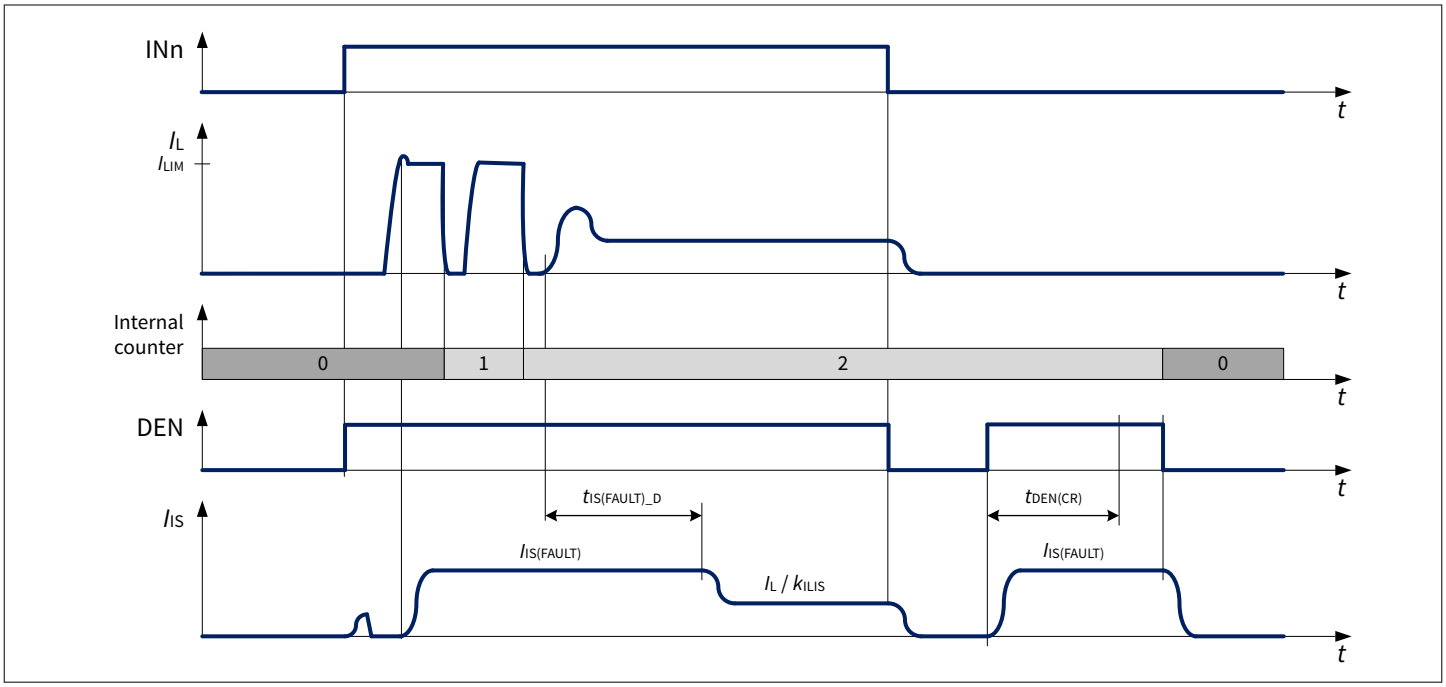


Figure 30 $I_{IS(FAULT)}$ at load switching

Figure 31 adds the behavior of SENSE signal to the timing diagram seen in Figure 26, while Figure 32 shows the relation between $I_{IS} = I_L/k_{ILIS}$, $I_{IS(SAT)}$ and $I_{IS(FAULT)}$.

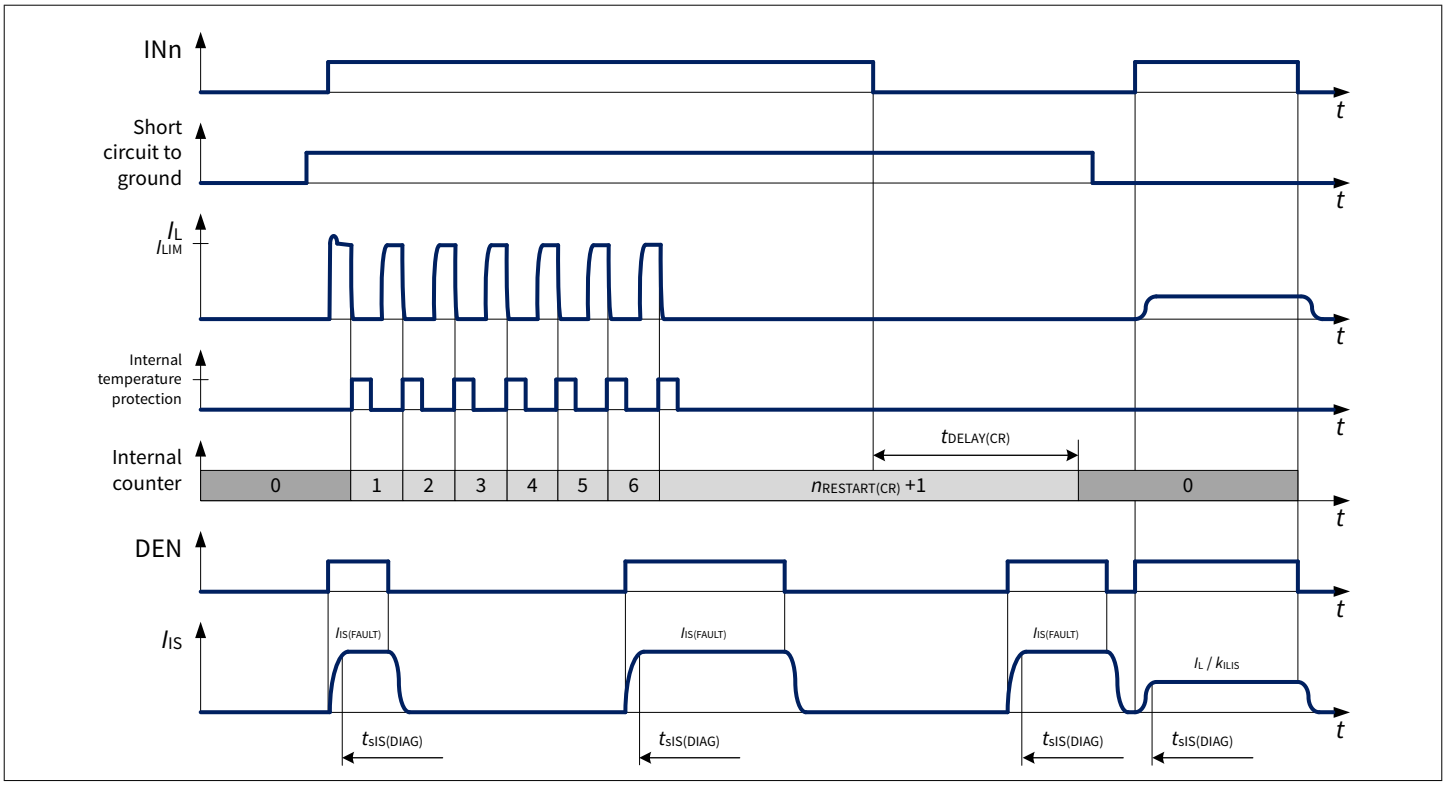


Figure 31 SENSE behavior in fault condition

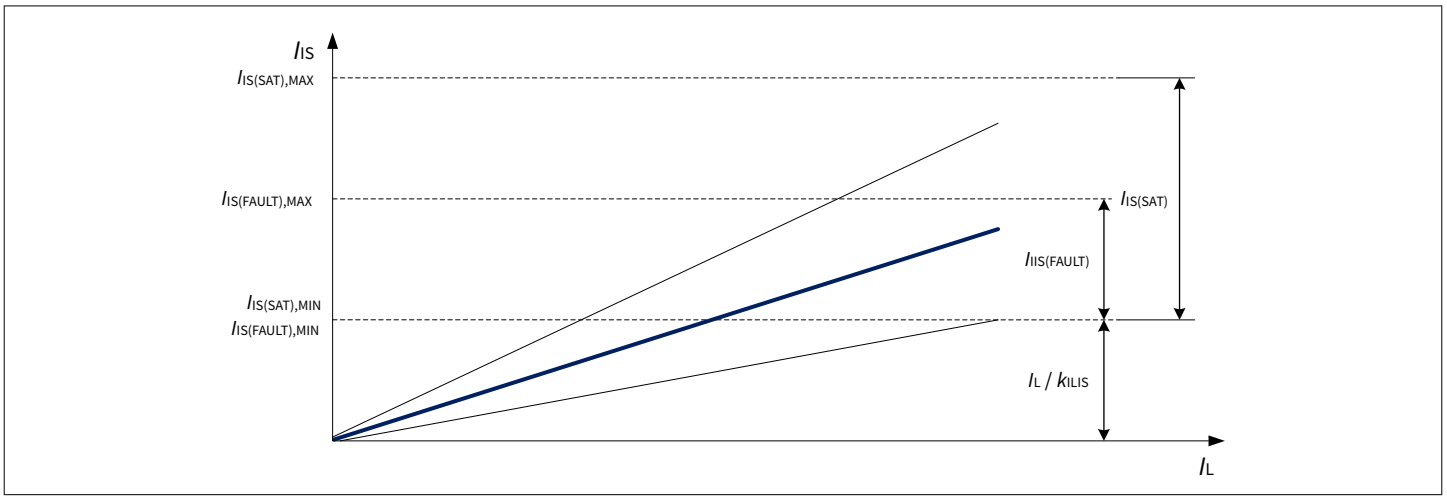


Figure 32 SENSE behavior - overview

8.3 Diagnosis in OFF State

When a power output stage is in OFF state, the device can measure the output voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source), it is possible to detect if the load is missing or if there is a short circuit to battery. If a fault condition was detected by the device (the internal counter has a value different from the reset value, as described in Chapter 8.2.2 a current $I_{IS(FAULT)}$ is provided by IS pin each time the channel diagnosis is checked also in OFF state. Additionally, the device can measure if the OCT pin is open $I_{OCT(OPEN)}$ or shorted to device ground $I_{OCT(SHORT2GND)}$. In case of an fault condition on the OCT pin $I_{IS(OCT\_PIN\_FAULT)}$ is provided. Figure 33 shows the relationship between $I_{IS(OLOFF)}$, $I_{IS(FAULT)}$ and $I_{IS(OCT\_PIN\_FAULT)}$ as functions of V_{DS}. The three currents do not overlap making it always possible to differentiate between open load in OFF, OCT pin fault and fault condition.

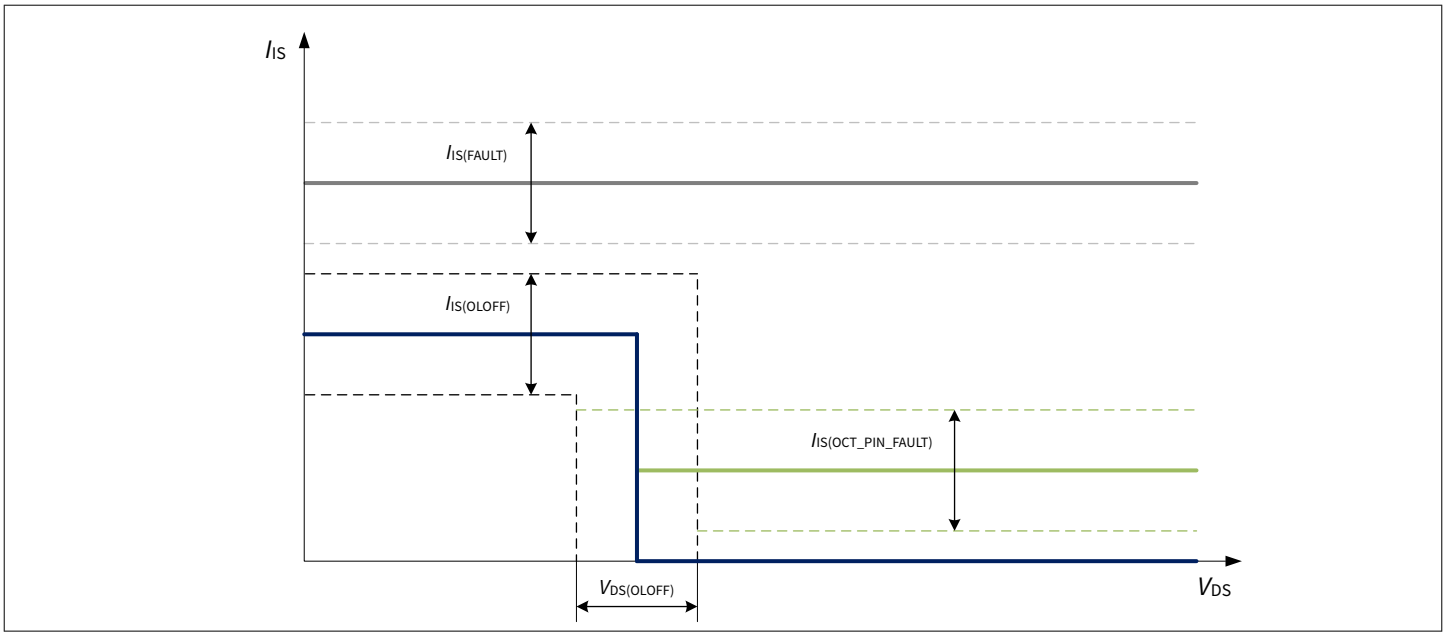


Figure 33 I_{IS} in OFF state

8.3.1 Open load current

In OFF state, while DEN pin is set to “high” and a channel is selected using DSEL pin, the V_{DS} voltage is compared with a threshold voltage $V_{DS(OLOFF)}$. When the diagnosis is active and $V_{DS} \leq V_{DS(OLOFF)}$, a current $I_{IS(OLOFF)}$ is provided by IS pin. If the load is properly connected and there is no short circuit to battery, $V_{DS} \sim V_S$, therefore, $V_{DS} > V_{DS(OLOFF)}$ the IS pin is set to high impedance.

It is necessary to wait a time $t_{IS(OLOFF)\_D}$ between the falling edge of the input pin and the sensing at pin IS for Open Load in OFF diagnosis to allow the internal comparator to settle. In Figure 34 the timings for an Open Load detection are shown - the load is always disconnected.

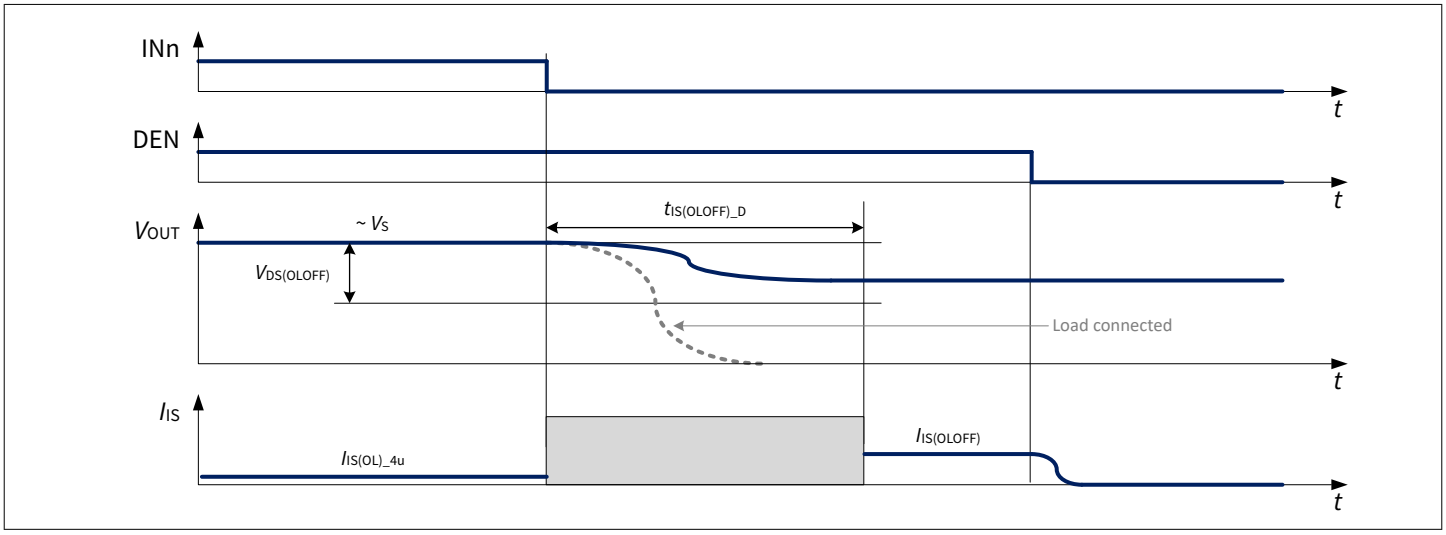


Figure 34 Open load in OFF timings - load disconnection

8.3.2 OCT pin fault current

When the device is in Inactive with Diagnosis mode and the OCT pin is open or shorted to device ground and $V_{DS} \geq V_{DS(OLOFF)}$, a current $I_{IS(OCT\_PIN\_FAULT)}$ is provided by IS pin. Figure 33 shows $I_{IS(OCT\_PIN\_FAULT)}$ as a function over V_{DS}.

8.4 SENSE timings

Figure 35 and Figure 36 show the timing during settling $t_{sIS(ON)}$ and disabling $t_{sIS(OFF)}$ of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before t_{ON}),

$$t_{sIS(DIAG)} = t_{sIS(ON)} + t_{ON} \tag{4}$$

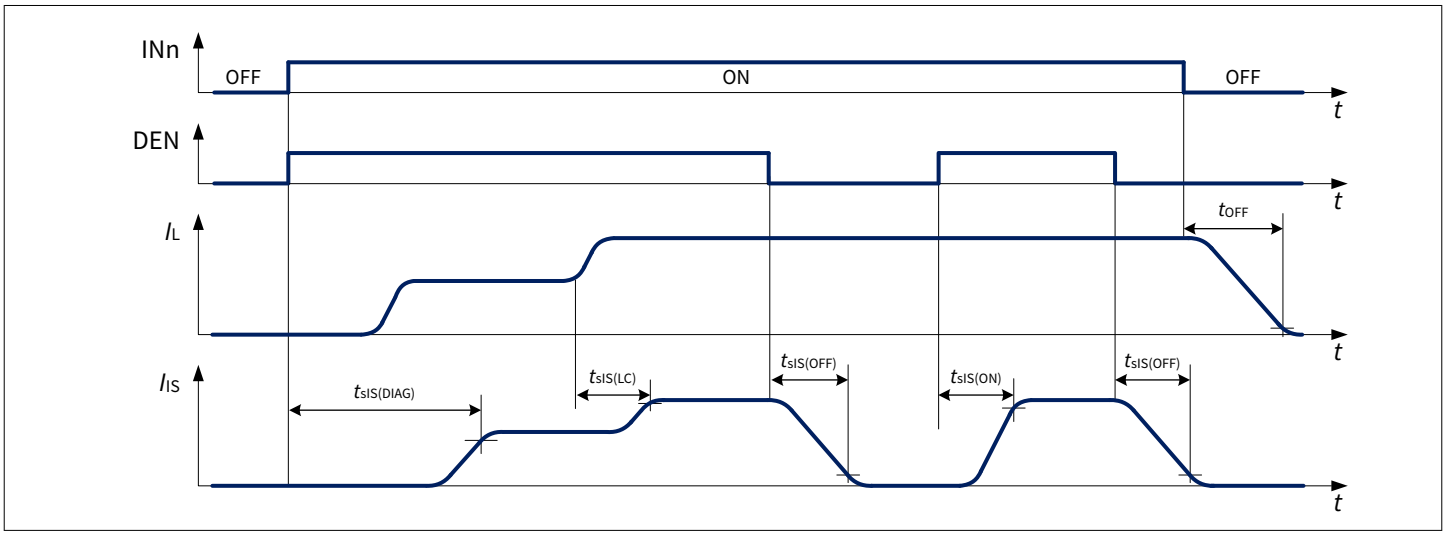


Figure 35 SENSE settling/disabling timing

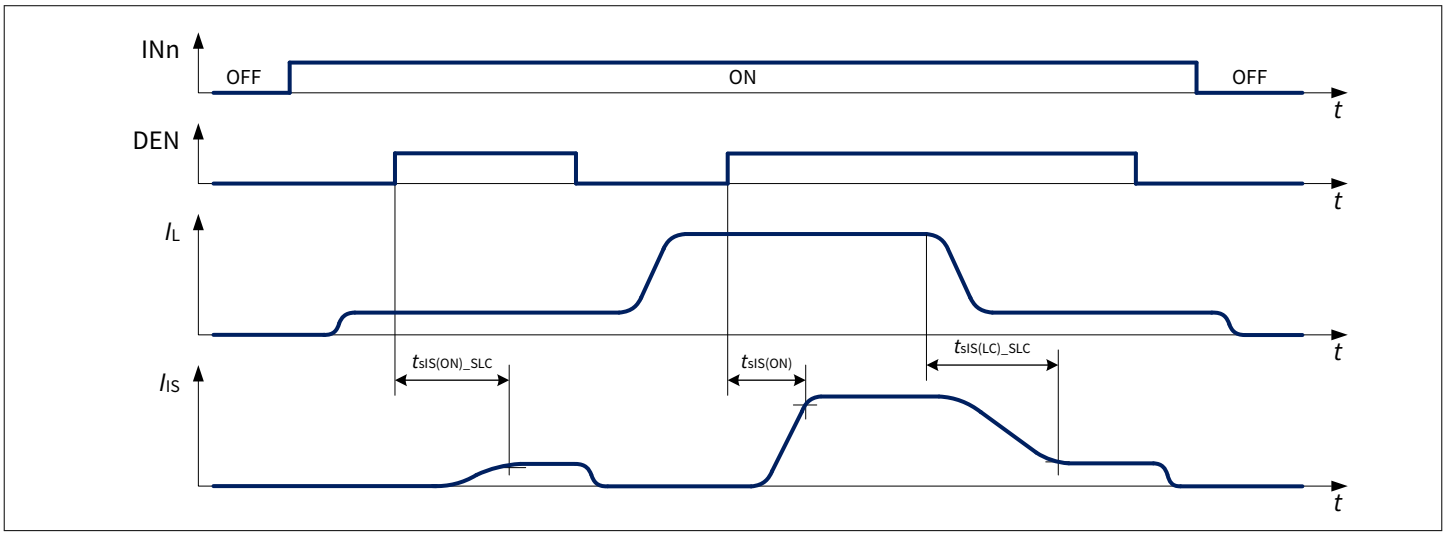


Figure 36 SENSE timing with small load current

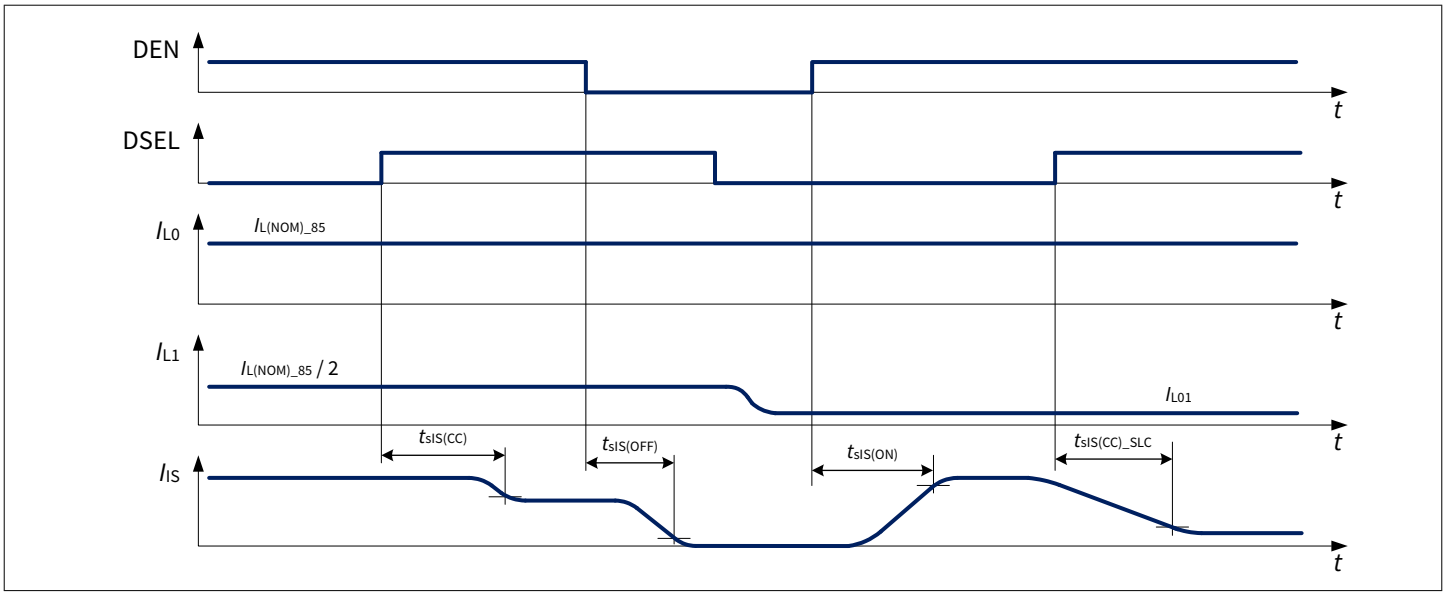


Figure 37 SENSE settling timing - channel change

8.5 Electrical characteristics diagnosis

V_S = 4 V to 20 V, T_J = -40°C to +150°C
Unless otherwise specified typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive loads connected to the outputs for testing (unless otherwise specified):
BTG7050-2EPL: R_L = 4.7 Ω

Table 13 Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE saturation current	$I_{IS(SAT)}$	4.4	–	15	mA	1) V_S = 6 V to 20 V R_{SENSE} = 1.2 kΩ See Figure 32	PRQ-215
SENSE leakage current when disabled	$I_{IS(OFF)}$	–	0.01	0.5	µA	DEN = "low" $I_L \geq I_{L(NOM)}$ V_{IS} = 0 V	PRQ-219
SENSE leakage current when enabled at TJ ≤ 85°C	$I_{IS(EN)\_85}$	–	0.2	2	µA	1) $T_J \leq$ 85°C DEN = "high" I_L = 0 A See Figure 29	PRQ-221
SENSE leakage current when enabled at TJ = 150°C	$I_{IS(EN)\_150}$	–	0.2	2	µA	T_J = 150°C DEN = "high" I_L = 0 A See Figure 29	PRQ-223

(table continues...)

Table 13 (continued) Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Saturation voltage in kILIS operation (VS-VIS)	V_{SIS_k}	–	0.5	1	V	1) V_S = 5 V IN = DEN = “high”	PRQ-226
Saturation voltage in open load at OFF diagnosis (VS-VIS)	V_{SIS_OL}	–	0.5	1	V	1) V_S = 5 V IN = "low" DEN = "high"	PRQ-682
Saturation voltage in fault diagnosis (VS-VIS)	V_{SIS_F}	–	0.5	1	V	1) V_S = 5 V IN = "low" DEN = "high" counter > 0	PRQ-684
Saturation voltage in OCT pin fault diagnosis (VS-VIS)	$V_{SIS\_OCT\_F}$	–	0.5	1	V	1) V_S = 5 V IN = "low" DEN = "high" I_{OCT} = $I_{OCT(SHORT2GND)}$ or $I_{OCT(OPEN)}$	PRQ-686
Power supply to IS pin clamping voltage at TJ =-40°C	$V_{SIS(CLAMP)\_-40}$	33	36.5	42	V	I_{IS} = 1mA T_J = -40°C See Chapter 6.2.2	PRQ-294
Power supply to IS pin clamping voltage at TJ ≥ 25°C	$V_{SIS(CLAMP)\_25}$	35	38	44	V	2) I_{IS} = 1 mA T_J ≥ 25°C See Chapter 6.2.2	PRQ-296
SENSE fault current	$I_{IS(FAULT)}$	4.4	5.5	10	mA	See Chapter 8	PRQ-298
SENSE open load in OFF current	$I_{IS(OLOFF)}$	1.9	2.5	3.5	mA	See Chapter 8	PRQ-306
SENSE OCT pin FAULT in OFF current	$I_{IS(OCT\_PIN\_FAULT)}$	0.2	1.2	1.7	mA	See Figure 33	PRQ-621
SENSE delay time at channel switch ON after last fault condition	$t_{IS(FAULT)\_D}$	–	500	–	µs	1) See Figure 30	PRQ-308

(table continues...)

Table 13 (continued) Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE open load in OFF delay time	$t_{IS(OLOFF)\_D}$	70	185	300	µs	$V_{DS} < V_{DS(OLOFF)}$ from INn falling edge to $I_{IS} = I_{IS(OLOFF),MIN} \cdot 0.9$ DEN = “high” $n_{RESTART(CR)} = 0$ See Figure 34	PRQ-310
VDS threshold for kILIS enable	$V_{DS(kILIS\_EN)}$	0.8	1.2	1.4	V	1)	PRQ-809
Open load VDS detection threshold in OFF state	$V_{DS(OLOFF)}$	1.3	1.8	2.3	V	See Chapter 8.3	PRQ-313
SENSE settling time with nominal load current stable	$t_{sIS(ON)}$	–	5	20	µs	$I_L = I_{L(NOM)}$ from DEN rising edge to $I_{IS} = I_L/(k_{ILIS,MAX} @ I_L) \cdot 0.9$ See Figure 35	PRQ-315
SENSE settling time with small load current stable	$t_{sIS(ON)\_SLC}$	–	–	60	µs	1) $I_L = I_{L01}$ from DEN rising edge to $I_{IS} = I_L/(k_{ILIS,MAX} @ I_L) \cdot 0.9$ See Figure 36	PRQ-317
SENSE disable time	$t_{sIS(OFF)}$	–	5	20	µs	1) $I_L = I_{L(NOM)}$ From DEN falling edge to $I_{IS} = I_{IS(OFF)}$ See Figure 35	PRQ-319
SENSE settling time after load change	$t_{sIS(LC)}$	–	5	20	µs	1) from $I_L = I_{L(NOM)}/2$ to $I_L = I_{L(NOM)}$ See Figure 35	PRQ-321
SENSE settling time after load change with small load current	$t_{sIS(LC)\_SLC}$	–	250	400	µs	1) DEN = "high" from load change to $I_{IS} = I_L/(k_{ILIS} @ I_L)$ from $I_{L(NOM)}$ to I_{L01} See Figure 36	PRQ-323
SENSE settling time after channel change	$t_{sIS(CC)}$	–	5	20	µs	1) Start channel: $I_L = I_{L(NOM)}$ End channel: $I_L = I_{L(NOM)}/2$ See Figure 37	PRQ-326

(table continues...)

Table 13 (continued) Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE settling time after channel change with small load current	$t_{sIS(CC)\_SLC}$	–	–	60	µs	1) DEN = “high” from DSEL toggling to $I_{IS} = I_L / (k_{ILIS,MIN} @ I_L) \cdot 1.1$ Start channel: $I_L = I_{L(NOM)}$ End Channel: $I_L = I_{L01}$ See Figure 37	PRQ-327
Open load output current at IIS = 4 µA	$I_{L(OL)\_4u}$	2	9.5	17	mA	$I_{IS} = I_{IS(OL)} = 4$ µA	PRQ-580
Current sense ratio at IL =IL02	k_{ILIS02}	-26%	2230	+26%	–	$I_{L02} = 20$ mA	PRQ-585
Current sense ratio at IL =IL04	k_{ILIS04}	-23.5%	2030	+23.5%	–	$I_{L04} = 50$ mA	PRQ-588
Current sense ratio at IL =IL05	k_{ILIS05}	-20%	2030	+20%	–	$I_{L05} = 100$ mA	PRQ-590
Current sense ratio at IL =IL08	k_{ILIS08}	-10%	2030	+10%	–	$I_{L08} = 250$ mA	PRQ-594
Current sense ratio at IL =IL11	k_{ILIS11}	-9.5%	2030	+9.5%	–	$I_{L11} = 1$ A	PRQ-598
Current sense ratio at IL =IL13	k_{ILIS13}	-6%	2030	+6%	–	$I_{L13} = 2$ A	PRQ-601
Current sense ratio at IL =IL15	k_{ILIS15}	-5%	2030	+5%	–	$I_{L15} = 4$ A	PRQ-604

1) Not subject to production test - specified by design
2) Tested at $T_J = 150$°C

9 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

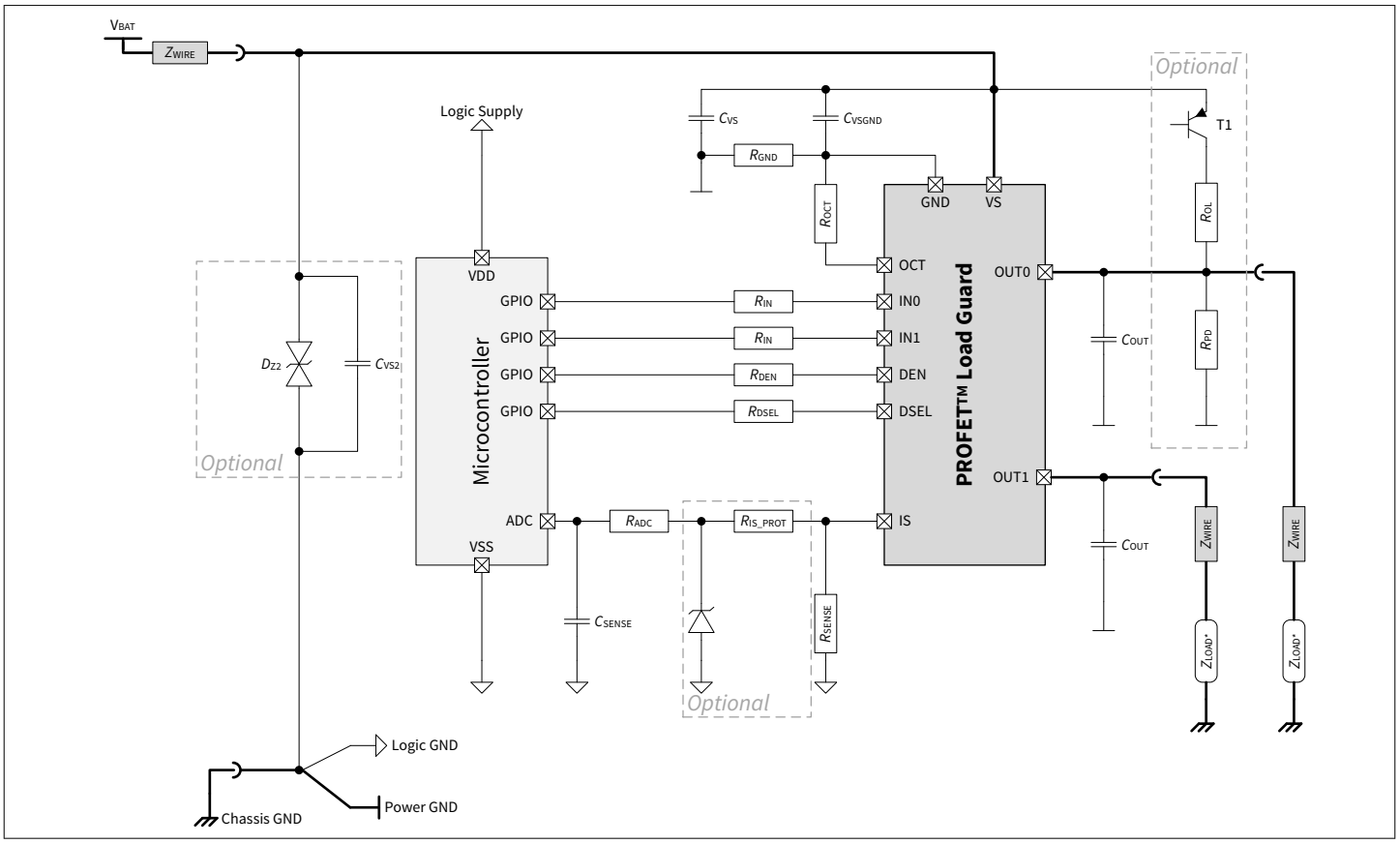


Figure 38 Application diagram

Table 14 Suggested component values

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
R_{DEN}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
R_{DSEL}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
R_{OCT}	2.2 kΩ - 25 kΩ	Adjustable overcurrent limitation resistor connected to device ground. Protection of the device during overvoltage and reverse polarity
R_{PD}	47 kΩ	Output polarization (pull-down). Ensures polarization of the outputs to distinguish between open load and short to VS in OFF diagnosis
R_{OL}	1.5 kΩ	Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis
C_{OUT}	10 nF	Protection of the output during ESD events and BCI
T_1	BC 807	Switch the battery voltage for open load in OFF diagnosis

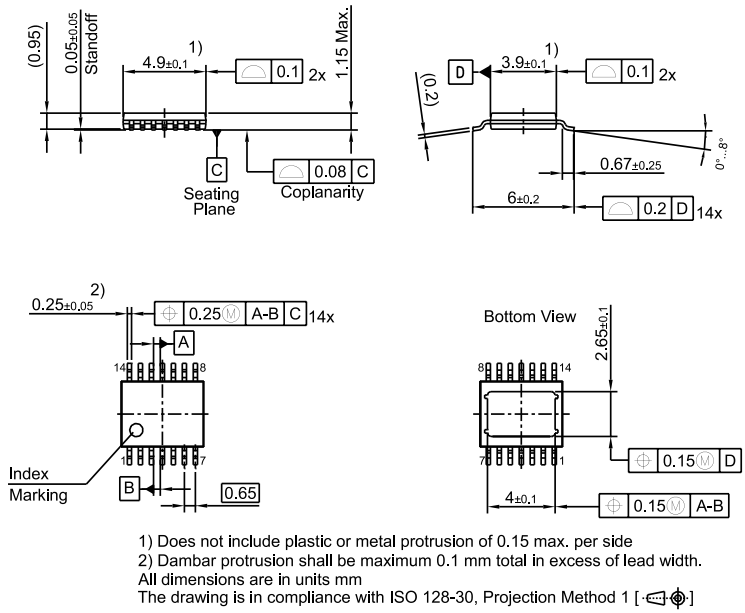
(table continues...)

Table 14 (continued) Suggested component values

Reference	Value	Purpose
C_{VS}	100 nF	Filtering of voltage spikes on the battery line
C_{VSGND}	47 nF	Buffer capacitor for fast transient
D_{Z2}	33V TVS Diode	Transient voltage suppressor diode. Protection during overvoltage and in case of loss of battery while driving an inductive load
C_{VS2}	–	Filtering/buffer capacitor located at VBAT connector
R_{SENSE}	1.2 kΩ	SENSE resistor
R_{IS_PROT}	4.7 kΩ	Protection during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
D_{Z1}	7V Z-Diode	Protection of microcontroller during overvoltage
R_{ADC}	4.7 kΩ	Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
C_{SENSE}	220 pF	Sense signal filtering. A time constant ($R_{ADC} \cdot C_{SENSE}$) longer than 1 µs is recommended
R_{GND}	47 Ω	Protection in case of overvoltage and loss of battery while driving inductive loads

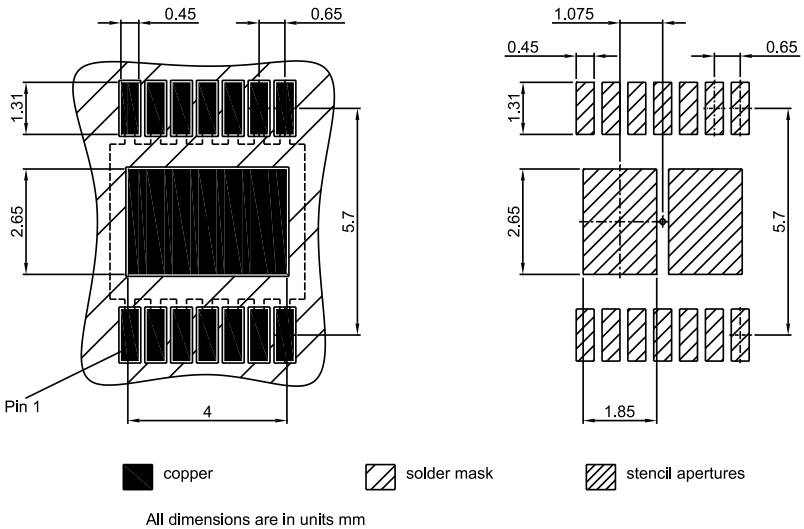
- Please contact us for information regarding the pin behavior assessment
- For further information you may contact http://www.infineon.com

10 Package outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 39 PG-TSDSO-14 dual small outline package dimensions



All dimensions are in units mm

Figure 40 PG-TSDSO-14 dual small outline footprint dimensions

Note: To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages *https://www.infineon.com/packages*

11 Revision history

Table 15 Revision history

Document version	Date of release	Description of changes
Rev.1.00	2022-09-20	Initial Datasheet

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