

# DATA SHEET

**74F534**

Octal D flip-flop, inverting (3-State)

Product specification  
Supersedes data of 1999 Jan 08  
IC15 Data Handbook

2000 Aug 01

# Octal D flip-flop, inverting (3-State)

# 74F534

## FEATURES

- 8-bit positive edge-triggered register
- 3-State inverting output buffers
- Common 3-State Output register
- Independent register and 3-State buffer operation

## DESCRIPTION

The 74F534 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ( $\overline{OE}$ ) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's  $\overline{Q}$  output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

active Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation. When  $\overline{OE}$  is Low, the latched or transparent data appears at the outputs. When  $\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

## ORDERING INFORMATION

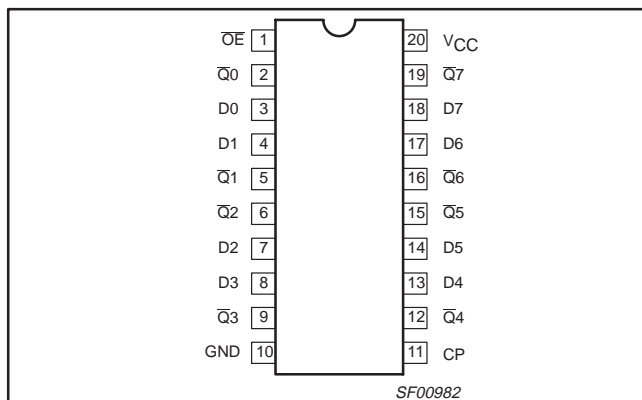
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
20-Pin Plastic DIP	N74F534N	SOT146-1
20-Pin Plastic SOL	N74F534D	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

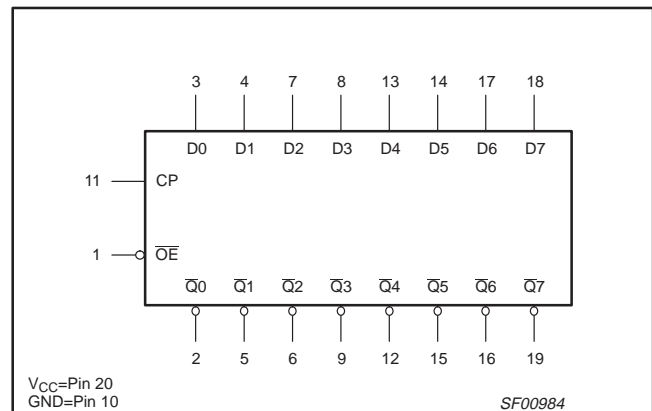
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{Q}0 - \overline{Q}7$	Data outputs	150/40	3.0mA/24mA

**NOTE:** One (1.0) FAST Unit Load (U.L.) is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## PIN CONFIGURATION



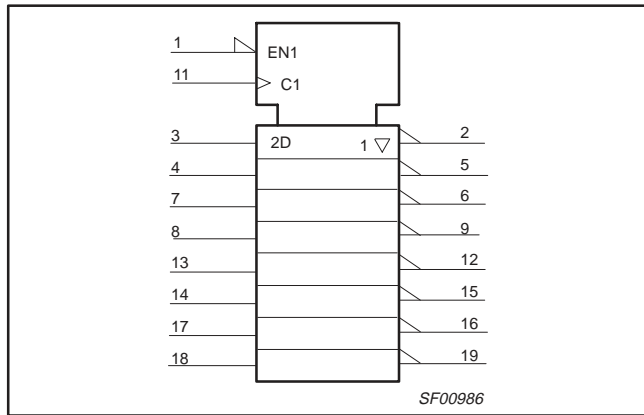
## LOGIC SYMBOL



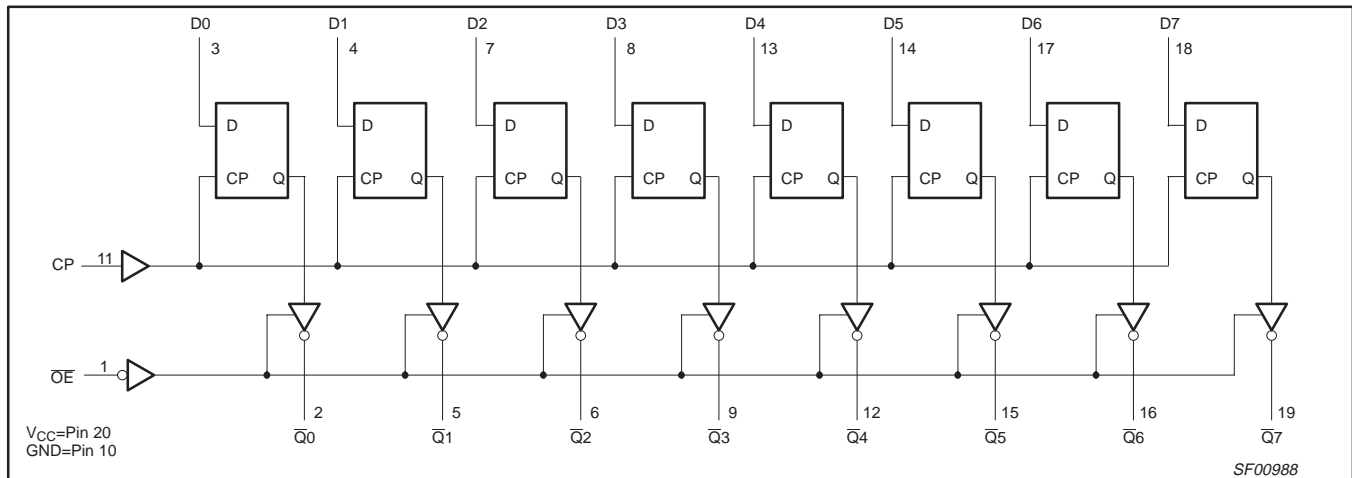
# Octal D flip-flop, inverting (3-State)

74F534

## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	CP	Dn		$\overline{Q0} - \overline{Q7}$	
L	$\uparrow$	l	L	H	Load and read register
L	$\uparrow$	h	H	L	
L	$\nabla$	X	NC	NC	Hold
H	$\nabla$	X	NC	Z	Disable outputs
H	$\uparrow$	Dn	Dn	Z	

- H = High voltage level
- h = High voltage level one setup time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the Low-to-High clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- $\uparrow$  = Low-to-High clock transition
- $\nabla$  = Not a Low-to-High clock transition

## Octal D flip-flop, inverting (3-State)

74F534

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5.0	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	48	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature	-65 to +125	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current			24	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

## Octal D flip-flop, inverting (3-State)

74F534

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.4		V	
			±5%V <sub>CC</sub>	2.7	3.3	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.35	0.50	V
			±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OZH</sub>	Off-state output current, High-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V			50	μA	
I <sub>OZL</sub>	Off-state output current, Low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V			-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-60		-150	mA	
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX $\overline{OE}$ =4.5V, Dn=GND		51	86	mA	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum Clock frequency	Waveform 1	150	165		135		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn	Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, Dn to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, Dn to CP	Waveform 2	0 0			0 0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP pulse width, High or Low	Waveform 1	3.0 3.5			3.5 4.0		ns

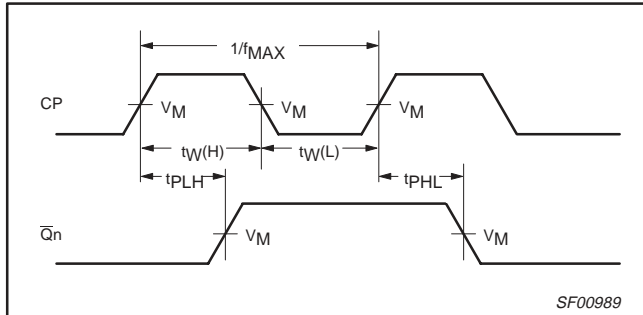
# Octal D flip-flop, inverting (3-State)

74F534

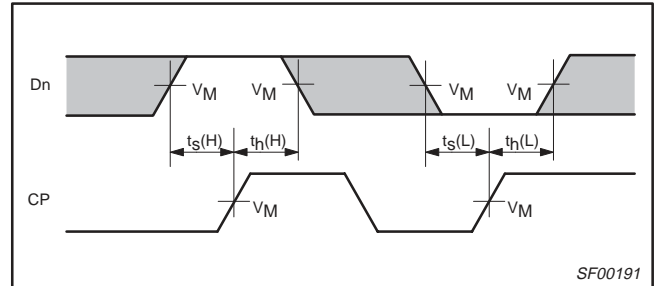
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$

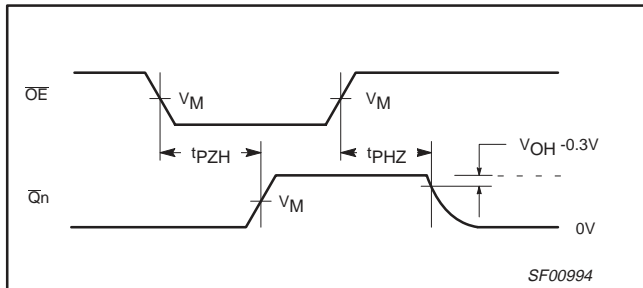
The shaded areas indicate when the input is permitted to change for predictable output performance.



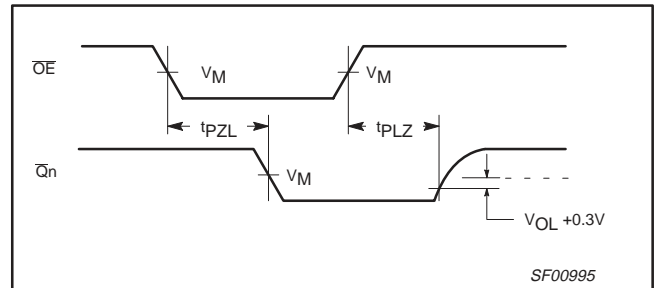
**Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency**



**Waveform 2. Data Setup and Hold Times**



**Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



**Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

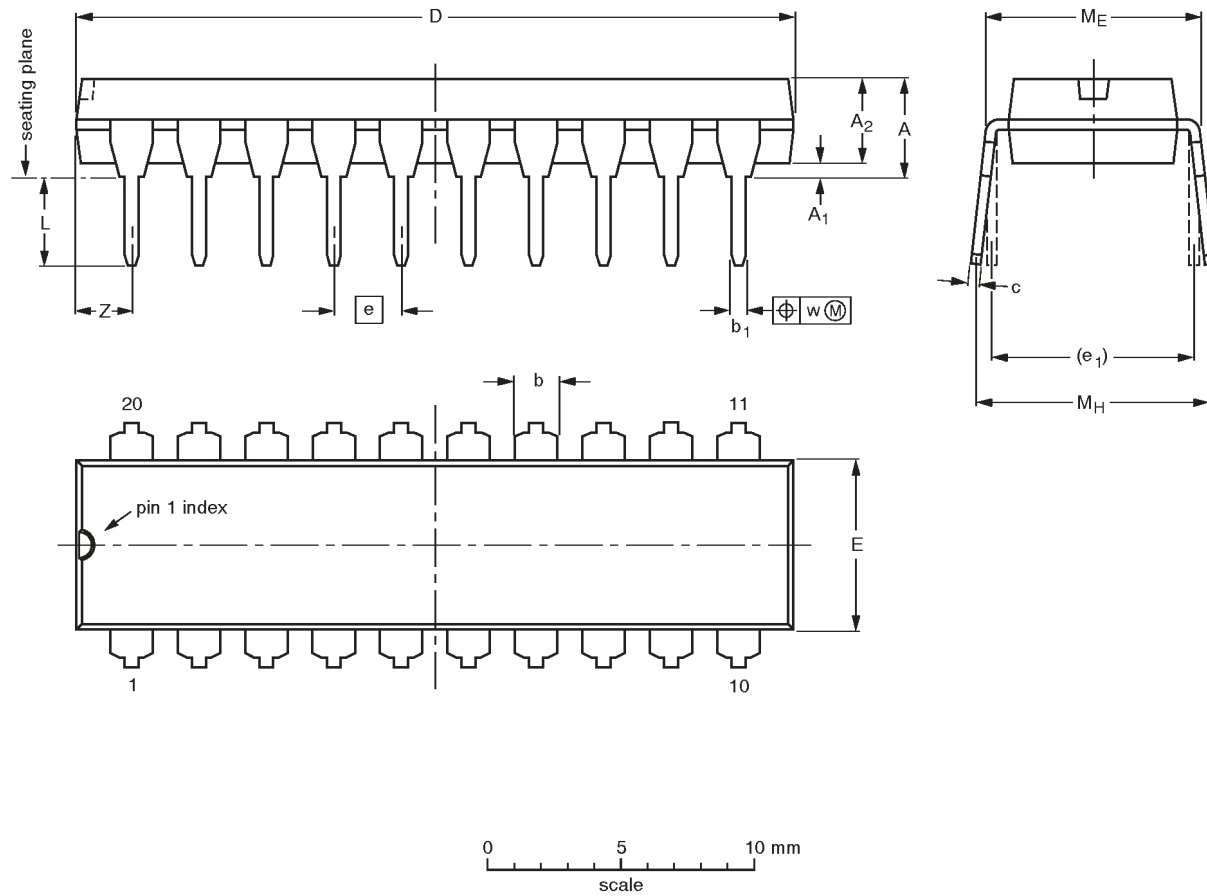
SF00777

# Octal D flip-flop, inverting (3-State)

74F534

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

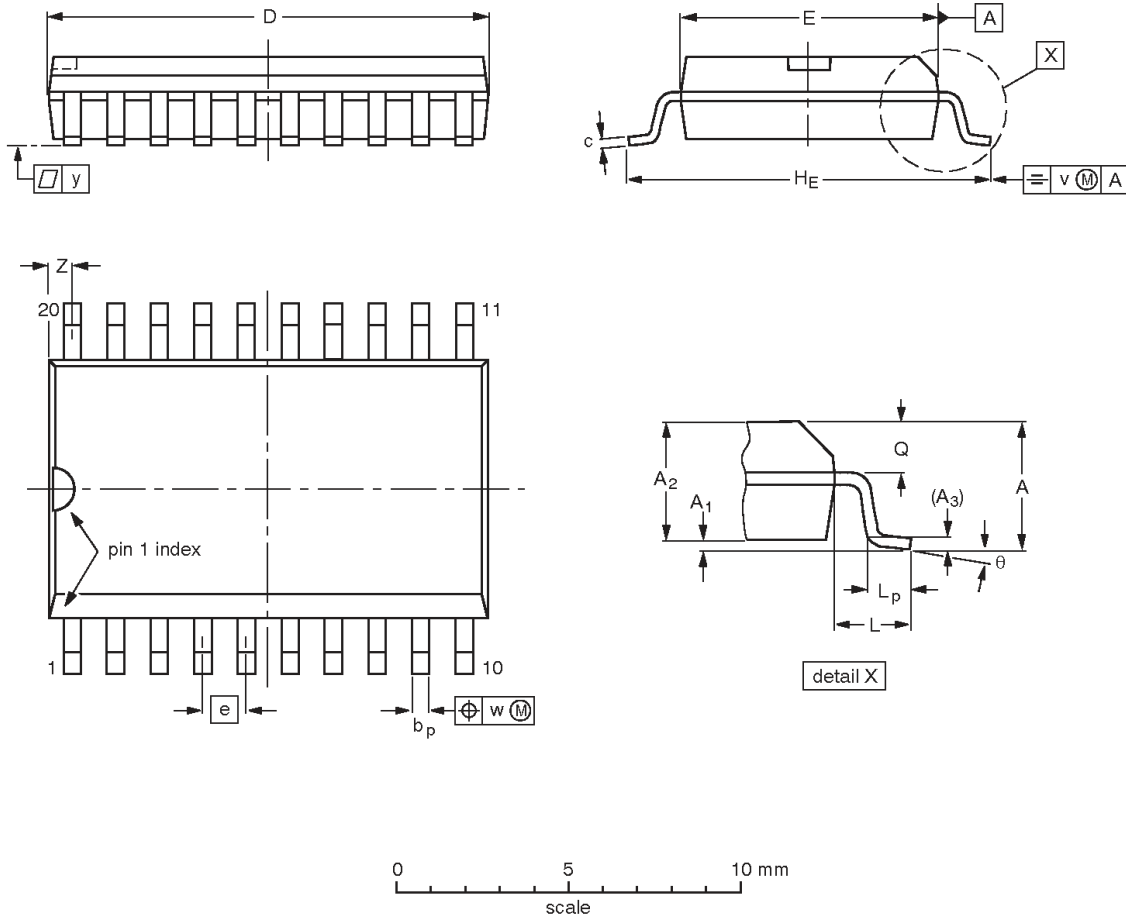
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal D flip-flop, inverting (3-State)

74F534

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22



---

Octal D flip-flop, inverting (3-State)

74F534

---

**NOTES**

## Octal D flip-flop, inverting (3-State)

74F534

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 2000  
All rights reserved. Printed in U.S.A.

Date of release: 08-00

Document order number:

9397-750-07377

*Let's make things better.*