MP4060

TRIAC Dimmable PFC, Primary Side Control LED Controller for 200-265VAC LEDs

The Future of Analog IC Technology

DESCRIPTION

The MP4060 is a TRIAC-dimmable, primary side control LED controller enables single stage AC to DC LED driver with excellent dimming performance. The dimming control method is optimized for high input AC voltages ranging from 200VAC to 265VAC.

The MP4060 implements power-factor correction and works in boundary-conduction mode to reduce MOSFET switching losses.

The adaptive dimmer type detection and phase-cut-based dimming control achieves good dimmer compatibility and a deep dimming range.

The active bleeder control circuit is integrated in BD pin to simplify the external bleeder design.

The MP4060 has an integrated charging circuit at the supply pin for fast start-up without a perceptible delay.

With the unique control of the driver DIM pin, the MP4060 supports color temperature and brightness control for warm sunset dimming application.

The MP4060 has multiple protection features that greatly enhance system reliability and safety including output over-voltage protection, output short-circuit protection, winding short-circuit protection, integrated thermal foldback, supply-pin under-voltage lockout, and over-temperature protection. All of the fault protections feature auto-restart.

The MP4060 is available in SOIC-8 / MSOP-10 packages.

FEATURES

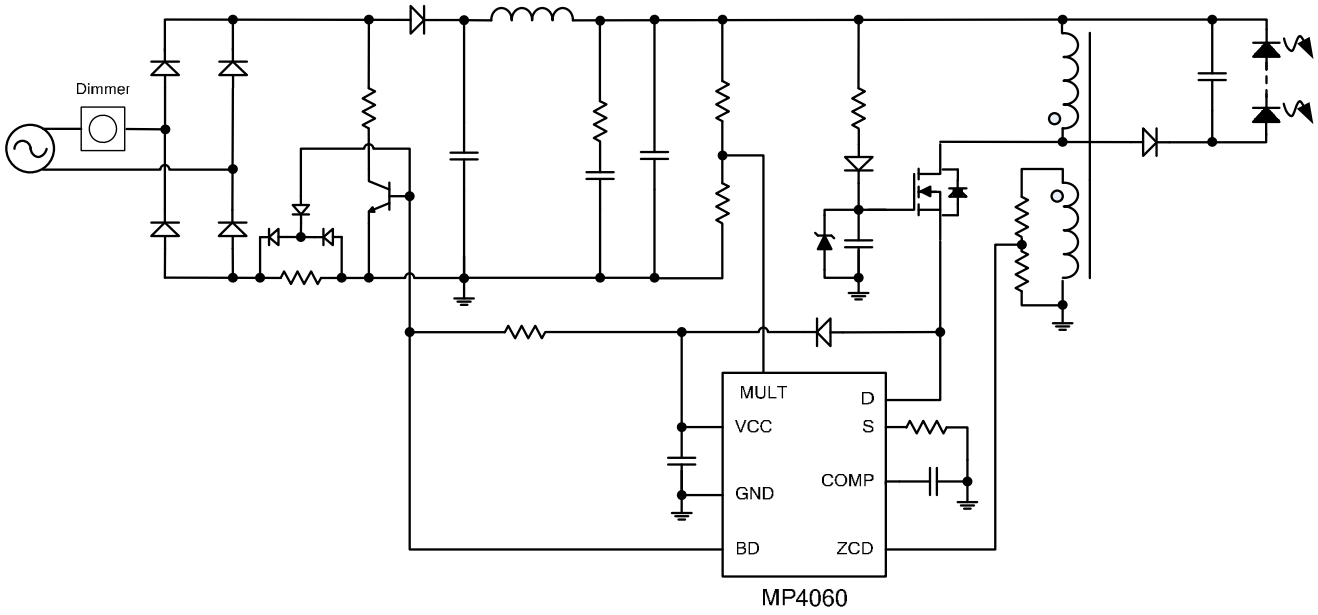
- Optimized for high line input 200-265VAC
- Primary-Side-Control without Requiring a Secondary-Side Feedback Circuit
- Adaptive Dimmer Type Detection and Phase-Cut-Based Dimming Control
- Active Bleeder Control Circuit Integrated
- Good Dimmer Compatibility and Deep Dimming Range
- Fast Start-Up without Perceptible Delay
- Integrated Thermal Current Foldback to Prolong the LED Lifetime
- Color Temperature and Brightness Control for Warm Sunset Dimming Application
- Accurate Line & Load Regulation
- High Power Factor
- Operates in Boundary Conduction Mode
- Cycle-by-Cycle Current Limit
- Winding Short-Circuit Protection
- Output Over-Voltage Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Available in SOIC-8 / MSOP-10 Packages

APPLICATIONS

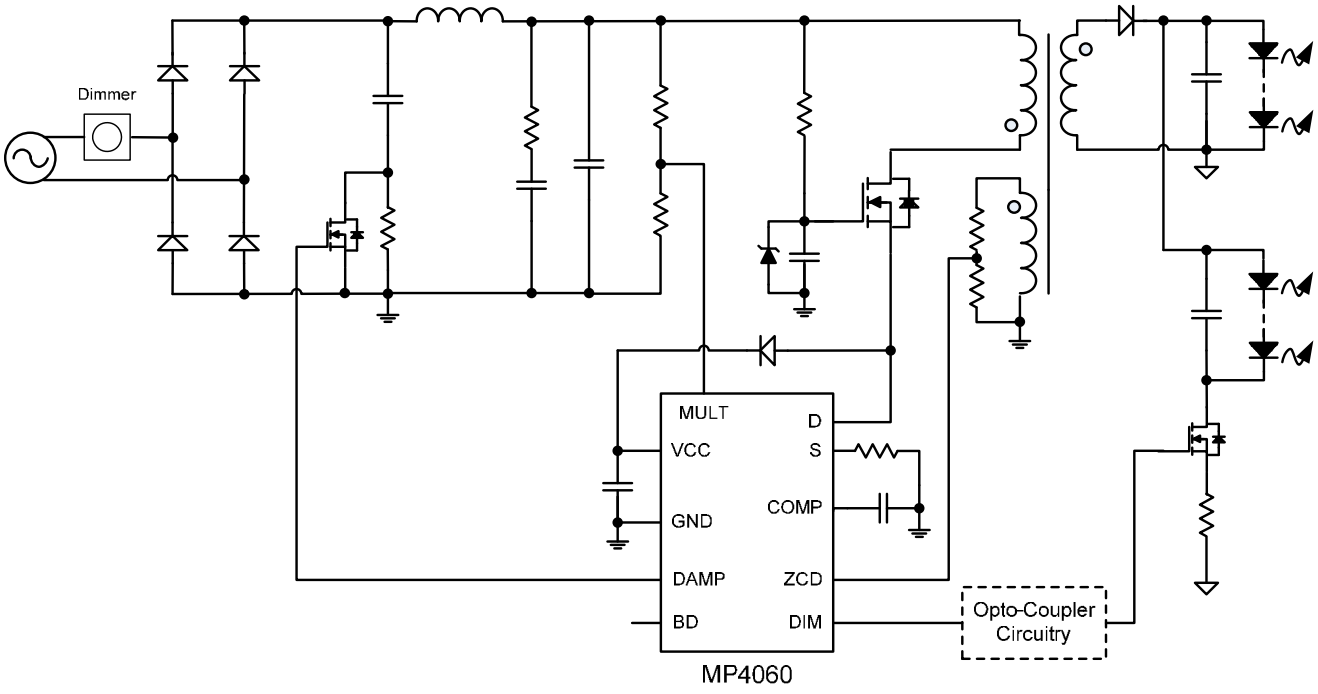
- Solid-State Lighting up to 50 W
- Industrial and Commercial Lighting
- Residential Lighting

TYPICAL APPLICATION

Non-Isolated Low-Side Buck-Boost LED Driver Solution



Isolated Dual-Channel LED Driver for Warm Sunset Dimming Application



ORDERING INFORMATION

Part Number	Package	Top Marking
MP4060GS*	SOIC-8	*See Below*
MP4060GK**	MSOP-10	

* For Tape & Reel, add suffix –Z (e.g. MP4060GS–Z)
** For Tape & Reel, add suffix –Z (e.g. MP4060GK–Z)

TOP MARKING (SOIC-8)

MP4060
LLLLLLLL
MPSYWW

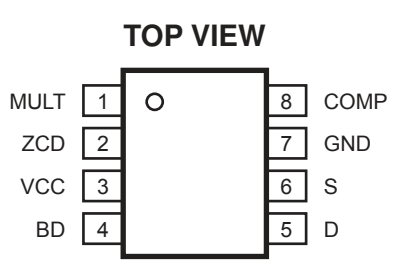
MP4060: First six digits of the part number
LLLLLLLL: Lot number
MPS : MPS prefix
Y: Year code
WW: Week code

TOP MARKING (MSOP-10)

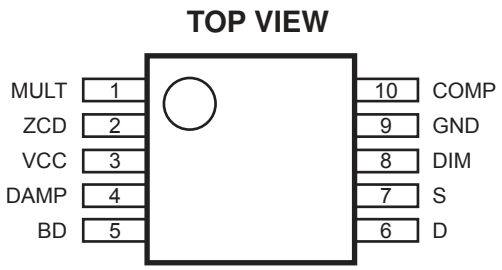
YWLLL
M4060

Y: Year code
W: Week code
LLL: Lot number
M4060: First five digits of the part number

PACKAGE REFERENCE



SOIC-8



MSOP-10

ABSOLUTE MAXIMUM RATINGS (1)

VCC pin voltage .....-0.3 V to +30 V
Low-side control MOSFET drain to source Voltage V_{DS} .....-0.3 V to +30 V
DAMP voltage .....-0.3 V to +16.5 V
ZCD current .....-5 mA to +5 mA
Other analog inputs and outputs-0.3 V to +6.5 V
Continuous power dissipation (T_A = +25°C)(2)
SOIC-8 ..... 1.3 W
MSOP-10 ..... 0.83 W
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage VCC.....11 V to 27 V
Operating junction temp(T_J). .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8 ..... 96 ..... 45... °C/W
MSOP-10 ..... 150 ..... 65... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical values are VCC = 20 V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VC = 20 V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply voltage						
Operating range	VCC	After turn on	11		27	V
VCC upper level: Internal charging circuit stops and IC turns on	VCC_H		9.5	10	10.5	V
VCC lower level: Internal charging circuit triggers	VCC_L		8.55	9	9.45	V
VCC Re-charge & IC turn-off level in fault condition	VCC_{EN}	Fault condition	6.7	7.15	7.6	V
Supply current						
VCC charging current from D	I_{D_CHARGE}	V_D = 16 V, VCC = 5 V	13	25	40	mA
Pull-down current before start-up	$I_{CC\_PULL\_DOWN}$	VCC = 9 V, rising	0.95	1.25	1.8	mA
Quiescent current	I_Q	No switching, VCC = 15 V		800	1500	µA
Quiescent current at fault	I_{Q_FAULT}	Fault condition, IC latch, VCC = 15 V	220	340	620	µA
Operating current	I_{CC}	f_S = 70 kHz, VCC = 15 V		1	2	mA
Multiplier						
Linear operation range	V_{MULT}	V_{COMP} from 1.9 V to 4.9 V	0		3	V
Gain	$K^{(5)}$	V_{COMP} = 2 V, V_{MULT} = 0.5 V	0.9	1.28	1.6	1/V
		V_{COMP} = 2 V, V_{MULT} =1.5 V	0.9	1.25	1.6	1/V
		V_{COMP} = 2 V, V_{MULT} = 3 V	0.9	1.24	1.6	1/V
TRIAC dimming phase-off detection threshold	V_{MULT_OFF}	V_{MULT} falling edge	0.08	0.1	0.12	V
TRIAC dimming phase-on detection threshold	V_{MULT_ON}	V_{MULT} rising edge	0.26	0.28	0.30	V
TRIAC dimming off line-cycle blanking ratio	D_{OFF_LEB}		28	30	33	%
Dimming pull-down MOSFET turn-on threshold	$V_{MULT\_DP\_ON\_TL}$	Trailing-edge dimmer, V_{MULT} falling edge	0.43	0.45	0.47	V
	$V_{MULT\_DP\_ON\_LD}$	Leading-edge dimmer, V_{MULT} falling edge	0.22	0.25	0.28	V
Dimming pull-down MOSFET turn-off threshold	$V_{MULT\_DP\_OFF\_TL}$	Trailing-edge dimmer, V_{MULT} rising edge	0.26	0.28	0.3	V
	$V_{MULT\_DP\_OFF\_LD}$	Leading- edge dimmer, V_{MULT} rising edge	0.32	0.35	0.38	V
Leading-edge dimming detection low threshold	$V_{MULT\_LD\_LOW}$	V_{MULT} rising edge, for MSOP only	0.08	0.1	0.12	V
Leading-edge dimming detection high threshold	$V_{MULT\_LD\_HIGH}$	V_{MULT} rising edge	0.26	0.28	0.30	V

ELECTRICAL CHARACTERISTICS *(Continued)*

Typical values are VCC = 20 V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20 V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Trailing-edge dimming detection high threshold	$V_{MULT\_TL\_HIGH}$	V_{MULT} rising edge: $V_{MULT\_PK} \geq 0.58$ V; V_{MULT} falling edge: $V_{MULT\_PK} \geq 0.5$ V	0.43	0.45	0.47	V
		V_{MULT} rising edge: 0.58 V > $V_{MULT\_PK} \geqslant$ 0.53 V; V_{MULT} falling edge: 0.5 V > $V_{MULT\_PK} \geq$ 0.45 V	0.38	0.4	0.42	V
		V_{MULT} rising edge: 0.53 V > $V_{MULT\_PK} \geqslant$ 0.48 V(6); V_{MULT} falling edge: 0.45 V > $V_{MULT\_PK} \geqslant$ 0.4 V(6)		0.35		V
		V_{MULT} rising edge: 0.48 V > $V_{MULT\_PK} \geqslant$ 0.43 V(6); V_{MULT} falling edge: 0.4 V > $V_{MULT\_PK} \geqslant$ 0.35 V(6)		0.3		V
		V_{MULT} rising edge: 0.43 V > $V_{MULT\_PK} \geqslant$ 0.38 V(6); V_{MULT} falling edge: 0.35 V > $V_{MULT\_PK} \geqslant$ 0.3 V(6)		0.25		V
Trailing-edge dimming detection high threshold hysteresis	$V_{MULT\_TL\_H\_HYS}$			80		mV
Trailing-edge dimming detection low threshold	$V_{MULT\_TL\_LOW}$	V_{MULT} falling edge	0.08	0.1	0.12	V
Leading-edge dimmer detection time	t_{LD}	V_{MULT} rising edge	86	100	134	µs
Leading-edge dimmer detection time hysteresis	t_{LD_HYS}(7)	When leading-edge dimming mode exits		160		µs
Trailing-edge dimmer detection time	t_{TL}	V_{MULT} falling edge	388	450	602	µs
Error amplifier						
Reference voltage	V_{REF}		0.4	0.414	0.428	V
Transconductance	G_{EA}(7)			130		µA/V
COMP lower clamp voltage	V_{COMPL_LD}	Leading-edge dimmer	1.83	1.88	1.94	V
	V_{COMPL_TL}	Trailing-edge dimmer	1.53	1.58	1.64	V
	V_{COMPL_N}	Without dimmer	1.53	1.58	1.64	V
Max source current	I_{COMP+}			57		µA
Max sink current	I_{COMP-}			-200		µA
Sink current at TRIAC dimming off	$I_{SINK\_DIM\_LD}$	Leading-edge dimmer		-85.5		µA
	$I_{SINK\_DIM\_TL}$	Trailing-edge dimmer		-155		µA

ELECTRICAL CHARACTERISTICS *(Continued)*

Typical values are VCC = 20 V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20 V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current sense comparator						
Leading-edge blanking time	t_{LEB}		350	500	750	ns
Over-current protection Leading-edge blanking time	t_{LEB_OCP}		260	350	550	ns
Over-current protection threshold	V_{OCP}		2.56	2.7	2.86	V
Current sense upper clamp voltage	$V_{S\_CLAMP\_H}$		1.97	2.07	2.17	V
Current sense lower clamp voltage	$V_{S\_CLAMP\_L}$	V_{COMP} = 2.2 V	10	35	90	mV
Zero-current detector						
Zero-current detect threshold	V_{ZCD_T}	V_{ZCD} falling edge	0.27	0.30	0.33	V
Zero-current detect hysteresis	V_{ZCD_HYS}		550	590	625	mV
Zero-current detect LEB	t_{ZCD_LEB}	After turn off when $V_{MULT\_O} \geq 0.25$ V	1.9	2.3	3.36	µs
		After turn off when $V_{MULT\_O} < 0.25$ V	0.95	1.18	1.68	µs
Over-voltage threshold	V_{ZCD_OVP}		4.9	5.3	5.7	V
OVP detect LEB	t_{OVP_LEB}	After turn off when $V_{MULT\_O} \geq 0.25$ V	1.9	2.3	3.36	µs
		After turn off when $V_{MULT\_O} < 0.25$ V	0.95	1.18	1.68	µs
Minimum off time	t_{OFF_MIN}		4	5.3	8	µs
Weak/strong DP mode detector current (for leading-edge dimmer)	$I_{DP\_DET\_LD}$		13	18	23	µA
Weak DP mode enable threshold (for leading-edge dimmer)	$V_{EN\_DP\_WK\_LD}$		1.13	1.18	1.23	V
Weak/strong DP mode detection time (for leading-edge dimmer)	$t_{DP\_DET\_LD}$		150	215	320	µs

ELECTRICAL CHARACTERISTICS *(Continued)*

Typical values are VCC = 20 V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20 V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal control MOSFET						
Breakdown voltage	BV_{DSS}	V_{GS} = 0	30			V
Drain-source on resistance	$R_{DS(ON)}$	I_D = 100 mA, T_J = 25 °C		250		mΩ
		I_D= 100 mA, T_J = 25 °C, VCC = VCC_{EN} + 50 mV		250		mΩ
Internal OVP pull-up MOSFET						
Breakdown voltage	$BV_{DSS\_D\_VCC}$	$V_{GS\_D\_VCC}$ = 0	30			V
Continued drain current	$I_{D\_D\_VCC}$		10	17	27	mA
Internal dimming pull-down current source						
Strong dimming pull-down current (for leading-edge dimmer)	$I_{DP\_STRONG\_LD}$		27	35	43	mA
Weak dimming pull-down current (for leading-edge dimmer)	$I_{DP\_WEAK\_LD}$		8	10	12	mA
Pull-down current (for trailing-edge dimmer)	I_{DP_TL}		133	150	167	mA
Min clamp ratio of pull-down current (for trailing-edge dimmer)	I_{DP_MIN}/I_{DP_TL}			13		%
DAMP						
Turn-off threshold	$V_{MULT\_DAMP\_OFF}$	V_{MULT} falling edge	0.22	0.25	0.28	V
Turn-on threshold	$V_{MULT\_DAMP\_ON}$	V_{MULT} rising edge	0.32	0.35	0.38	V
Pull-down current	$I_{DAMP\_PULL\_DOWN}$	V_{DAMP} = 5 V	290	370	450	µA
Pull-up current	$I_{DAMP\_PULL\_UP}$	V_{DAMP} = 0.3 V	70	90	110	µA
Upper clamp voltage	V_{DAMP_CLAMP}		13	15	16.5	V
Min pull-up voltage	V_{DAMP_MIN}	VCC = VCC_{EN} +50 mV	5.5			V
Internal bleeder disable MOSFET (open-drain output)						
Bleeder disable FET on resistance	$R_{DS(ON)\_BD}$	I_{BD} = 5 mA		60	115	Ω
		I_{BD} = 5 mA, VCC = VCC_{EN} + 50 mV		60	115	Ω

ELECTRICAL CHARACTERISTICS *(Continued)*

Typical values are VCC = 20 V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20 V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

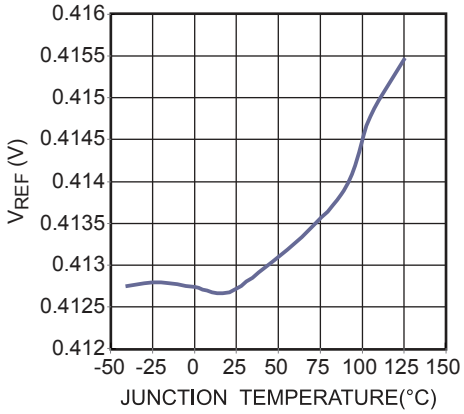
Parameter	Symbol	Condition	Min	Typ	Max	Units
DIM						
Source current	I_{DIM_SOURCE}		2	3	4	mA
Sink current	I_{DIM_SINK}		1.5	2.8	4	mA
Output high level	V_{DIM_HIGH}		5.0		6.1	V
Output low level	V_{DIM_LOW}				0.3	V
Starter						
Re-start timer period	t_{START}		100	130	165	µs
Short-circuit detection						
Short-circuit detection timer	t_{SC}	In auto-restart mode, only dimming on time is counted		60		ms
Thermal protection						
Thermal foldback threshold	T_{START}(6)			145		°C
Thermal shutdown threshold	T_{SD}(6)			155		°C
Thermal shutdown recovery hysteresis	T_{HYS}(6)			25		°C

NOTES:

5) The multiplier output is given by: Vs = K•VMULT• (VCOMP-1.5).
6) Guaranteed by characterization.
7) Guaranteed by design.

TYPICAL CHARACTERISTICS

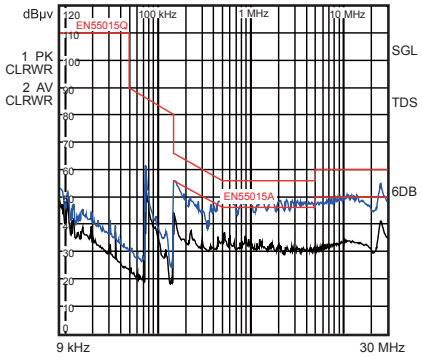
Reference Voltage vs. Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Conducted EMI L-Line

V_{IN} = 230V_{AC}/50Hz, Full Load,
RBW = 9kHz, MT = 20ms



Conducted EMI N-Line

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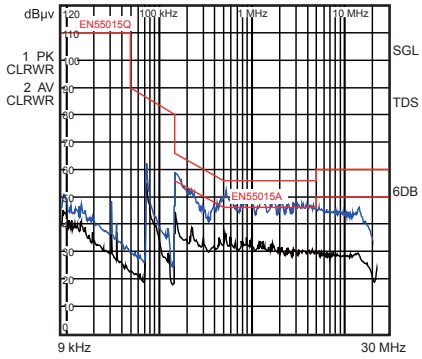
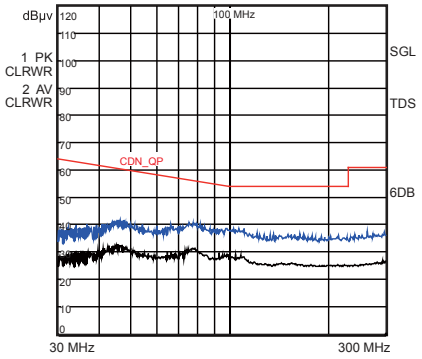
RBW = 9kHz, MT = 20ms



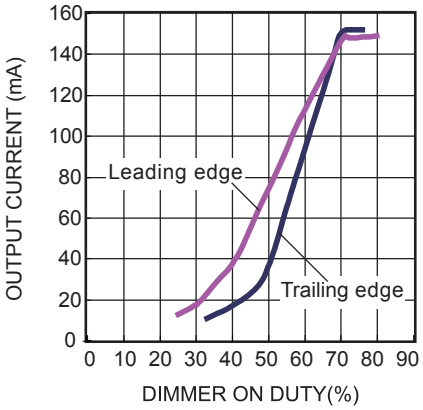
Radiated EMI

Tested by CDN,
V_{IN}=230V_{AC}/50Hz, Full Load



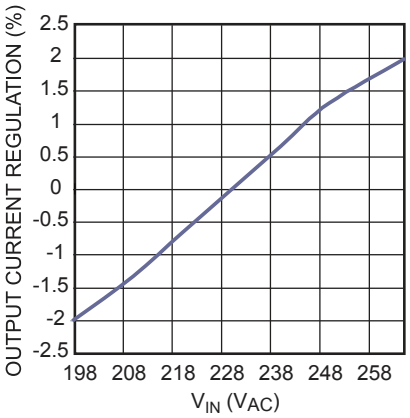
Dimming Curve

V_{IN}=230VAC/50Hz , Full load,
with different dimmers



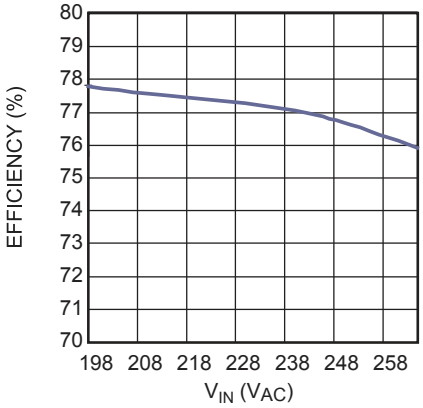
Line Regulator

V_{IN}=198-265VAC/50Hz,Full load



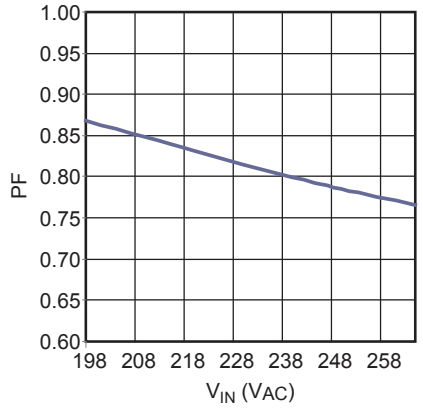
Efficiency vs. V_{IN}

V_{IN}=198-265V_{AC}/50Hz, Full Load



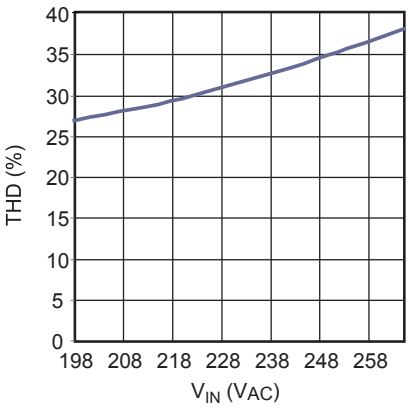
PF vs. V_{IN}

V_{IN}=198-265V_{AC}/50Hz, Full Load



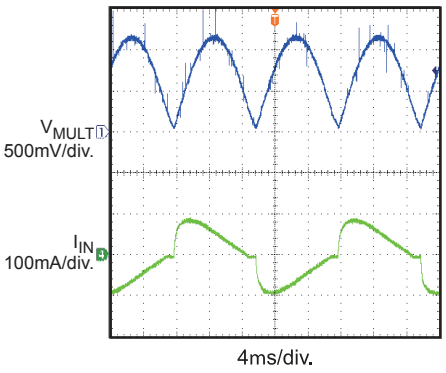
THD vs. V_{IN}

V_{IN}=198-265VAC/50Hz, Full load

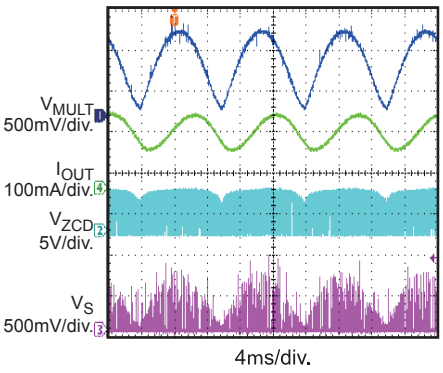


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

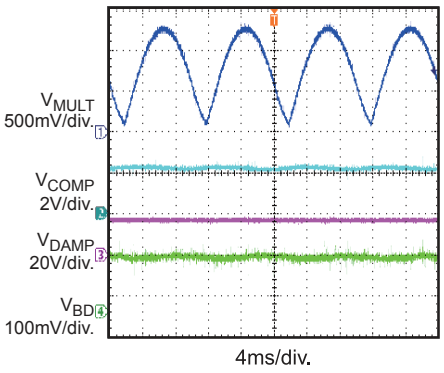
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



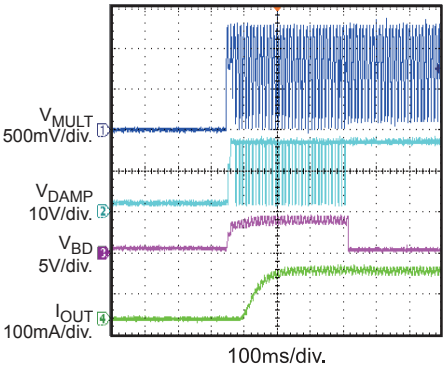
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



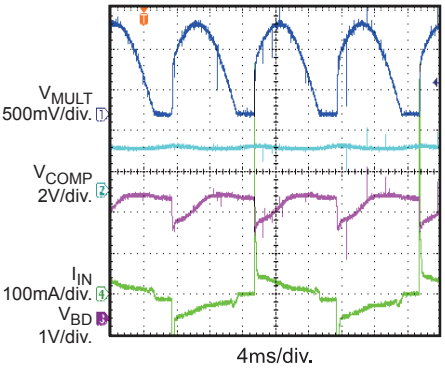
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



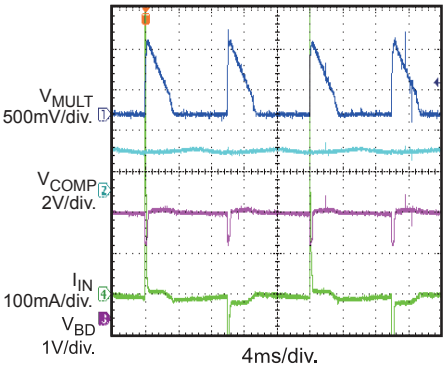
V_{IN} Start Up
V_{IN}=230V_{AC}/50Hz, Full Load



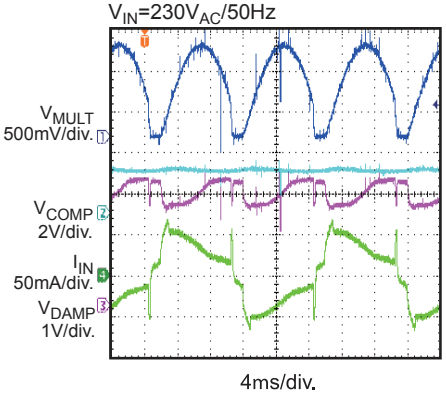
Dimming Performance
Max dimming on phase
with leading-edge dimmer
V_{IN}=230V_{AC}/50Hz



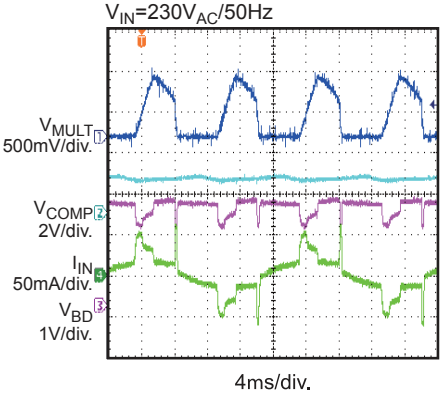
Dimming Performance
Min dimming on phase
with leading-edge dimmer
V_{IN}=230V_{AC}/50Hz



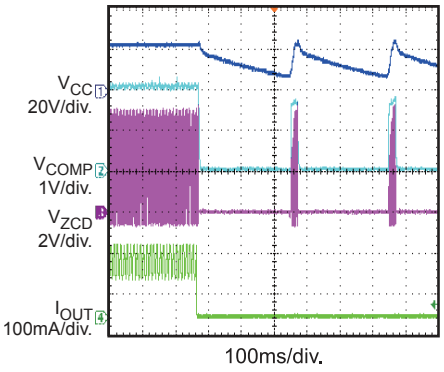
Dimming Performance
Max dimming on phase
with trailing-edge dimmer
V_{IN}=230V_{AC}/50Hz



Dimming Performance
Min dimming on phase
with trailing-edge dimmer
V_{IN}=230V_{AC}/50Hz



OVP
LED load open at normal operation
V_{IN}=230V_{AC}/50Hz

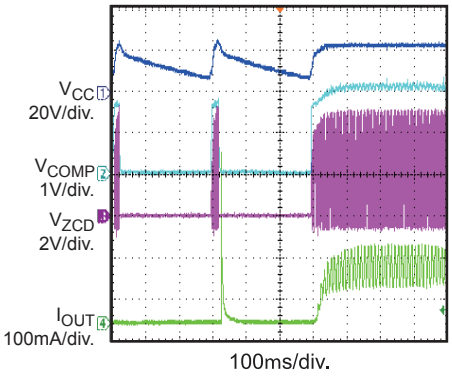


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

OVP

LED load open and recovery

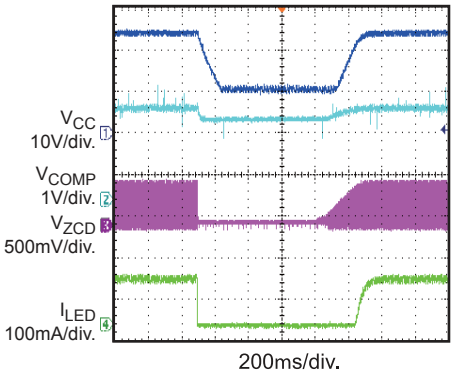
V_{IN}=230V_{AC}/50Hz



Output Short Circuit

Short LED+ to LED- and recovery

V_{IN}=230V_{AC}/50Hz



PIN FUNCTIONS

Pin # SOIC-8	Pin# MSOP-10	Name	Description
1	1	MULT	**One of the internal multiplier inputs.** Connect MULT to the tap of a resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal on MULT provides a reference signal for the internal current control loop. MULT is also used for dimmer type detection and dimming phase detection.
2	2	ZCD	**Zero-current detection**. A falling edge triggers the internal MOSFET's turn-on signal. Connect ZCD to the tap of a resistor divider from the auxiliary winding to GND. ZCD detects the over-voltage condition. Over-voltage occurs if V_{ZCD} exceeds the over-voltage protection (OVP) threshold (after a blanking time) when the internal MOSFET turns off. ZCD is also used to select the strong/weak dimming pull-down current in leading-edge dimming. ZCD detects the output short-circuit condition.
3	3	VCC	**Supply voltage.** VCC provides the supply power for both the control signal and the internal MOSFET's gate driver. Connect VCC to an external bulk capacitor (22 µF, typically).
4	5	BD	**Bleeder disable output.** BD integrates a FET. Its open-drain output is applied to pull down the external active bleeder's control signal to disable the bleeder.
5	6	D	**Internal low-side main MOSFET drain.** D is connected to the source of the external high-side main MOSFET. Also, B is connected internally to VCC through a diode and a JFET to form an internal charging circuit for VCC. There is a MOSFET and diode connected in series internally to pull up D to VCC during a fault condition, which turns off the main switch reliably. There is an intelligent dimming pull-down current source on D.
6	7	S	**Internal low-side main MOSFET source.** Connect a resistor from S to GND to sense the internal MOSFET current. An internal comparator compares the resulting voltage to the internal sinusoid shaped current reference signal to determine when the MOSFET turns off. If the voltage exceeds the upper current-clamp threshold (after the leading-edge blanking time during the turn-on interval), the gate signal turns off. Over-current occurs if V_s exceeds OCP voltage during the gate-on interval after the OCP leading-edge blanking time.
7	9	GND	**Ground**. Current return of the control signal and power signal.
8	10	COMP	**Loop compensation.** Connect COMP to a compensation network to stabilize the LED driver and accurately control the LED driver current.
--	4	DAMP	**Gate control pin of the external damping MOSFET.**
--	8	DIM	**Gate driver.** The DIM signal from the internal control logic. DIM is used to control the color temperature and brightness for warm sunset dimming or drive an external dummy Load to enlarge the dimming depth.

FUNCTIONAL BLOCK DIAGRAM

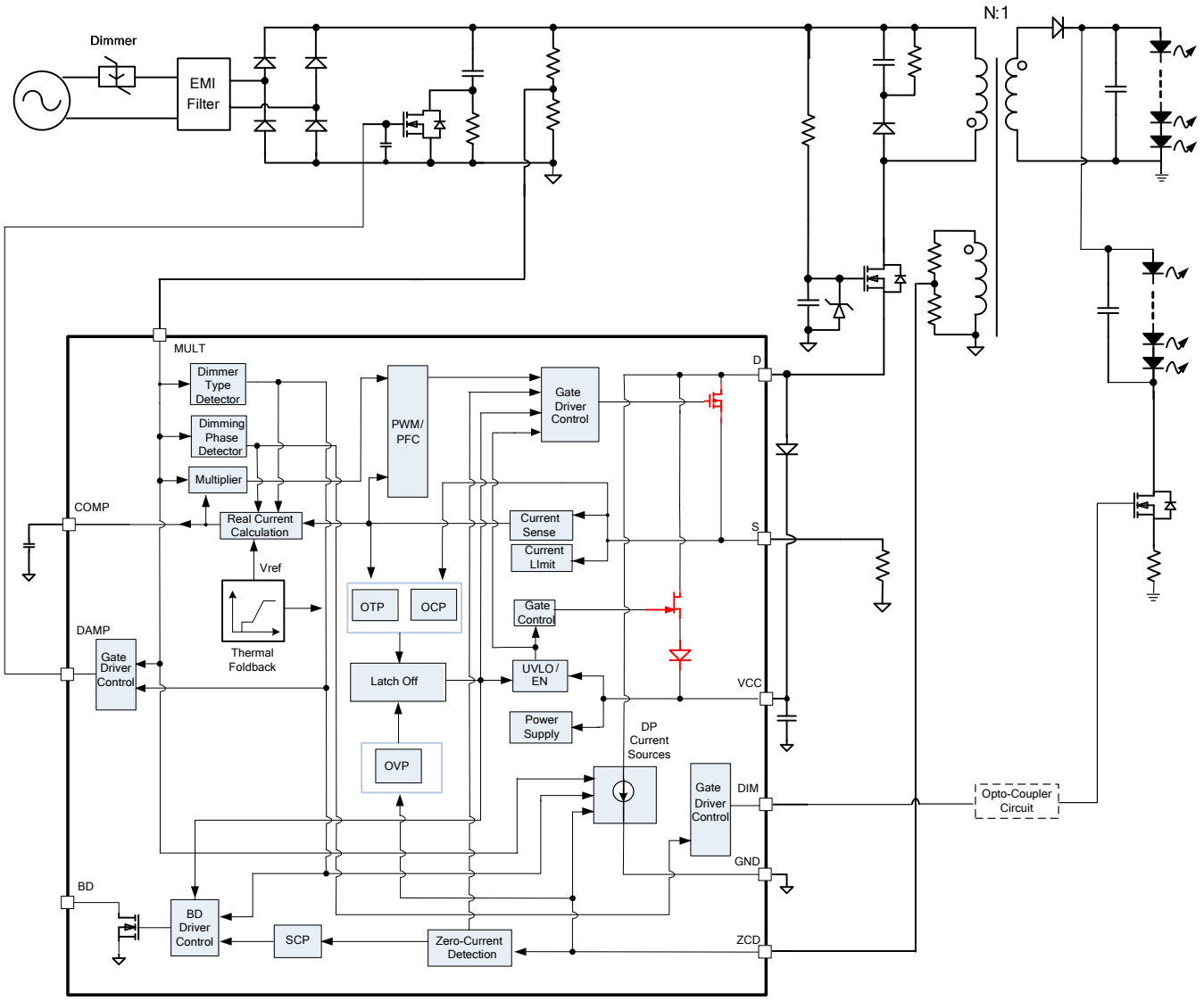


Figure 1—MP4060 functional block diagram

OPERATION

The MP4060 is a TRIAC-dimmable primary-side control, offline LED controller designed for high-performance LED lighting. The MP4060 controls accurately the LED current using the real-current control method based on primary-side information. The adaptive dimmer type detection and phase-cut-based dimming control provide good dimmer compatibility and a deep dimming range. Also, it achieves a high power factor to eliminate noise pollution on the AC line. The integrated VCC charging circuitry achieves fast start-up without any perceptible delay. The integrated thermal current foldback function can prolong the lifetime of the LED. With a duty ratio that varies with the dimming cycle, DIM easily supports color temperature and brightness control for warm sunset dimming application.

Boundary-Conduction Mode

During the external MOSFET on time (T_{ON}), the rectified input voltage applied on the primary-side inductor (Lm) makes the primary current through Lm increase linearly from zero to the peak value (I_{pk}). Then, the external MOSFET turns off, the energy stored in Lm forces the secondary-side rectifier diode to turn on, and the inductor current decreases linearly from the peak value to zero.

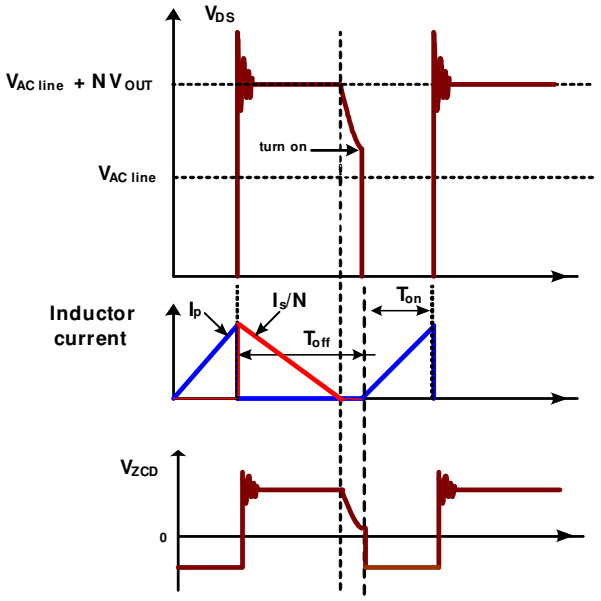


Figure 2—Boundary-conduction mode

When the current decreases to zero, the voltage drop on the main MOSFET drain-to-source falls and oscillates. The oscillation frequency is determined by the primary-side inductor and the combined parasitic capacitances. The resonance is reflected on the auxiliary winding (see Figure 2).

The zero-current detector generates the external MOSFET turn-on signal when the ZCD voltage falls below V_{ZCD_T} after a blanking time (t_{ZCD_LEB}) and ensures the MOSFET turns on at a relatively low voltage (see Figure 3).

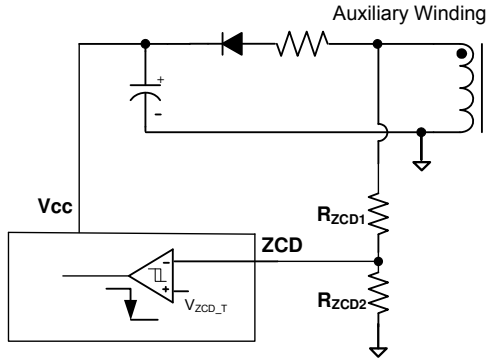


Figure 3—Zero-current detector

As a result, there are incredibly small primary switching-on losses and no secondary-diode reverse-recovery losses. This ensures high efficiency and low EMI noise.

Real-Current Control

The proprietary real-current–control method allows the MP4060 to control the secondary-side LED current based on primary-side information. The output LED mean current can be calculated approximately with Equation (1):

$$I_o \approx \frac{N \cdot V_{REF}}{2 \cdot R_s} \quad (1)$$

Where:

N is the turn ratio of the primary side to the secondary side,

V_{REF} is the internal reference voltage (typically 0.414), and

R_S is the sense resistor between the internal MOSFET source and GND.

Power-Factor Correction

MULT is connected to the tap of a resistor divider from the rectified instantaneous line voltage, driving a sinusoidal multiplier output. This signal provides the reference for the current comparator, which shapes the primary peak current into a sinusoid and has the same phase with the input line voltage. This guarantees a high power factor (see Figure 4).

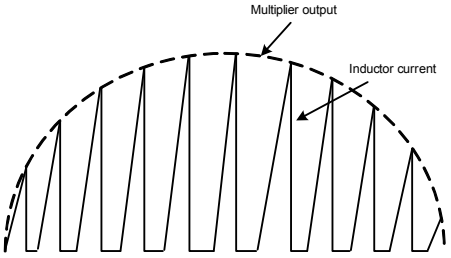


Figure 4—Power-factor correction

The multiplier's maximum output voltage to the current comparator is clamped to $V_{S\_CLAMP\_H}$ to limit the cycle-by-cycle current. The multiplier's minimum output voltage is clamped to $V_{S\_CLAMP\_L}$ to ensure a turn-on signal during the TRIAC dimming-off interval, which pulls down the rectifier input voltage and accurately detects the dimming phase.

VCC Timing Sequence

The VCC timing sequence is shown in Figure 5. Initially, VCC is charged through the internal charging circuit from the AC line. When VCC reaches VCC_H, the internal charging circuit stops charging, the control logic initializes, and the internal main MOSFET begins to switch. The auxiliary winding takes over the power supply. However, the initial auxiliary winding positive voltage may not be large enough to charge VCC, causing VCC to drop. Instead, if the VCC voltage drops below the VCC_L threshold, the internal charging circuit triggers and charges VCC to VCC_H again. This cycle repeats until the auxiliary winding voltage is high enough to power VCC

If any fault occurs during this time, the switching and the internal charging circuit stop, and VCC drops. When VCC drops below VCC_{EN}, the internal re-charge is enabled to auto-restart.

To simplify the power supply circuitry, an external charging diode is applied between D (the source of the external power MOSFET) and the VCC capacitor (see Typical Application). D takes over the VCC power supply at normal operation, without an auxiliary winding. If any fault occurs, the system re-starts after the input AC line powers down/up again.

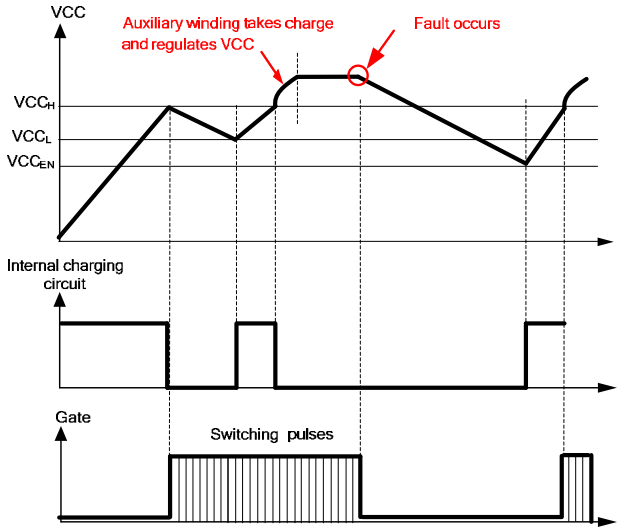


Figure 5—VCC timing sequence

Auto Start

The MP4060 contains an auto starter that starts timing when the MOSFET turns off. If ZCD fails to send a turn-on signal after t_{START}, automatically the starter sends a turn-on signal to avoid an unnecessary shutdown.

Minimum off Time

The MP4060 operates with a variable switching frequency. The frequency changes with the instantaneous input BUS voltage. In order to limit the maximum frequency and get good EMI performance, the MP4060 employs an internal minimum off-time limiter.

Leading-Edge Blanking

In order to avoid premature switching-pulse termination due to the parasitic capacitances discharging when the MOSFET turns on, an internal leading-edge-blanking (LEB) time is introduced on S. The current comparator blocks the input path from S during the blanking time (see Figure 6)

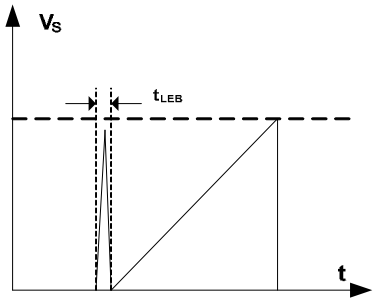


Figure 6—Leading-edge blanking

Output Over-Voltage Protection (OVP)

Output over-voltage protection (OVP) prevents the components from over-voltage damage. The voltage of the auxiliary winding positive plateau is proportional to the output voltage, so the OVP block monitors this auxiliary winding voltage to apply an OVP function (see Figure 7). Once ZCD voltage exceeds V_{ZCD_OVP}, the OVP signal is triggered, the gate driver turns off, and the IC works in quiescent current mode. When the VCC voltage drops below the UVLO threshold, the IC shuts down and the system re-starts. The output OVP set point is calculated with Equation (2):

$$V_{out\_ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1}+R_{ZCD2}} = V_{ZCD\_OVP} \quad (2)$$

Where:

V_{OUT_OVP} is the output OVP threshold,

N_{AUX} is the turns of the auxiliary winding, and

N_{SEC} is the turns of the secondary winding.

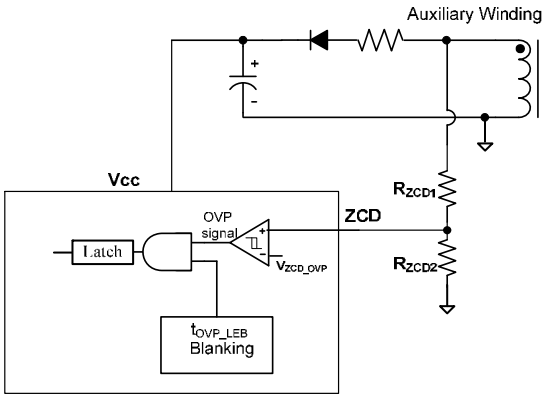


Figure 7—OVP sampling circuit

To avoid switch-off spikes mis-triggering OVP, OVP sampling has a t_{OVP_LEB} blanking period (see Figure 8).

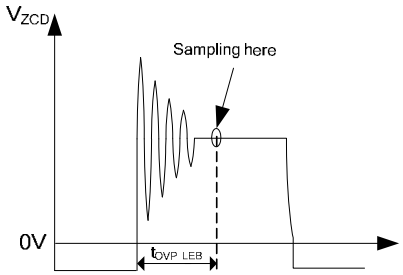


Figure 8—ZCD voltage & OVP sampling

Cycle-by-Cycle Current Limit

There is cycle-by-cycle current limit on S. When the voltage on S reaches $V_{S\_CLAMP\_H}$ (after a blanking time), the switching turns off to limit the peak current value.

Primary Over-Current Protection (OCP)

S has an internally integrated comparator for primary side OCP. When the gate is on, the comparator is enabled. Over-current occurs when VS exceeds V_{OCP} after a blanking time. The IC shuts down and re-starts after VCC drops below UVLO. The OCP function block diagram is shown in Figure 9.

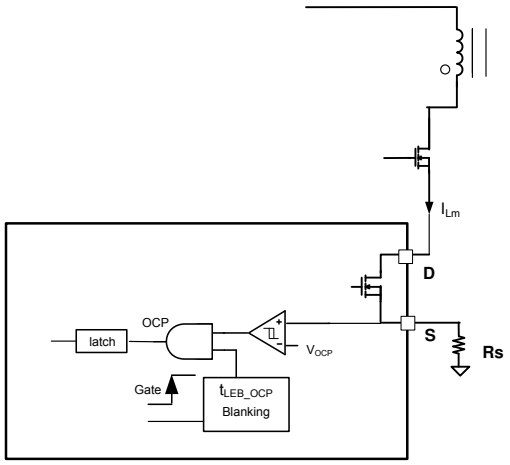


Figure 9—Over-current protection circuit

LED Short-Circuit Protection (SCP)

When an LED short circuit occurs, the IC reduces the switching frequency to 7 kHz. The the output power at this condition is limited within a safe range.

Thermal Protection

To prevent the IC and the system from any lethal thermal damage (when the junction temperature exceeds T_{START}), the MP4060 chops the reference to decrease the output current, which limits the rising temperature speed of the IC. Typically, the output current drops to 20 percent when the IC temperature rises to T_{SD}. Once it exceeds T_{SD}, the MP4060 shuts down the switching cycle and is latched until VCC drops below UVLO. When the junction temperature drops a recovery hysteresis (T_{HYS}), the chip re-starts again.

Bleeder Disable

If the external active bleeder is applied to improve the TRIAC-dimming compatibility, the MP4060 features a bleeder disable function to pull down the bleeder transistor by BD. This improves system efficiency and thermal performance if the bleeder is useless in certain conditions. Figure 10 shows the bleeder disable circuit.

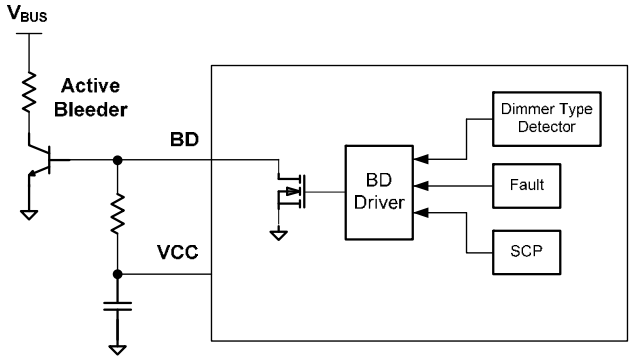


Figure 10—Bleeder disable circuit

The integrated BD FET works in an open-drain configuration when VCC drops below UVLO or the active bleeder is activated.

The BD FET is turned on to pull down the bleeder transistor under the following conditions:

I. The dimmer is not connected to the driver.

II. The fault (OVP/OCP/OTP) triggers.

III. The system works in auto-restart mode over t_{SC}. For example, SCP occurs.

The BD timing sequence is shown in Figure 11.

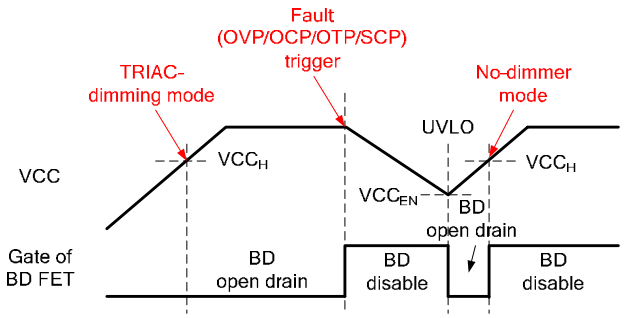


Figure 11—BD timing sequence

Adaptive Dimmer Type Detection

The MP4060 integrates adaptive dimmer type detection to detect accurately which kind of dimmer is connected at the system start-up (leading-edge dimmer, trailing-edge dimmer, or no dimmer). The MP4060 works in different modes depending on the dimmer types to achieve the best dimmer compatibility with the highest performance.

Phase-Cut-Based Dimming Control

The MP4060 implements phase-cut-based dimming control (both for leading-edge and trailing-edge dimmers). For leading-edge dimmers, most are TRIAC-based. Usually, the TRIAC dimmer consists of a bi-directional SCR and an adjustable turn-on phase. Figure 12 shows the leading-edge TRIAC dimmer waveforms.

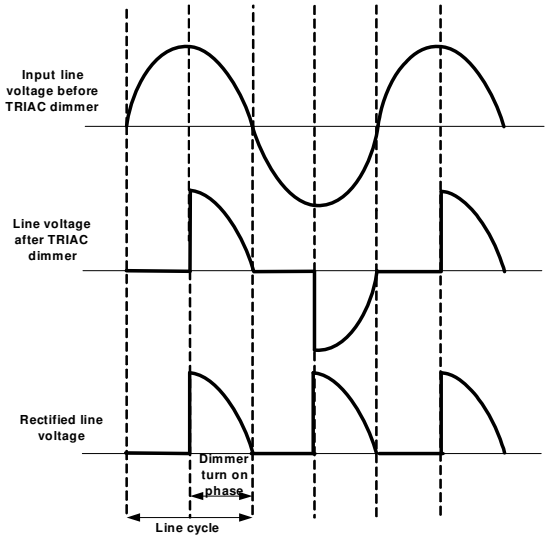


Figure 12—Leading-edge dimmer waveforms

For trailing-edge dimmers, the waveforms are shown in Figure 13.

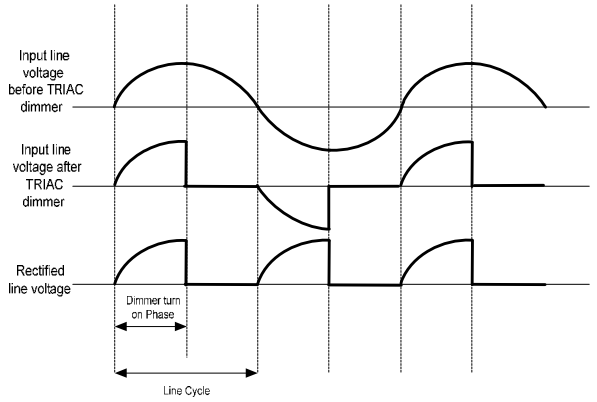


Figure 13—Trailing-edge dimmer waveforms

The MP4060 detects the dimming turn-on cycle through MULT. Based on the turn-on cycle, the control circuitry adjusts the internal reference voltage. MULT voltage exceeding V_{MULT_ON} is recognized as a dimmer turn-on signal. MULT voltage below V_{MULT_OFF} is recognized as a dimmer turn-off signal. The MP4060 has a 30 percent line-cycle-detection blanking time at each line cycle. The real phase detector output is added to this blanking time to determine the reference voltage. If it is higher than 100 percent, the reference voltage is clamped to 100 percent (see Figure 14). This means if the turn-on cycle exceeds 70 percent of the line cycle, the reference maintains the maximum value, which means the maximum output current with different dimmers is almost the same as the rated output current.

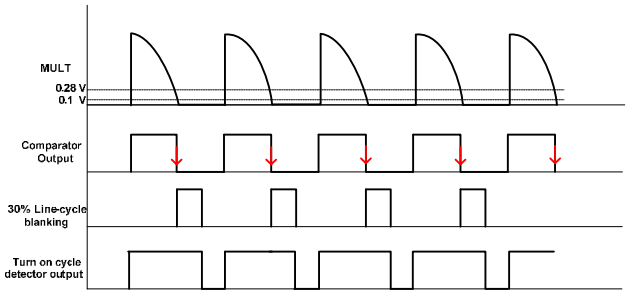


Figure14—Dimming turn-on cycle detector

The internal reference voltage decreases when the turn-on cycle decreases to less than 70 percent of the line cycle, lowering the output current. As the dimming turn-on cycle decreases, the COMP voltage decreases. For a leading-edge dimmer, once the COMP voltage reaches V_{COMPL_LD}, it is clamped. The output current decreases slowly to maintain the TRIAC holding current and avoid random flicker. Figure15 shows the relationship between the leading-edge dimming turn-on phase and the output current.

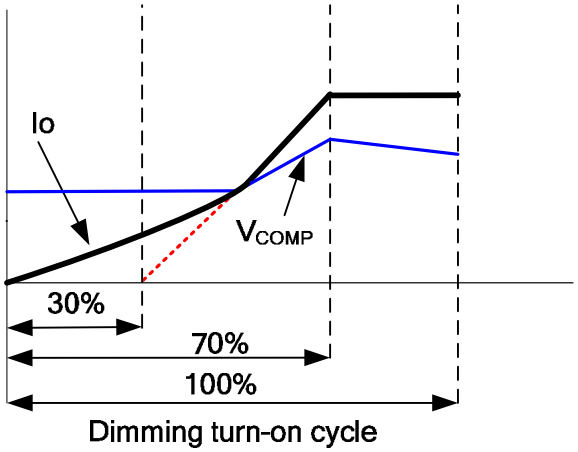


Figure 15—Leading-edge dimming curve

For a trailing-edge dimmer, there is no holding current. The COMP voltage is clamped at a lower level (V_{COML_TL}) to get a deeper dimming depth. Figure 16 shows the relationship between the trailing-edge dimming turn-on phase and the output current.

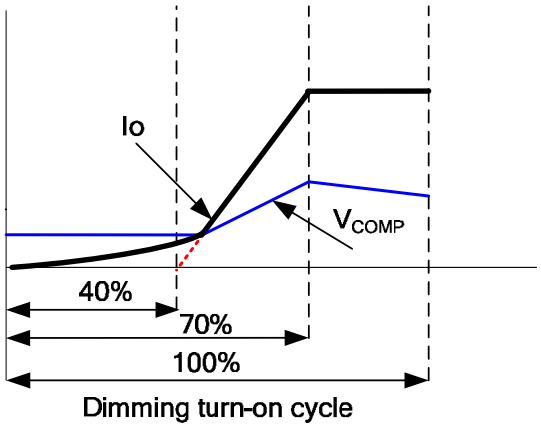


Figure 16:—Trailing-edge dimming curve

Dimming Pull-Down Current Source

There are three kinds of dimming pull-down current sources in MP4060. The I_{DP_TL} current source is for trailing-edge dimming, the other two (weak/strong) current sources are for leading-edge dimming. The dimming pull-down current is used to pull down the rectified line voltage to zero quickly to avoid a mis-detection on MULT.

If the leading-edge dimmer is detected, the dimming pull-down current source turns on when MULT decreases to $V_{MULT\_DP\_ON\_LD,}$ and it turns off when MULT increases to $V_{MULT\_DP\_OFF\_LD}$. If the trailing-edge dimmer is detected, the dimming pull-down current source turns on when MULT decreases to $V_{MULT\_DP\_ON\_TL,}$ and it turns off when MULT increases to $V_{MULT\_DP\_OFF\_TL}$.

The weak/strong dimming pull-down current sources are selected through different resistances on ZCD. Figure 17 shows the selected logic:

If $I_{DP\_DET\_LD}$ *(R1+R2//R3) $\geqslant V_{EN\_DP\_STR\_LD}$, a strong dimming pull-down current source is selected; otherwise, a weak dimming pull-down current source is selected.

In real application design, the weak/strong dimming pull-down current selection is related to the detailed application SPEC.

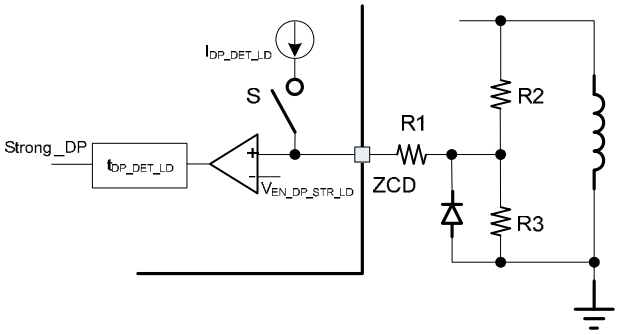


Figure 17—Weak/strong dimming pull-down current source selection

Damping Circuit Control

If a leading-edge dimmer or trailing-edge dimmer is detected, the damping circuit is enabled to limit the inrush current the moment the dimmer turns on. If no dimmer is detected, the damping circuit is disabled by pulling up the damp pin voltage, so the damping resister is shorted by the damping MOSFET. The damp pin voltage is pulled up if MULT voltage increases higher than $V_{MULT\_DAMP\_ON.}$ It is pulled down when MULT voltage decreases lower than $V_{MULT\_DAMP\_OFF}$. The maximum pull-up current source is 100 μA while the maximum pull-down current source is 400 μA.

Color Temperature and Brightness Control for Warm Sunset Dimming application

The color temperature and brightness control circuit is shown in Figure 18.

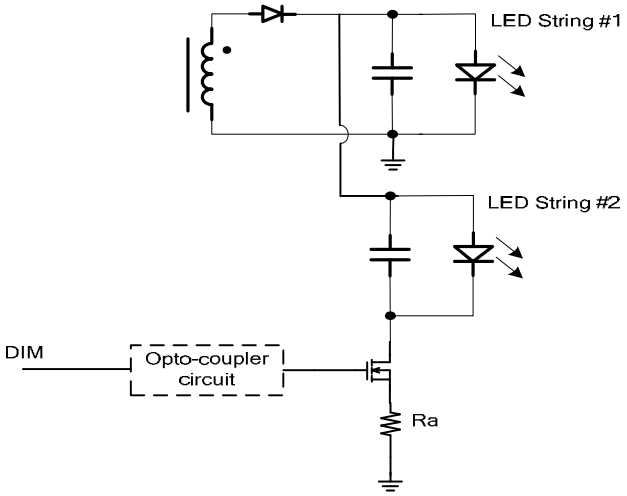


Figure 18—Color temperature and brightness control circuit

DIM of MP4060 outputs a driving signal for the external MOSFET. The DIM control logic is shown in Figure 19.

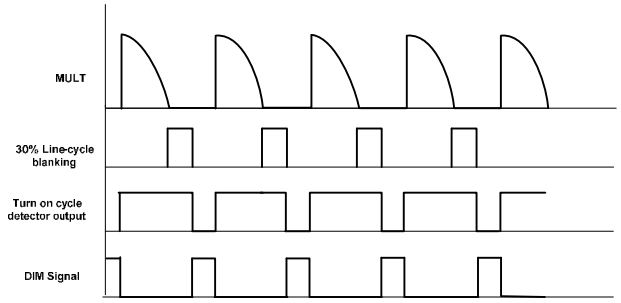


Figure 19—DIM signal logic

The DIM turn-on signal is the compliment signal of the dimming turn-on signal. This means the longer the dimming turn-on cycle, the smaller the DIM turn-on cycle. The DIM stays low and the output current flows only through the 1st LED string when the dimming turn-on cycle is greater than 70 percent. As the dimming turn-on cycle decreases, the DIM turn-on duty cycle proportionally increases the current in the 2nd LED string. The total current through the 1st string and the 2nd string remains constant. This current balance achieves color temperature and brightness control. The maximum current through

the 2nd string is adjusted by changing the resistance of Ra.

Dimming Depth Enlargement

Driving a MOSFET to pull down a resistor from the auxiliary winding to GND forms a dummy load, which helps distribute the output current. DIM working timing means a shorter the dimming duty cycle results in a higher dummy load distribution current. This method enlarges the dimming depth. The dimming depth enlargement circuit is shown in Figure 20.

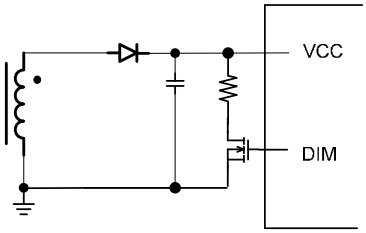


Figure 20—Dimming depth enlargement circuit

TYPICAL APPLICATION CIRCUITS

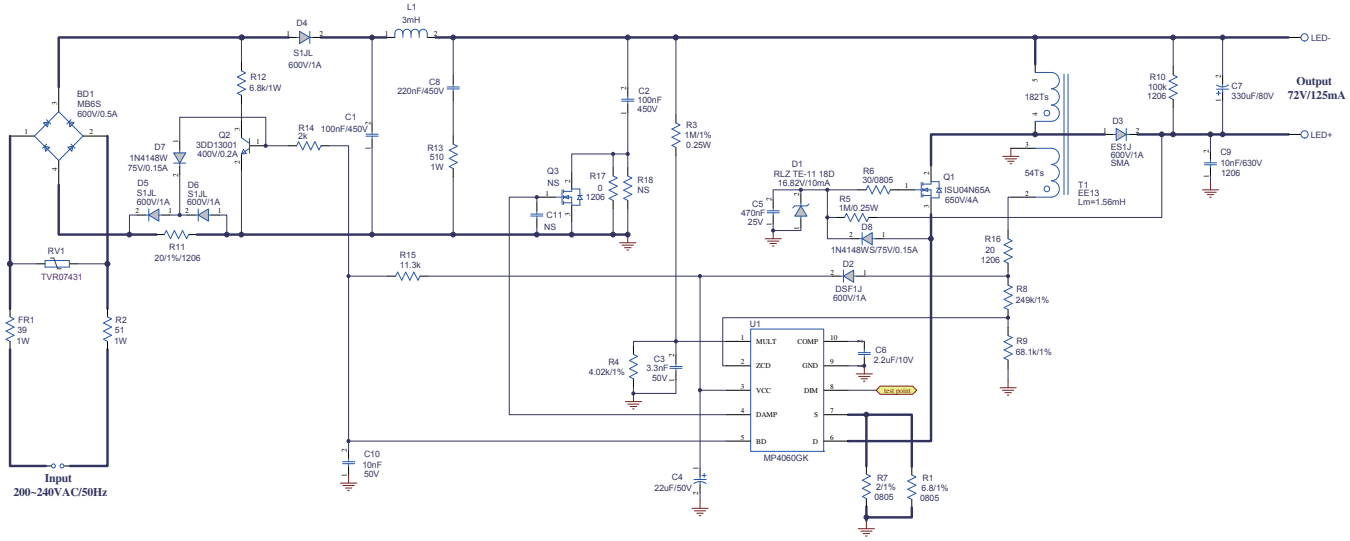
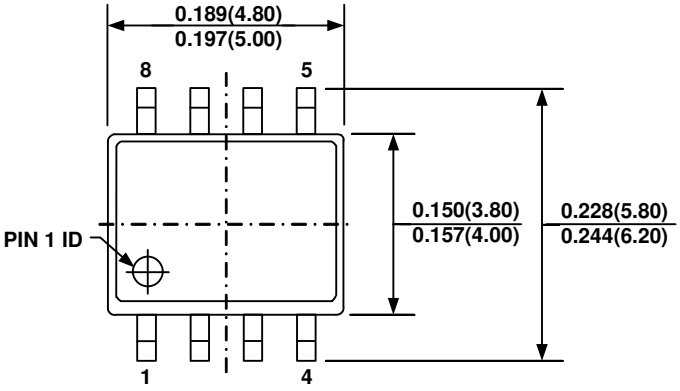


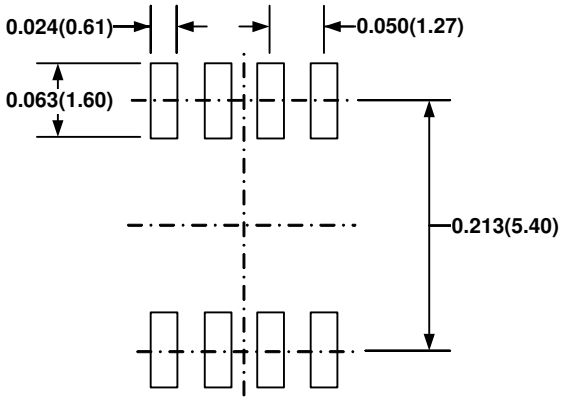
Figure 21—A19 bulb driver, 200 VAC-240 VAC/50 Hz input, V_O = 72 V, I_O = 125 mA, buck-boost converter, high-performance. EVB model: EV4060-K-00A

PACKAGE INFORMATION

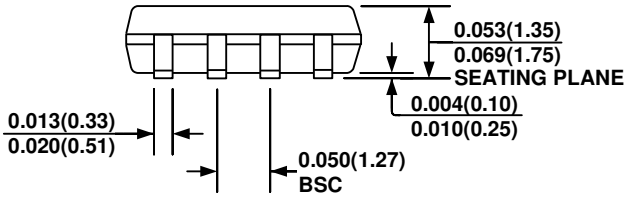
SOIC-8



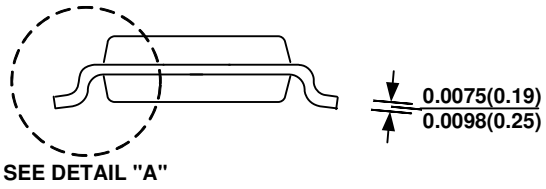
TOP VIEW



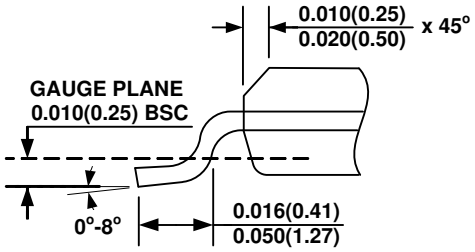
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

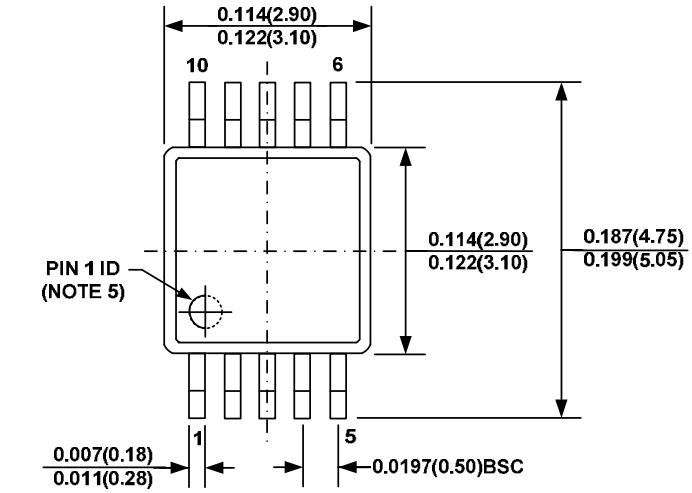


DETAIL "A"

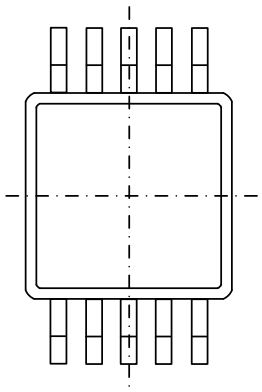
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

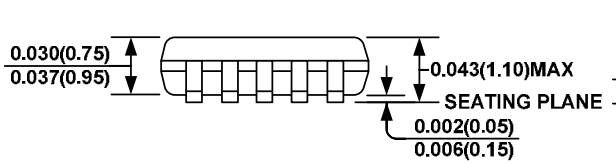
MSOP-10



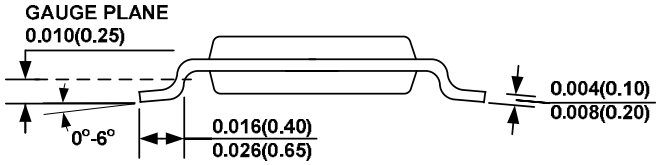
TOP VIEW



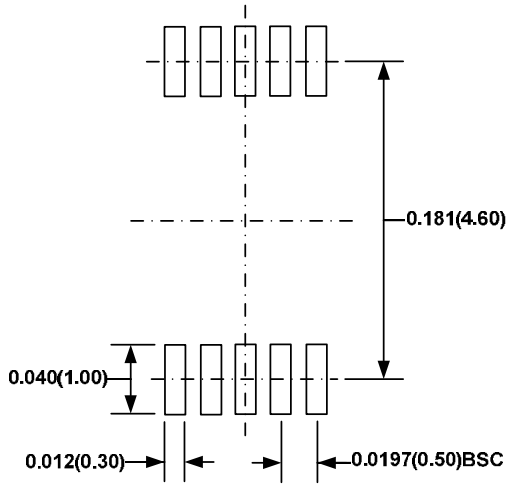
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.