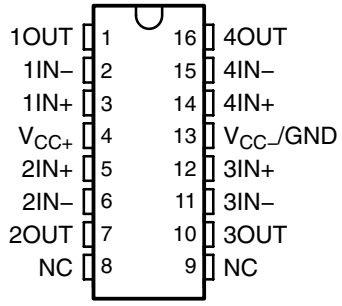
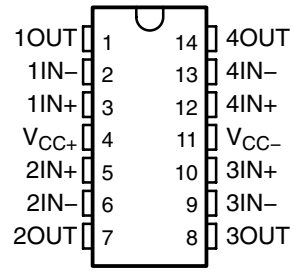
- **Single-Supply Operation: Input Voltage Range Extends to Ground, and Output Swings to Ground While Sinking Current**
- **Input Offset Voltage 300 μV Max at 25°C for LT1014**
- **Offset Voltage Temperature Coefficient 2.5 μV/°C Max for LT1014**
- **Input Offset Current 1.5 nA Max at 25°C for LT1014**
- **High Gain 1.2 V/μV Min (R_L = 2 kΩ), 0.5 V/μV Min (R_L = 600 Ω) for LT1014**
- **Low Supply Current 2.2 mA Max at 25°C for LT 1014**
- **Low Peak-to-Peak Noise Voltage 0.55 μV Typ**
- **Low Current Noise 0.07 pA/$\sqrt{\text{Hz}}$ Typ**

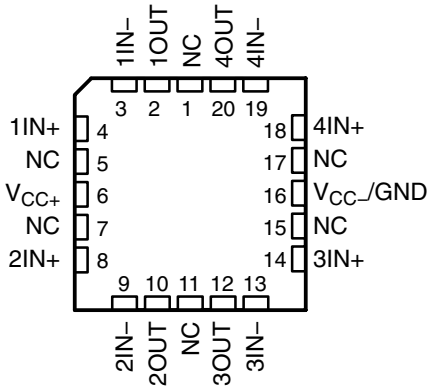
DW PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The LT1014, LT1014A, and LT1014D are quad precision operational amplifiers with 14-pin industry-standard configuration. They feature low offset-voltage temperature coefficient, high gain, low supply current, and low noise.

The LT1014, LT1014A, and LT1014D can be operated with both dual ±15-V and single 5-V power supplies. The common-mode input voltage range includes ground, and the output voltage can also swing to within a few milivolts of ground. Crossover distortion is eliminated.

The LT1014C and LT1014D are characterized for operation from 0°C to 70°C. The LT1014I and LT1014DI are characterized for operation from –40°C to 105°C. The LT1014M, LT1014AM and LT1014DM are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS†

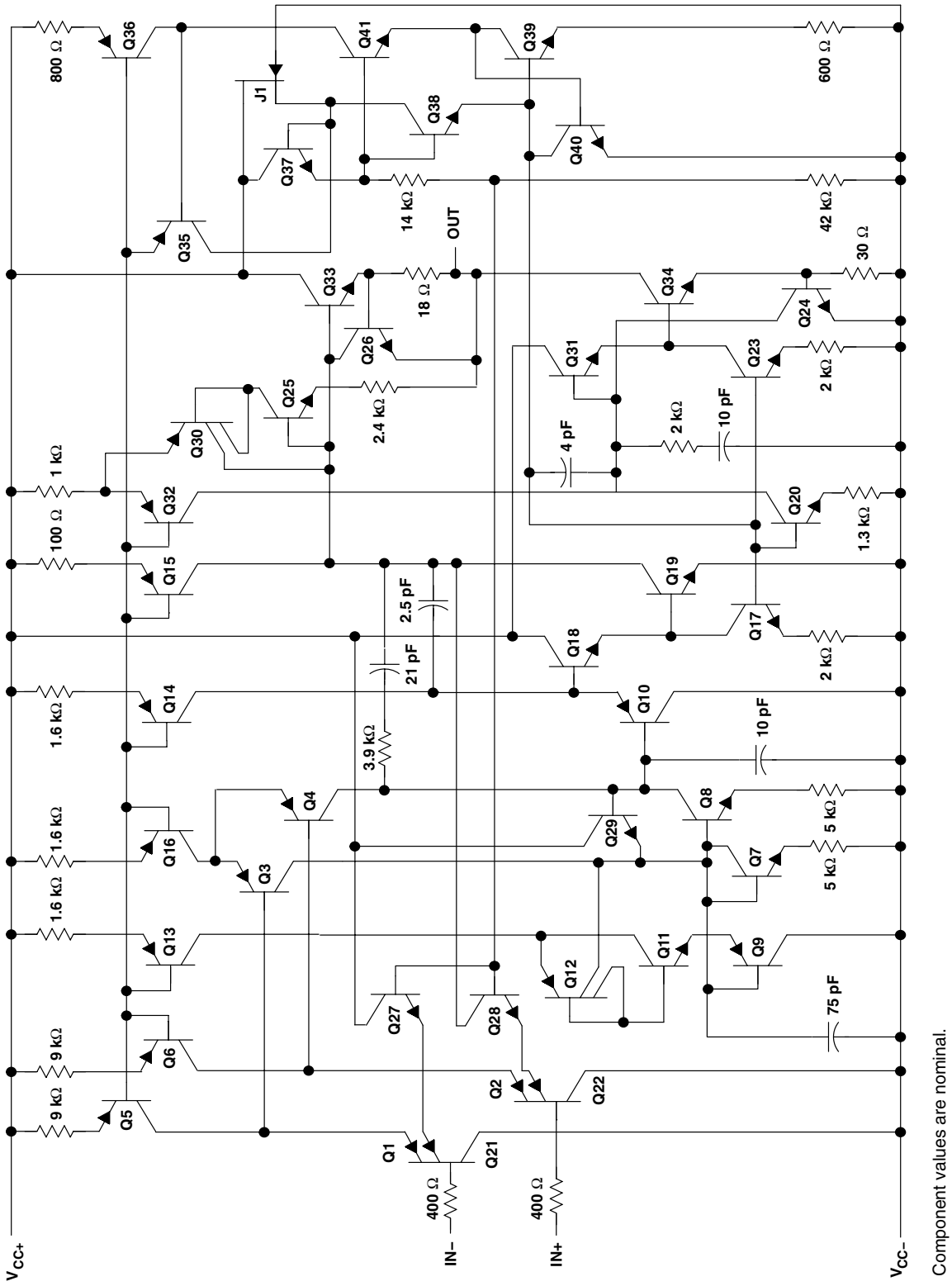
T_A	V_{IO} max AT 25°C	PACKAGED DEVICES‡			
		SMALL OUTLINE (DW)§	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	300 μV	—	—	—	LT1014CN
	800 μV	LT1014DDW	—	—	LT1014DN
–40°C to 105°C	300 μV	—	—	—	LT1014IN
	800 μV	LT1014DIDW	—	—	LT1014DIN
–55°C to 125°C	180 μV	—	LT1014AMFK	LT1014AMJ	—
	300 μV	—	LT1014MFK	LT1014MJ	LT1014MN
	800 μV	LT1014DMDW	—	—	LT1014DMN

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

§ The DW package is available taped and reeled. Add the suffix R to the device type (e.g., LT1014DDWR).

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} . . . . . 22 V
V_{CC-} . . . . . –22 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage range, V_I (any input) (see Note 1) . . . . . V_{CC-} – 5 V to V_{CC+}
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . . . Unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: LT1014C, LT1014D . . . . . –0°C to 70°C
LT1014I, LT1014DI . . . . . –40°C to 105°C
LT1014M, LT1014AM, LT1014DM . . . . . –55°C to 125°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mV	8.2 mW/°C	656 mW	369 mW	205 mW
FK	1375 mV	11.0 mW/°C	880 mW	495 mW	275 mW
J	1375 mV	11.0 mW/°C	880 mW	495 mW	275 mW
N	1150 mV	9.2 mW/°C	736 mW	414 mW	230 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1014C			LT1014D			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		60	300		200	800	μV
			Full range			550			1000	
$\alpha_{V_{IO}}$	Temperature coeficient of input offset voltage		Full range		0.4	2.5		0.7	5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.15	1.5		0.15	1.5	nA
			Full range			2.8			2.8	
I_{IB}	Input bias current		25°C		–12	–30		–12	–30	nA
			Full range			–38			–38	
V_{ICR}	Common-mode input voltage range		25°C	–15 to 13.5	–15.3 to 13.8		–15 to 13.5	–15.3 to 13.8		V
			Full range	–15 to 13			–15 to 13			
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±14		±12.5	±14		V
			Full range	±12			±12			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 600 Ω	25°C	0.5	2		0.5	2		V/μV
		V_O = ±10 V, R_L = 2 kΩ	25°C	1.2	8		1.2	8		
			Full range	0.7			0.7			
CMRR	Common-mode rejection ratio	V_{IC} = –15 V to 13.5 V	25°C	97	117		97	117		dB
		V_{IC} = –15 V to 13 V	Full range	94			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±18 V	25°C	100	117		100	117		dB
			Full range	97			97			
	Channel separation	V_O = ±10 V, R_L = 2 kΩ	25°C	120	137		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.55	mA
			Full range			0.6			0.6	

† Full range is 0°C to 70°C.
‡ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1014C			LT1014D			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		250	950	μV
			Full range			570			1200	
I_{IO}	Input offset current		25°C		0.2	2		0.2	2	nA
			Full range			6			6	
I_{IB}	Input bias current		25°C		−15	−50		−15	−50	nA
			Full range			−90			−90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		V
			Full range	0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10	
			Full range			13			13	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		
			Full range	3.2			3.2			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1		V/μV
I_{CC}	Supply current per amplifier		25°C		0.3	0.5		0.3	0.5	mA
			Full range			0.55			0.55	

† Full range is 0°C to 70°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1014I			LT1014DI			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		60	300		200	800	μV
			Full range			550			1000	
$\alpha_{V_{IO}}$	Temperature coeficient of input offset voltage		Full range		0.4	2.5		0.7	5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.15	1.5		0.15	1.5	nA
			Full range			2.8			2.8	
I_{IB}	Input bias current		25°C		–12	–30		–12	–30	nA
			Full range			–38			–38	
V_{ICR}	Common-mode input voltage range		25°C	–15 to 13.5	–15.3 to 13.8		–15 to 13.5	–15.3 to 13.8		V
			Full range	–15 to 13			–15 to 13			
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±14		±12.5	±14		V
			Full range	±12			±12			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 600 Ω	25°C	0.5	2		0.5	2		V/μV
		V_O = ±10 V, R_L = 2 kΩ	25°C	1.2	8		1.2	8		
			Full range	0.7			0.7			
CMRR	Common-mode rejection ratio	V_{IC} = –15 V to 13.5 V	25°C	97	117		97	117		dB
			Full range	94			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±18 V	25°C	100	117		100	117		dB
			Full range	97			97			
	Channel separation	V_O = ±10 V, R_L = 2 kΩ	25°C	120	137		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.55	mA
			Full range			0.6			0.6	

† Full range is –40°C to 105°C.
‡ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1014I			LT1014DI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		250	950	μV
			Full range			570			1200	
I_{IO}	Input offset current		25°C		0.2	2		0.2	2	nA
			Full range			6			6	
I_{IB}	Input bias current		25°C		–15	–50		–15	–50	nA
			Full range			–90			–90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	–0.3 to 3.8		0 to 3.5	–0.3 to 3.8		V
			Full range	0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10	
			Full range			13			13	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		
			Full range	3.2			3.2			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1		V/μV
I_{CC}	Supply current per amplifier		25°C		0.3	0.5		0.3	0.5	mA
			Full range			0.55			0.55	

† Full range is –40°C to 105°C.

operating characteristics, V_{CC}+ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1014M			LT1014AM			LT1014DM			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		60	300		60	180		200	800	μV
			Full range			550			350			1000	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		Full range		0.5	2.5		0.5	2		0.5	2.5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.5			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.15	1.5		0.15	0.8		0.15	1.5	nA
			Full range			5			2.8			5	
I_{IB}	Input bias current		25°C		–12	–30		–12	–20		–12	–30	nA
			Full range			–45			–30			–45	
V_{ICR}	Common-mode input voltage range		25°C	–15 to 13.5	–15.3 to 13.8		–15 to 13.5	–15.3 to 13.8		–15 to 13.5	–15.3 to 13.8		V
			Full range	–14.9 to 13			–14.9 to 13			–14.9 to 13			
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±11.5			±12			±11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 600 Ω	25°C	0.5	2		0.8	2.2		0.5	2		V/μV
		V_O = ±10 V, R_L = 2 kΩ	25°C	1.2	8		1.5	8		1.2	8		
			Full range	0.25			0.4			0.25			
CMRR	Common-mode rejection ratio	V_{IC} = –15 V to 13.5 V	25°C	97	117		100	117		97	117		dB
		V_{IC} = –14.9 V to 13 V	Full range	94			96			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±18 V	25°C	100	117		103	117		100	117		dB
			Full range	97			100			97			
	Channel separation	V_O = ±10 V, R_L = 2 kΩ	25°C	120	137		123	137		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	300		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			4			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.50		0.35	0.55	mA
			Full range			0.7			0.6			0.7	

† Full range is –55°C to 125°C.
‡ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1014M			LT1014AM			LT1014DM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50Ω	25°C		90	450		90	280		250	950	μV
			Full range		400	1500		400	960		800	2000	
		R_S = 50Ω, V_{IC} = 0.1 V	125°C		200	750		200	480		560	1200	
I_{IO}	Input offset current		25°C		0.2	2		0.2	1.3		0.2	2	nA
			Full range			10			7			10	
I_{IB}	Input bias current		25°C		–15	–50		–15	–35		–15	–50	
			Full range			–120			–90			–120	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	–0.3 to 3.8		0 to 3.5	–0.3 to 3.8		0 to 3.5	–0.3 to 3.8		V
			Full range	0.1 to 3			0.1 to 3			0.1 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600Ω to GND	25°C		5	10		5	10		5	10	
			Full range			18			15			18	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high,	25°C	3.4	4		3.4	4		3.4	4		
		R_L = 600Ω to GND	Full range	3.1			3.2			3.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500Ω	25°C		1			1			1		V/μV
I_{CC}	Supply current per amplifier		25°C		0.3	0.5		0.3	0.45		0.3	0.5	mA
			Full range			0.65			0.55			0.65	

† Full range is –55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

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I_{IO}	Input offset current vs Free-air temperature		4
I_{IB}	Input bias current vs Free-air temperature		5
V_{IC}	Common-mode input voltage vs Input bias current		6
A_{VD}	Differential voltage amplification	vs Load resistance	7, 8
		vs Frequency	9, 10
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	Pulse response (large signal) vs Time		20, 22, 23
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TYPICAL CHARACTERISTICS†

**LT1014
INPUT OFFSET VOLTAGE
vs
BALANCED SOURCE RESISTANCE**

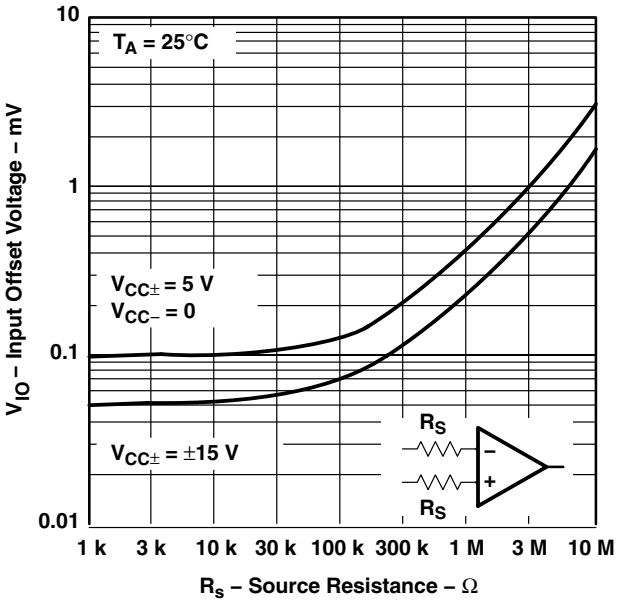


Figure 1

**INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE**

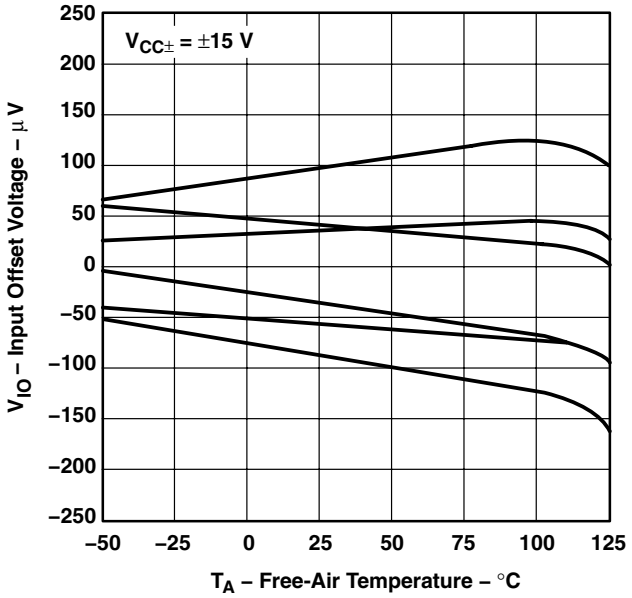


Figure 2

**WARM-UP CHANGE IN INPUT OFFSET VOLTAGE
vs
ELAPSED TIME**

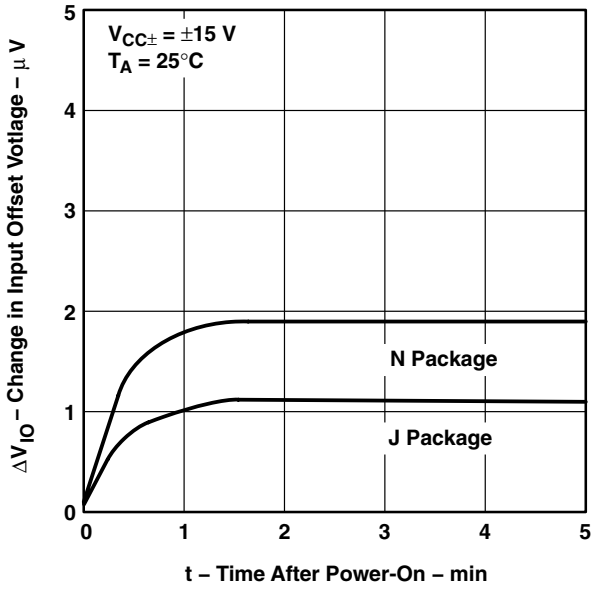


Figure 3

**INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

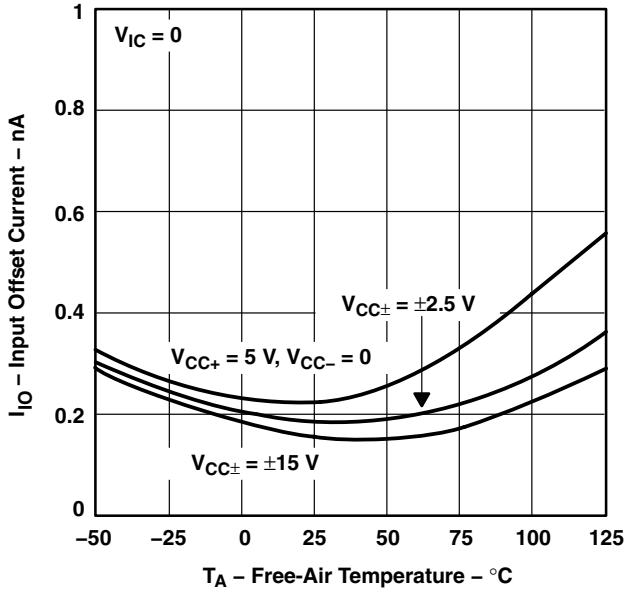


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

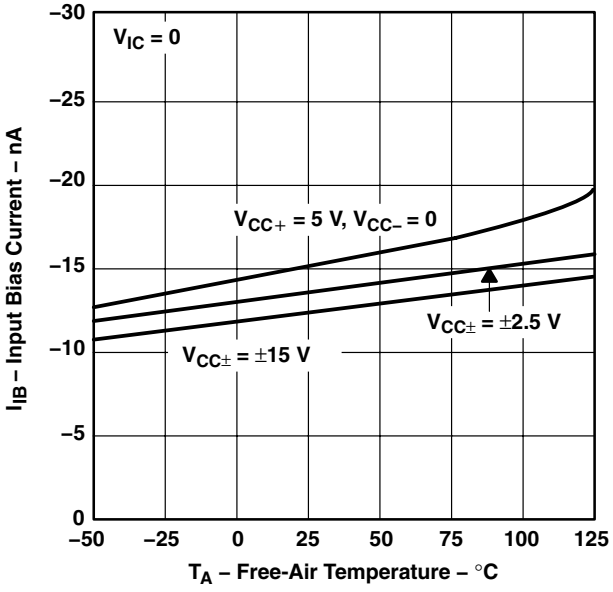


Figure 5

COMMON-MODE INPUT VOLTAGE vs INPUT BIAS CURRENT

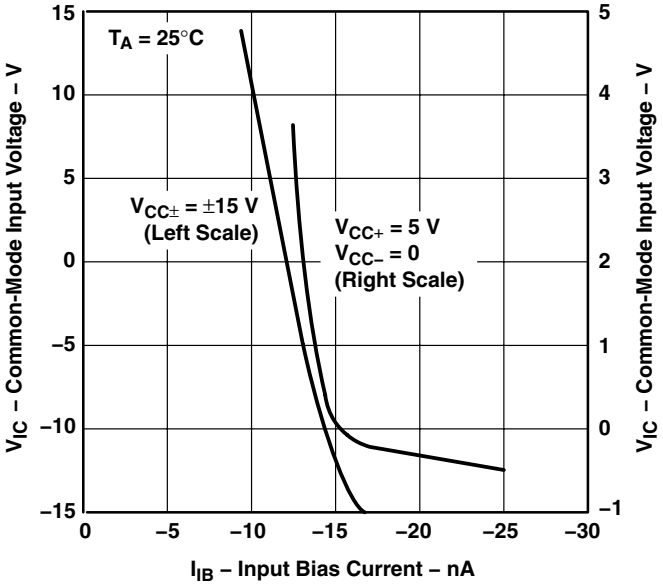


Figure 6

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

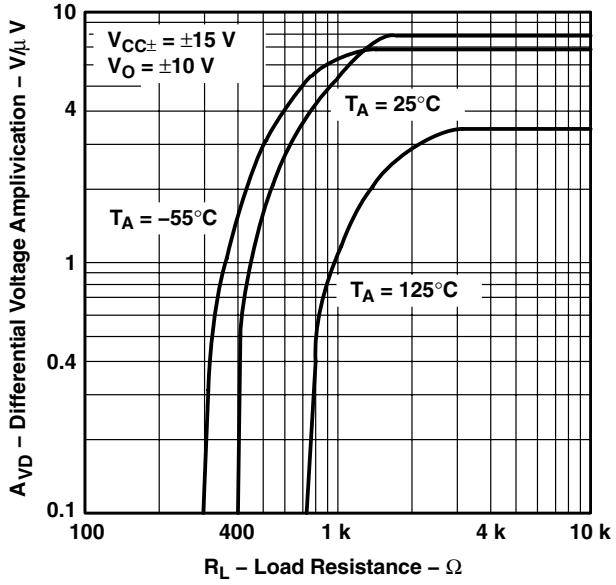


Figure 7

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

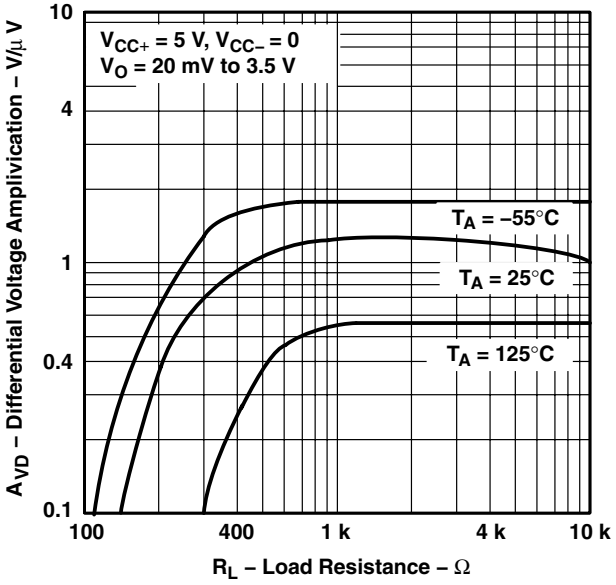


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

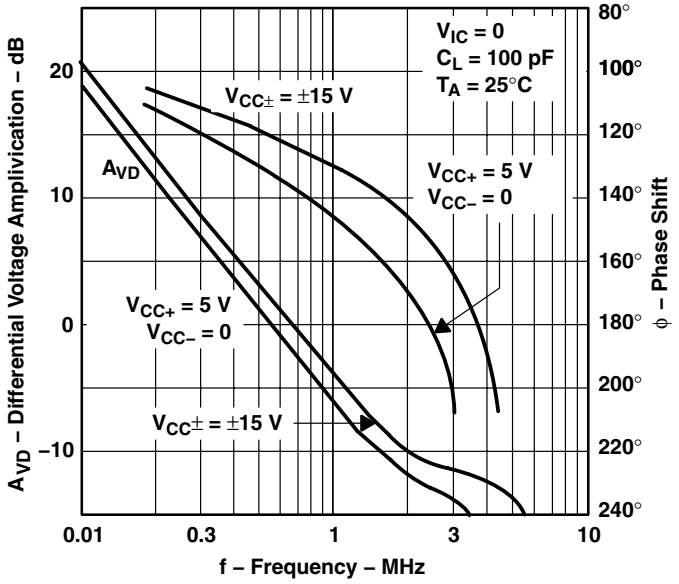


Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

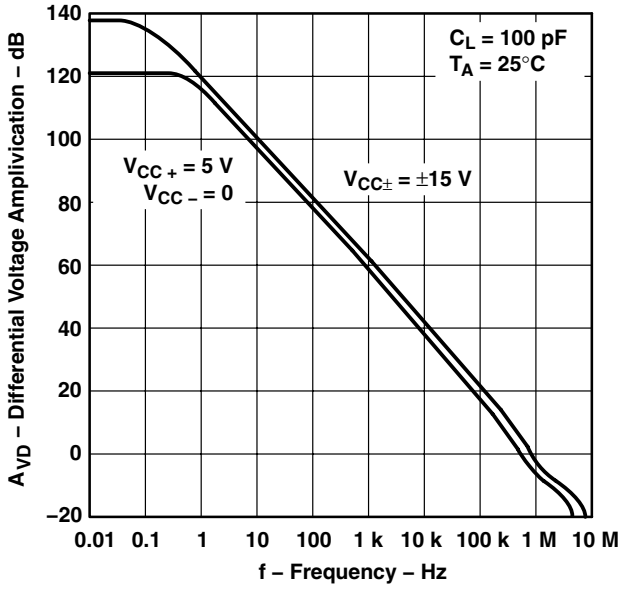


Figure 10

CHANNEL SEPARATION vs FREQUENCY

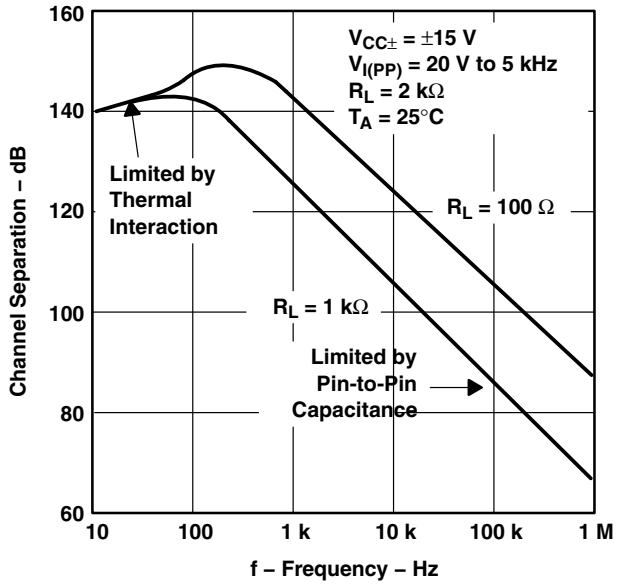


Figure 11

OUTPUT SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

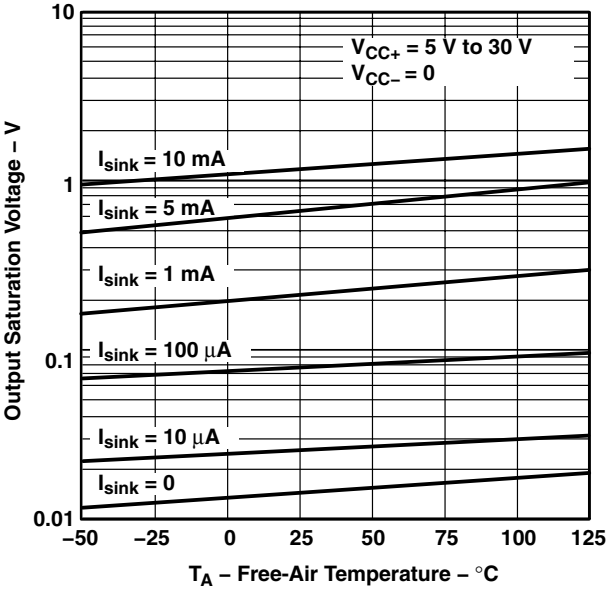


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

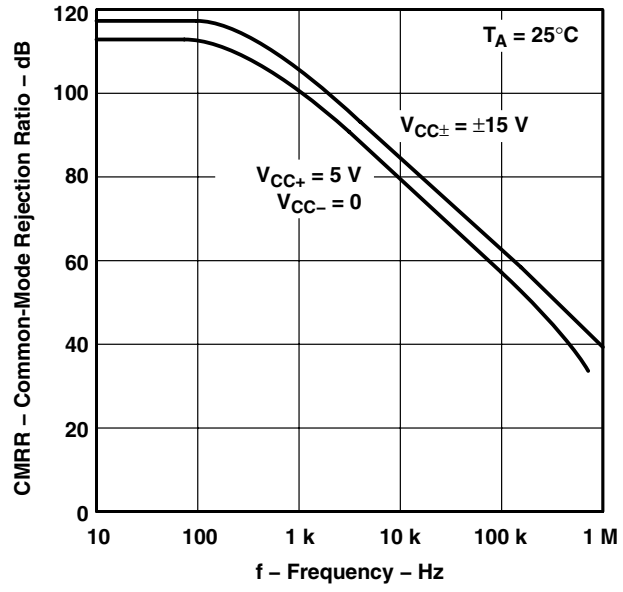


Figure 13

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

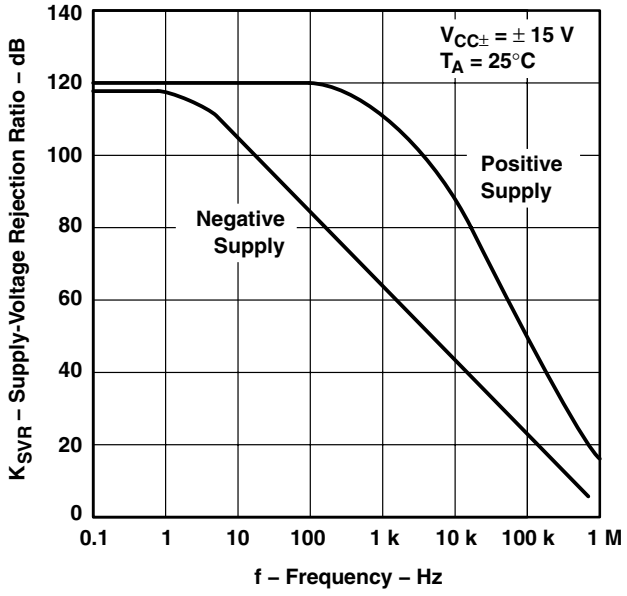


Figure 14

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

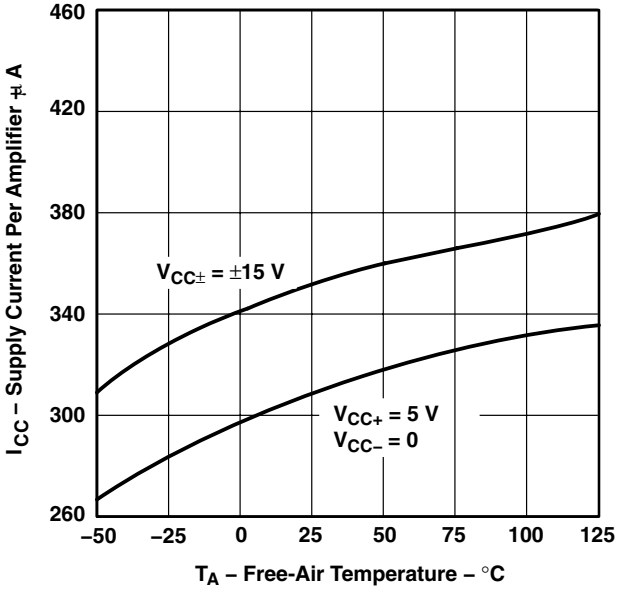


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

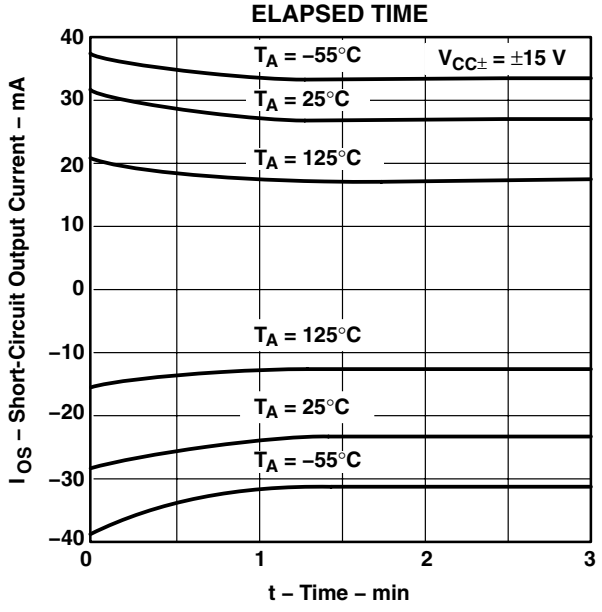


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE AND EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

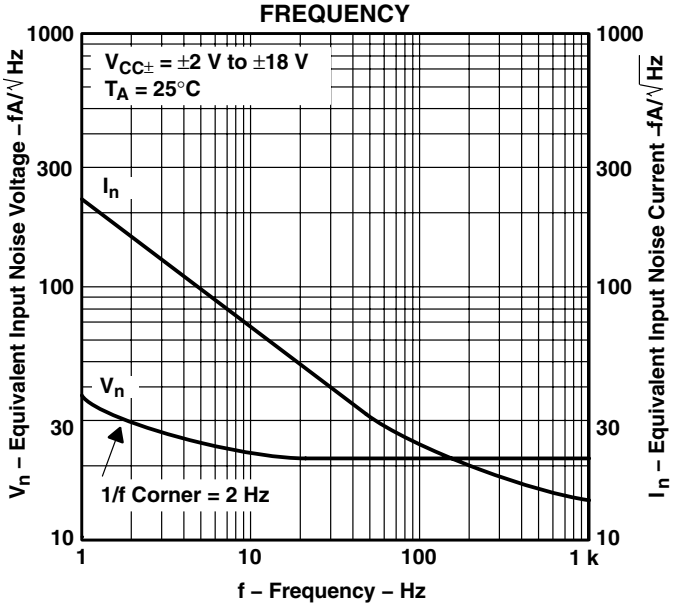


Figure 17

PEAK-TO-PEAK INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD vs TIME

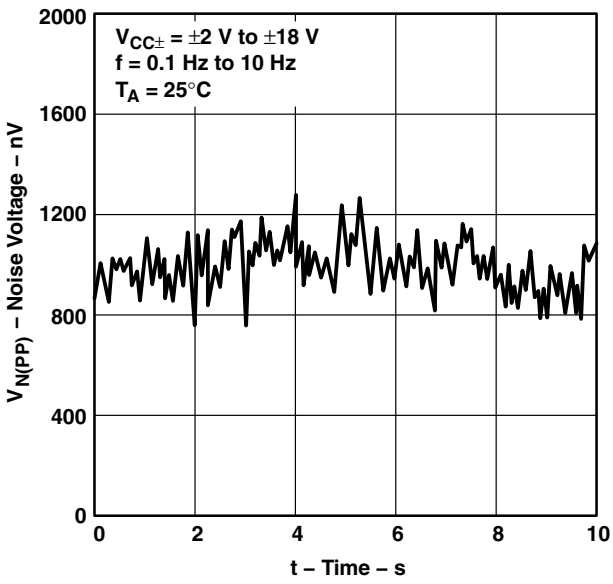


Figure 18

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE vs TIME

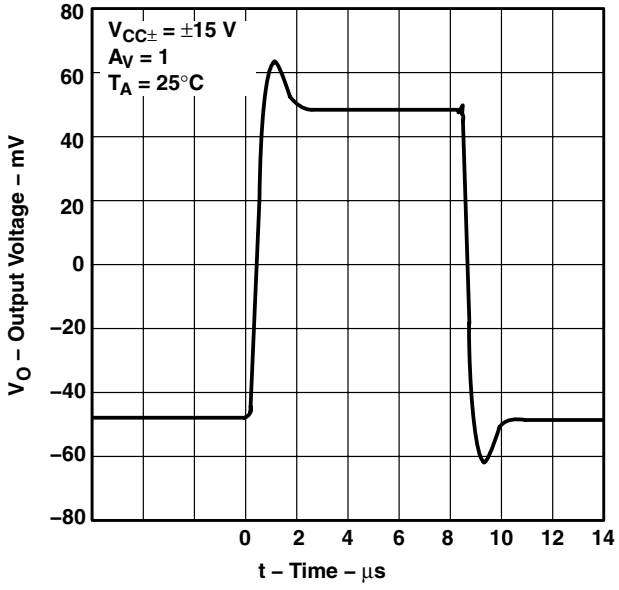


Figure 19

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE vs TIME

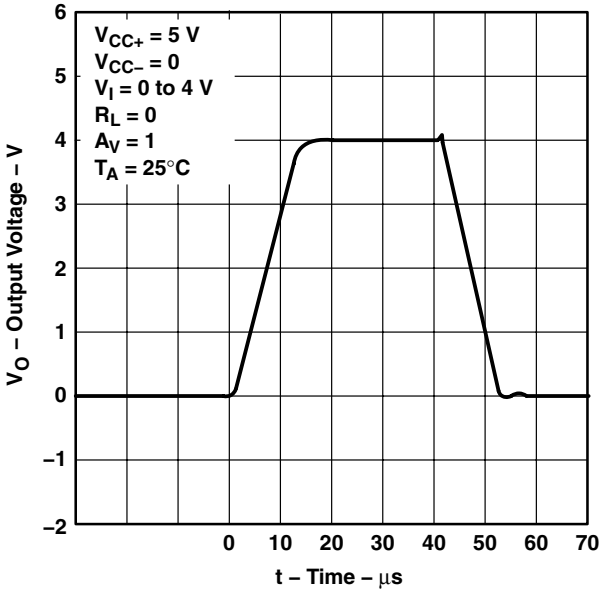


Figure 20

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE vs TIME

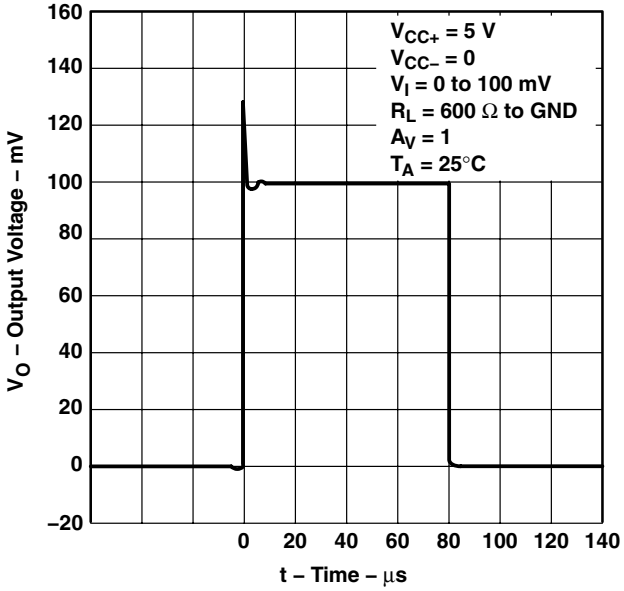


Figure 21

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE vs TIME

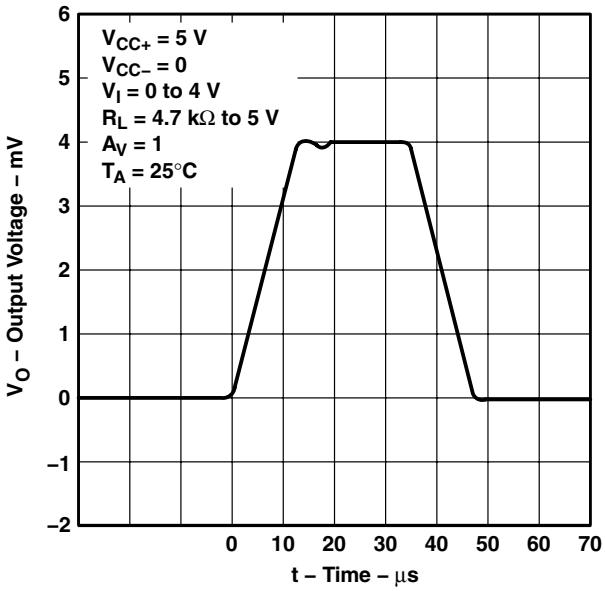


Figure 22

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE vs TIME

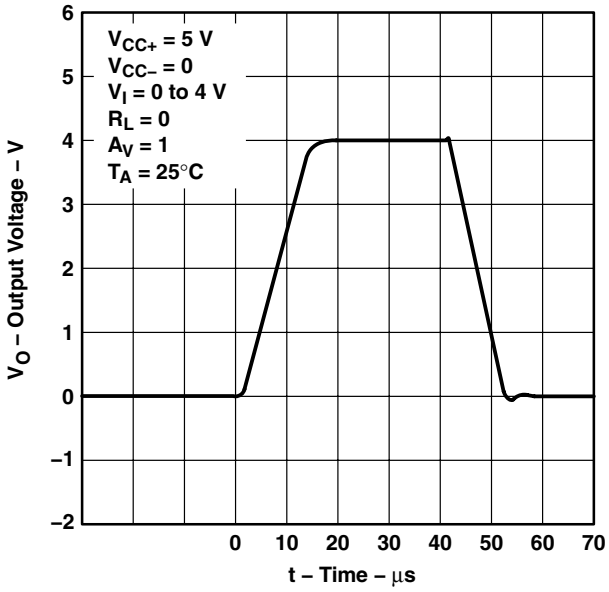


Figure 23

APPLICATION INFORMATION

single-supply operation

The LT1014 is fully specified for single-supply operation (V_{CC-} = 0). The common-mode input voltage range includes ground, and the output swings within a few millivolts of ground.

Furthermore, the LT1014 has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1014 is designed to deal with the following two problems that can occur:

1. On many other operational amplifiers, when the input is more than a diode drop below ground, unlimited current flows from the substrate (V_{CC-} terminal) to the input, which can destroy the unit. On the LT1014, the 400-Ω resistors in series with the input (see schematic) protect the device even when the input is 5 V below ground.
2. When the input is more than 400 mV below ground (at T_A = 25°C), the input stage of similar type operational amplifiers saturates, and phase reversal occurs at the output. This can cause lockup in servo systems. Because of unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1014 outputs do not reverse, even when the inputs are at –1.5 V (see Figure 24).

However, this phase-reversal protection circuitry does not function when the other operational amplifier on the LT1014 is driven hard into negative saturation at the output. Phase-reversal protection does not work on an amplifier:

- When 4's output is in negative saturation (the outputs of 2 and 3 have no effect)
- When 3's output is in negative saturation (the outputs of 1 and 4 have no effect)
- When 2's output is in negative saturation (the outputs of 1 and 4 have no effect)
- When 1's output is in negative saturation (the outputs of 2 and 3 have no effect)

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few microproamperes while swinging to ground. The all-npn output stage of the LT1014 maintains its low output resistance and high gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.

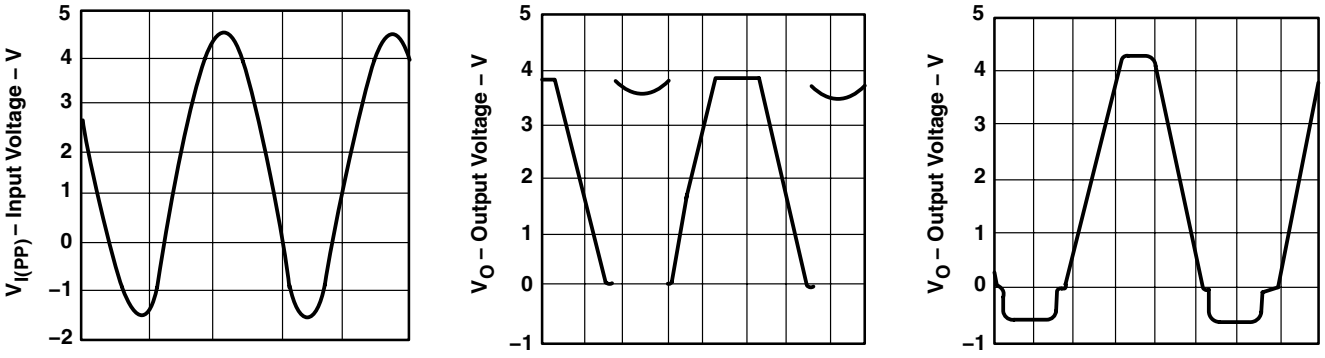


Figure 24. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage Range

APPLICATION INFORMATION

comparator applications

The single-supply operation of the LT1014 can be used as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1014 can perform multiple duties (see Figures 25 and 26).

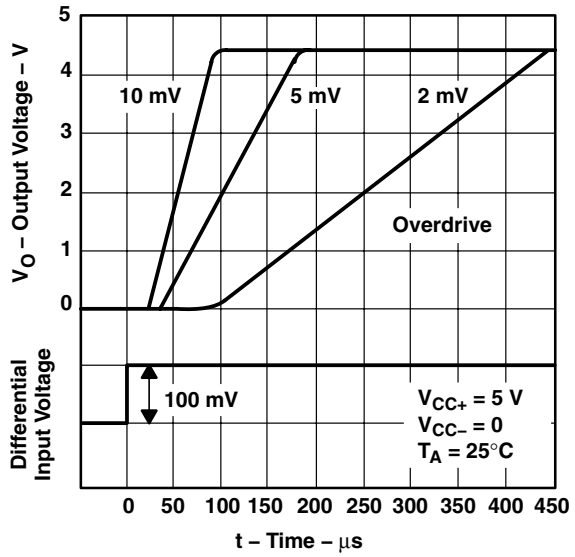


Figure 25. Low-to-High-Level Output Response for Various Input Overdrives

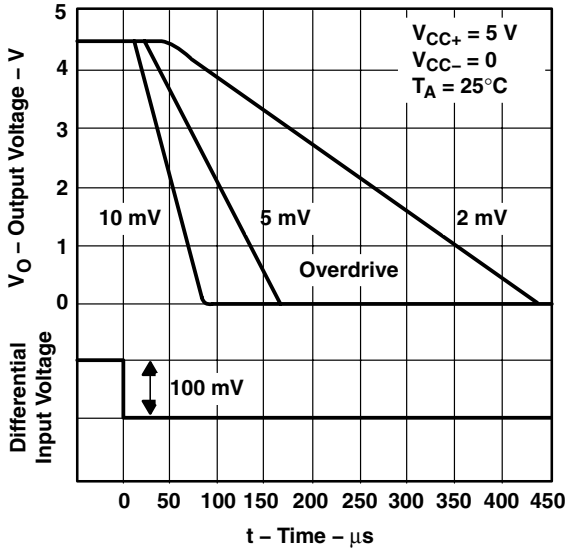


Figure 26. High-to-Low-Level Output Response for Various Input Overdrives

low-supply operation

The minimum supply voltage for proper operation of the LT1014 is 3.4 V (three Ni-Cad batteries). Typical supply current at this voltage is 290 μA; therefore, power dissipation is only 1 mW per amplifier.

offset voltage and noise testing

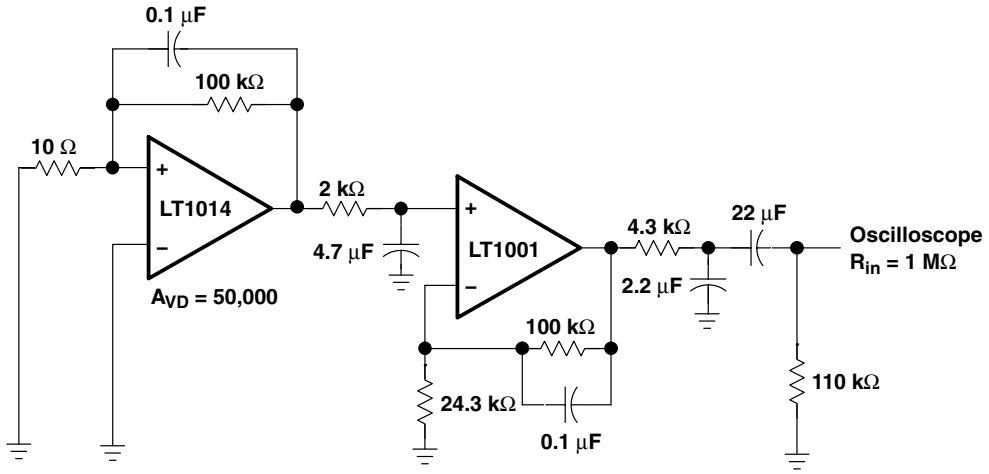
Figure 30 shows the test circuit for measuring input offset voltage and its temperature coefficient. This circuit with supply voltages increased to ±20 V is also used as the burn-in configuration.

The peak-to-peak equivalent input noise voltage of the LT1014 is measured using the test circuit shown in Figure 27. The frequency response of the noise tester indicates that the 0.1-Hz corner is defined by only one zero. The test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contribution from the frequency band below 0.1 Hz.

An input noise-voltage test is recommended when measuring the noise of a large number of units. A 10-Hz input noise-voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

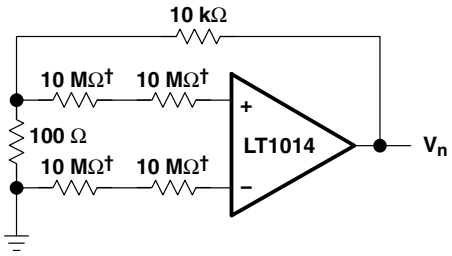
Noise current is measured by the circuit and formula shown in Figure 28. The noise of the source resistors is subtracted.

APPLICATION INFORMATION



NOTE A: All capacitor values are for nonpolarized capacitors only.

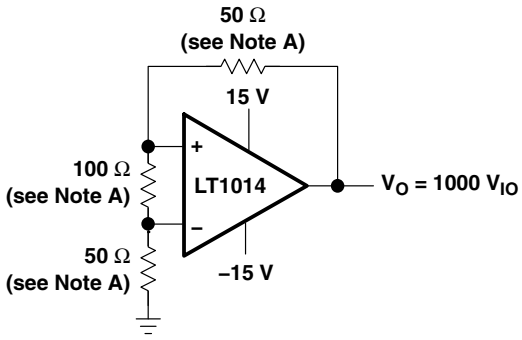
Figure 27. 0.1-Hz to 10-Hz Peak-to-Peak Noise Test Circuit



$$I_n = \frac{\left[V_{no2} - (820\ nV)^2\right]^{1/2}}{40\ M\Omega \times 100}$$

† Metal-film resistor

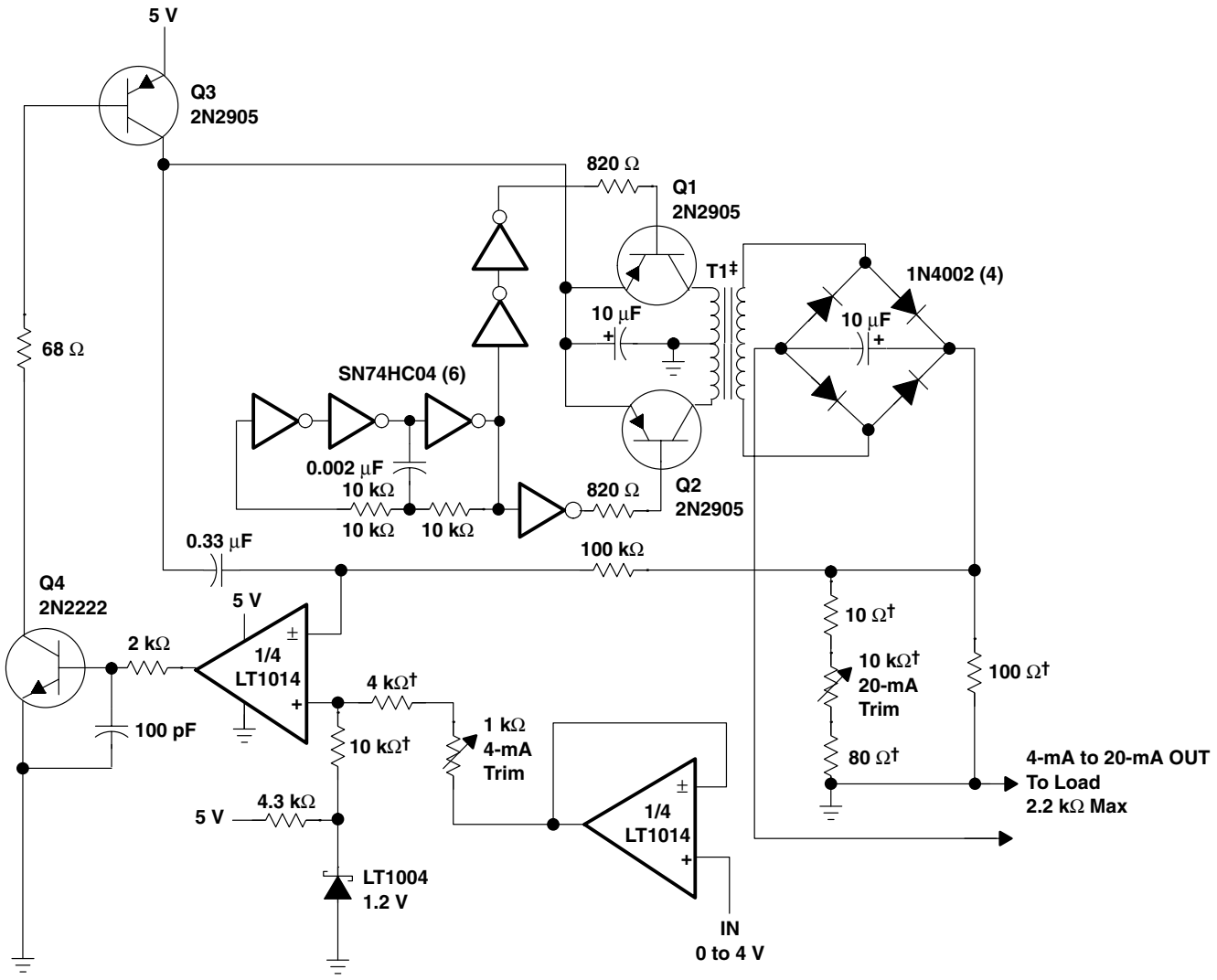
Figure 28. Noise-Current Test Circuit and Formula



NOTE A: Resistors must have low thermoelectric potential.

Figure 29. Test Circuit for V_{IO} and αV_{IO}

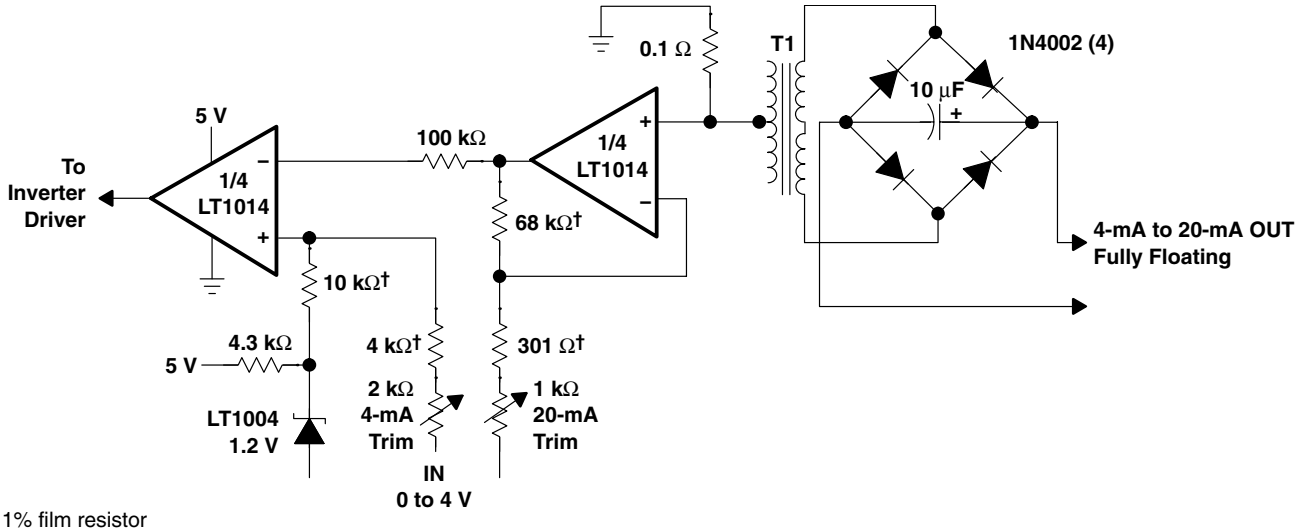
APPLICATION INFORMATION



† 1% film resistor. Match 10-kΩ resistors 0.05%.
‡ T1 = PICO-31080

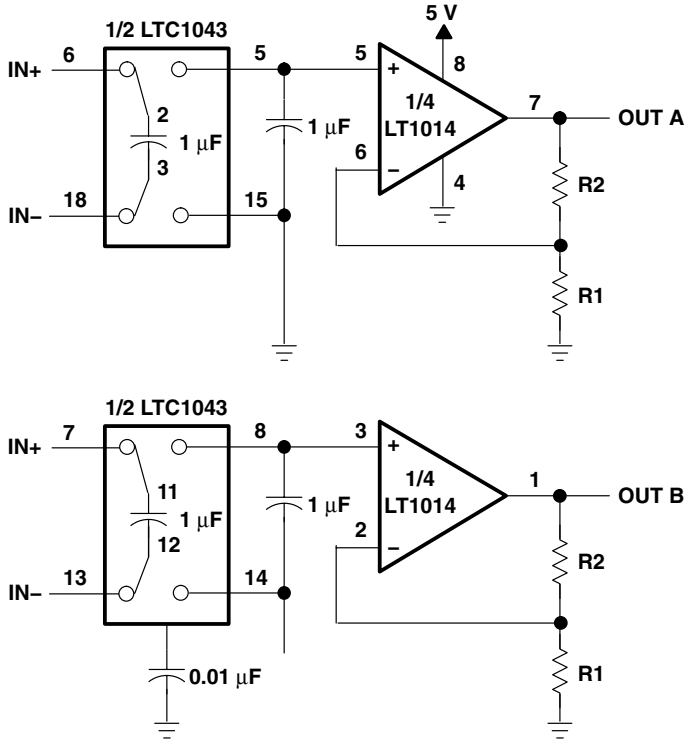
Figure 30. 5-V Powered, 4-mA to 20-mA Current-Loop Transmitter With 12-Bit Accuracy

APPLICATION INFORMATION



† 1% film resistor

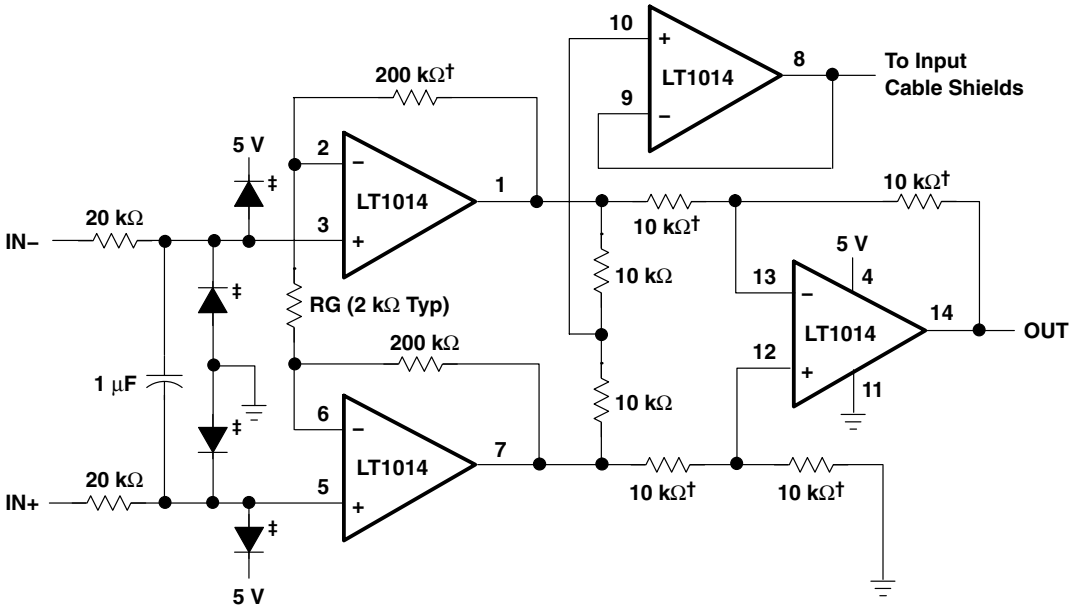
Figure 31. Fully Floating Modification to 4-mA to 20-mA Current-Loop Transmitter With 8-Bit Accuracy



NOTE A: V_{IO} = 150 μV, A_{VD} = (R1/R2) + 1, CMRR = 120 dB, V_{ICR} = 0 to 5 V

Figure 32. 5-V Single-Supply Dual Instrumentation Amplifier

APPLICATION INFORMATION



† † 1% film resistor. Match 10-kΩ resistors 0.05%.
‡ For high source impedances, use 2N2222 as diodes (with collector connected to base).
NOTE A: A_{VD} = (400,000/RG) + 1

Figure 33. 5-V Powered Precision Instrumentation Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89677012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89677012A LT1014 AMFKB	Samples
5962-8967701CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8967701CA LT1014AMJB	Samples
5962-89677022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89677022A LT1014MFKB	Samples
5962-8967702CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8967702CA LT1014MJB	Samples
LT1014AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type		5962-89677012A LT1014 AMFKB	Samples
LT1014AMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type		LT1014AMJ	Samples
LT1014AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type		5962-8967701CA LT1014AMJB	Samples
LT1014CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1014CN	Samples
LT1014CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1014CN	Samples
LT1014DDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1014D	Samples
LT1014DDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1014D	Samples
LT1014DDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1014D	Samples
LT1014DDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1014D	Samples
LT1014DDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1014D	Samples
LT1014DIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	LT1014DI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1014DIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	LT1014DI	Samples
LT1014DIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	LT1014DI	Samples
LT1014DIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	LT1014DIN	Samples
LT1014DINE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	LT1014DIN	Samples
LT1014DMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LT1014DM	Samples
LT1014DMDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LT1014DM	Samples
LT1014DN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1014DN	Samples
LT1014MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89677022A LT1014MFKB	Samples
LT1014MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	LT1014MJ	Samples
LT1014MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type		5962-8967702CA LT1014MJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LT1014D :

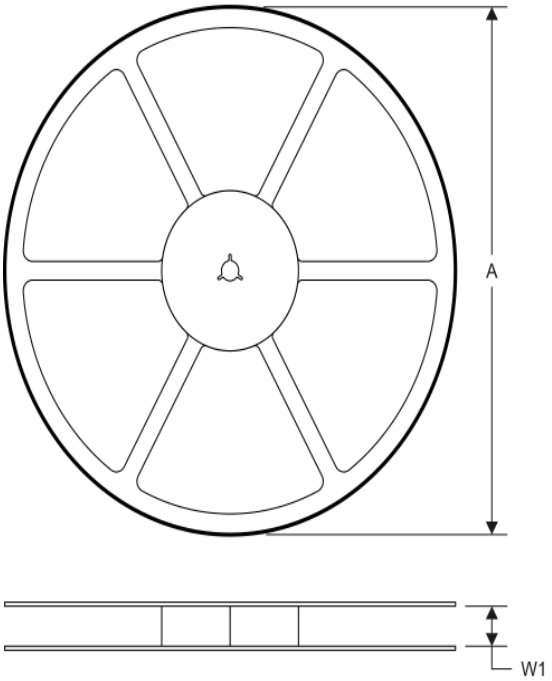
- Enhanced Product: LT1014D-EP

NOTE: Qualified Version Definitions:

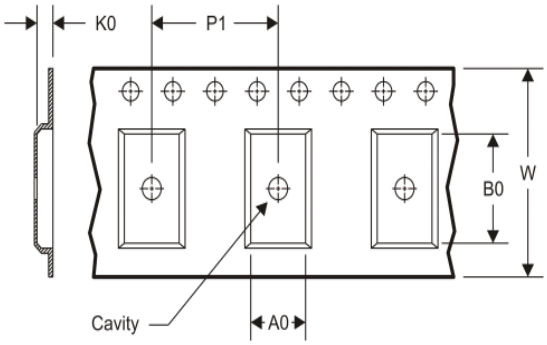
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



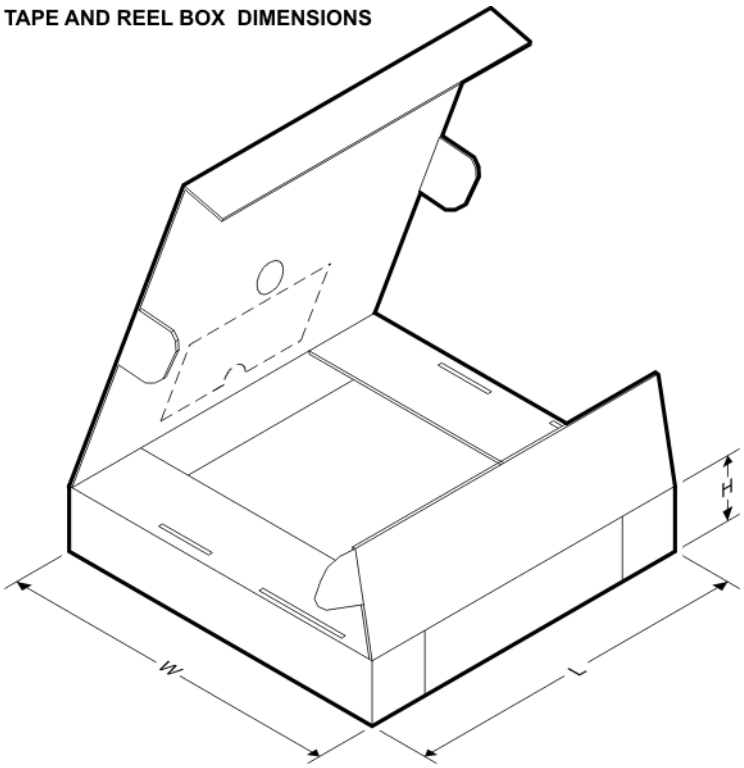
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1014DDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
LT1014DIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

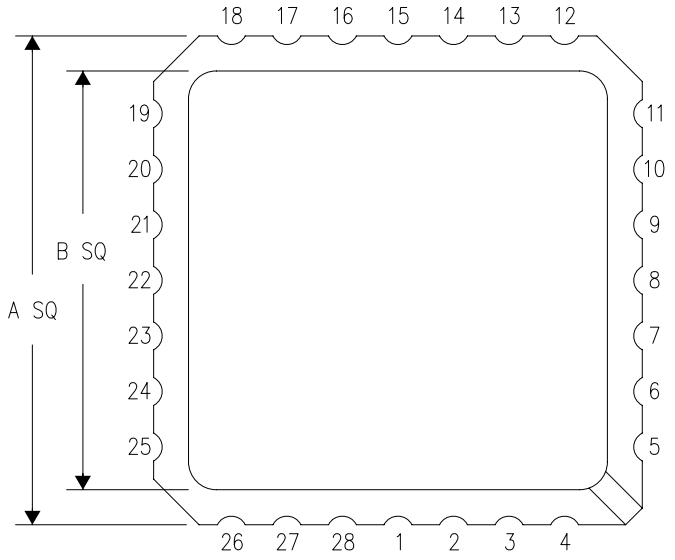


*All dimensions are nominal

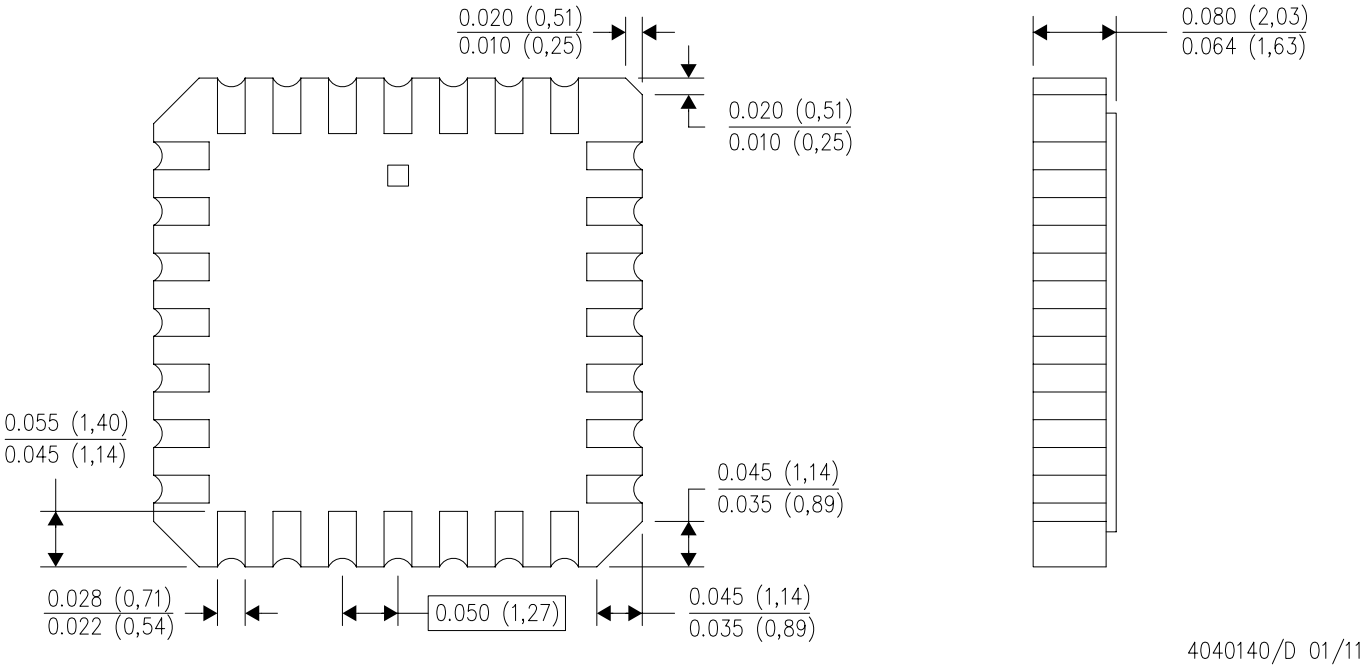
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1014DDWR	SOIC	DW	16	2000	367.0	367.0	38.0
LT1014DIDWR	SOIC	DW	16	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



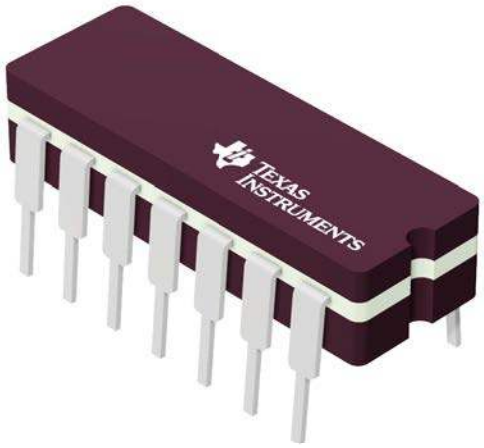
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

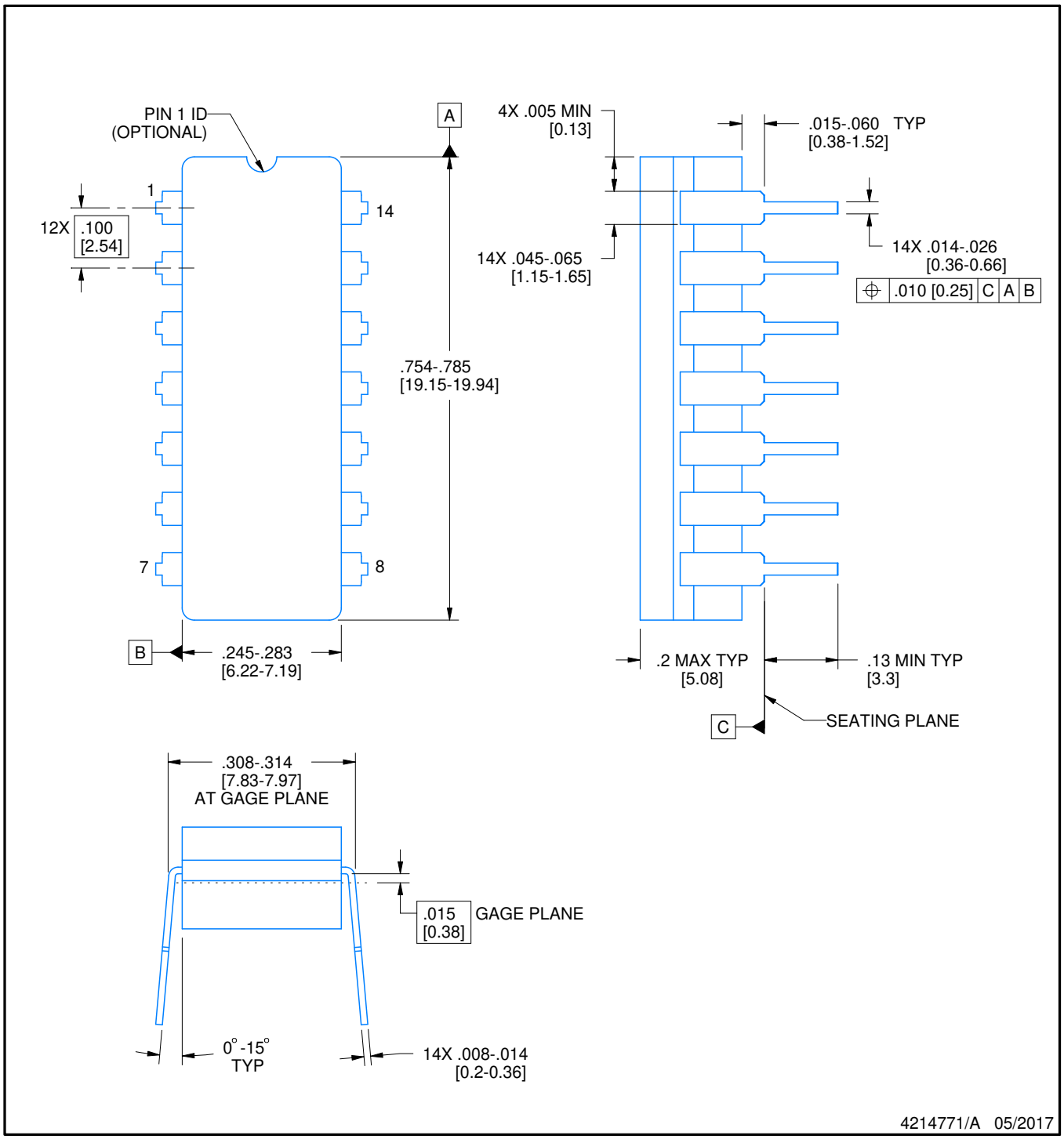
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

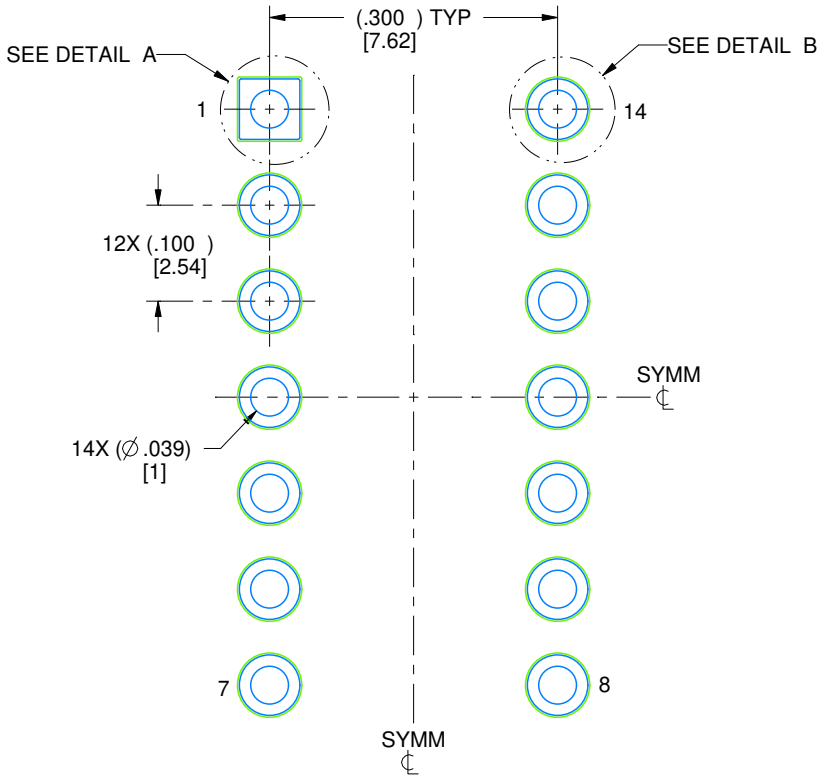
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

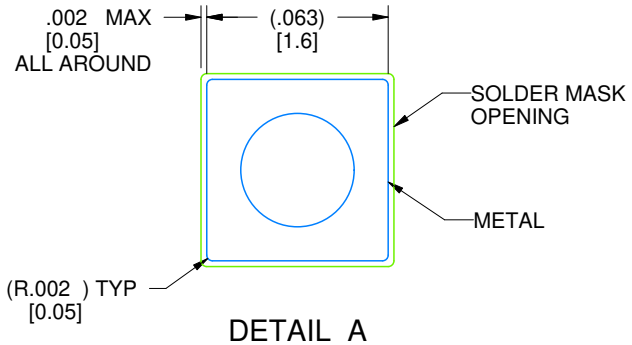
J0014A

CDIP - 5.08 mm max height

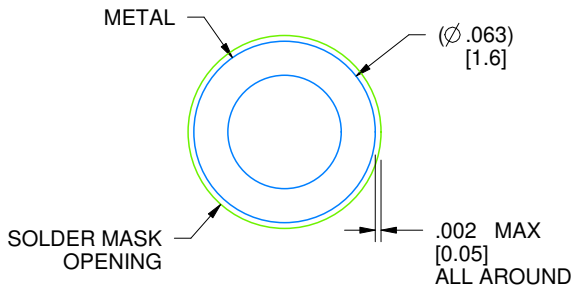
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

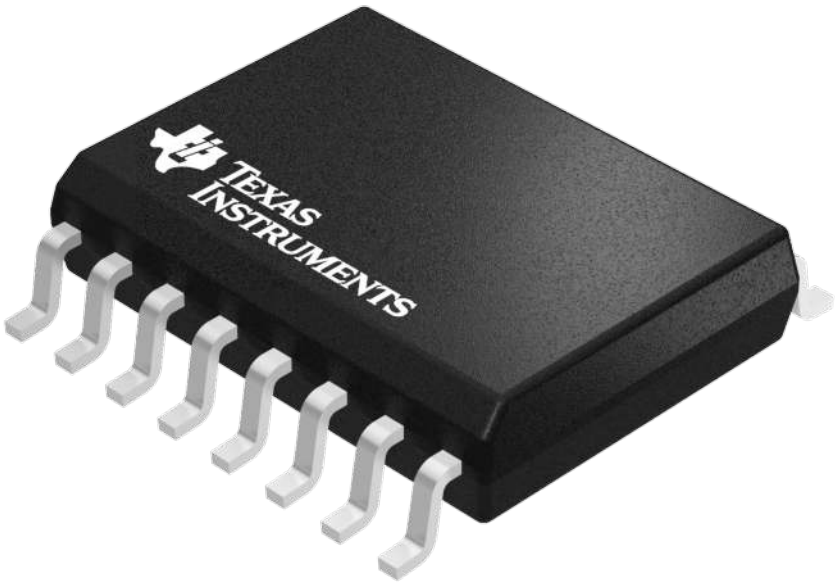


DETAIL B
13X, SCALE: 15X

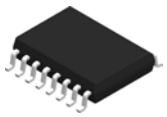
4214771/A 05/2017

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

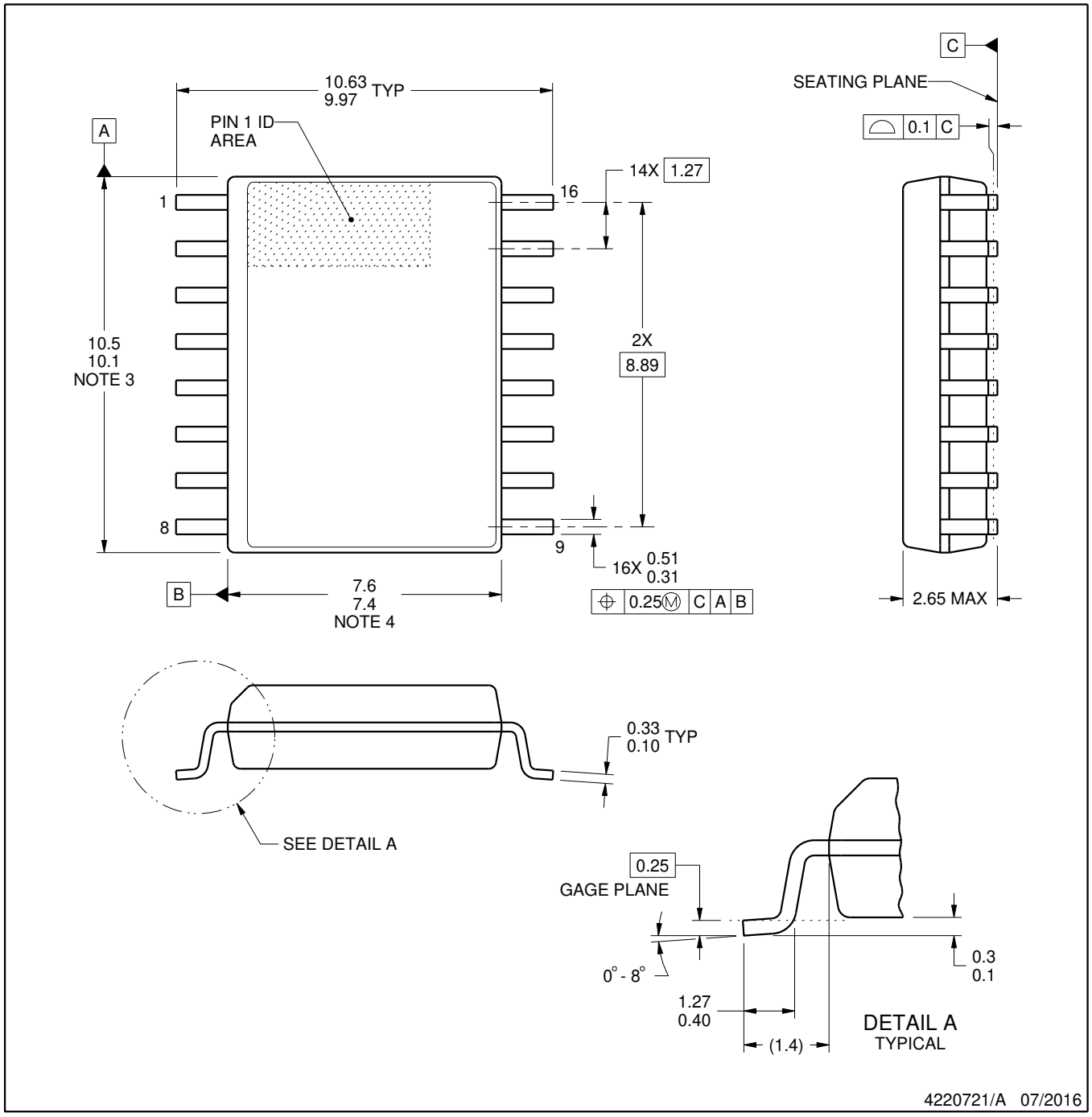


PACKAGE OUTLINE

DW0016A

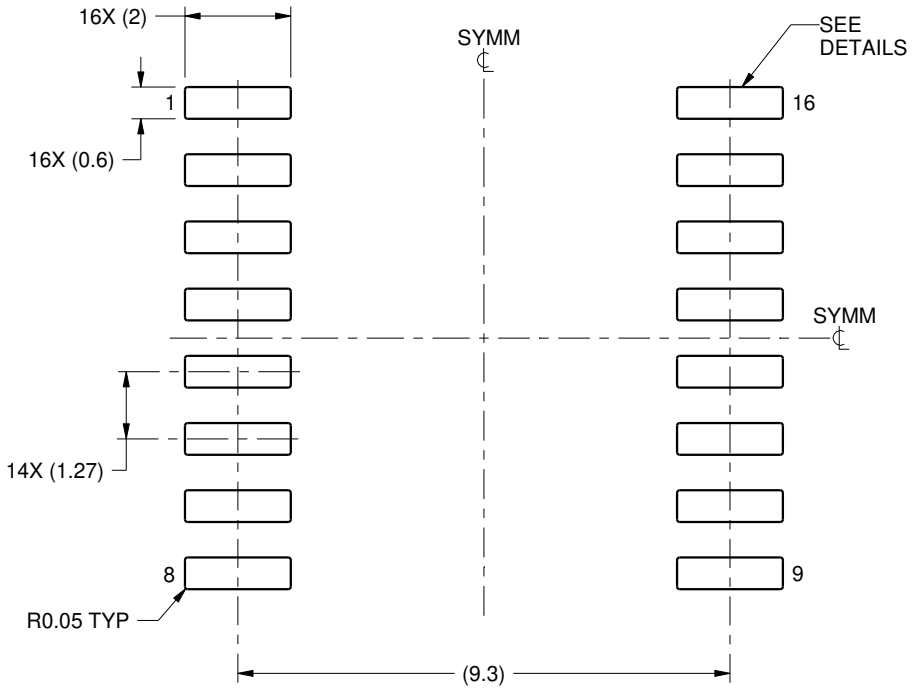
SOIC - 2.65 mm max height

SOIC

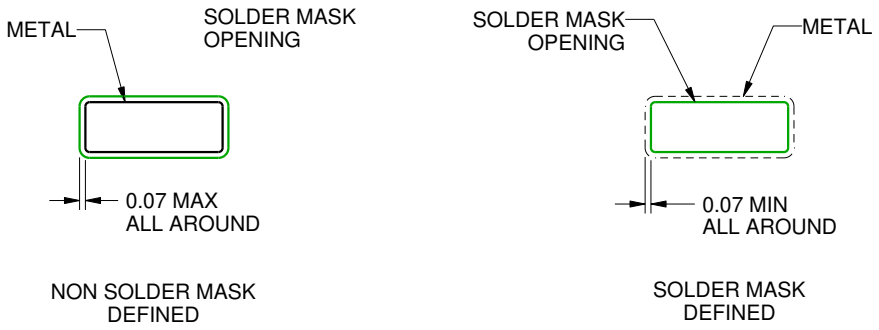


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

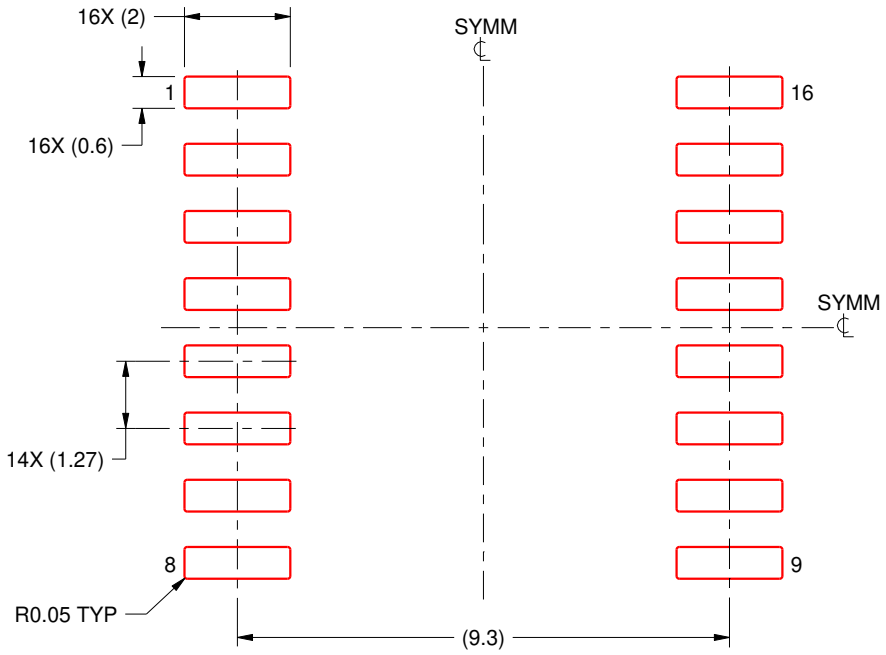


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

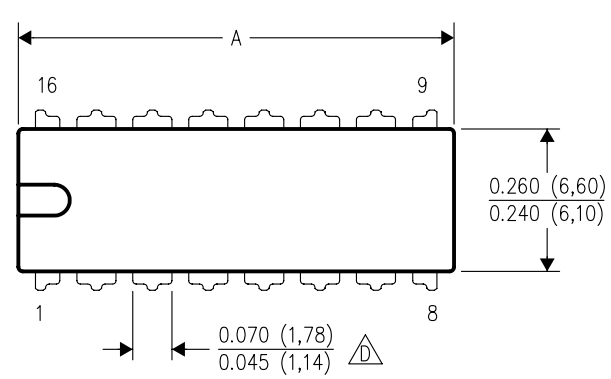
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

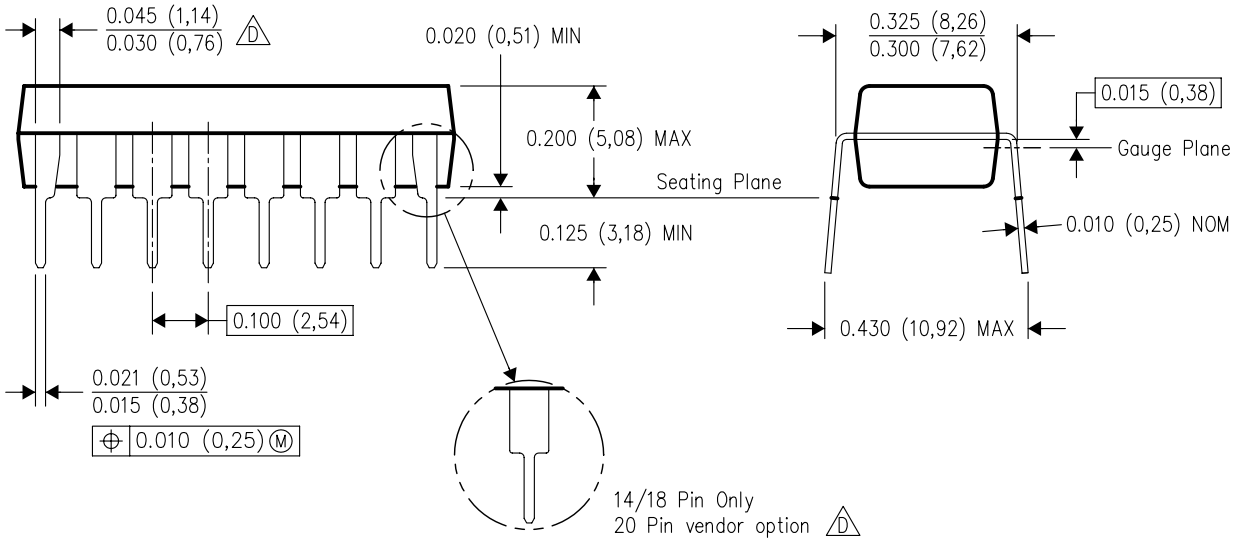
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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