TW2816

4-Channel Video Decoders for Security Applications

FN7736
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The TW2816 includes four high quality NTSC/ PAL video decoders, which convert analog composite to digital component YCbCr for security application. The TW2816 contains four analog anti-aliasing filters, 10-bit ADCs and proprietary digital gain/clamp controllers and utilizes proprietary techniques for separating luminance & chrominance to reduce both cross-luminance and cross-chrominance artifacts. The TW2816 also adopts the image enhancement techniques such as IF compensation filter, CTI and luminance programmable peaking filter to produce a high quality pictures.

Features

Four Video Decoders

- Accepts all NTSC(M/N/4.43) / PAL(B/D/G/H/I/K/L/M/N/60) standards with auto detection
- Integrated four video analog anti-aliasing filters and 10 bit CMOS ADCs
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system for non-realtime application
- Supports the standard ITU-R BT.656 format or time multiplexed output with 54MHz
- Provides simultaneous four channel Full D1 and CIF time-multiplexed outputs with 54MHz
- Supports a two-wire serial host interface
- Ultra low power consumption (Typical 480mW)
- 100 TQFP package

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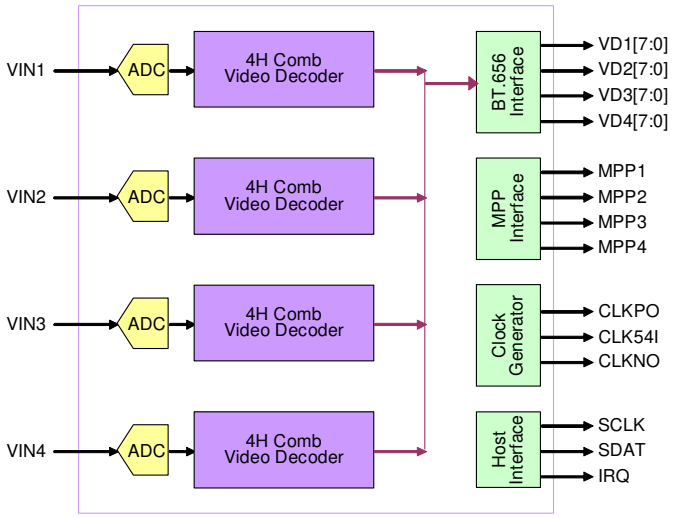
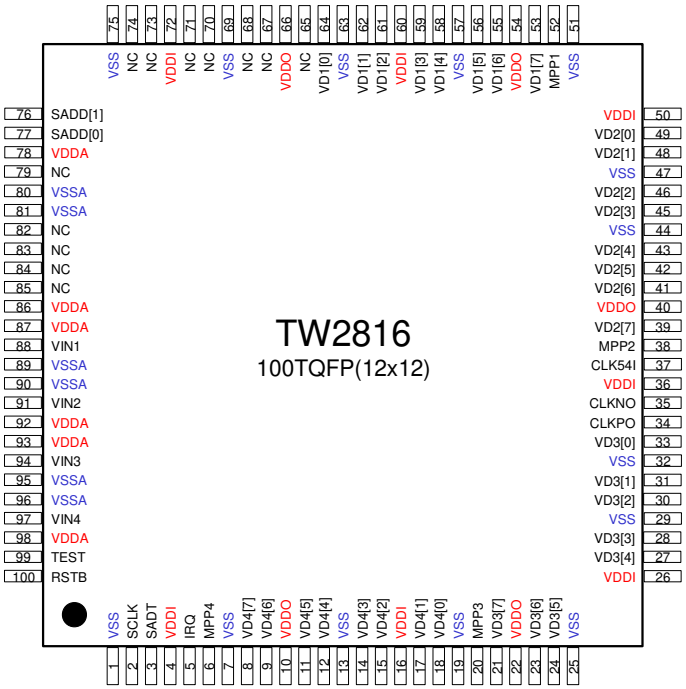
Block Diagram



Pin Diagram


TW2816
100TQFP(12x12)
1 VSS
2 SCLK
3 SADT
4 VDDI
5 IRQ
6 MPP4
7 VSS
8 VD4[7]
9 VD4[6]
10 VDDO
11 VD4[5]
12 VD4[4]
13 VSS
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47 VSS
48 VD2[1]
49 VD2[0]
50 VDDI
51 VSS
52 MPP1
53 VD1[7]
54 VDDO
55 VD1[6]
56 VD1[5]
57 VSS
58 VD1[4]
59 VD1[3]
60 VDDI
61 VD1[2]
62 VD1[1]
63 VSS
64 VD1[0]
65 NC
66 VDDO
67 NC
68 NC
69 VSS
70 NC
71 NC
72 VDDI
73 NC
74 NC
75 VSS
76 SADD[1]
77 SADD[0]
78 VDDA
79 NC
80 VSSA
81 VSSA
82 NC
83 NC
84 NC
85 NC
86 VDDA
87 VDDA
88 VIN1
89 VSSA
90 VSSA
91 VIN2
92 VDDA
93 VDDA
94 VIN3
95 VSSA
96 VSSA
97 VIN4
98 VDDA
99 TEST
100 RSTB

Pin Descriptions

Analog Video Interface Pins

Name	Number	Type	Description
VIN1	88	A	Composite video input of channel 1.
VIN2	91	A	Composite video input of channel 2.
VIN3	94	A	Composite video input of channel 3.
VIN4	97	A	Composite video input of channel 4.

Digital Video Interface Pins

Name	Number	Type	Description
VD1[7:0]	53,55,56,58, 59,61,62,64	O	Video data output of channel 1.
VD2[7:0]	39,41,42,43, 45,46,48,49	O	Video data output of channel 2.
VD3[7:0] *	21,23,24,27, 28,30,31,33	O	Video data output of channel 3.
VD4[7:0] *	8,9,11,12, 14,15,17,18	O	Video data output of channel 4.
MPP1	52	O	HS/VS/FLD/ACTIVE/NOVID of channel 1.
MPP2	38	O	HS/VS/FLD/ACTIVE/NOVID of channel 2.
MPP3*	20	O	HS/VS/FLD/ACTIVE/NOVID of channel 3.
MPP4*	6	O	HS/VS/FLD/ACTIVE/NOVID of channel 4.

Note : * Not supported for TW2816H

System Control Pins

Name	Number	Type	Description
RSTB	100	I	System reset.
CLK54I	37	I	54MHz system clock input.
CLKPO	34	O	27/54MHz clock output.
CLKNO	35	O	27/54MHZ clock output.
TEST	99	I	Test pin. Connect to ground.
SCLK	2	I	Serial control clock line.
SDAT	3	IO	Serial control data line.
SADD[1:0]	76,77	I	Serial control address.
IRQ	5	O	Interrupt request output.

Power and Ground Pins

Name	Number	Type	Description
VDDI	4,16,26, 36,50,60,72	P	1.8V Power for internal logic.
VDDO	10,22,40, 54,66	P	3.3V Power for output driver.
VSS	1,7,13,19, 25,29,32,44, 47,51,57,63, 69,75	G	Ground for internal logic and output driver.
VDDA	87,92,93,98, 78,86	P	1.8V Power for analog video.
VSSA	89,90,95,96, 80,81	G	Ground for analog video.

No Connection

Name	Number	Type	Description
NC	65,67,68,70, 71,73,74,79, 82,83,84,85	NC	No Connection

Functional Description

Video Input Formats

The TW2816 supports all NTSC/PAL standard formats and has built-in automatic standard detection circuit. The following Table1 shows the identified standards. Automatic standard detection can be overridden by writing the value into the IFMTMAN and IFORMAT register (0x01, 0x11, 0x21, 0x31). Even in no-video status, the device can be forced to free-run in a particular video standard mode for fast locking by programming IFORMAT register.

Table1 Input Video Format Supported

Format	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)
NTSC-M* NTSC-J	525/59.94	15.734	3.579545
NTSC-4.43*	525/59.94	15.734	4.43361875
NTSC-N	625/50	15.625	3.579545
PAL-BDGHI PAL-N*	625/50	15.625	4.43361875
PAL-M*	525/59.94	15.734	3.57561149
PAL-NC	625/50	15.625	3.58205625
PAL-60	525/59.94	15.734	4.43361875

Note : * 7.5 IRE Setup

Analog-to-Digital Converter

The TW2816 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the ADC_PWDN (0x50) register. The TW2816 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. The following Fig1 shows the frequency response of the anti-aliasing filter.

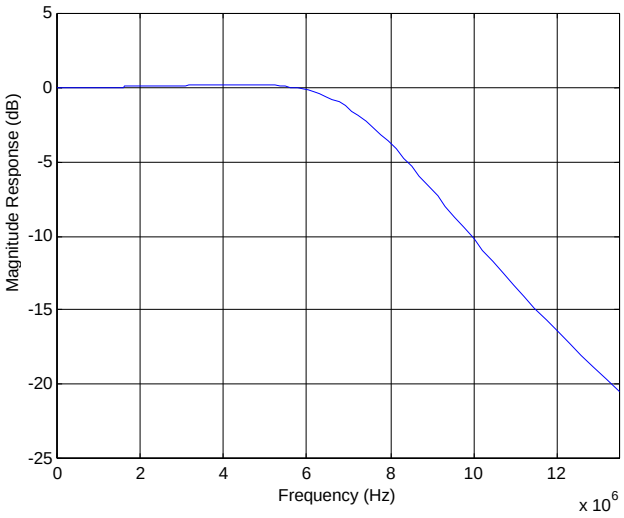


Fig1 The frequency response of anti-aliasing filter

Sync Processing

The sync processor of TW2816 detects horizontal and vertical synchronization signals in the composite. The TW2816 utilizes proprietary technology for locking to weak, noisy, or unstable signals such as those from on-air signal and fast forward or backward of VCR system.

Automatic Gain Control and Clamping

A patented digital gain and clamp control circuit restores the ac coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video pedestal level to a fixed dc reference voltage. In no AGC mode, the gain control circuit adjusts only the video sync gain to achieve desired sync amplitude so that the active video is bypassed regardless of the gain control. But when AGC mode is enabled, both active video and sync are adjusted by the gain control. The range of AGC is from –6dB to 18dB approximately. Additionally, an automatic white peak control circuit is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Horizontal Sync Processing

The horizontal synchronization processing contains a sync separator, a PLL and the related decision logic. The horizontal sync separator detects the horizontal sync by examining low-pass filtered video input whose level is lower than a threshold. Additional logic is also used to avoid false detection on glitches. The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. In case the horizontal sync is missing, the PLL is on free running status that matches the standard raster frequency.

Vertical Sync Processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field.

Color Decoding

Decimation Filter

The digitized composite video data at 2X pixel clock rate first passes through decimation filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image. Fig2 shows the characteristic of the decimation filter.

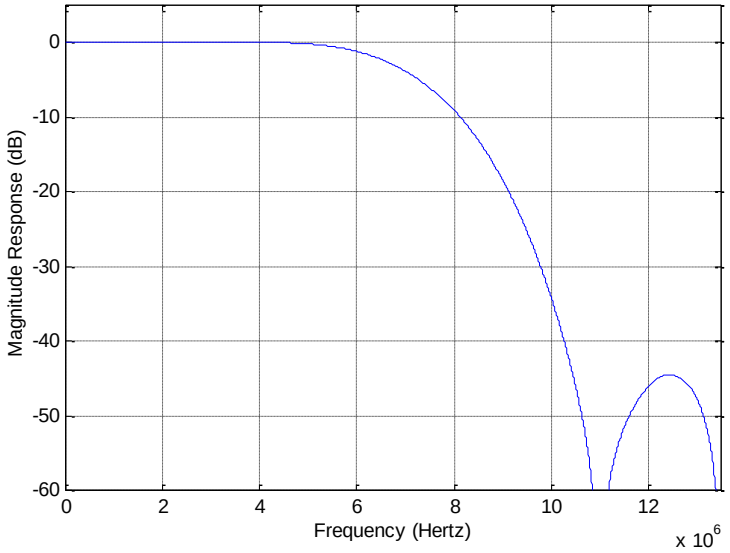
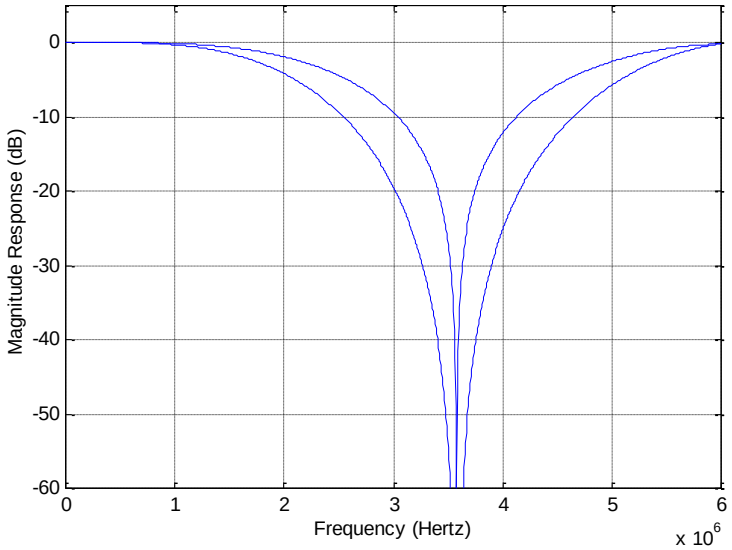


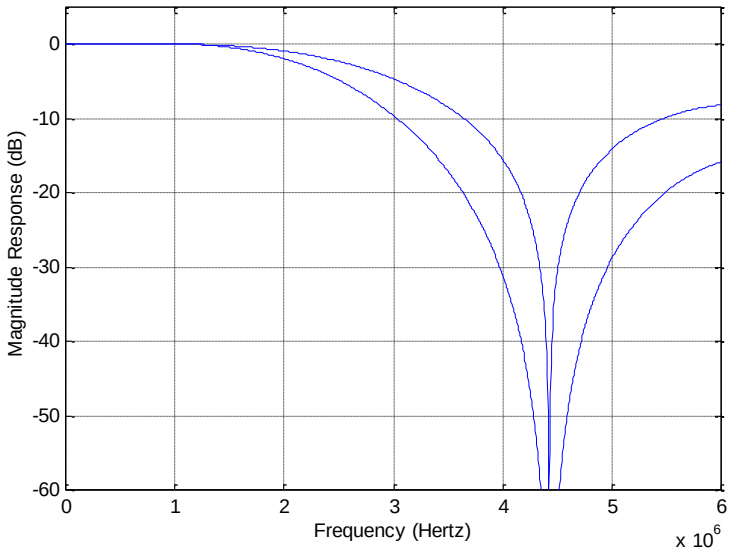
Fig2 The Characteristic of the Decimation Filter

Y/C Separation

A proprietary 4H adaptive comb filter is used for high quality luminance/chrominance separation from NTSC/PAL composite video signals. The 4H adaptive comb filter improves the luminance resolution and reduces noise such as cross-luminance and cross-color. The adaptive algorithm eliminates most of errors without introducing new artifacts or noise. To accommodate some viewing preferences, additional chrominance trap filters are also available in the luminance path. The Fig3 show the frequency response of notch filter for each system NTSC and PAL.



(a) Notch Filter for NTSC



(b) Notch Filter for PAL

Fig3 The Characteristics of Luminance Notch Filter for PAL

Luminance Processing

The luminance signal is separated by adaptive comb or trap filter is then fed to a peaking circuit. The peaking filter enhances the high frequency components of the luminance signal via the YPEAK_GN (0x0B, 0x1B, 0x2B, 0x3B) register. The Fig4 shows the characteristics of the peaking filter for four different gain modes.

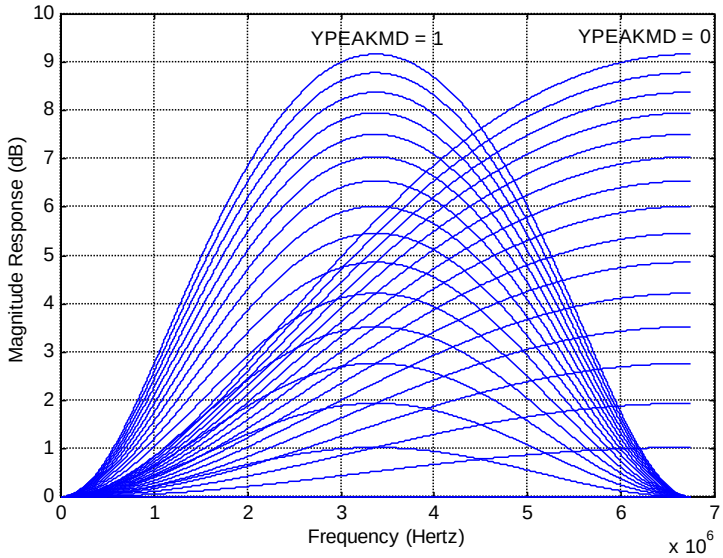


Fig4 The Characteristic of Luminance Peaking filter

The picture contrast and brightness adjustment is provided through CONT (0x09, 0x19, 0x29, 0x39) and BRT (0x0A, 0x1A, 0x2A, 0x3A) registers. The contrast adjustment range is from approximately 0 to 200 percent, and the brightness adjustment is in the range of ±25 IRE.

Chrominance Processing

Chrominance Demodulation

The chrominance demodulation is done by first quadrature mixing for NTSC and PAL. The mixing frequency is equal to the sub-carrier frequency of NTSC and PAL. After the mixing, a LPF is used to remove 2X carrier signal and yield chrominance components. The LPF characteristic can be selected for optimized transient color performance. In case of a mistuned IF source, IF compensation filter makes up for any attenuation at higher frequencies or asymmetry around the color sub-carrier. The gain for the upper chrominance side band is controlled by IFCOMP (0x47) register. The Fig5 and Fig6 show the frequency response of IF-compensation filter and chrominance LPF.

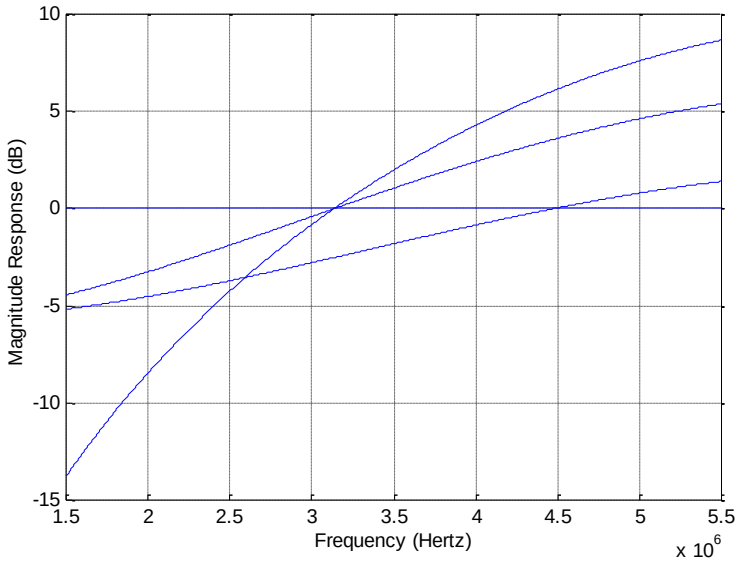


Fig5 The Characteristics of IF-compensation Filter

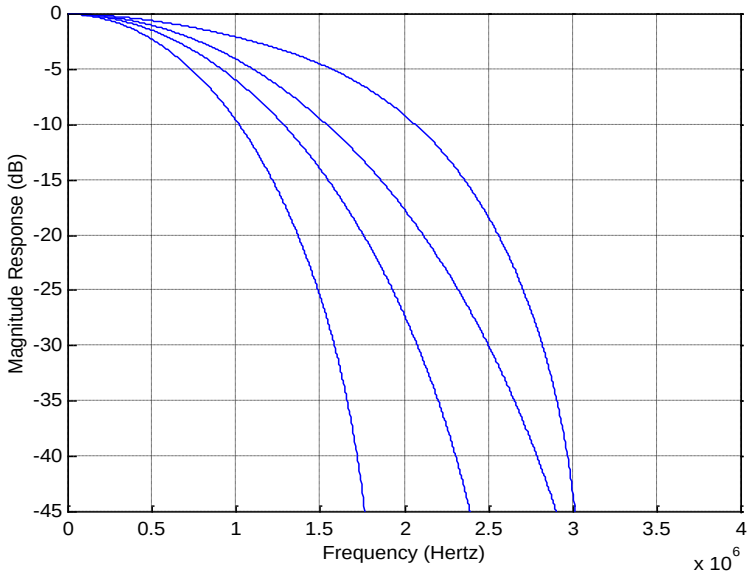


Fig6 The Characteristics of Chrominance Low Pass Filter

ACC (Automatic Color gain control)

The ACC (Automatic Color gain Control) compensates for reduced amplitudes caused by high frequency suppression in video signal. The range of ACC is from –6dB to 30dB approximately. For black & white video or very weak & noisy signals, the color will be off by the internal color killing circuit. The color killer function can also be always enabled or disabled by programming CKIL (0x0C, 0x1C, 0x2C, 0x3C) register.

Chrominance Gain, Offset and Hue Adjustment

The color saturation can be adjusted by changing the register SAT (0x08, 0x18, 0x28, 0x38). The Cb and Cr gain can be also adjusted independently by programming UGAIN (0x49) and VGAIN (0x4A) register. Likewise, the Cb and Cr offset can be programmed through U_OFF (0x4B) and V_OFF (0x4C) registers. Hue control is achieved with phase shift of the digitally controlled oscillator. The phase shift can be programmed through HUE (0x07, 0x17, 0x27, 0x37) register.

CTI (Color Transient Improvement)

A programmable Color Transient Improvement (CTI) is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

Video Cropping

The cropping function allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig7. The first active line is defined by the VDELAY register and the first active pixel is defined by the HDELAY register. The VACTIVE register can be programmed to define the number of active lines in a video field, and the HACTIVE register can be programmed to define the number of active pixels in a video line.

The horizontal delay register HDELAY determines the number of pixel delays between the horizontal reference and the leading edge of the active region. The horizontal active register HACTIVE determines the number of active pixels to be processed. Note that these values are referenced to the pixel number before scaling. Therefore, even if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HDEALY and HACTIVE register. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line
Where the total number of pixels per line is 858 for 60Hz and 864 for 50Hz

To process full size region, the HDELAY should be set to 32 and HACTIVE set to 720 for both 60Hz and 50Hz system.

The vertical delay register VDELAY determines the number of line delays from the vertical reference to the start of the active video lines. The vertical active register (VACTIVE) determines the number of lines to be processed. These values are referenced to the incoming scan lines before the vertical scaling. In order for the vertical cropping to work properly, the following equation should be satisfied.

VDELAY + VACTIVE < Total number of lines per field
Where the total number of lines per field is 262 for 60Hz and 312 for 50Hz

To process full size region, the VDELAY should be set to 7 and VACTIVE set to 240 for 60Hz and the VDELAY should be also set to 4 and VACTIVE set to 288 for 50Hz.

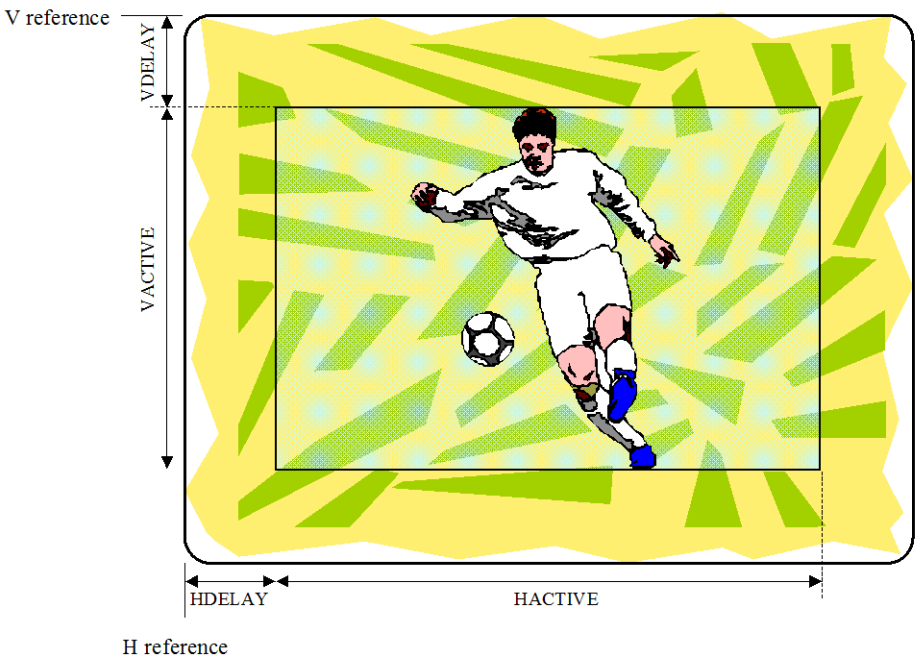


Fig7 The Effect of Cropping Registers

Output Format

The TW2816 supports a standard ITU-R BT.656 format. All video data and timing signal of four channels are synchronous with the pins CLKPO or CLKNO output. Therefore, CLKPO or CLKNO can be connected to four channel interfaces for synchronizing data. And, the phase of CLKPO or CLKNO can be controlled by 2ns unit via the CLKP_DEL or CLKN_DEL (0x4D) registers independently.

ITU-R BT.656 Format

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Fig8. The SAV and EAV sequences are shown in Table2. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit (0x43).

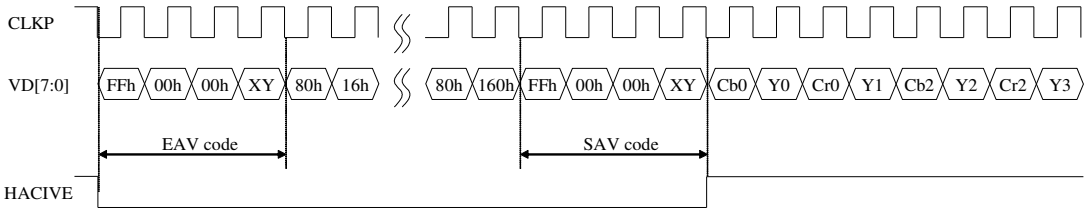


Fig8 Timing Diagram of ITU-R BT.656 format

Table2 ITU-R BT.656 SAV and EAV Code Sequence

Condition			656 FVH Value			SAV/EAV Code Sequence				
Field	V time	H time	F	V	H	First	Second	Third	Fourth	
									Normal	Option*
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

Note : * Option includes video loss information in ITU-R BT.656

Two Channel ITU-R BT.656 Time-multiplexed Format with 54MHz

The TW2816 supports two channel ITU-R BT.656 time-multiplexed format with 54MHz that is useful to security application requiring two channel outputs through one channel video port. The DUAL_CH (0x0D/0x1E/0x2E/0x3E) register enables the dual ITU-R BT.656 time-multiplexed format and the SEL_CH (0x0D/0x1E/0x2E/0x3E) register selects another channel output to be multiplexed with its own channel on each VD pins. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID (0x42) register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. The following Fig9 illustrates the timing diagram in the case of CH1 and CH2 time-multiplexed output through CH1 video output port.

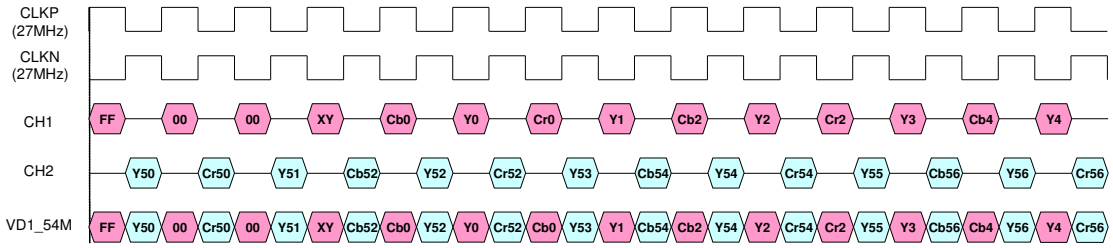


Fig9 Timing Diagram of Two Channel Time-multiplexed Format with 54MHz

Four Channel CIF Time-multiplexed Format with 54MHz

Four channel CIF (360x480) time-multiplexed format is also provided for specific security application using the CIF_54M (0x75) register. For this format, each channel ITU-R BT.656 data stream is down-sampled into 13.5MHz ITU-R BT.656 data stream except the sync code. To reject an aliasing noise in this format, the HSCL_LPF (0x71) register should be set to high. Optionally, the vertical scaling can also be enabled to support Quad (360x240) format using the VSCL_ENA (0x71) register. Then, these four 13.5MHz ITU-R BT.656 data stream are time-multiplexed into 54MHz data stream. This format requires only one channel video port to transfer whole four channel CIF data independently so that it can be supported simultaneously with two channel Full D1 ITU-R BT.656 time-multiplexed format through the other video ports. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID (0x42) register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Optionally, when the vertical scaling is enabled, the ITU-R BT.656 sync code will be skipped in the invalid line through the VSCL_SYNC (0x71) register. The following Fig10 and Table3 illustrate the timing diagram and detailed channel ID format for four channel CIF time-multiplexed format with 54MHz.

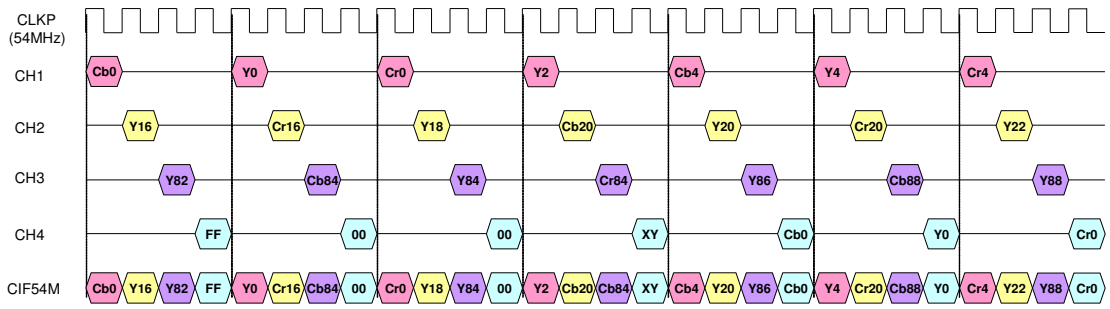


Fig10 Timing Diagram of 4 Ch CIF Time-multiplexed Format with 54MHz

Table3 The Channel ID Format for 4 Ch CIF Time-multiplexed Format with 54MHz

Condition			656 FVH Value			SAV/EAV Code Sequence						
Field	Vtime	Htime	F	V	H	First	Second	Third	Fourth			
									Ch1	Ch2	Ch3	Ch4
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

(a) ITU-R BT.656 Sync Code with Channel ID

Channel	H Blanking Code with Channel ID		
	Y	Cb	Cr
Ch1	8'h10	8'h80	8'h80
Ch2	8'h11	8'h81	8'h81
Ch3	8'h12	8'h82	8'h82
Ch4	8'h13	8'h83	8'h83

(b) Horizontal Blanking Code with Channel ID

Extra Sync Output

The additional timing information such as syncs and field flag are also supported through the MPP pins. The video output timing is illustrated in Fig11 and Fig12.

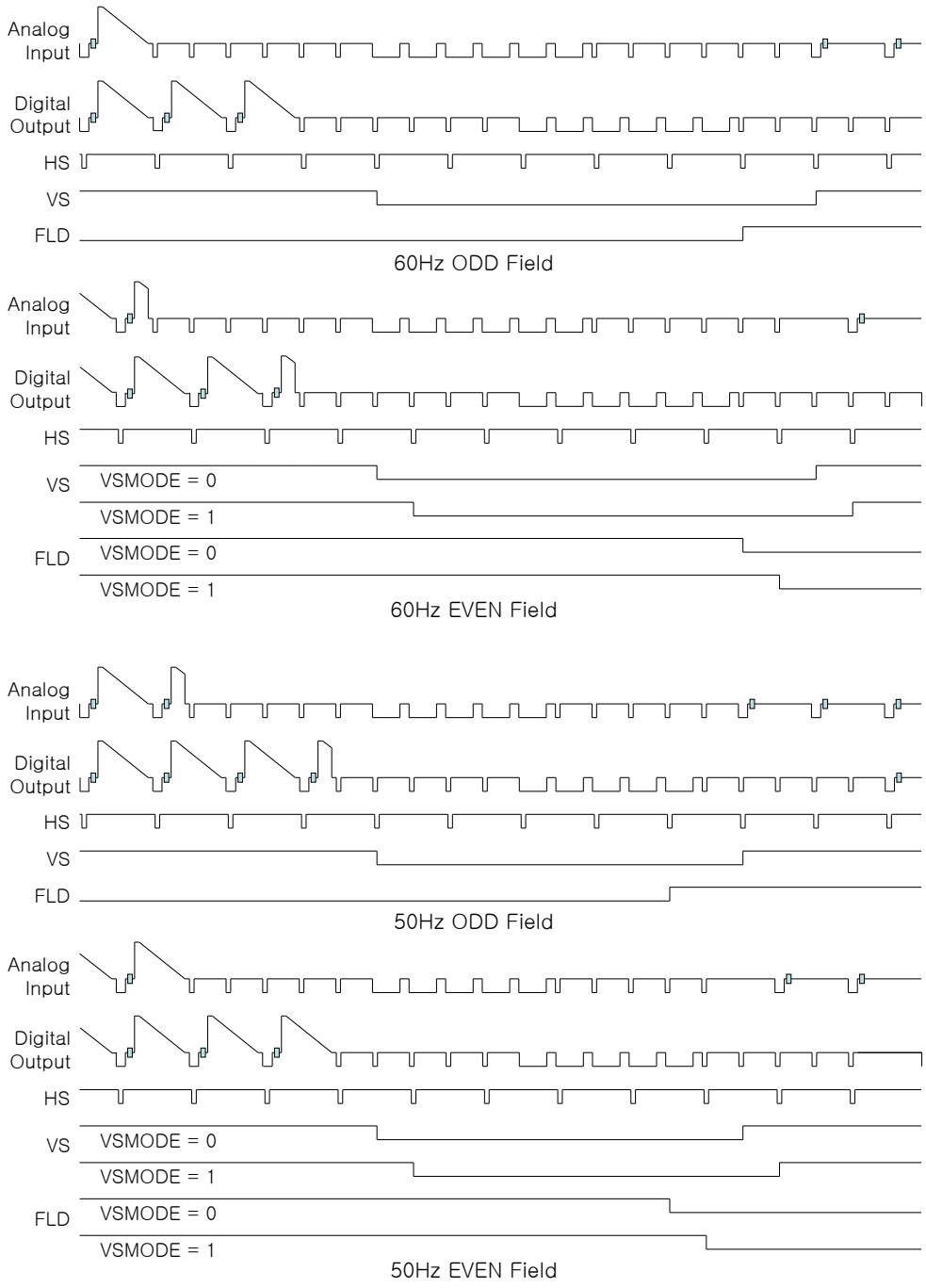
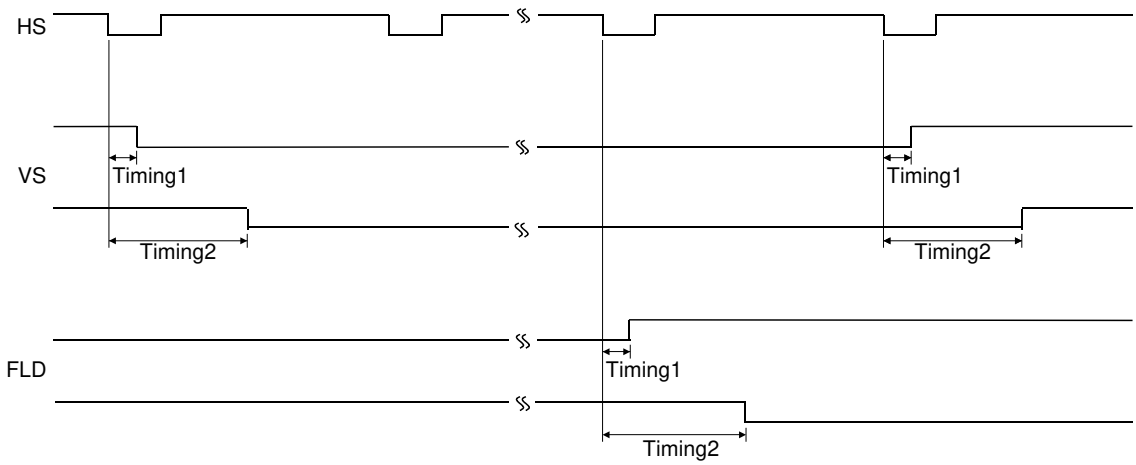


Fig11 Vertical Timing for 60Hz / 50Hz Video



Timing1 : 40 system clock(54MHz) for the Even field with VSMODE=1 or Odd field
Timing2 : 1760 system clock(54MHz) for the Even field with VSMODE=0

Fig12 Horizontal and Vertical Timing in Video Output

Output Enabling Act

After power-up, the TW2816 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to its default values. After reset, the TW2816 data outputs are tri-stated. The OE (0x43) register should be written after reset to enable outputs desired.

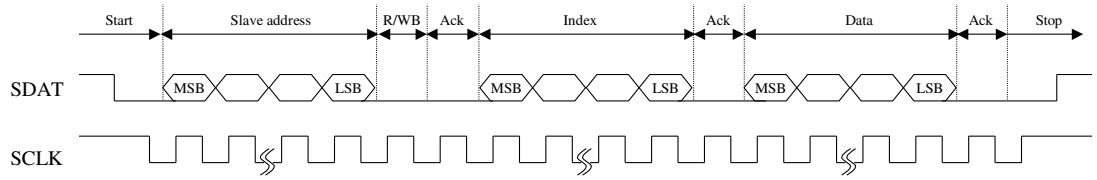
Host Interface

Serial Interface

The two wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the TW2816 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDD. The SADD[1:0] defines two LSB of the slave device address by tying the SADD pins either to VDD or GND.

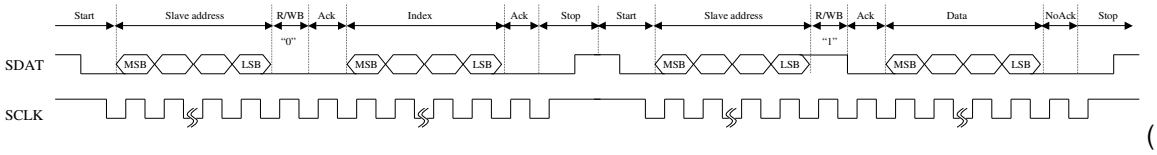
Slave Address							R/W
0	1	0	1	0	SADD[1]	SADD[0]	1 = Read 0 = Write

The TW2816 supports auto index increments in write/read mode if the data are in sequential order. Data transfer rate on the bus is up to 400 Kbits/s.



(a)

Write Mode



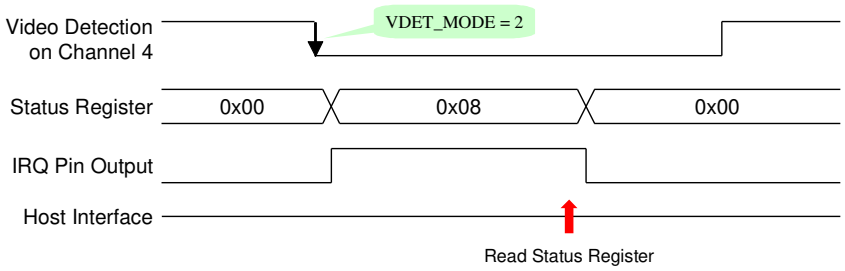
(

b) Read Mode

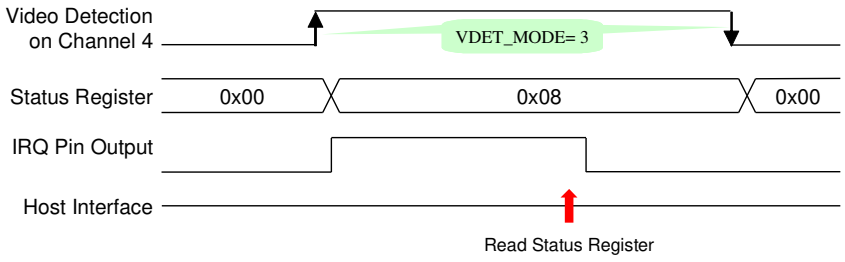
Fig13 Timing Chart of Serial Interface

Interrupt Interface

The TW2816 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video from TW2816. To use interrupt request function, the interrupt request should be enabled by the IRQENA (0x5C) and polarity of the IRQ pin should be selected by the IRQPOL (0x5C). Also, each channel of video detection should be enabled by the VDET_ENA (0x5B). Then, the interrupt mode should be defined by the VDET_MODE (0x5C) that control the time to request interrupt and set the status register VDET_STATE (0x5A). The Fig14 shows operation of interrupt when the VDET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading the VDET_STATE. When the VDET_MODE is 1 or 2, the status register VDET_STATE will also be cleared automatically by reading VDET_STATE. However, when the VDET_MODE are 3, the status register VDET_STATE will not be cleared automatically, but has the same value as actual status of video detection flag.



(a) Status Register of Automatic Cleared Mode



(b) Status Register same as Video Detection Flag Mode

Fig14 Timing Diagram of Interrupt Interface

Control Register

Register Map

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x00	0x10	0x20	0x30	VIDSTAT *	DET_FORMAT*			DET_COLOR*	LOCK_COLOR*	LOCK_GAIN*	LOCK_OFST*	LOCK_HPLL*
0x01	0x11	0x21	0x31	FORMAT	IFMTMAN	IFORMAT			AGC	PEDEST	DET_NONSTD *	DET_FLD60 *
0x02	0x12	0x22	0x32	HDELAY	HDELAY [7:0]							
0x03	0x13	0x23	0x33	HACTIVE	HACTIVE [7:0]							
0x04	0x14	0x24	0x34	VDELAY	HDELAY [7:0]							
0x05	0x15	0x25	0x35	VACTIVE	HACTIVE [7:0]							
0x06	0x16	0x26	0x36	MSB_ACTV	0	0	VACTIVE [8]	VDELAY [8]	HACTIVE [9:8]		HDELAY [9:8]	
0x07	0x17	0x27	0x37	HUE	HUE							
0x08	0x18	0x28	0x38	SAT	SAT							
0x09	0x19	0x29	0x39	CONT	CONT							
0x0A	0x1A	0x2A	0x3A	BRT	BRT							
0x0B	0x1B	0x2B	0x3B	LUMCON	YBWI	COMBMD		YPEAK_MD	YPEAK_GN			
0x0C	0x1C	0x2C	0x3C	COLRCON	0	0	CKILL		CTI_GN			
0x0D	0x1D	0x2D	0x3D	CH_CON	0	BGND_EN	BGND_COLR	ANA_SW	SW_RESET	DUAL_CH	SEL_CH	
0x0E	0x1E	0x2E	0x3E	ANA_FIL	0	0	0	1	0	0	0	1

Note : * Read only registers

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x40				DET_SYNC *	FLD4*	FLD3*	FLD2*	FLD1*	VAV4*	VAV3*	VAV2*	VAV1*
0x41				PEAKAGC1	WPEAK_MD4		WPEAK_MD3		WPEAK_MD2		WPEAK_MD1	
0x42				PEAKAGC2	CHID		WPEAK_REF		WPEAK_RNG		WPEAK_TIME	
0x43				MISC	OE	AUTO_BGND	LIM16	NOVID_656	CLKN_OEB	CLKP_OEB	CLKN_MD	CLKP_MD
0x44				AGC TIME	0	1	0	0	GNTIME		OSTIME	
0x45				HSWIDTH	1	0	HSWIDTH					
0x46				SYNCPOL	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
0x47				CFILTER	IFCOMP		CLPF		ACCTIME		APCTIME	
0x48				CDEL	0	1	C_CORE		0	CDEL		
0x49				U_GAIN	U_GAIN							
0x4A				V_GAIN	V_GAIN							
0x4B				U_OFF	U_OFF							
0x4C				V_OFF	V_OFF							
0x4D				CLK_MD	CLKN_DEL				CLKP_DEL			
0x4E				CLK_DEL1	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0x4F				CLK_DEL2	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		
0x50				ADC_PWDN	0	0	1	1	ADC_PWDN4	ADC_PWDN3	ADC_PWDN2	ADC_PWDN1
0x51				NOVID_MD	0	0	0	0	NOVID_MD		1	1
0x52				RESERVED	0	0	0	0	0	1	0	1
0x53				RESERVED	0	0	0	0	0	0	0	0
0x54				RESERVED	0	0	0	0	0	0	0	0
0x55				RESERVED	1	0	0	0	0	0	0	0
0x56				RESERVED	0	0	0	0	0	1	1	0
0x57				RESERVED	0	0	0	0	0	0	0	0
0x58				DEV_ID *	0	1	0	0	0	0	0	0
0x59				DEV_ID *	0	0	1	0	0	0	0	0
0x5A				VDET_STATE*					VDET_STATE			
0x5B				VDET_ENA	0	0	0	0	VDET_ENA			
0x5C				VDET_MODE	IRQENA	IRQPOL	1	0	0	0	VDET_MODE	

Note : * Read only registers

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x60				RESERVED	0	0	0	0	0	0	0	0
0x61				RESERVED	0	0	0	0	0	0	0	0
0x62				RESERVED	0	0	0	0	0	0	0	0
0x63				RESERVED	0	0	0	0	0	0	0	0
0x64				RESERVED	0	0	0	0	0	0	0	0
0x65				RESERVED	0	0	0	0	0	0	0	0
0x66				RESERVED	0	0	0	0	0	0	0	0
0x67				RESERVED	0	0	0	0	0	0	0	0
0x68				RESERVED	0	0	0	0	0	0	0	0
0x69				RESERVED	0	0	0	0	0	0	0	0
0x6A				RESERVED	0	0	0	0	0	0	0	0
0x6B				RESERVED	0	0	0	0	0	0	0	0
0x6C				RESERVED	0	0	0	0	0	0	0	0
0x6D				RESERVED	0	0	0	0	0	0	0	0
0x6E				RESERVED	0	0	0	0	0	0	0	0
0x6F				RESERVED	0	0	0	0	0	0	0	0
0x70				RESERVED	0	0	0	0	0	0	0	0
0x71				CIF_MODE	HSCL_LPF	VSCL_ENA	VSCL_SYNC	0	0	0	0	0
0x72				RESERVED	0	0	0	0	0	0	0	0
0x73				RESERVED	0	0	0	0	0	0	0	0
0x74				RESERVED	0	0	0	0	0	0	0	0
0x75				CIF_54M	0	0	0	0	CIF_54M4	CIF_54M3	CIF_54M2	CIF_54M1

Note : * Read only registers

Recommended Value

Address				Mnemonic	NTSC	PAL	Non-realtime
CH1	CH2	CH3	CH4				
0x00	0x10	0x20	0x30	VIDSTAT *	8'h00		
0x01	0x11	0x21	0x31	FORMAT	C8	88	
0x02	0x12	0x22	0x32	HDELAY	20		
0x03	0x13	0x23	0x33	HACTIVE	D0		
0x04	0x14	0x24	0x34	VDELAY	06	05	
0x05	0x15	0x25	0x35	VACTIVE	F0	20	
0x06	0x16	0x26	0x36	MSB_ACTV	08	28	
0x07	0x17	0x27	0x37	HUE	80		
0x08	0x18	0x28	0x38	SAT	80		
0x09	0x19	0x29	0x39	CONT	80		
0x0A	0x1A	0x2A	0x3A	BRT	80		
0x0B	0x1B	0x2B	0x3B	LUMCON	02	82	
0x0C	0x1C	0x2C	0x3C	COLRCON	06		
0x0D	0x1D	0x2D	0x3D	OUTFMT	00		
0x0E	0x1E	0x2E	0x3E	RESERVED	11		
0x40				DET_SYNC *	00		
0x41				PEAKAGC1	00		
0x42				PEAKAGC2	00		
0x43				MISC	C0		
0x44				AGCTIME	45		4F
0x45				HSWIDTH	A0		
0x46				SYNCPOL	D0		10
0x47				CFILTER	2F		
0x48				CDEL	64		
0x49				U_GAIN	80		
0x4A				V_GAIN	80		
0x4B				U_OFF	82		
0x4C				V_OFF	82		
0x4D				CLK_CON	80		
0x4E				MPP_MODE1	00		
0x4F				MPP_MODE2	00		
0x50				ADC_PWDN	30		
0x51				NOVID_MD	0F		00
0x52				RESERVED	05		
0x53				RESERVED	00		
0x54				RESERVED	00		
0x55				RESERVED	80		88
0x56				RESERVED	06		
0x57				RESERVED	00		
0x58				DEV_ID *	40		
0x59				DEV_ID *	20		
0x5A				STATE_DET	00		
0x5B				VDET_ENA	0F		
0x5C				DET_MODE	00		
0x60				RESERVED	00		
0x61				RESERVED	00		
0x62				RESERVED	00		
0x63				RESERVED	00		
0x64				RESERVED	00		

Address				Mnemonic	NTSC	PAL	Non-realtime
CH1	CH2	CH3	CH4				
0x65				RESERVED	00		
0x66				RESERVED	00		
0x67				RESERVED	00		
0x68				RESERVED	00		
0x69				RESERVED	00		
0x6A				RESERVED	00		
0x6B				RESERVED	00		
0x6C				RESERVED	00		
0x6D				RESERVED	00		
0x6E				RESERVED	00		
0x6F				RESERVED	00		
0x70				RESERVED	00		
0x71				CIF_MODE	00		
0x72				RESERVED	00		
0x73				RESERVED	00		
0x74				RESERVED	00		
0x75				OUT_54M	00		

Note : Blanks is the same value as NTSC value

Register Description

CH	Index	Video Status Flag *(Read only)*							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x00	DET_ FORMAT			DET_ COLOR	LOCK_ COLOR	LOCK_ GAIN	LOCK_ OFST	LOCK_ HPLL
2	0x10								
3	0x20								
4	0x30								

DET_FORMAT Status of video standard detection *(Read only)*

0 PAL-B/D
1 PAL-M
2 PAL-N
3 PAL-60
4 NTSC-M
5 NTSC-4.43
6 NTSC-N

DET_COLOR Status of color detection *(Read only)*

0 Color is not detected
1 Color is detected

LOCK_COLOR Status of locking for color demodulation loop *(Read only)*

0 Color demodulation loop is not locked
1 Color demodulation loop is locked

LOCK_GAIN Status of locking for AGC loop *(Read only)*

0 AGC loop is not locked
1 AGC loop is locked

LOCK_OFST Status of locking for clamping loop *(Read only)*

0 Claming loop is not locked
1 Claming loop is locked

LOCK_HPLL Status of locking for horizontal PLL *(Read only)*

0 Horizontal PLL is not locked
1 Horizontal PLL is locked

CH	Index	Input Video Format							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x01	IFMTMAN	IFORMAT			AGC	PEDEST	DET_ NONSTD *	DET_ FLD60 *
2	0x11								
3	0x21								
4	0x31								

Notes : * Read only bits

IFMTMAN — Setting video standard manually with IFORMAT

0 Detect video standard automatically according to incoming video signal (default)

1 Video standard is selected with IFORMAT

IFORMAT — Force the device to operate in a particular video standard when IFMTMAN is high or to free-run in a particular video standard on no-video status when IFMTMAN is low

0 PAL-B/D (default)

1 PAL-M

2 PAL-N

3 PAL-60

4 NTSC-M

5 NTSC-4.43

6 NTSC-N

AGC — Enable the AGC

0 Disable the AGC (default)

1 Enable the AGC

PEDEST — Enable gain correction for 7.5 IRE black (pedestal) level

0 No pedestal level (0 IRE is ITU-R BT.656 code 16) (default)

1 7.5 IRE setup level (7.5 IRE is ITU-R BT.656 code 16)

DET_NONSTD — Status of non-standard video detection *(Read only)*

0 The incoming video source is standard

1 The incoming video source is non-standard

DET_FLD60 — Status of field frequency of incoming video *(Read only)*

0 50Hz field frequency

1 60Hz field frequency

CH	Index	Horizontal Delay Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x06	0	0	VACTIVE[8]	VDELAY[8]	HACITIVE[9:8]		HDELAY[9:8]	
2	0x16								
3	0x26								
4	0x36								
1	0x02	HDELAY[7:0]							
2	0x12								
3	0x22								
4	0x32								

HDELAY This 10bit register defines the starting location of horizontal active pixel. A unit is 1 pixel. The default value is decimal 32.

CH	Index	Horizontal Active Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x06	0	0	VACTIVE[8]	VDELAY[8]	HACITIVE[9:8]		HDELAY[9:8]	
2	0x16								
3	0x26								
4	0x36								
1	0x03	HACTIVE[7:0]							
2	0x13								
3	0x23								
4	0x33								

HACTIVE This 10bit register defines the number of horizontal active pixel. A unit is 1 pixel. The default value is decimal 720.

CH	Index	Vertical Delay Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x06	0	0	VACTIVE[8]	VDELAY[8]	HACITIVE[9:8]		HDELAY[9:8]	
2	0x16								
3	0x26								
4	0x36								
1	0x04	VDELAY[7:0]							
2	0x14								
3	0x24								
4	0x34								

VDELAY This 9bit register defines the starting location of vertical active. A unit is 1 line. The default value is decimal 6.

CH	Index	Vertical Active Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x06	0	0	VACTIVE[8]	VDELAY[8]	HACITIVE[9:8]		HDELAY[9:8]	
2	0x16								
3	0x26								
4	0x36								
1	0x05	VACTIVE[7:0]							
2	0x15								
3	0x25								
4	0x35								

VACTIVE This 9bit register defines the number of vertical active lines. A unit is 1 line. The default value is decimal 240.

CH	Index	Hue Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x07	HUE							
2	0x17								
3	0x27								
4	0x37								

HUE

Control the hue information. The resolution is 1.4° / LSB.

0	-180°
:	:
128	0° (default)
:	:
255	180°

CH	Index	Saturation Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x08	SAT							
2	0x18								
3	0x28								
4	0x38								

SAT

Control the color saturation. The resolution is 0.8% / LSB.

0	0 %
:	:
128	100 % (default)
:	:
255	200 %

CH	Index	Contrast Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x09	CONT							
2	0x19								
3	0x29								
4	0x39								

CONT Control the contrast. The resolution is 0.8% / LSB.

0 0 %
: :
128 100 % (default)
: :
255 200 %

CH	Index	Brightness Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0A	BRT							
2	0x1A								
3	0x2A								
4	0x3A								

BRT Control the brightness. The resolution is 0.2IRE / LSB.

0 -25 IRE
: :
128 0 (default)
: :
255 25 IRE

CH	Index	Luminance Peaking Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0B	YBWI	COMBMD		YPEAK_MD	YPEAK_GN			
2	0x1B								
3	0x2B								
4	0x3B								

YBWI Select the luminance trap filter mode

- 0 Narrow bandwidth trap filter mode (default)
- 1 Wide bandwidth trap filter mode

COMBMD Select the adaptive comb filter mode

- 0,1 Adaptive comb filter mode (default)
- 2 Force trap filter mode
- 3 Not supported

YPEAK_MD Select the luminance peaking frequency band

- 0 4~5 MHz frequency band (default)
- 1 2~4 MHz frequency band

YPEAK_GN Control the luminance peaking gain

- 0 No peaking (default)
- 1 12.5 %
- 2 25 %
- 3 37.5 %
- 4 50 %
- 5 62.5 %
- 6 75 %
- 7 87.5 %
- 8 100 %
- 9 112.5 %
- 10 125 %
- 11 137.5 %
- 12 150 %
- 13 162.5 %
- 14 175 %
- 15 187.5 %

CH	Index	Color Killer and CTI Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0C	0	0	CKILL		CTI_GN			
2	0x1C								
3	0x2C								
4	0x3C								

CKIL Control the color killing mode

0,1 Auto detection mode (default)

2 Color is always alive

3 Color is always killed

CTI_GN Control the CTI gain

0 No CTI

1 12.5 %

2 25 %

3 37.5 %

4 50 %

5 62.5 %

6 75 % (default)

7 87.5 %

8 100 %

9 112.5 %

10 125 %

11 137.5 %

12 150 %

13 162.5 %

14 175 %

15 187.5 %

CH	Index	Channel Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0D	0	BGNDEN	BGNDCLR	0	SW_ RESET	DUAL_CH	SEL_CH	
2	0x1D								
3	0x2D								
4	0x3D								

BGNDEN Control the background color on/off

0 Normal video image is displayed (default)

1 Background color is displayed

BGNDCLR Select the background color only if BGNDEN bit is high

0 Blue color (default)

1 Black color

SW_RESET Reset the system by software except control registers.

This bit is self-clearing in a few clocks after enabled.

0 Normal operation (default)

1 Enable soft reset

DUAL_CH Enable dual ITU-R BT.656 format with time-multiplexed 54MHz

0 Standard ITU-R BT.656 format (default)

1 Dual ITU-R BT.656 format with time-multiplexed 54MHz

SEL_CH Select another channel output to be multiplexed with its own channel on each VD pins

0 CH1 output (default)

1 CH2 output

2 CH3 output

3 CH4 output

CH	Index	Reserved							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0E	0	0	0	1	0	0	0	1
2	0x1E								
3	0x2E								
4	0x3E								

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Vertical Sync and Field Flag *(Read only)*							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x40	FLD				VAV			

FLD Status of the field flag for corresponding channel
FLD[3:0] stands for CH4 to CH1. *(Read only)*
0 Odd field when FLDPOL (0x46) = 1
1 Even field when FLDPOL (0x46) = 1

VAV Status of the vertical active video signal for corresponding channel
VAV[3:0] stands for CH4 to CH1. *(Read only)*
0 Vertical blanking time
1 Vertical active time

Index	Automatic White Peak Control Mode							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x41	WPEAK_MD4		WPEAK_MD3		WPEAK_MD2		WPEAK_MD1	

WPEAK_MD Select the automatic white peak control mode.
WPEAK_MD1~4 stands for CH1 to CH4.
0 No automatic white peak control (default)
1 Suppress the excessive white peak level into WPEAK_REF level
2 Increase the low level into WPEAK_REF level
3 Suppress and Increase the input level into WPEAK_REF level

Index	Automatic White Peak Control Parameter							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x42	CHID_MD		WPEAK_REF		WPEAK_RNG		WPEAK_TIME	

CHID_MD Select the Channel ID format for time-multiplexed 54MHz output
0 No channel ID (default)
1 CHID with the specific ITU-R BT.656 Sync Code
2 CHID with the specific horizontal blanking code
3 CHID with the specific ITU-R BT.656 sync & horizontal blanking code

WPEAK_REF Control the white peak reference level for automatic white peak control
0 100 IRE (default)
1 110 IRE
2 130 IRE
3 140 IRE

WPEAK_RNG Control the range of automatic white peak control
0 -3 ~ 3 dB (default)
1 -6 ~ 6 dB
2,3 -9 ~ 9 dB

WPEAK_TIME Control the time constant of automatic white peak control loop
0 Slower (default)
1 Slow
2 Fast
3 Faster

Index	Miscellaneous Function Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x43	OE	AUTO_ BGND	LIM16	NOVID_ 656	CLKN_ OEB	CLKP_ OEB	CLKN_MD	CLKP_MD

OE — Control the tri-state of output pin
- 0 Outputs are Tri-state except clock output (CLKPO, CLKNO) pin (default)
- 1 Outputs are enabled

AUTO_BGND — Enable the auto background mode when No-video is detected
- 0 Disable the auto background mode (default)
- 1 Enable the auto background mode

LIM16 — Control the output range
- 0 Output ranges are limited to 2 ~ 254 (default)
- 1 Output ranges are limited to 16 ~ 239

NOVID_656 — Select the optional set of 656 SAV/EAV code for No-video status
- 0 Normal ITU-R BT.656 SAV/EAV code (default)
- 1 An optional set of ITU-R BT.656 SAV/EAV code for No-video status

CLKN_OEB — Control the tri-state of CLKNO pin
- 0 Output is enabled (default)
- 1 Output is Tri-state

CLKP_OEB — Control the tri-state of CLKPO pin
- 0 Output is enabled (default)
- 1 Output is Tri-state

CLKN_MD — Control the clock frequency of CLKNO pin
- 0 27MHz (default)
- 1 54MHz

CLKP_MD — Control the clock frequency of CLKPO pin
- 0 27MHz (default)
- 1 54MHz

Index	AGC and Clamp Loop Time Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x44	0	1	0	0	GNTIME		OSTIME	

GNTIME Control the time constant of gain tracking loop

0 Slower
1 Slow (default)
2 Fast
3 Faster

OSTIME Control the time constant of offset tracking loop

0 Slower
1 Slow (default)
2 Fast
3 Faster

Index	Horizontal Sync Pulse Width Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x45	1	0	HSWIDTH					

HSWIDTH Define the width of horizontal sync output.
A unit is 1 pixel. The default value is decimal 32.

Index	Sync Pulse Polarity Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x46	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0

FLDMODE Select the field flag generation mode
- 0 Field flag is detected from incoming video (default)
- 1 Field flag is generated from small accumulator of detected field
- 2 Field flag is generated from medium accumulator of detected field
- 3 Field flag is generated from large accumulator of detected field

VSMODE Control the VS and field flag timing
- 0 VS and field flag is aligned with vertical sync of incoming video (default)
- 1 VS and field flag is aligned with HS

FLDPOL Select the FLD polarity
- 0 Odd field is high (default)
- 1 Even field is high

HSPOL Select the HS polarity
- 0 Low for sync duration (default)
- 1 High for sync duration

VSPOL Select the VS polarity
- 0 Low for sync duration (default)
- 1 High for sync duration

Index	Color Filter Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x47	IFCOMP		CLPF		ACCTIME		APCTIME	

IFCOMP — Select the IF-compensation filter mode

0 No compensation (default)
1 +1 dB/ MHz
2 +2 dB/ MHz
3 +3 dB/ MHz

CLPF — Select the Color LPF mode

0 550KHz bandwidth
1 750KHz bandwidth (default)
2 950KHz bandwidth
3 1.1MHz bandwidth

ACCTIME — Control the time constant of auto color control loop

0 Slower
1 Slow
2 Fast
3 Faster (default)

APCTIME — Control the time constant of auto phase control loop

0 Slower
1 Slow
2 Fast
3 Faster (default)

Index	Chroma Coring and Delay Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x48	0	1	C_CORE		0	CDEL		

C_CORE — Coring to reduce the noise in the chrominance

0 No coring
1 Coring value is within 128 +/- 1 range
2 Coring value is within 128 +/- 2 range (default)
3 Coring value is within 128 +/- 4 range

CDEL — Adjust the group delay of chrominance path relative to luminance

0 -2.0 pixel
1 -1.5 pixel
2 -1.0 pixel
3 -0.5 pixel
4 0.0 pixel (default)
5 0.5 pixel
6 1.0 pixel
7 1.5 pixel

Index	U Gain							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x49	U_GAIN							

U_GAIN Adjust gain for U (or Cb) component. The resolution is 0.8% / LSB.

0 0 %
: :
128 100 % (default)
: :
255 200 %

Index	V Gain							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4A	V_GAIN							

V_GAIN Adjust gain for V (or Cr) component. The resolution is 0.8% / LSB.

0 0 %
: :
128 100 % (default)
: :
255 200 %

Index	U Offset							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4B	U_OFF							

U_OFF

U (or Cb) offset adjustment register. The resolution is 0.4% / LSB.

0 -50 %

: :

128 0 % (default)

: :

255 50 %

Index	V Offset							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4C	V_OFF							

V_OFF

V (or Cr) offset adjustment register. The resolution is 0.4% / LSB.

0 -50 %

: :

128 0 % (default)

: :

255 50 %

Index	Clock Output Delay Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4D	CLKN_DEL				CLKP_DEL			

CLKN_DEL Control the clock delay of CLKNO pin.
The delay can be controlled with 1ns step for 54MHz / 2ns step for 27MHz.
The default value is “0”.

CLKP_DEL Control the clock delay of CLKPO pin.
The delay can be controlled with 1ns step for 54MHz / 2ns step for 27MHz.
The default value is “0”.

Index	MPP Pin Output Mode Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4E	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0x4F	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		

GPP_VAL Select the general purpose value through the MPP pin

0 “0” value (default)

1 “1” value

MPP_MODE Select the output mode for MPP pins

0 Horizontal sync output (default)

1 Vertical sync output

2 Field flag output

3 Horizontal active signal output

4 Vertical active & horizontal active signal output

5 No video flag

6 Not supported

7 GPP_VAL

Index	ADC Power Down							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x50	0	0	1	1	ADC_PDWN			

ADC_PWDN Power down the video ADC.
ADC_PWDN[3:0] stands for CH4 to CH1.
0 Normal operation (default)
1 Power down

Index	NO-Video Mode Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x51	0	0	0	0	NOVID_MD		1	1

NOVID_MD Select the No-video flag generation mode
0 Faster
1 Fast
2 Slow
3 Slower (default)

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x52	0	0	0	0	0	1	0	1
0x53	0	0	0	0	0	0	0	0
0x54	0	0	0	0	0	0	0	0
0x55	1	0	0	0	0	0	0	0
0x56	0	0	0	0	0	1	1	0
0x57	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	**Device and Revision ID Flag** *(Read only)*							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x58	DEV_ID[6:5]		0	0	0	0	0	0
0x59	DEV_ID[4:0]					REV_ID		

DEV_ID The TW2816 product ID code is “7’b0100100”. *(Read only)*

REV_ID The revision number is “3’b000”. *(Read only)*

Index	State of Video Detection							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5A	0	0	0	0	VDET_STATE			

VDET_STATE State of Video detection.
These bit is activated according to VDET_MODE
[0] : Video input VIN1.
[1] : Video input VIN2.
[2] : Video input VIN3.
[3] : Video input VIN4.

0 Inactivated
1 Activated

Index	Video Detection Enable							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5B	0	0	0	0	VDET_ENA			

VDET_ENA

Enable state register updating and interrupt request of video detection for each input.

[0] : Video input VIN1.

[1] : Video input VIN2.

[2] : Video input VIN3.

[3] : Video input VIN4.

0 Disable state register updating and interrupt request

1 Enable state register updating and interrupt request (default)

Index	IRQ Enable							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5C	IRQENA	IRQPOL	1	0	0	0	VDET_MODE	

IRQENA — Enable/Disable the interrupt request through the IRQ pin.

0 Disable (default)

1 Enable

IRQPOL — Select the polarity of interrupt request through the IRQ pin.

0 Falling edge requests the interrupt and keeps its state until cleared (default)

1 Rising edge requests the interrupt and keeps its state until cleared

VDET_MODE — Define the polarity of state register and interrupt request for video detection.

0 Never request interrupt by the video detection

1 Make the interrupt request rising only when the video signal comes in

2 Make the interrupt request falling only when the video signal goes out

3 Make the interrupt request rising and falling when the video comes in and goes out (default)

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x60	0	0	0	0	0	0	0	0
0x61	0	0	0	0	0	0	0	0
0x62	0	0	0	0	0	0	0	0
0x63	0	0	0	0	0	0	0	0
0x64	0	0	0	0	0	0	0	0
0x65	0	0	0	0	0	0	0	0
0x66	0	0	0	0	0	0	0	0
0x67	0	0	0	0	0	0	0	0
0x68	0	0	0	0	0	0	0	0
0x69	0	0	0	0	0	0	0	0
0x6A	0	0	0	0	0	0	0	0
0x6B	0	0	0	0	0	0	0	0
0x6C	0	0	0	0	0	0	0	0
0x6D	0	0	0	0	0	0	0	0
0x6E	0	0	0	0	0	0	0	0
0x6F	0	0	0	0	0	0	0	0
0x70	0	0	0	0	0	0	0	0
0x72	0	0	0	0	0	0	0	0
0x73	0	0	0	0	0	0	0	0
0x74	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	CIF Mode							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x71	HSCL_LPF	VSCL_ENA	VSCL_SYNC	0	0	0	0	0

HSCL_LPF Enable the horizontal LPF for CIF time-multiplexed format with 54MHz.

0 Full bandwidth (default)

1 3.375MHz bandwidth

VSCL_ENA Enable the vertical scaler for CIF time-multiplexed format with 54MHz.

0 Full size for vertical direction (default)

1 Half size for vertical direction

VSCL_SYNC Enable the optional ITU-R BT.656 sync code format.

0 Standard ITU-R BT.656 sync code (default)

1 Skip ITU-R BT.656 sync code for non-valid vertical line

Index	Four Channel CIF Time-multiplxed Format							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x75	0	0	0	0	CIF_54M4	CIF_54M3	CIF_54M2	CIF_54M1

CIF_54M Enable four channel CIF time-multiplexed format with 54MHz

CIF_54M1~4 stands for CH1 to CH4.

0 Standard ITU-R BT.656 format (default)

1 Four channel CIF time-multiplexed format with 54MHz

Electrical Information

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VDDV (measured to VSSV)	VDD_{VM}	-0.5		2.3	V
VDDA (measured to VSSA)	VDD_{AM}	-0.5		2.3	V
VDDI (measured to VSS)	VDD_{IM}	-0.5		2.3	V
VDDO (measured to VSS)	VDD_{OM}	-0.5		4.5	V
Digital Input/Output Voltage	-	–0.5		4.5	V
Analog Input Voltage	-	–0.5		2.0	V
Storage Temperature	T_S	–65		150	° C
Junction Temperature	T_J	0		125	° C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}			220	° C

Note : Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
VDDV (measured to VSSV)	VDD_V	1.62	1.8	1.98	V
VDDI (measured to VSS)	VDD_I	1.62	1.8	1.98	V
VDDO (measured to VSS)	VDD_O	3.0	3.3	3.6	V
Analog Input Voltage(AC coupling required)	V_{AIN}	0	0.5	1.0	V
Ambient Operating Temperature	T_A	0		70	° C

Note : Power On/Off sequence should keep the following rule.

- Apply power to VDDV, VDDI and VDDO at the same time
- If it is difficult to apply the power to these pins at the same time, apply the power to VDDO first and to VDDV, VDDI later.
- Cut the power of VDDV, VDDI and VDDO at the same time
- If it is difficult to cut the power of these pins at the same time, cut the power of VDDV, VDDI first and of VDDO later

DC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=2.5V or 0V)	I_L			±10	uA
Input Capacitance	C_{IN}		6		pF
Digital Outputs					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@V_{OH}=2.4V)	I_{OH}	6.3	12.8	21.2	mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	4.9	7.4	9.8	mA
Tri-state Output Leakage Current (@V_O=2.5V or 0V)	I_{OZ}			±10	uA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF
Supply Current					
Analog Video Supply Current (VDDV, 1.8V)	I_{DDV}		30	33	mA
Digital Internal Supply Current (VDDI, 1.8V)	I_{DDI}		200	220	mA
Digital I/O Supply Current (VDDO, 3.3V)	I_{DDO}		20	22	mA
Total Power Dissipation	P		480	530	mW

AC Electrical Parameters

CLK54I and Video Data/Sync Timing

Parameter	Symbol	Min	Typ	Max	Units
Delay from CLK54I to CLKP/N (27MHz)	1	24		30	ns
Hold from CLKP/N to Video Data/Sync (27MHz)	2a	16			ns
Delay from CLKP/N to Video Data/Sync (27MHz)	2b			20	ns
Delay from CLK54I to CLKP/N (54MHz)	3	12		18	ns
Hold from CLKP/N to Video Data/Sync (54MHz)	4a	7			ns
Delay from CLKP/N to Video Data/Sync (54MHz)	4b			11	ns

Note : CLKP/N timing is related with CLKP_DEL, CLKN_DEL (0x4D) register value. The following timing diagram is illustrated in the case that the CLKP/N_DEL is set to “4’h8”.

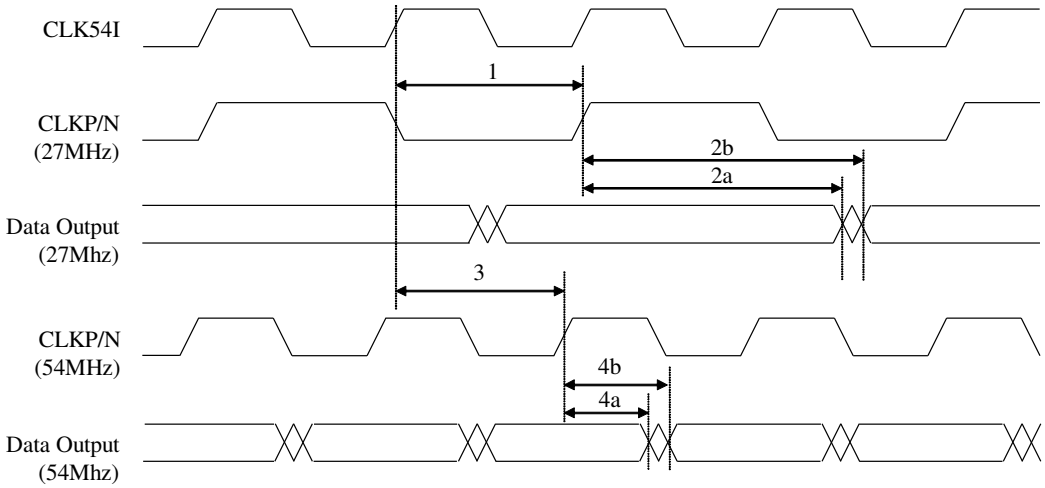


Fig15 CLK54I and Video Data Timing Diagram

Serial Host Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	1.3			us
SDAT setup time	t_{sSDAT}	100			ns
SDAT hold time	t_{hSDAT}	0		0.9	us
Setup time for START condition	t_{sSTA}	0.6			us
Setup time for STOP condition	t_{sSTOP}	0.6			us
Hold time for START condition	t_{hSTA}	0.6			us
Rise time for SCLK and SDAT	t_R			300	ns
Fall time for SCLK and SDAT	t_F			300	ns
Capacitive load for each bus line	C_{BUS}			400	pF
SCLK clock frequency	f_{SCLK}			400	KHz

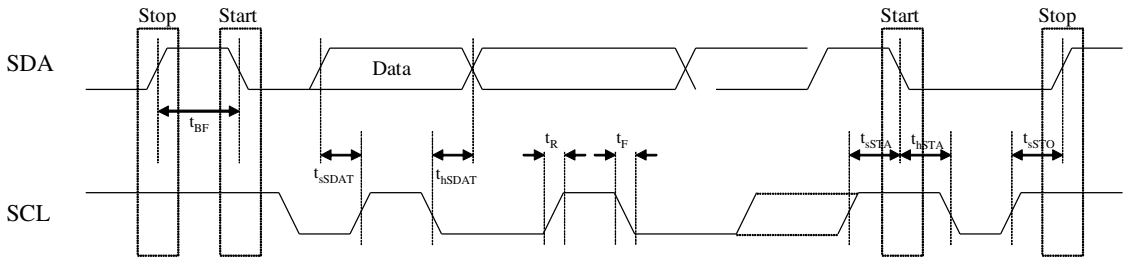
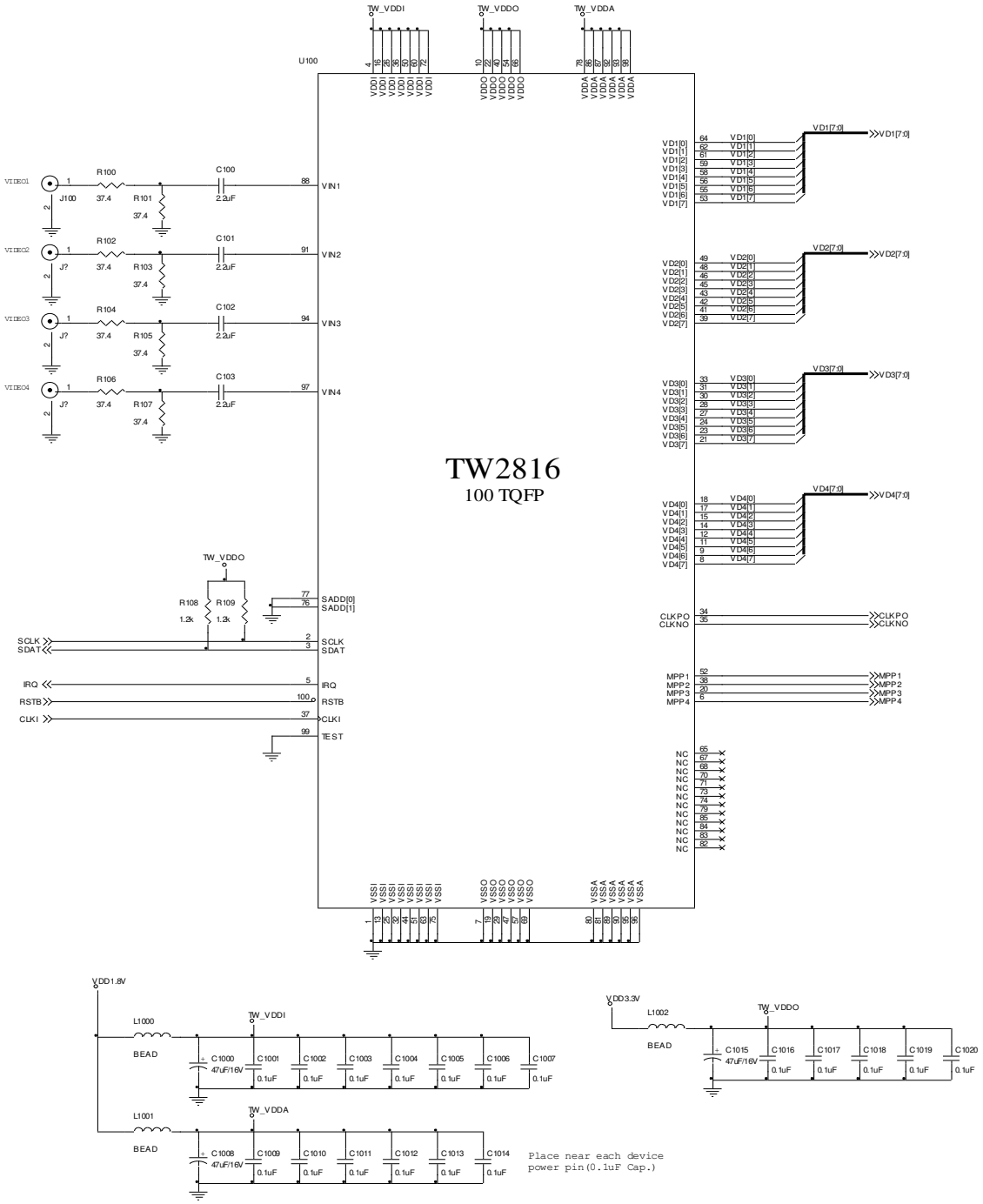


Fig16 Serial Host Interface Timing

Decoder Performance Parameter

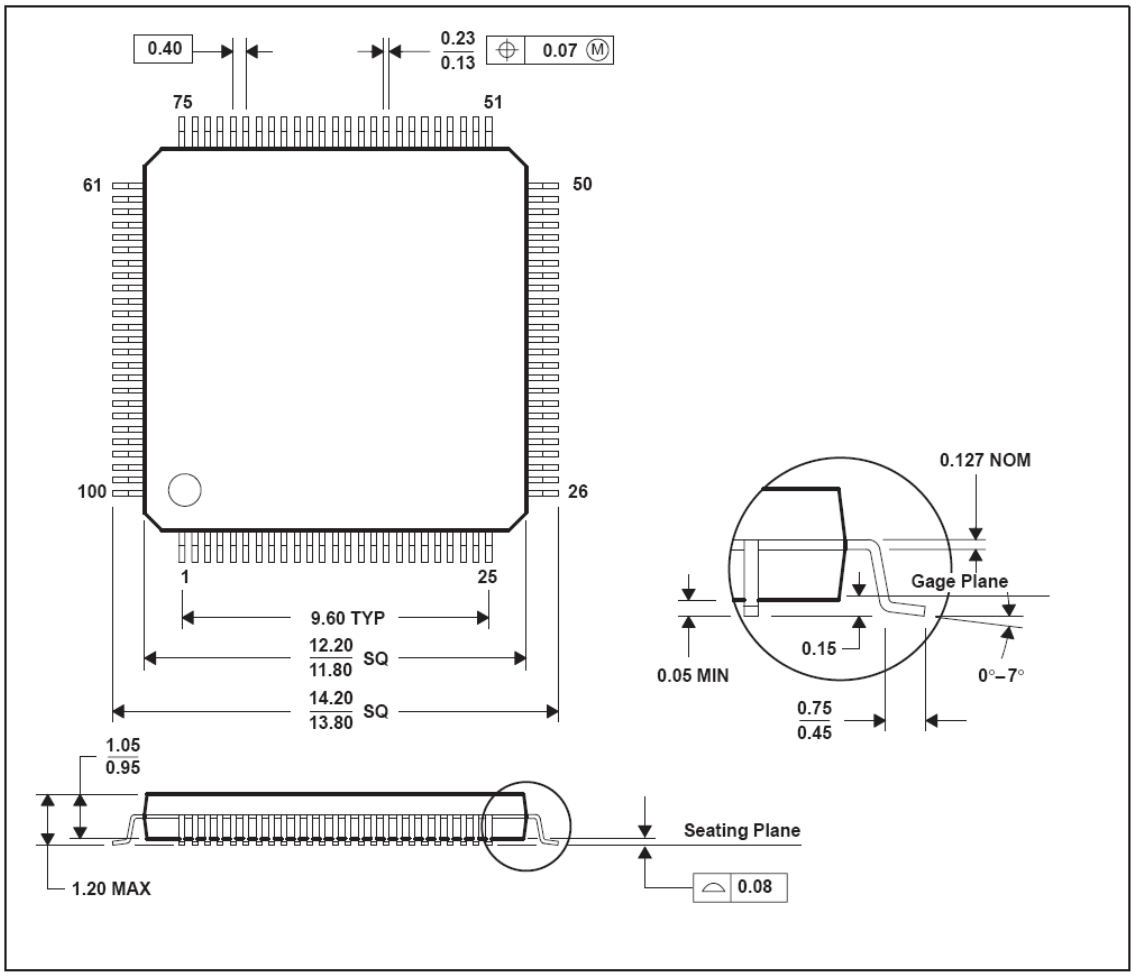
Parameter	Symbol	Min	Typ	Max	Units
Analog characteristics					
Differential gain	D_G			3	%
Differential phase	D_P			2	deg
Channel Cross-talk	α_{ct}			-50	dB
Bandwidth (at –3dB)	BW		7		MHz
Horizontal PLL					
Line frequency (60Hz)	f_H		15.734		KHz
Line frequency (50Hz)	f_H		15.625		KHz
Permissible static deviation	Δf_H			±6	%
Subcarrier PLL					
Subcarrier frequency (NTSC-M)	f_{SC}		3.579545		MHz
Subcarrier frequency (PAL-BDGHI)	f_{SC}		4.433619		MHz
Subcarrier frequency (PAL-M)	f_{SC}		3.575612		MHz
Subcarrier frequency (PAL-N)	f_{SC}		3.582056		MHz
Lock in range	Δf_{SC}	±800			Hz
AGC (Auto Gain Control)					
Range	AGC	-6		18	dB
ACC (Auto Color Gain Control)					
Range	ACC	-6		30	dB
Oscillator Input					
Nominal frequency	f_{OSC}		54		MHz
Permissible frequency deviation	$\Delta f_{OSC}/f_{OSC}$			±100	ppm
Duty cycle	dt_{OSC}			60	%

Recommended Schematic



Package Dimension

100Pins TQPF Package Mechanical Drawing



Note : A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Revision History

Revision	Date	Description	Product Code
1.0	Dec / 16 / 2005	Preliminary Specification Release	DATA1
1.1	Apr / 21 / 2006	(1) Add the HSCL_LPF (0x71) register information (P.20) (2) Change the polarity of VDET_STATE / VDET_ENA (0x71/ 72) register (P.53, P54) (3) Change the Ambient Operating Temperature range and add the power on/off sequence (P.58)	DATA1
1.2	Oct / 10 / 2006	(1) Add the CHID (0x42) register information (P.19) (2) Insert the timing diagram of CLKP/N pin (54MHz mode) (P.76)	DATA1
1.3	08/17/2007	Remove TW2818 Device option (P.04)	
1.4	02/21/2008	Correct DEV_ID value at register 0x58[7:6]	
FN7736.0	1/31/2011	Assigned file number FN7736 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. No changes to datasheet content.	
FN7736.1	5/11/2017	Applied new header/footer. Moved introduction and features list from page 4 to page 1	